THEORY OF OPERATION

INTRODUCTION

The Midland 70-101/201BD series of RF Link Modules utilizes the latest technology in its design and manufacturing. Both the UHF and VHF models are PLL (Phase Lock Loop Synthesizer)/microprocessor controlled, and offers one to five watts of power with 16 channel capability. Multiple functions including 1200 to 19,200 baud rates, AC and/or DC audio coupling, GMSK and FSK modulation are standard in these fully programmable wide bandwidth RF Link Module units.

The radio is programmed using an IBM Personal Computer, DOS® based software, an interface module and a programming cable. This allows the radio to be tailored to meet the requirements of the individual user and of the System(s) it is operating within.

The VHF and UHF radios are composed of two PCB's (a RF PCB and a digital PCB). These boards are connected with an 18 pin female and male connector. The digital board is interfaced with external data equipment through the 9 pin d-sub male connector, which controls the radio and data receiving and sending.

DIGITAL CIRCUITS

The Digital circuit contains the CPU, the channel select switch, and associated digital circuits.

TX-SIGNAL CIRCUIT

The TX data signal comes from Pin 2 of Con401, and goes through U404D. The TX-signal is filtered by U405A & B which is a 4'th order low pass filter, the output of U405A is then fed to the RF board for TX modulation. The TX microphone signal comes from pin 7 of Con401 through U405D, the pre-emphasis network, and U405C. The output level is set by RV402 before mixing with other AF signal inputs at U406C.

RX-SIGNAL CIRCUIT

The RX-data signal comes from the RF board, which is connected with pin 10 of Con403. The RX-signal is switched by U404A and adjusted by RV403 and amplified by U407. The amplified signal goes to pin10 of Con401.

RSSI DETECTOR

From the RF board, the RSSI (Received Signal Strength Indicator) signal flows to U403A & B through R461. The pulse is injected from pin5 of U403B every 1mS and C451 is discharged. It is then charged by R464. The RSSI signal is simultaneously input to pin 7 of U403A and those signals are compared. The compared signal is output from U403A. Pin 1 of U403A and the CPU detects the pulse width. The pulse width is varied by RSSI DC voltage, therefore, the carrier detection is controlled by the CPU.

EEPROM

RX/TX channel and RSSI detection level as well as other data from the programmer are stored in the EEPROM. The data stored is retained without power supplied. This is a non-volatile memory. The EEPROM may have information re-programmed or erased. U402 is an EEPROM with 2048 (8 x 256) capacity and data is written and read serially.

CHANNEL SELECTOR

One of 16 channels may be selected using the Dip Switch (SW401). SW401 encodes the channel number, selected into 4-bit binary code. The binary code plus one equals the channel number. The binary code is decoded by the CPU enabling the appropriate RX or TX frequency and associated data to be selected from the EEPROM.

DC TO DC CONVERTER

The main DC power is injected to the DC to DC converter. The DC to DC converter regulates the various input power supply voltage and outputs a constant voltage of 7.5 Volts. It is a source for all of the RF and digital circuits.

The DC to DC converter is formed by U801, Q801, Q802, L801 and R804. U801 is a switch mode DC to DC converter IC. Input DC various appears as a voltage and controls the switching pulse. As the switching pulses, Q801 and Q802 switches the input Dc of various supply voltages and generates the constant DC of supply voltage.

RF CIRCUITS

TRANSMITTER

The transmitter is comprised of:

1. Buffer
2. P.A. Module
3. Low Pass Filter
4. Antenna Switch
5. A.P.C. Circuits

BUFFER

VCO output level is –6dBm and amplified to +10dBm (UHF), +6dBm (VHF). The buffer consists of Q16 and Q17 for isolation and gain.

P.A. MODULE

The P.A. Module contains Q501, Q502, and Q503. Three stage amplifier Q501 amplifies the TX signal from +10dBm to 100 mW. Q502 is amplified to 0.5W. Q503 amplifies to 3W and then matched to 50 Ohms using the L.C. network, thereby reducing the harmonics by –30dB.

LOW PASS FILTER

L7, L8, L11, C72, C73, C74, AND C75 are the 7^{th} order Chebyshev low pass filter. Unwanted harmonics are reduced by –70dBc.

ANTENNA SWITCH

When transmitting, the diodes D5 and D6 are forward biased enabling the RF signal passage to the antenna. D6 is shorted to ground inhibiting the RF signal to front end. In receive the diodes D5 and D6 are reversed biased passing the signal from the antenna through L13 and C83 to the front end without signal loss.

AUTOMATIC CURRENT CONTROL (ACC) CIRCUITS

The ACC circuit consists of R109, variable resistor RV1, IC3 (B) and transistors Q21 and Q22. The supply current is monitored by the difference voltage on R109 (0.1 Ohm). If the current varies by RF power output or other reasons, it produces some bias voltage by IC3A and Q19. The differential signal at the output of IC3 is passed to Q21 and Q22 that produces a constant power output to the antenna. RV1 is used to adjust the RF power level.

RF CIRCUITS PLL SYNTHESIZER

12.8 MHz TCXO

The TCXO contains the 3-stage thermistor network compensation and crystal oscillator and modulation ports. Compensation is –5ppm or less from –30C to +60C.

PLL IC DUAL MODULES PRESCALER

Input frequency of 12.8MHz to IC2 MC14519 pin 20 is divided to 6.25kHz or 5kHz by the reference counter, and then supplied to the comparator. RF signal input from VCO is divided to 1/64 at the prescaler in IC2, divided by A and N counter in IC2 to determine frequency steps, and then supplied to the comparator. PLL comparison frequency is 6.25/5kHz so that minimum programmable frequency step is 5/6.25kHz. The A and N counter is programmed to obtain the desired frequency by serial data in the CPU. In the comparator, the phase difference between reference and VCO signal is compared. When the phase of the reference frequency is leading, Fv is the output, but when VCO frequency is leading, Fr is the output. When Fv=Fr, phase detector out is a very small pulse. 64.65 modulus prescaler is comprised in IC2, and has two output ports:

- Port A pin 16: TX enable 2
- Port B pin 15: prescaler power save control in PLL IC Pin 13 labeled test 2 allows the technician to see the output of the dual modulus prescaler for trouble shooting purposes, no connection should be made to this pin.

LEVEL SHIFTER & CHARGE PUMP

The charge pump is used for changing output signals Fr, Fv at PLL IC from 0-5V to 0-12V necessary for controlling the VCO.

REFERENCE FREQUENCY LPF

The Loop Filter contains R12, C21, and C22. LPF settling time is 12mS with 1kHz frequency. This also reduces the residual side-band noise for the best signal-to-noise ratio.

DC TO DC CONVERTER

The DC to DC converter converts the 5V to 14-16V to supply the necessary voltage for wide range frequency in the VCO.

VCO

The VCO consist of an RX VCO and a TX VCO. It is switched TX/RX by the power source. It is configured as a Colpits oscillator and connected to the buffer as a cascade bias in order to save power. The varicap diodes, D201/D301 are low-resistance elements and produce a change in frequency with a

change in reverse bias voltage (2-11V). L203/L303 are resonant coils, which changes the control voltage by the tuning core. D202 modulation diode, modulates the audio signal. C204 compensates for the non-linearity of the VCO due to modulation diode, and maintains a constant modulation regardless of frequency.

RECEIVER

FRONT-END

The receive signal is routed backward through the low pass filter, then onward to Pin 1 of the Hybrid Receiver Front End Module to a bandpass filter consisting of (VHF C622 through C608, L607 through L604) and (UHF C601 through C610, L601 through L603) then coupled to the base of Q601 which serves as an RF amplifier. Diode D601 serves as protection from static RF overload from nearby transmitters. The output of Q601 is then coupled to a second bandpass filter consisting of (VHF C607 through C623 and L604 through L607). The output of Pin 6 is then coupled to the doubly balanced mixer D9. The receiver front end module is factory pre-tuned and requires no adjustment. Repair is effected by replacement of the entire module of the proper banded module. These are VHF 148MHz to 174MHz and UHF 440MHz to 470MHz. The receiver front end module signal pins are as follows:

1. RF Input
2. Input Ground
3. N/A
4. Receive +5V
5. Ground
6. Output

FIRST MIXER

D9, T2 and T3 are double balanced mixers which provide the 45.1MHz intermediate frequency output. The filtered frequency from the front end module is coupled to T2. The 45.1MHz IF output is matched to the input of the 2-pole monolithic filter by L14, L31, C69 and C97. The crystal filter provides a bandwidth of –7.2kHz from the operating frequency providing a high degree of spurious and intermodulation protection. Additionally, a 90MHz trap (XF1) is also placed at the filter output to provide additional attenuation of the second order IMD. The output of the filter is impedance matched by C97 and C69 to the base of the post of filter IF amplifier Q25.

SECOND OSCILLATOR MIXER LIMITER AND FM DETECTOR

The output of the post filter amplifier, Q25, is coupled via C98 to the input of IC5 (MC3371). IC5 is a monolithic single conversion FM transceiver, containing a mixer, the second local oscillator, limiter and quadrature detector. Crystal X1 44.645MHz is used to provide resultant 455kHz signal from the output of the second mixer. The mixer output is then routed to CF1 (455F). These ceramic filters provide the adjacent channel selectivity of 25kHz bandwidth.

RSSI (RECEIVER SIGNAL STRENGTH INDICATOR)

The RSSI signal is output from IC5 on pin 13. As the receiver signals the output, DC voltage is varied as much as receiver signal strength. Also, the DC signal is temperature compensated with a thermistor (TH1).