OPERATIONAL DESCRIPTION OF JASPER

The equipment under test (EUT) is the transmitter of RENESAS, a Tri-band (900/1800/1900) GSM mobile phone. The transmitter operates in a half-duplex system according to the GSM standards.

The majority of the phone circuitry consists of a four device chipset; the HB155165BP Transceiver IC, the RFMD3166 Power Amplifier, the TWL3025BZGMR analog device (IOTA) and the D751749ZHHR digital baseband Processor (CALYPSO). The remainder of the major radio components are the receiver SAW filters, transmit/receive switch and directional coupler. There is also a combination Flash Memory/SRAM IC. The system is powered by a rechargeable lithium-ion battery with a nominal voltage of 3.7 volts.

The transmitter oscillators which comprise the translational loop architecture are internal to the transceiver IC and are phase locked to a 13 MHz reference signal derived from the 26 MHz crystal oscillator. The HD155165BP includes a RFVCO oscillator circuit which operates in the region 3.45GHz~4.0GHz. High-speed dividers are used to generate the 900MHz, 1800MHz and 1900MHz I/Q local oscillator signals for the receiver mixers. In addition, dividers are used to generate the LO signal for the transmit OPLL down-conversion mixer. The IC includes an IFLO oscillator circuit. The oscillator runs around 640~656MHz and provides a signal for the transmit divider chains which generate LO signals at 80~82MHz for the transmit vector modulator. The total divide ratio is 8:1. This guarantees I/Q accuracy of the LO signals for the transmit vector modulator which will ensure good unwanted sideband suppression in the modulator.

The main oscillator signals are amplified by the power amplifier, routed to transmit /receive (T/R) switch and finally delivered to the antenna. The power settings are calibrated at the factory and stored in the flash memory IC. These settings are used as the reference level for the power control loop. Power ramping functions are also controlled by analog device (IOTA).

The GMSK modulation is provided in-loop by quartered I/Q signals which are sent to the transceiver IC from the analog device which converted the digital stream from the digital baseband processor into an analog signal used by the modulator. The RF performance conforms to the ETSI specifications for spectrum due to modulation, transient switching modulation spectrum, power ramp, and power output, as well as

all the other ETSI requirements.

The receiver is a direct-conversion design; the incoming RF signals are mixed directly down to baseband I/Q by the front-end block. This incorporates four LNA and Gilbert Cell mixer blocks optimized for operation at 900MHz, 1800MHz, and 1900MHz respectively. The front-end block is followed by two closely matched baseband amplifier chains. These include distributed low pass filtering and switched –gain amplifiers. In addition, the baseband section integrates A/D and D/A converters which provide on-chip correction of DC offsets. The received signals now at baseband frequencies are routed from the transceiver to the analog device for further processing and ultimately to the baseband processor.

The analog device digitizes the baseband I/Q signals using Sigma-Delta DACs and sends them to the digital baseband processor through a serial digital interface. This IC also has analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to directly interface to the handset speaker and microphone. The voice band Codec section provides a 32 ohm interface to the speaker and microphone and also provides Line In/Out signals for the headset. Additional the mixed signal device contains all required system power supply regulators.

The digital baseband processor handles all physical layer radio control signals and network interfaces. The 32 KHz clock oscillator operates the baseband IC from a backup battery when the main battery is removed. The baseband processor is a dual-core device that splits the processing between a DSP core and an ARM-7 processor. The DSP handles the physical and layer 1 processing, while the ARM7 executes the layer 2 and layer 3 protocols and the man-machine interface (MMI). The dual cores communicate through a dedicated block of dual port memory. It also communicates with the Subscriber Identity Module (SIM) through an interface to the mixed signal device. The baseband processor also communicates to the calibration system or external devices through a digital serial link that is available on the system connector. The other main signals on the system connector include the digital audio interface (DAI) and allows for an external battery charging voltage.

The MMI completes the phone design and includes the displays, keypads, vibration motor, LEDs, speaker, microphone, receiver, and headset.