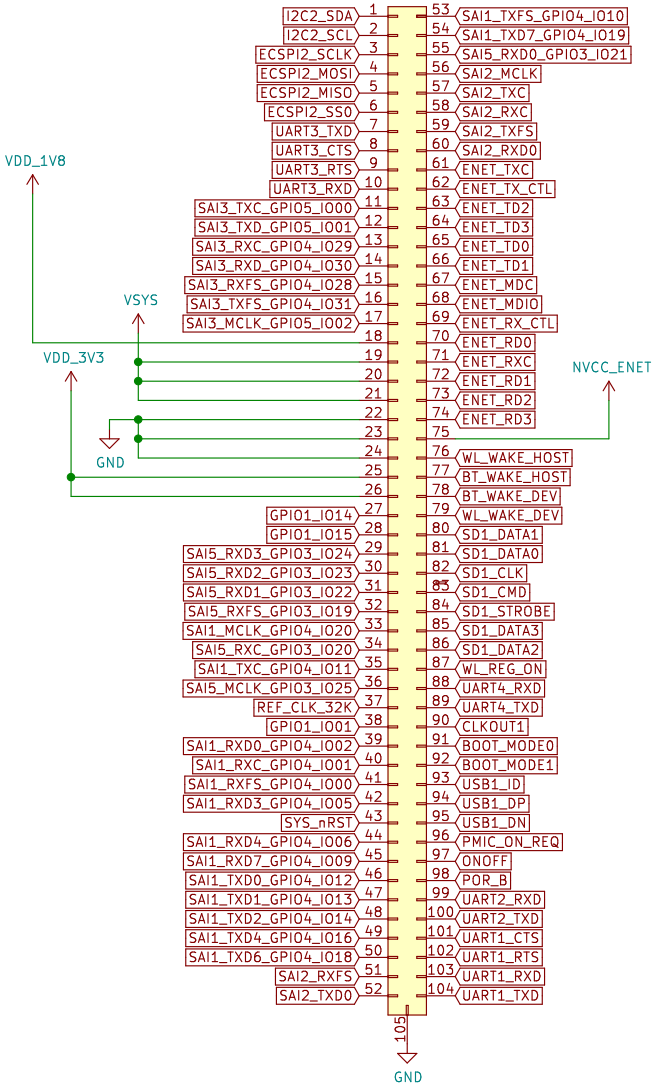
SOM contains iMX8M Mini, LPDDR4 SDRAM, eMMC and PMIC PCA9450DS



SAI1_TXDx & SAI1_RXDx are output only,
because of boot mode at power up

Sheet: eMMC

File: emmc.sch

Sheet: i.MX8M Mini Power

File: MX8MM_PWR.sch

Sheet: SYS PMIC

File: PCA9450.sch

Sheet: i.MX8M Mini PHYs

File: MX8MM_PHYs.sch

Sheet: LPDDR4

File: LPDDR4.sch

Sheet: i.MX8M Mini IO Interface

File: MX8MM_IO.sch

Sheet: Boot Mode

File: boot_mode.sch

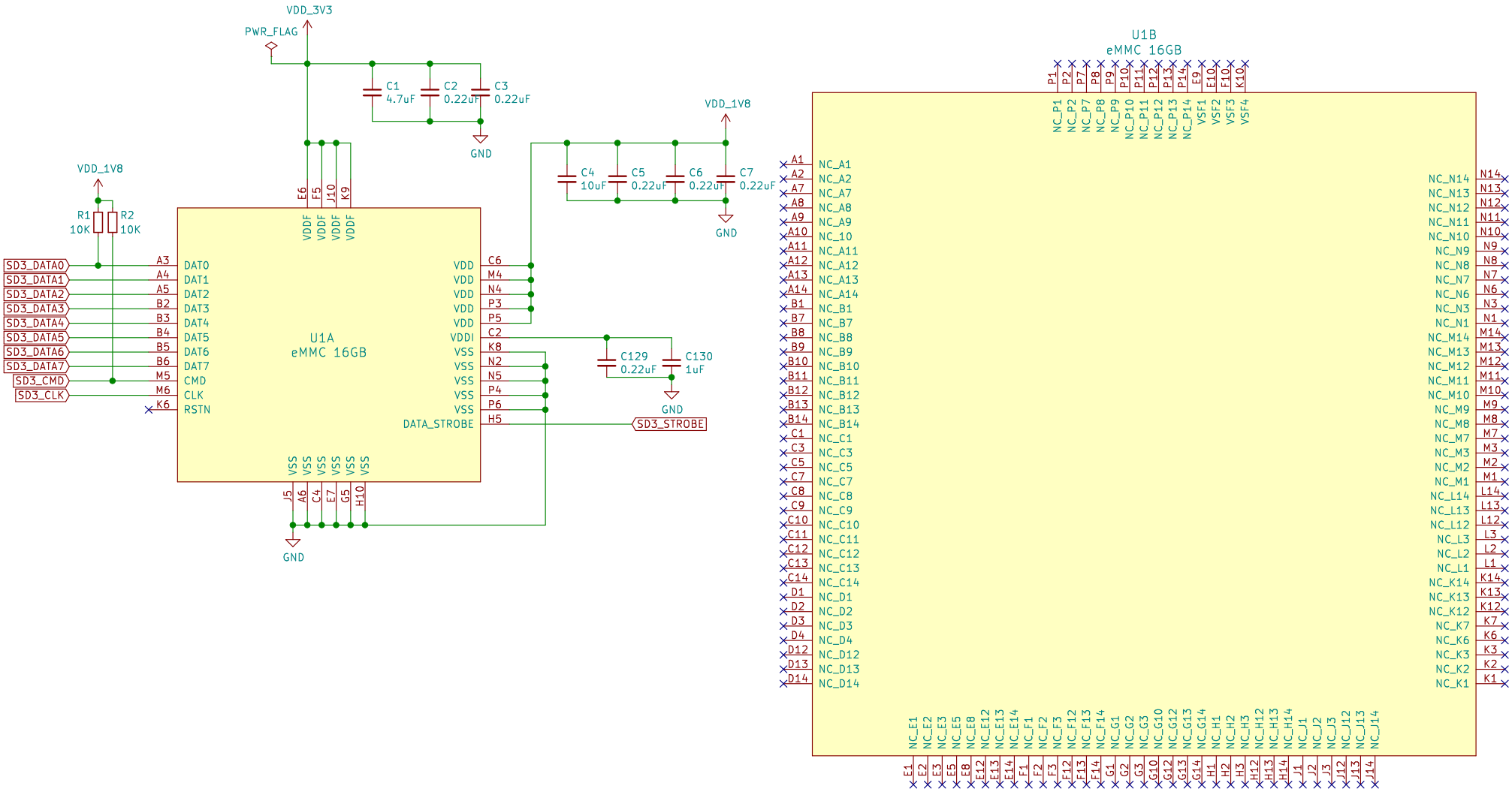
Sheet: i.MX8M Mini MISC

File: MX8MM_MISC.sch

Sheet: /
File: imx8_som.sch

Title:

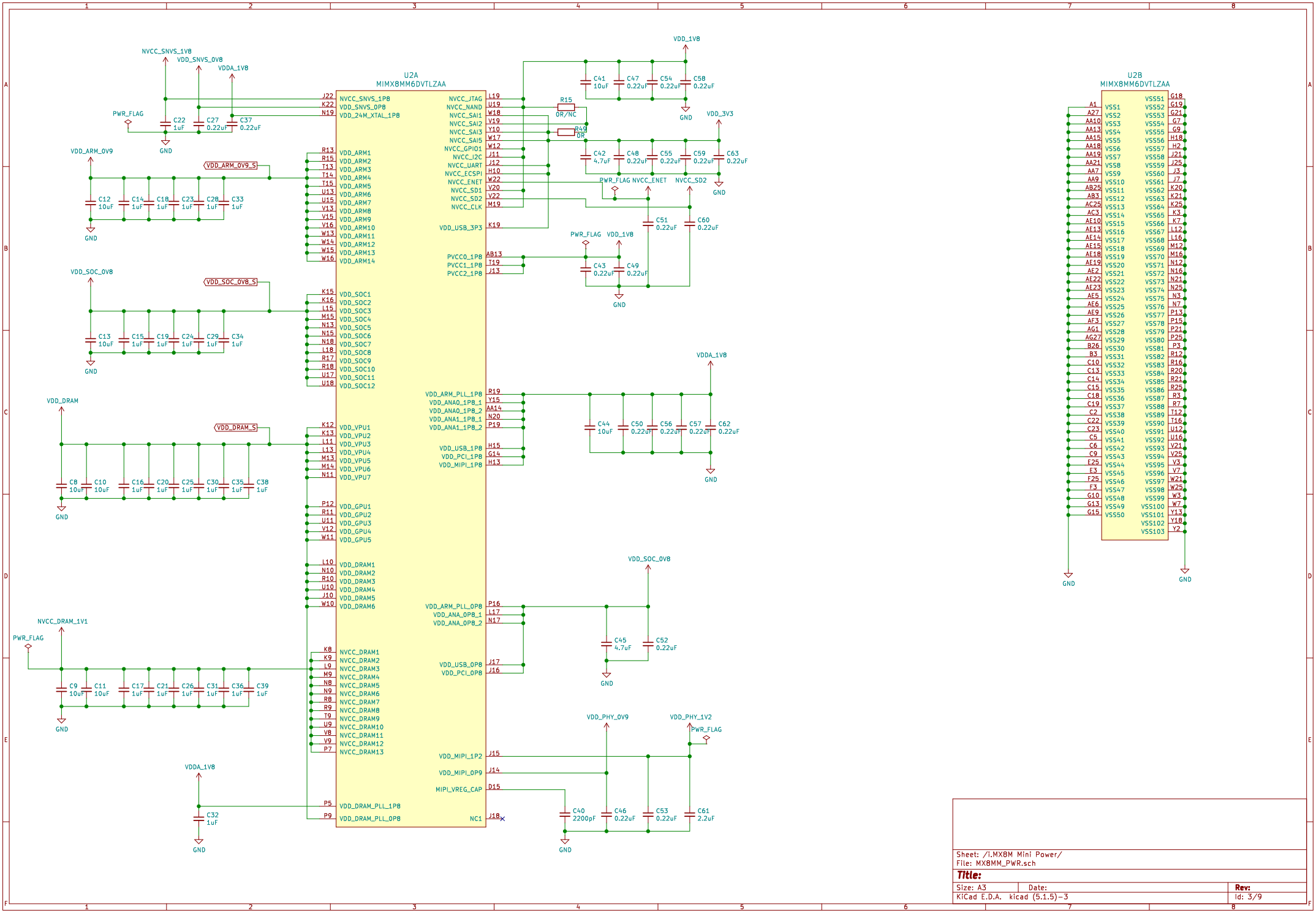
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/9



Sheet: /eMMC/
File: emmc.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/9


U2A
MIMX8MM6DVTLZAA
U2B
MIMX8MM6DVTLZAA
NVCC_SNVS_1V8
VDD_SNVS_0V8
VDDA_1V8
VDD_1V8
VDD_3V3
PWR_FLAG
GND
VDD_ARM_0V9
VDD_ARM_0V9_S
VDD_SOC_0V8
VDD_SOC_0V8_S
VDD_DRAM
VDD_DRAM_S
NVCC_DRAM_1V1
VDD_PHY_0V9
VDD_PHY_1V2
NVCC_ENET
NVCC_SD2
R15
0R/NC
R49
0R
NVCC_SNVS_1P8
VDD_SNVS_0P8
VDD_24M_XTAL_1P8
NVCC_JTAG
NVCC_NAND
NVCC_SAI1
NVCC_SAI2
NVCC_SAI3
NVCC_SAI5
NVCC_GPIO1
NVCC_I2C
NVCC_UART
NVCC_ECSPI
NVCC_ENET
NVCC_SD1
NVCC_SD2
NVCC_CLK
VDD_USB_3P3
PVCC0_1P8
PVCC1_1P8
PVCC2_1P8
VDD_ARM1
VDD_ARM2
VDD_ARM3
VDD_ARM4
VDD_ARM5
VDD_ARM6
VDD_ARM7
VDD_ARM8
VDD_ARM9
VDD_ARM10
VDD_ARM11
VDD_ARM12
VDD_ARM13
VDD_ARM14
VDD_SOC1
VDD_SOC2
VDD_SOC3
VDD_SOC4
VDD_SOC5
VDD_SOC6
VDD_SOC7
VDD_SOC8
VDD_SOC9
VDD_SOC10
VDD_SOC11
VDD_SOC12
VDD_VPU1
VDD_VPU2
VDD_VPU3
VDD_VPU4
VDD_VPU5
VDD_VPU6
VDD_VPU7
VDD_GPU1
VDD_GPU2
VDD_GPU3
VDD_GPU4
VDD_GPU5
VDD_DRAM1
VDD_DRAM2
VDD_DRAM3
VDD_DRAM4
VDD_DRAM5
VDD_DRAM6
NVCC_DRAM1
NVCC_DRAM2
NVCC_DRAM3
NVCC_DRAM4
NVCC_DRAM5
NVCC_DRAM6
NVCC_DRAM7
NVCC_DRAM8
NVCC_DRAM9
NVCC_DRAM10
NVCC_DRAM11
NVCC_DRAM12
NVCC_DRAM13
VDD_DRAM_PLL_1P8
VDD_DRAM_PLL_0P8
VDD_ARM_PLL_1P8
VDD_ANA0_1P8_1
VDD_ANA0_1P8_2
VDD_ANA1_1P8_1
VDD_ANA1_1P8_2
VDD_USB_1P8
VDD_PCI_1P8
VDD_MIPI_1P8
VDD_ARM_PLL_0P8
VDD_ANA_0P8_1
VDD_ANA_0P8_2
VDD_USB_0P8
VDD_PCI_0P8
VDD_MIPI_1P2
VDD_MIPI_0P9
MIPI_VREG_CAP
NC1
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
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VSS91
VSS92
VSS93
VSS94
VSS95
VSS96
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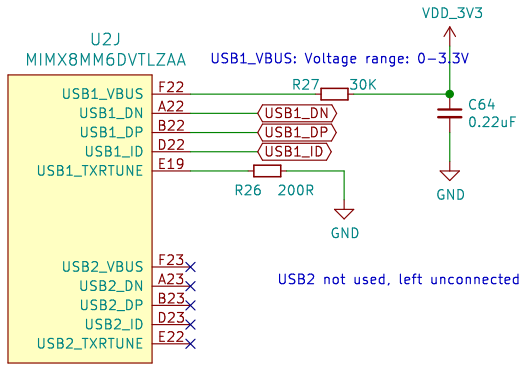
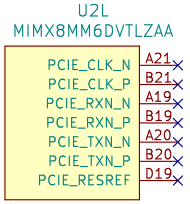
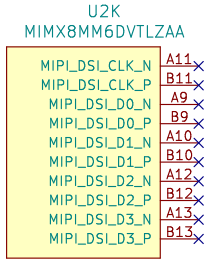
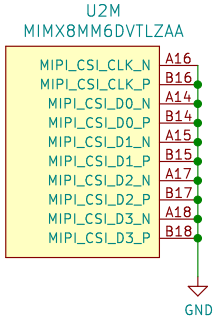
VSS98
VSS99
VSS100
VSS101
VSS102
VSS103
Sheet: /i.MX8M Mini Power/
File: MX8MM_PWR.sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad (5.1.5)-3
Id: 3/9









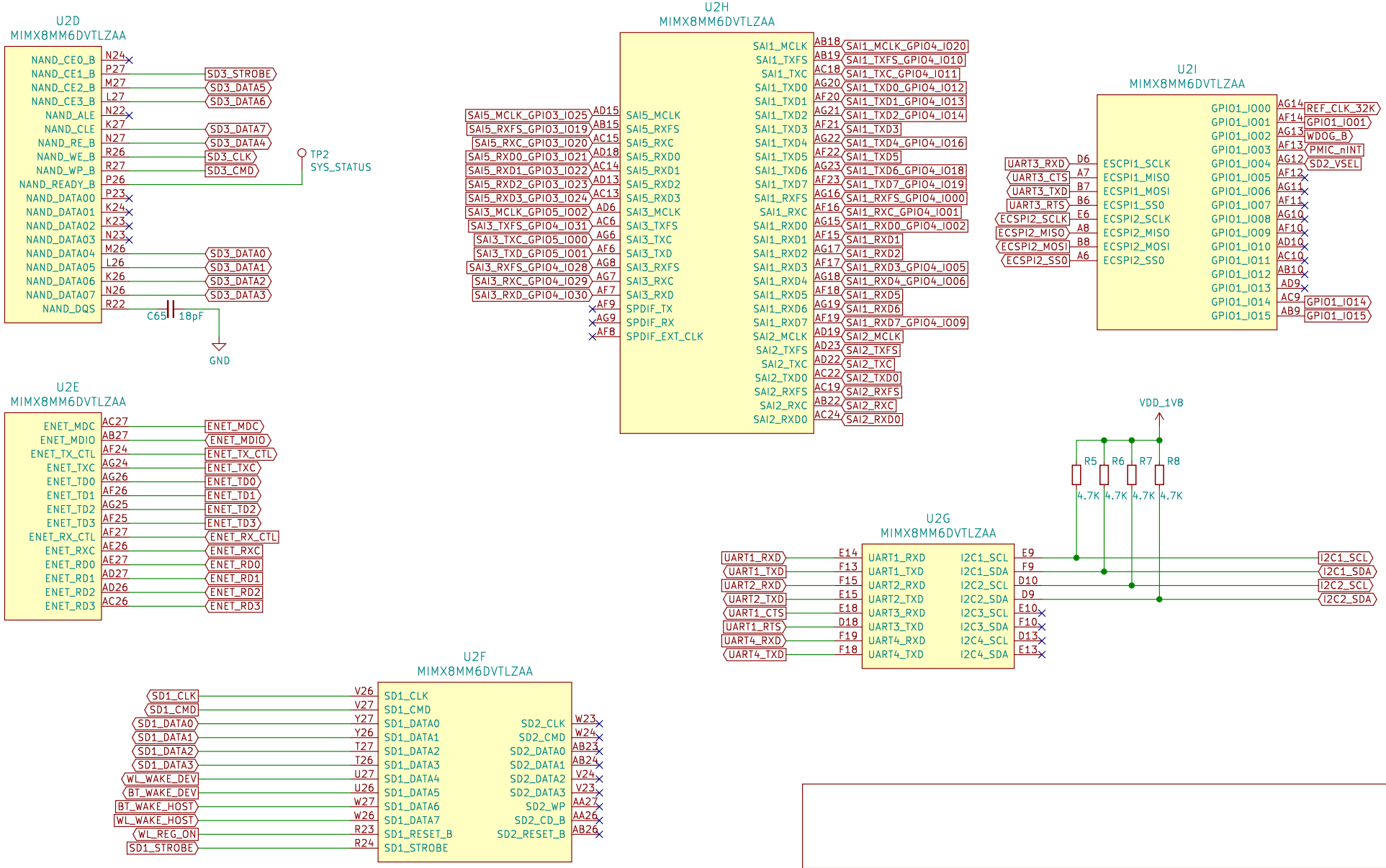
Sheet: /i.MX8M Mini PHYs/
File: MX8MM_PHYs.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/9

i.MX8M Mini IO Interface

SAI1_RXD1, SAI_RXD2, SAI1_RXD5, SAI1_RXD6, SAI1_TXD3, SAI1_TXD5 used in boot-mode selection



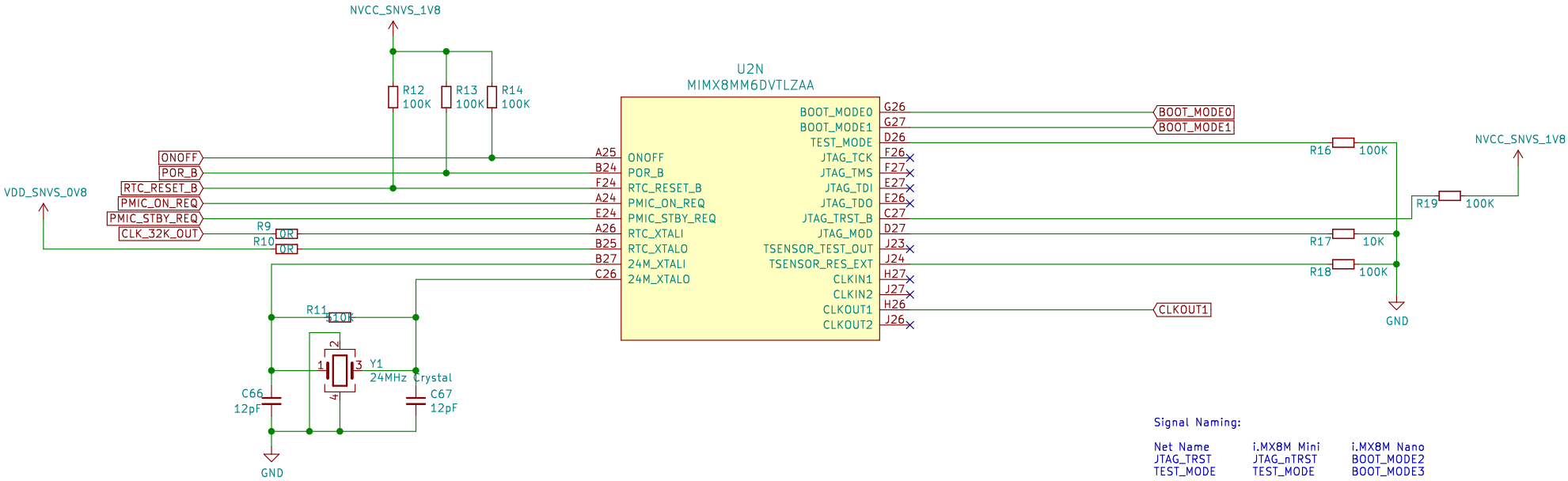
Caution:
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

Sheet: /i.MX8M Mini IO Interface/
File: MX8MM_IO.sch

Title:

Size: A4 | Date: | Rev:
KiCad E.D.A. kicad (5.1.5)-3 | Id: 5/9

i.MX8M Mini MISC



Signal Naming:

Net Name	i.MX8M Mini	i.MX8M Nano
JTAG_TRST	JTAG_nTRST	BOOT_MODE2
TEST_MODE	TEST_MODE	BOOT_MODE3

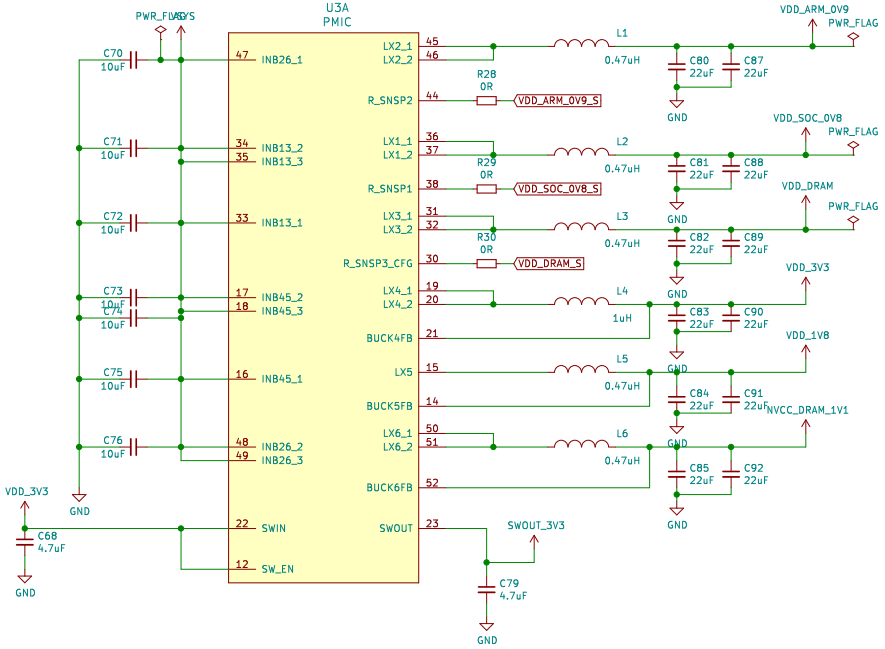
Note:
BOOT_MODE2(JTAG_nTRST) must be pull up on BB for i.MX8M Mini
BOOT_MODE3(TEST_MODE) must be pull down on BB for i.MX8M Mini

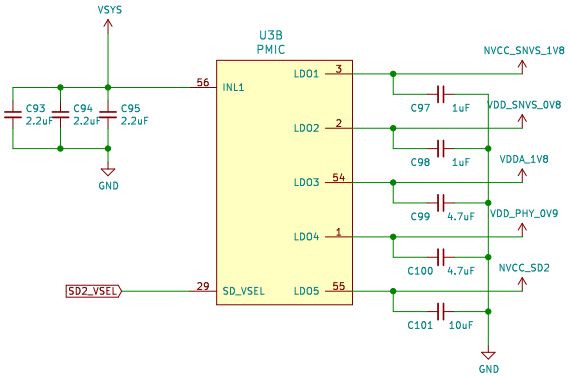
Caution:

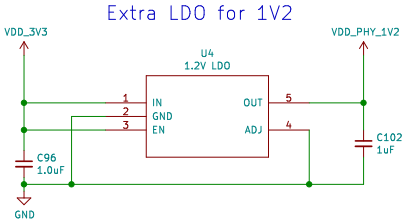
BOOT_MODE0, BOOT_MODE1, JTAG_MOD and TEST_MODE must be pulled to "1101" for i.MX8M Mini to enter Boundary Scan mode.

Sheet: /i.MX8M Mini MISC/	
File: MX8MM_MISC.sch	
Title:	
Size: A4	Date:
KiCad E.D.A. kicad (5.1.5)-3	Id: 6/9
	Rev:

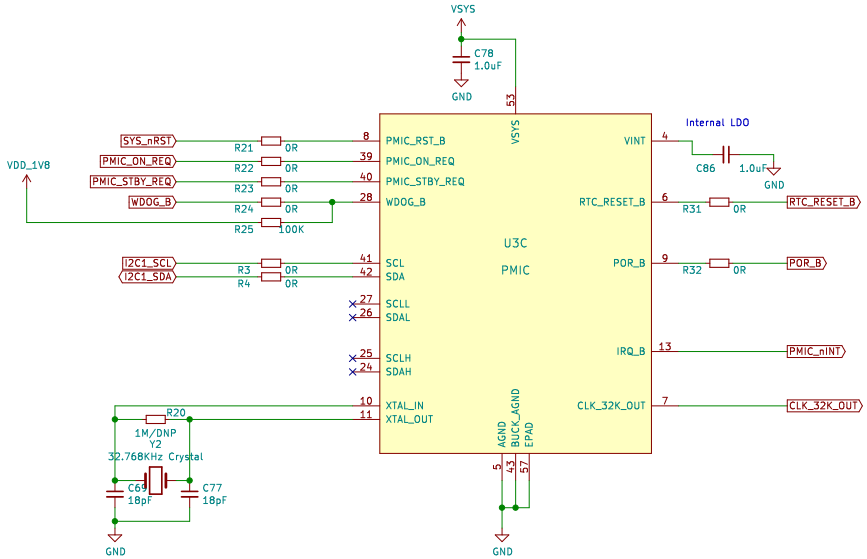
SYS PMIC







Note:
BUCK2 default output voltage is 0.85V for A53 1.2GHz. Software will change it to 0.95V for A53 1.6GHz, 1.0V for A53 1.8GHz.
BUCK3 default output voltage is 0.85V for DDRC 1GHz. Software will change it to 0.9V for DDRC 1.2GHz, 0.95V for DDRC 1.5GHz in SPL before DDR initialization.



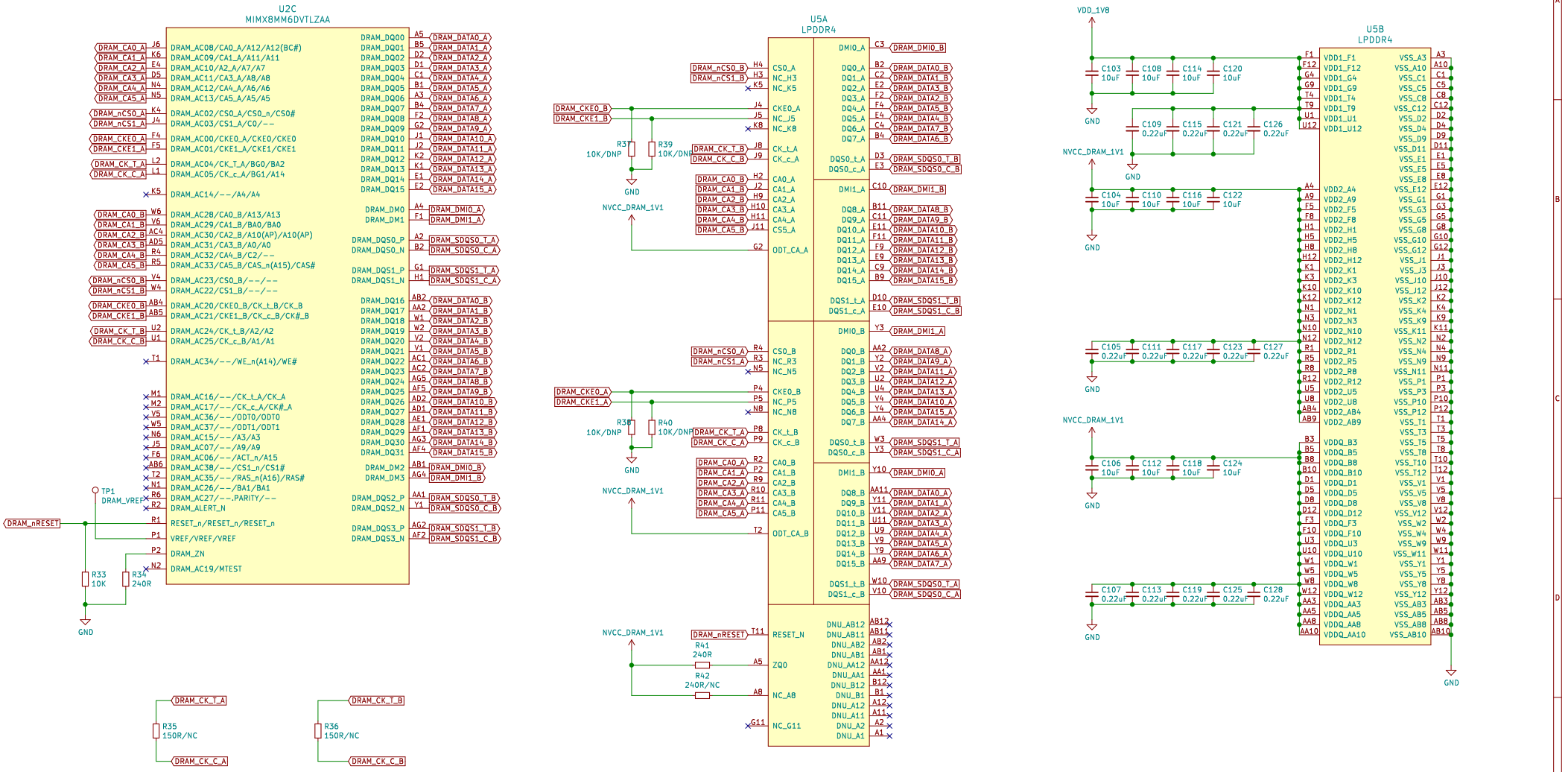
Sheet: /SYS PMIC/
File: PCA9450.sch

Title:

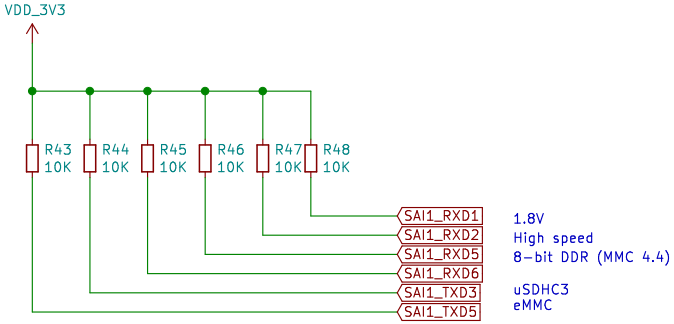
Size: A3 | Date: | **Rev:**
KiCad E.D.A. kicad (5.1.5)-3 | Id: 7/9

Note:
1. PWRON is used as RESET Button as default, need to configure PWRON long push as 10ms/Cold Reset, and disable short push detect!
2. WDOG_B is used as Cold Reset, external pull up is needed. For normal usage, WDOG_B/GPIO1_IO02 has internal pull up, dont need the external PU resistor, but in Boundary Scan mode, this pin is floating, external PU is necessary.

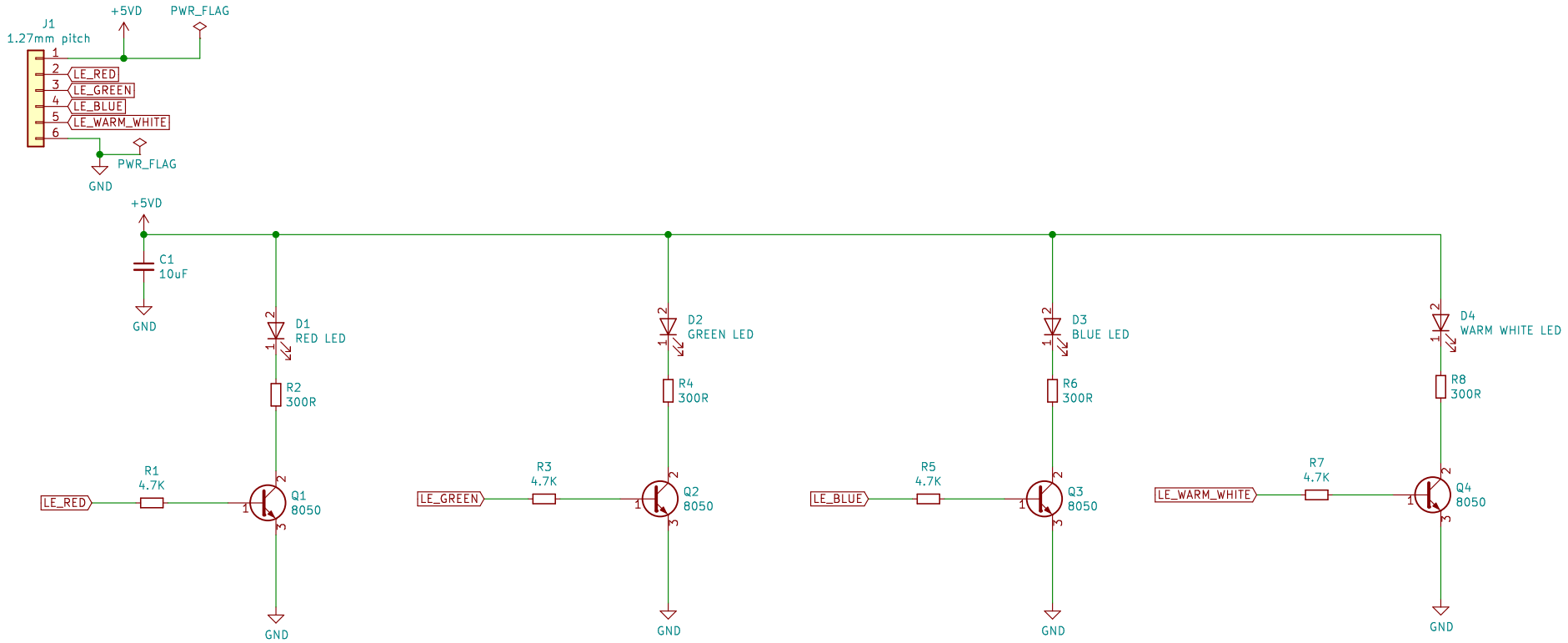
LPDDR4 1GB



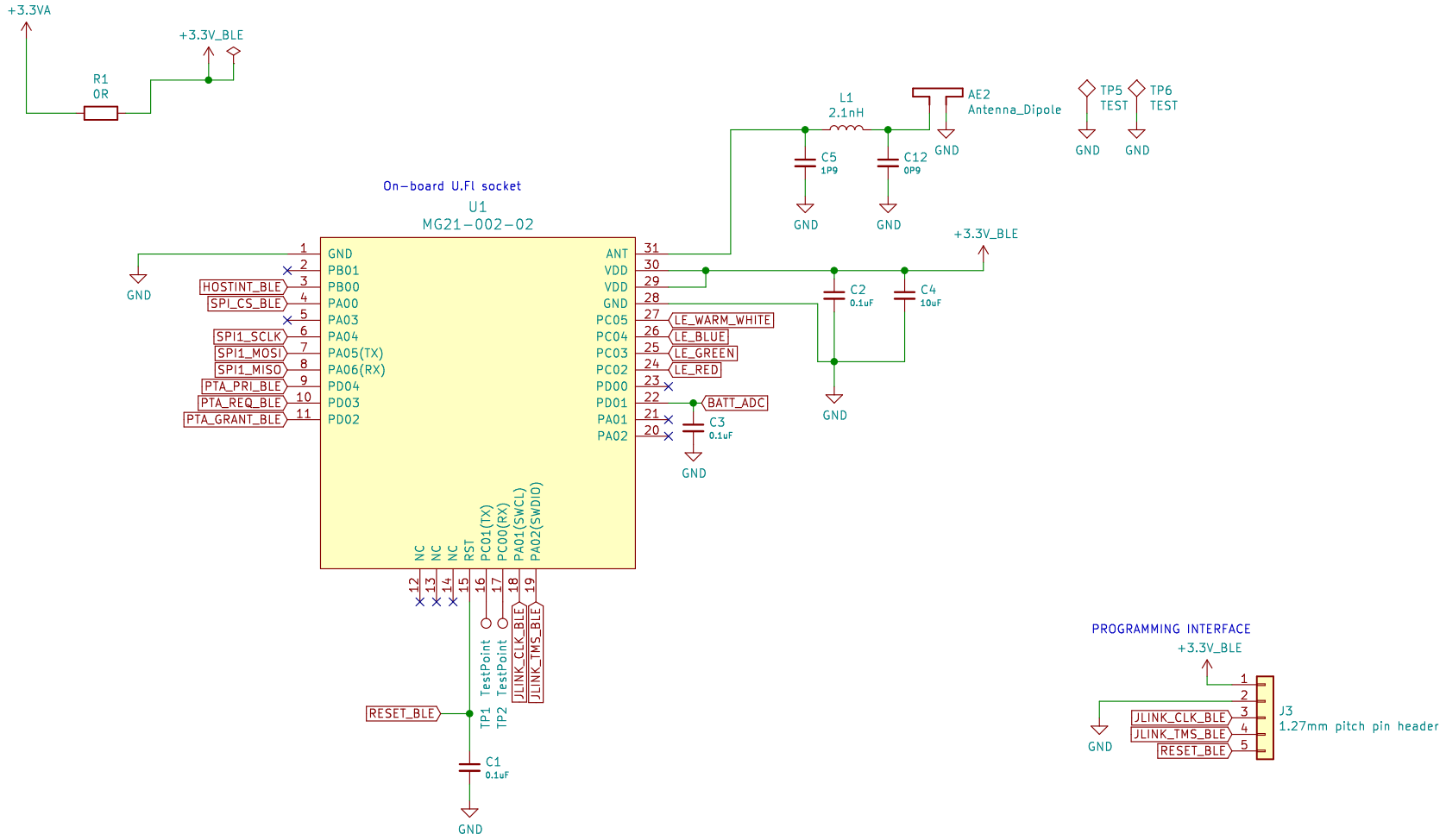
Sheet: /LPDDR4/		
File: LPDDR4.sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 8/9



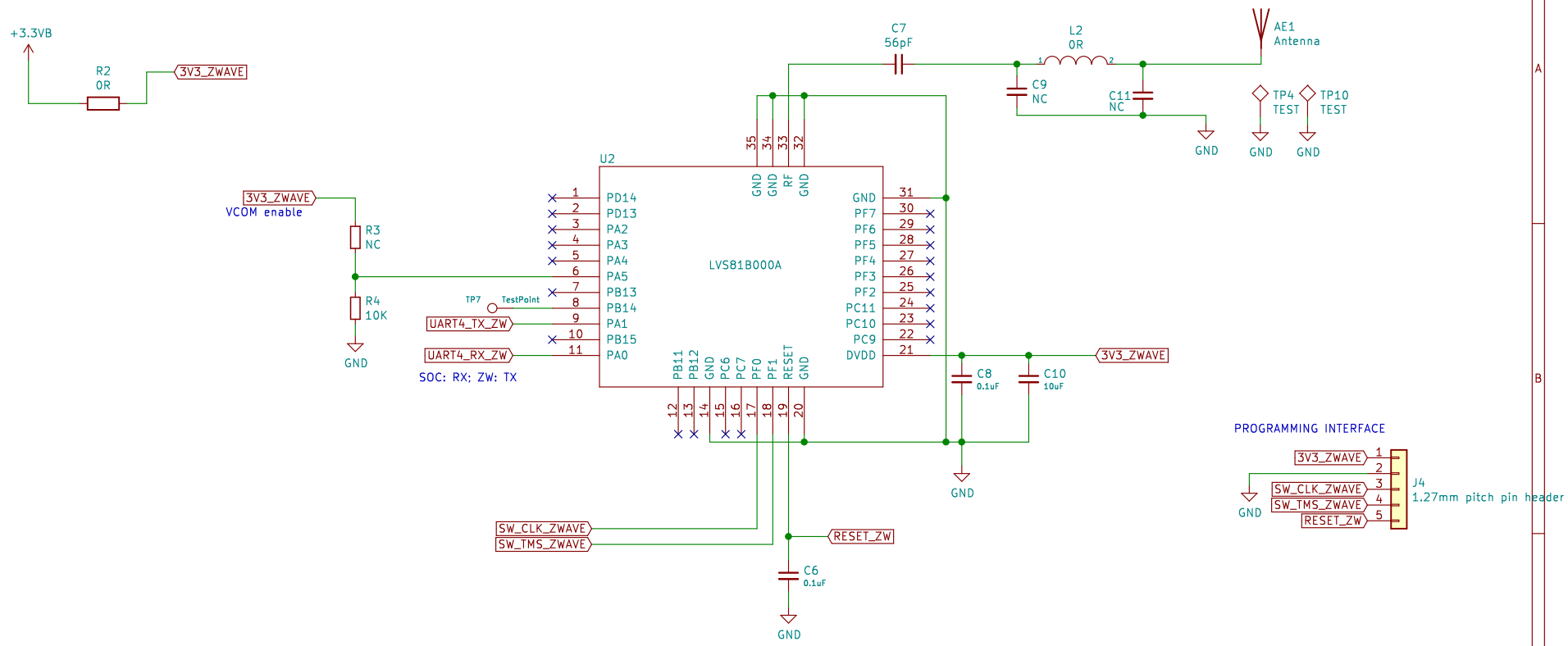
Sheet: /Boot Mode/ File: boot_mode.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/9



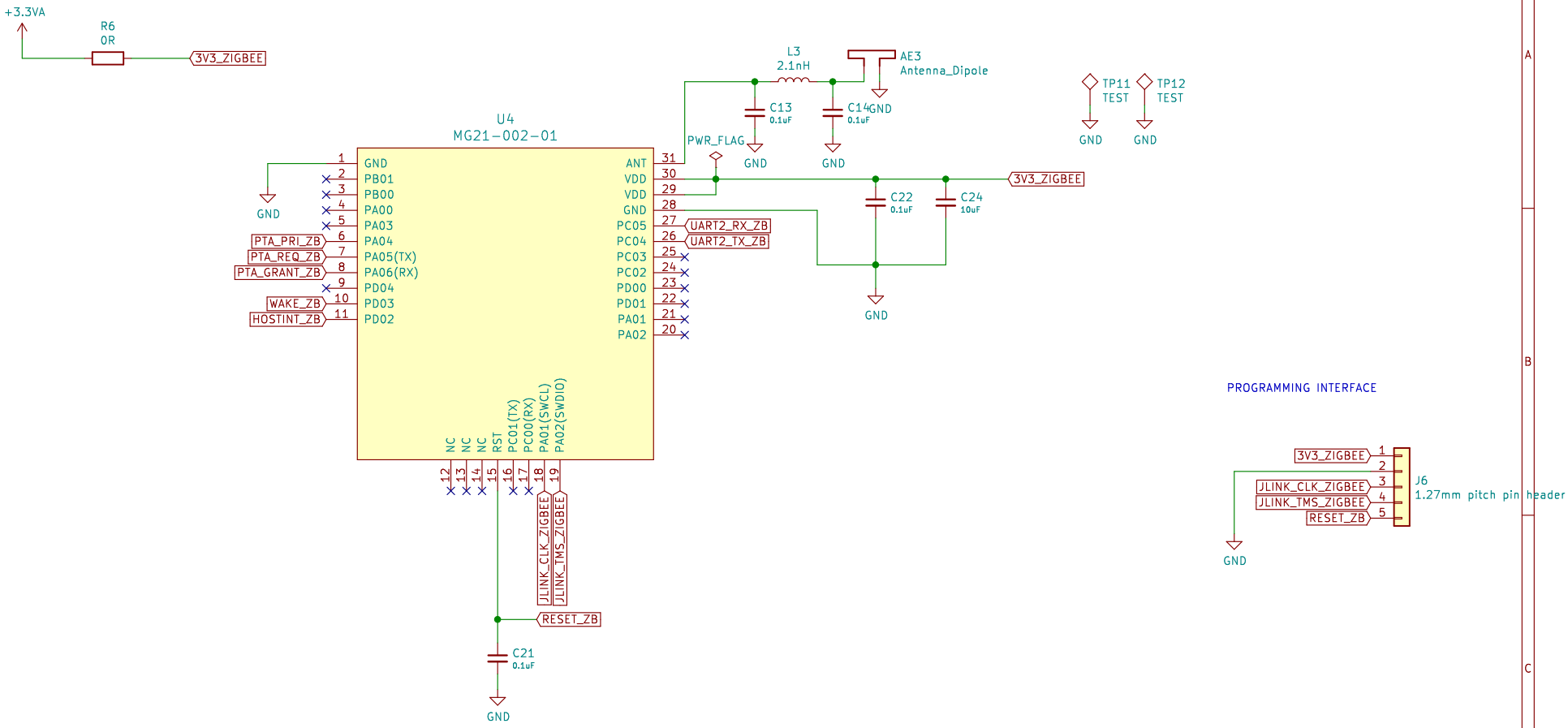
Sheet: /LED_Board/ File: LED_Board.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/2



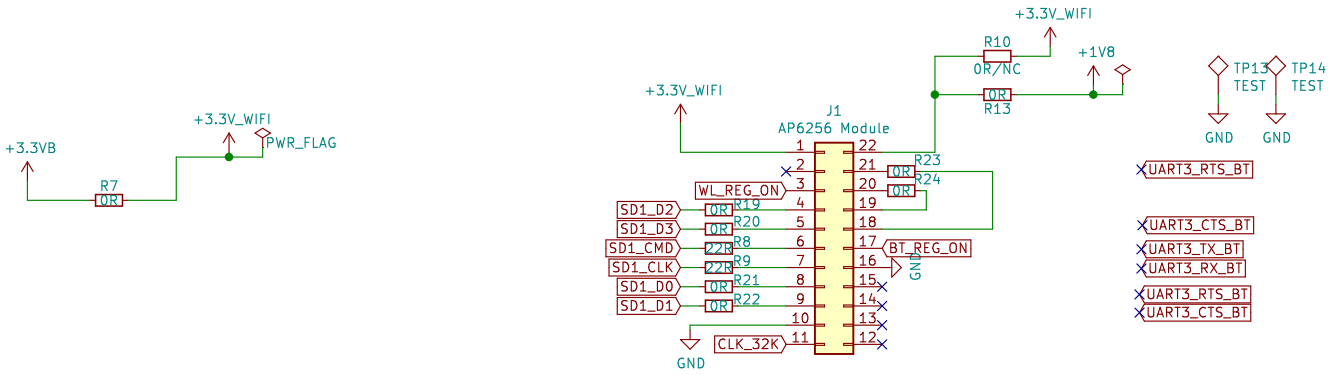
Sheet: /BLE_LDS73B00A/		
File: BLE_LDS73B00A.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/9



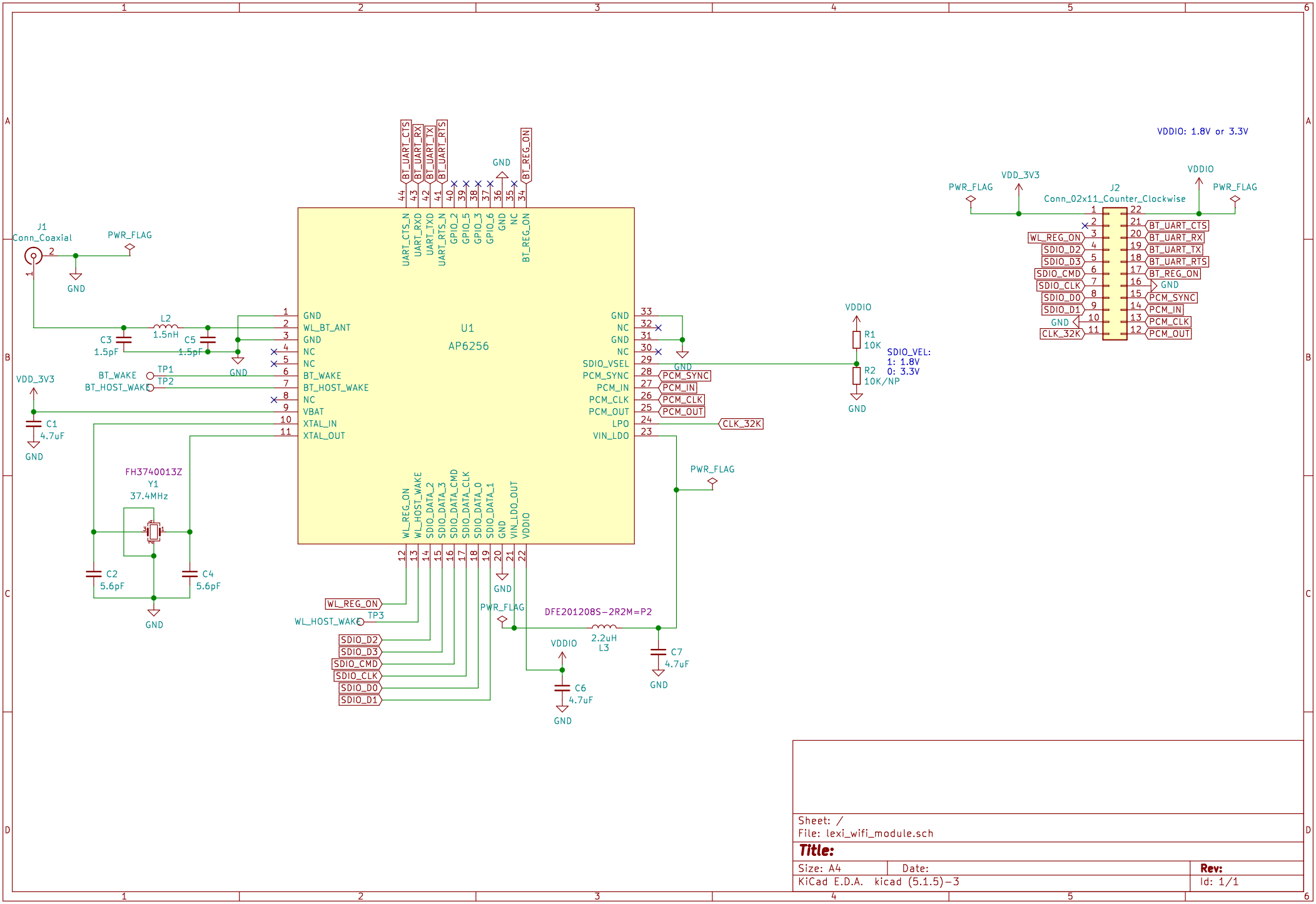
Sheet: /ZWave_LVS81B000A/		
File: ZWave_LVS81B000A.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 3/9



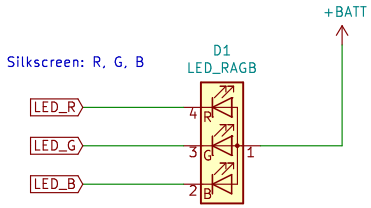
Sheet: /Zigbee_LDS73B000A/		
File: Zigbee_LDS73B00A.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/9

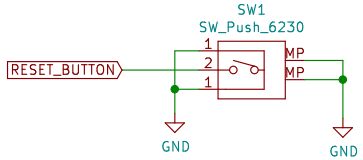


Sheet: /WiFi/		
File: wifi_esp8089.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/9

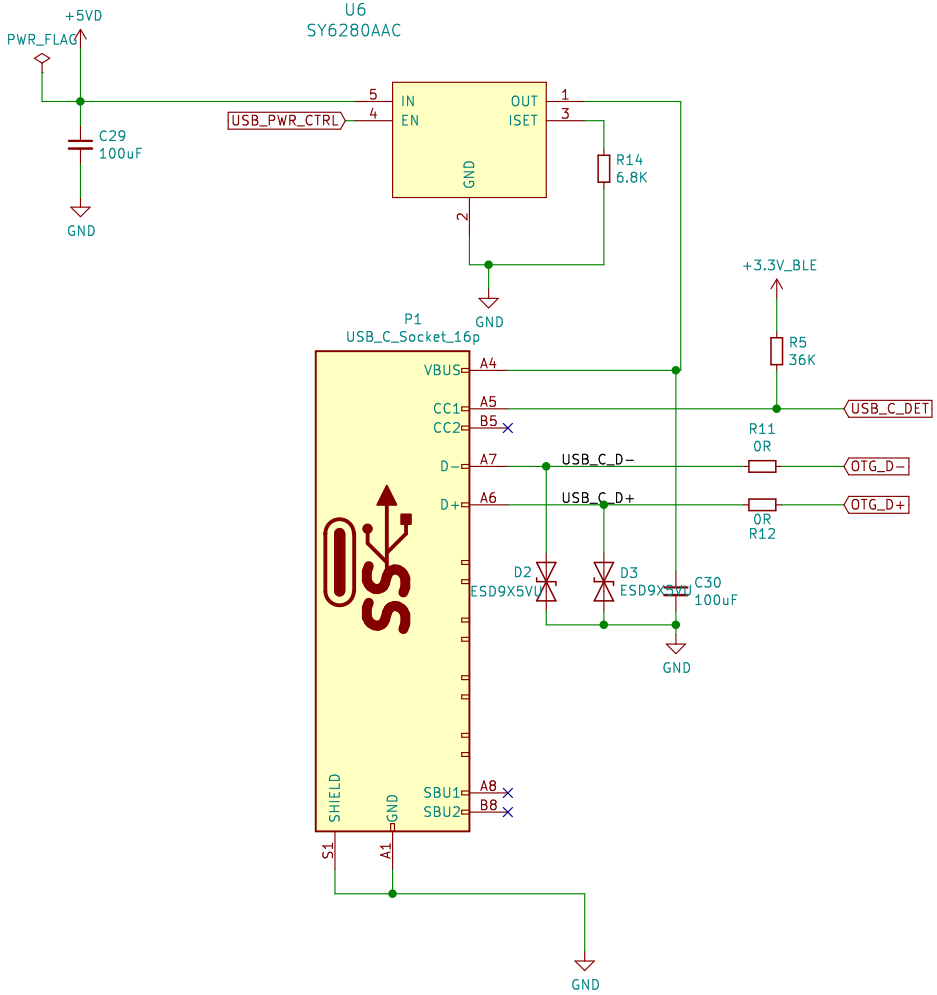


Sheet: /		
File: lexi_wifi_module.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1





Sheet: /indicator_LED/ File: indicator_LED.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 6/9

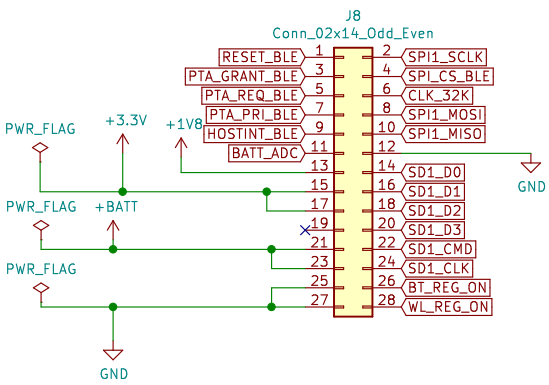


Sheet: /USB_Host/		
File: USB_Host.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 7/9

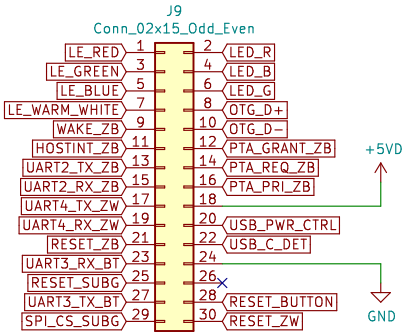
Placement of RF board
(BOTTOM) Mesh – Zigbee – Type C – Indicator RGB LED – reset button (TOP)
(BOTTOM) Zwave – Wifi – Type C – Indicator RGB LED – reset button (TOP)

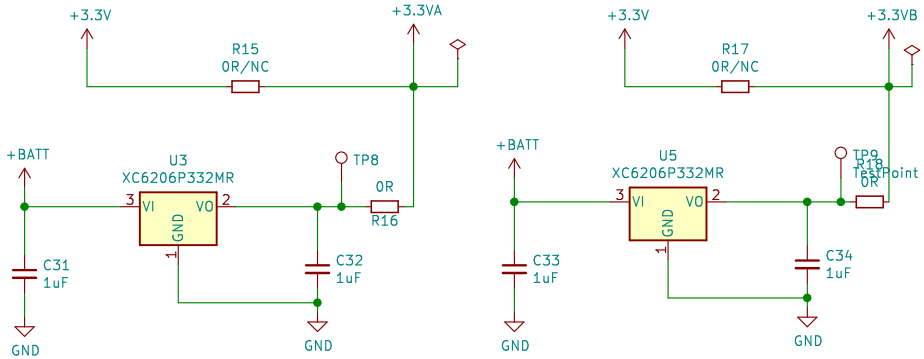
History:
UART3_CTS and UART3_RTS change to chip_cs and RESET_SUBG 28_1_2022

Near Bottom,



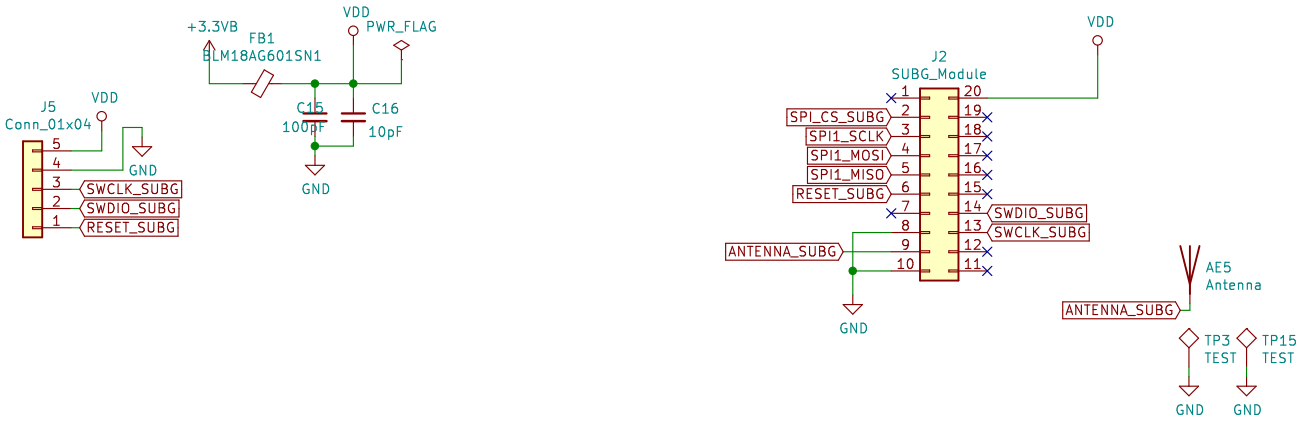
Near TOP, RJ45, Wifi, Type C



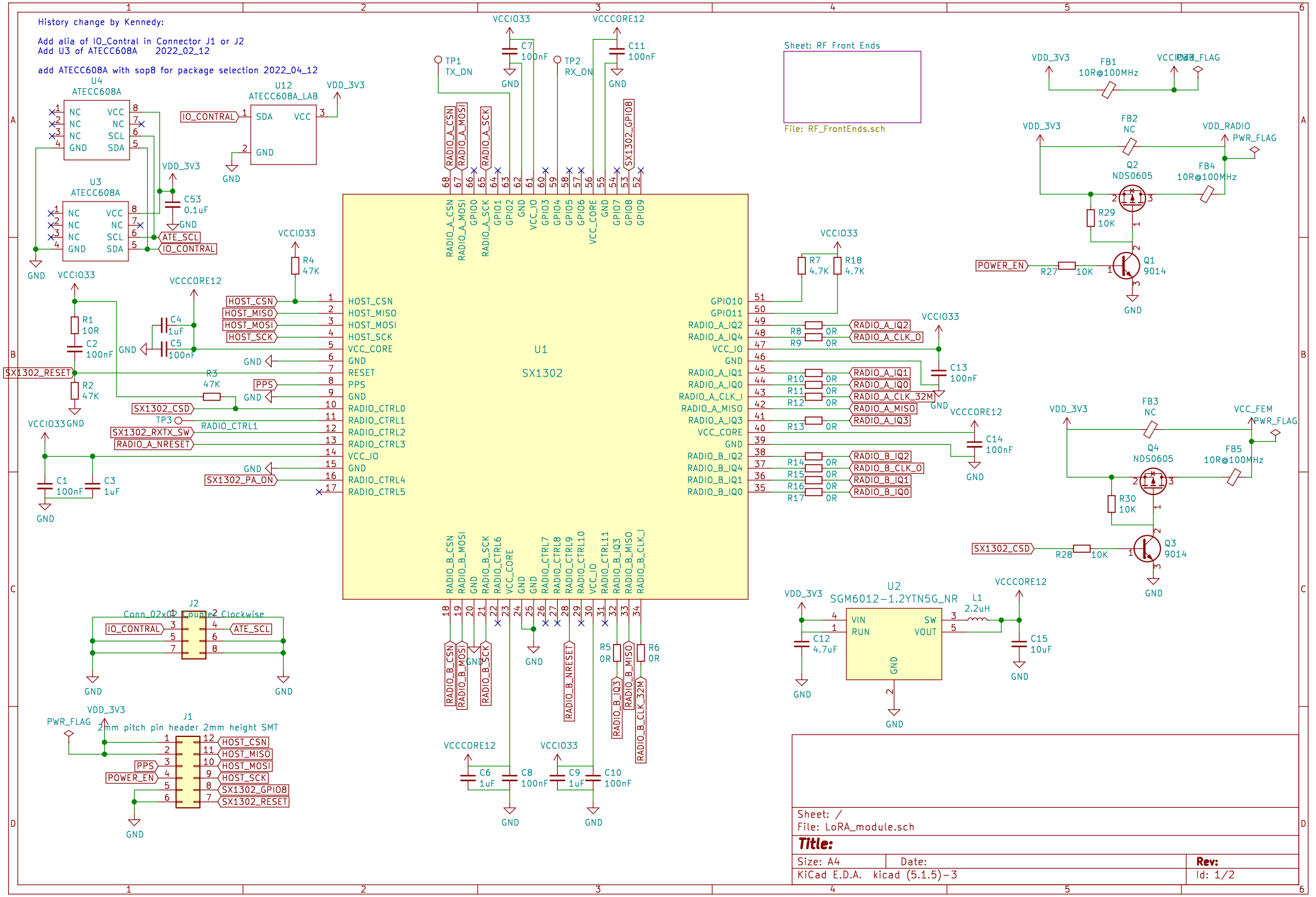


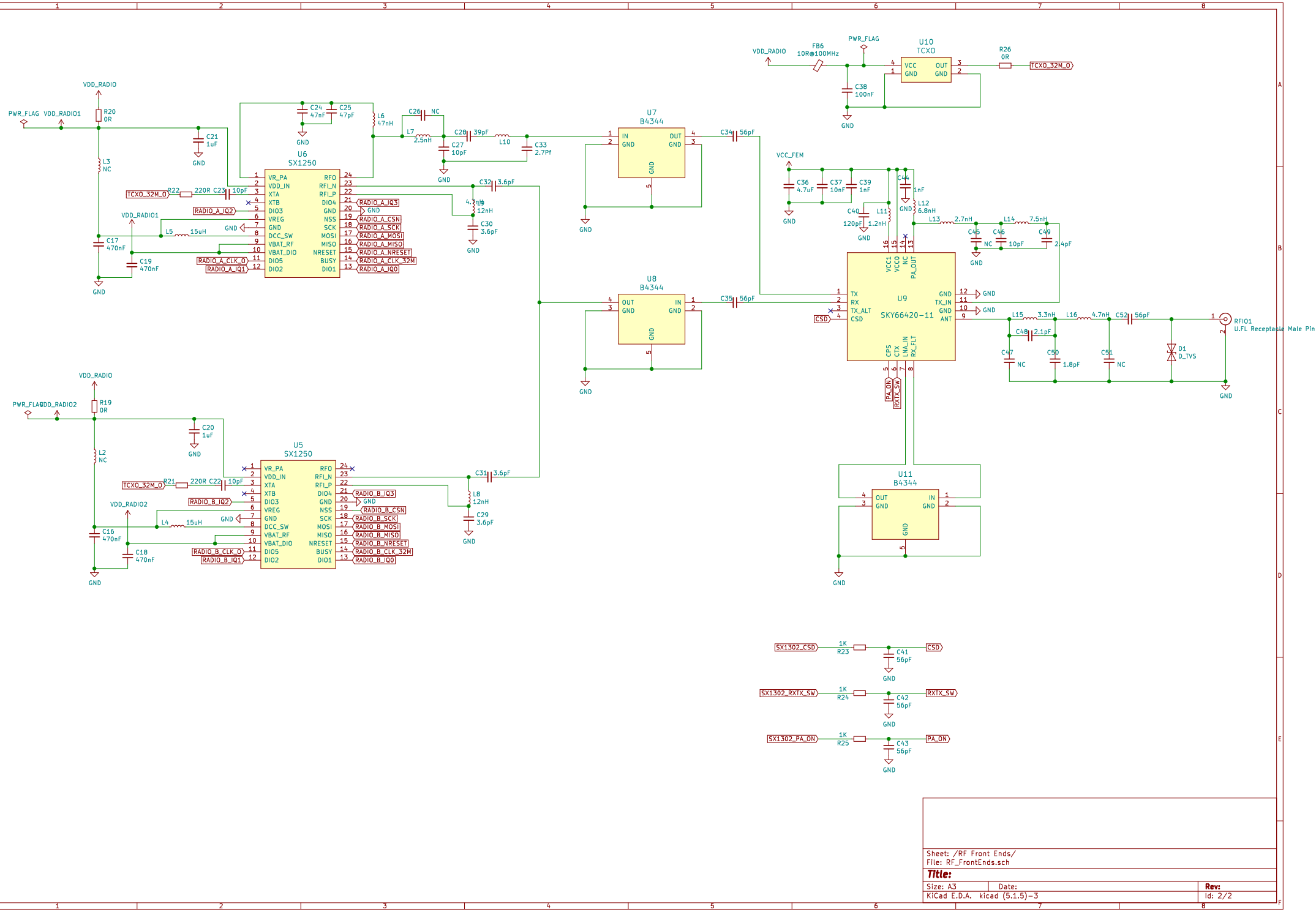
Sheet: /Board_Connector/ File: Board_Connector.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)–3		Id: 8/9

* Add test points on all unused IO



Sheet: /SubG_EFR32FG12/		
File: SubG_EFR32FG12.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/9


History change by Kennedy:
Add alia of IO_Contral in Connector J1 or J2
Add U3 of ATECC608A 2022_02_12
add ATECC608A with sop8 for package selection 2022_04_12
U1
SX1302
U2
SGM6012-1.2YTN5G_NR
U4
ATECC608A
U3
ATECC608A
U12
ATECC608A_LAB
J1
2mm pitch pin header 2mm height SMT
J2
Conn_02x04_Counter_Clockwise
Sheet: RF Front Ends
File: RF_FrontEnds.sch
Sheet: /
File: LoRA_module.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.5)-3
Id: 1/2

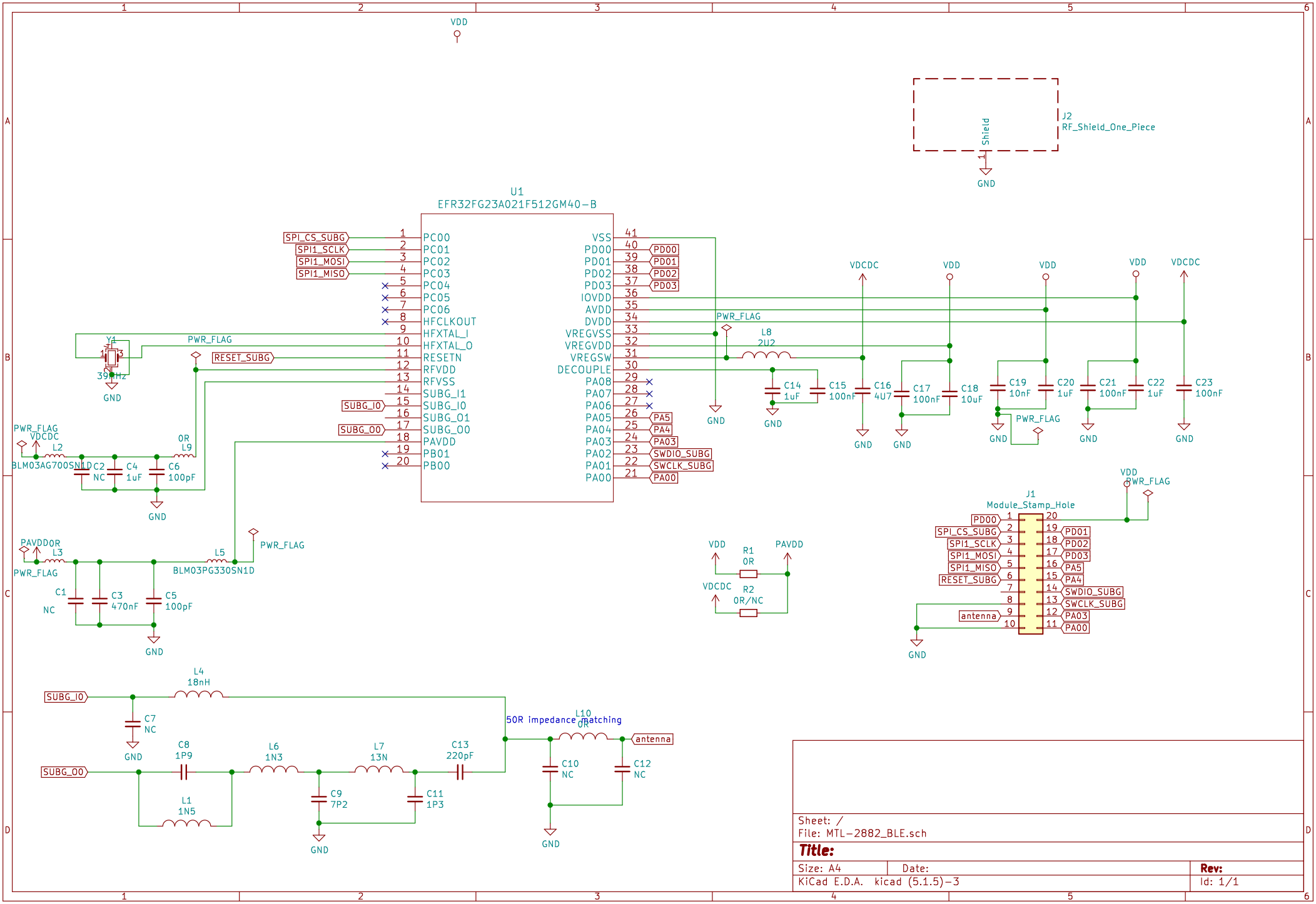


Sheet: /RF Front Ends/
File: RF_FrontEnds.sch

Title:

Size: A3 | Date: | **Rev:**

KiCad E.D.A. kicad (5.1.5)-3 | Id: 2/2



Sheet: /
File: MTL-2882_BLE.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1