General Description

Based on the SmartBond DA14695 Bluetooth® low energy 5.2 system on chip (SoC), the DA14695 Module brings out all the DA14695 hardware features and capabilities. The module integrates all passives, antenna, a 32Mbit QSPI FLASH and is supported by software that is easy to work with. The DA14695 Module targets broad market use and will be certified across regions providing significant reductions in development cost and risks, and time-to-market.

The DA14695 is a multi-core wireless microcontroller, combining the latest Arm® Cortex®-M33 application processor with floating-point unit, advanced power management functionality, a cryptographic security engine, analog and digital peripherals, a dedicated sensor node controller, and a software configurable protocol engine with a radio that is compliant to the Bluetooth® 5.2 low energy standard.

The DA14695 is based on an Arm® Cortex®-M33 CPU with an 8-region MPU and a single-precision FPU offering up to 144 dMIPS. The dedicated application processor executes code from embedded memory (RAM) or external QSPI FLASH via a 16 kB 4-way associative cache controller, which is equipped with an on-the-fly decrypting capability without extra wait states.

Bluetooth® 5.2 connectivity is guaranteed by a new software-configurable Bluetooth® low energy protocol engine (MAC) with an ultra-low-power radio transceiver, capable of +6 dBm output power and -96 dBm sensitivity offering a total link budget of 102 dB.

An optimized programmable sensor node controller allows sensor node operations and data acquisition without CPU intervention, achieving best-in-class power consumption. The advanced power management unit of the DA14695 enables it to run on primary and secondary batteries, as well as provide power to external devices through the integrated SIMO DCDC and integrated LDOs. The on-chip JEITA-compliant hardware charger makes it possible to natively charge rechargeable batteries over USB. A variety of standard and advanced peripherals enable interaction with other system components and the development of advanced user interfaces and feature-rich applications.

Key Features

- Bluetooth
  - Compatible with Bluetooth® 5.2, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
  - Supports up to eight connections
  - Supports up to 2 Mbps throughput
  - Renesas registered BD address preprogrammed in OTP
- Processing and memories
  - 32 kHz up to 96 MHz 32-bit Arm Cortex-M33 with 16 kB, 4-way associative cache and FPU
  - A flexible and configurable Bluetooth® LE MAC engine implementing the controller stack up to HCI
  - A sensor node controller running uCode for sensors manipulation
  - 4 MB onboard FLASH
  - 512 kB RAM
  - 128 kB ROM
  - 4 kB OTP
- Current Consumption
  - 1.8 mA RX at V_{BAT} = 3 V
  - 3 mA TX at VBAT = 3 V and 0 dBm
  - 18.4 µA at sleep with all RAM retained
- Radio
  - Programmable RF transmit power from -18 to +6 dBm
  - -96 dBm receiver sensitivity
- Interfaces
  - Up to 40 General Purpose IOs
  - Decrypt-on-the-fly QSPI FLASH interface and Separate QSPI PSRAM interface
  - SPI LCD Controller with own DMA
  - 4-channels 10-bit SAR ADC, 3.4 Msamples/sec
  - 4-channels 14-bit ΣΔ ADC, 1000 samples/sec
  - 2 x general purpose timers with PWM
  - 3 x UARTs up to 1 Mbps, one UART extended to support ISO7816
  - 2 x SPI+™ controllers

- 2 x I2C controllers at 100 kHz, 400 kHz, or 3.4 MHz
- 1 x PDM interface with HW sample rate converter
- 1 x I2S/PCM master/slave interface up to eight channels
- USB 1.1 Full Speed device interface

- Power Management
  - Operating range: from 2.4 V to 4.75 V
  - Hardware charger (up to 5.0 V) with programmable curves and JEITA support
  - Programmable thresholds for brownout detection
- Other
  - Real Time Clock
  - Trimmed 32 MHz Crystal
- Packaging
  - 15.85 mm x 20 mm x 2.5 mm package
- Module software Development Kit
  - SDK10 support
  - MicroPython/Zephyr support
- Module software tools
  - Flash/OTP programmer
  - SUOTA support
  - Battery Life Estimation
  - Data Rate Monitoring
  - Real-Time Power Profiling
  - Production Line Testing
- Standards conformance
  - BT SIG QDID 149229
  - Europe (CE/RED)
  - US (FCC)
  - Canada
  - Japan
  - South Korea
  - Taiwan
  - South Africa
  - Brazil
  - China
  - Thailand
  - India

Applications

- Beacons
- Positioning
- Proximity tags
- Low Power Sensors
- Commissioning/Provisioning
- RF pipe
- Industrial applications
- Data acquisition
- Wellness
- Infotainment
- IoT
- Robotics
- Gaming

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1 Terms and Definitions

ADC	Analog-to-digital converter
DIO	Digital input-output
MSL	Moisture sensitivity level
NTC	Negative temperature coefficient
PCB	Printed circuit board
RDS	Reduced driving strength
VSWR	Voltage standing wave ratio

2 References

[1] DA1469x, Datasheet, Renesas Electronics.
[2] UM-B-092, DA1469x Software Platform Reference Manual, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3 Block Diagram

The DA14695 SmartBond™ Module is based on the Renesas Electronics DA14695 SoC. With an integrated 32 Mbit QSPI Flash, 32 MHz XTAL and a printed antenna, the module enables a faster time to market at reduced development costs.

The module, as seen in Figure 1, is comprised of:

- A 32 Mbit QSPI FLASH (U2)
- A 32 MHz XTAL (X1)
- A 32 kHz XTAL (X2)
- Ten decoupling capacitors (Cx)
- A power inductor (L2)
- A CLC filter and matching components for the printed antenna

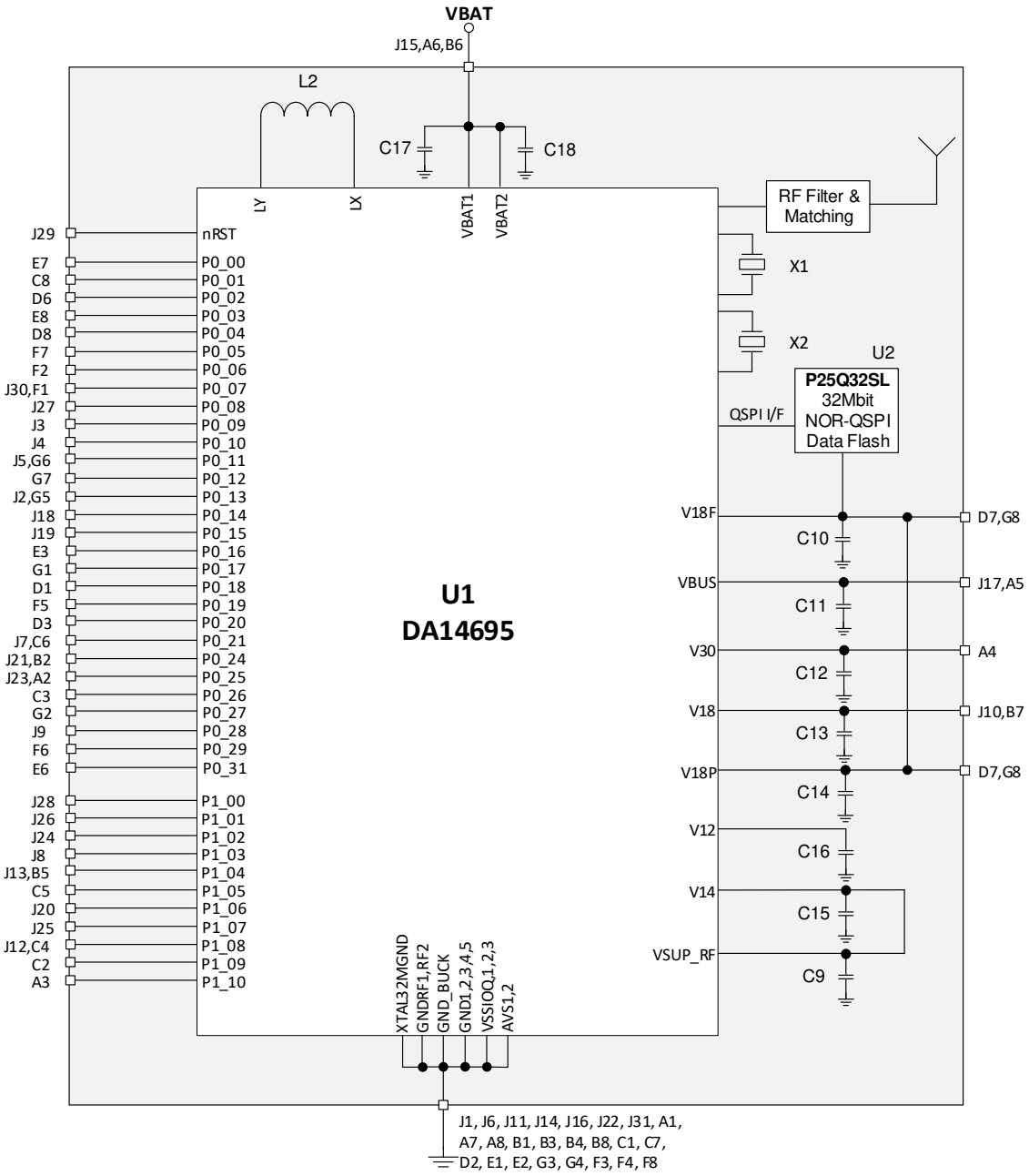

Figure 1: DA14695 SmartBond™ Module Block Diagram

4 Pinout

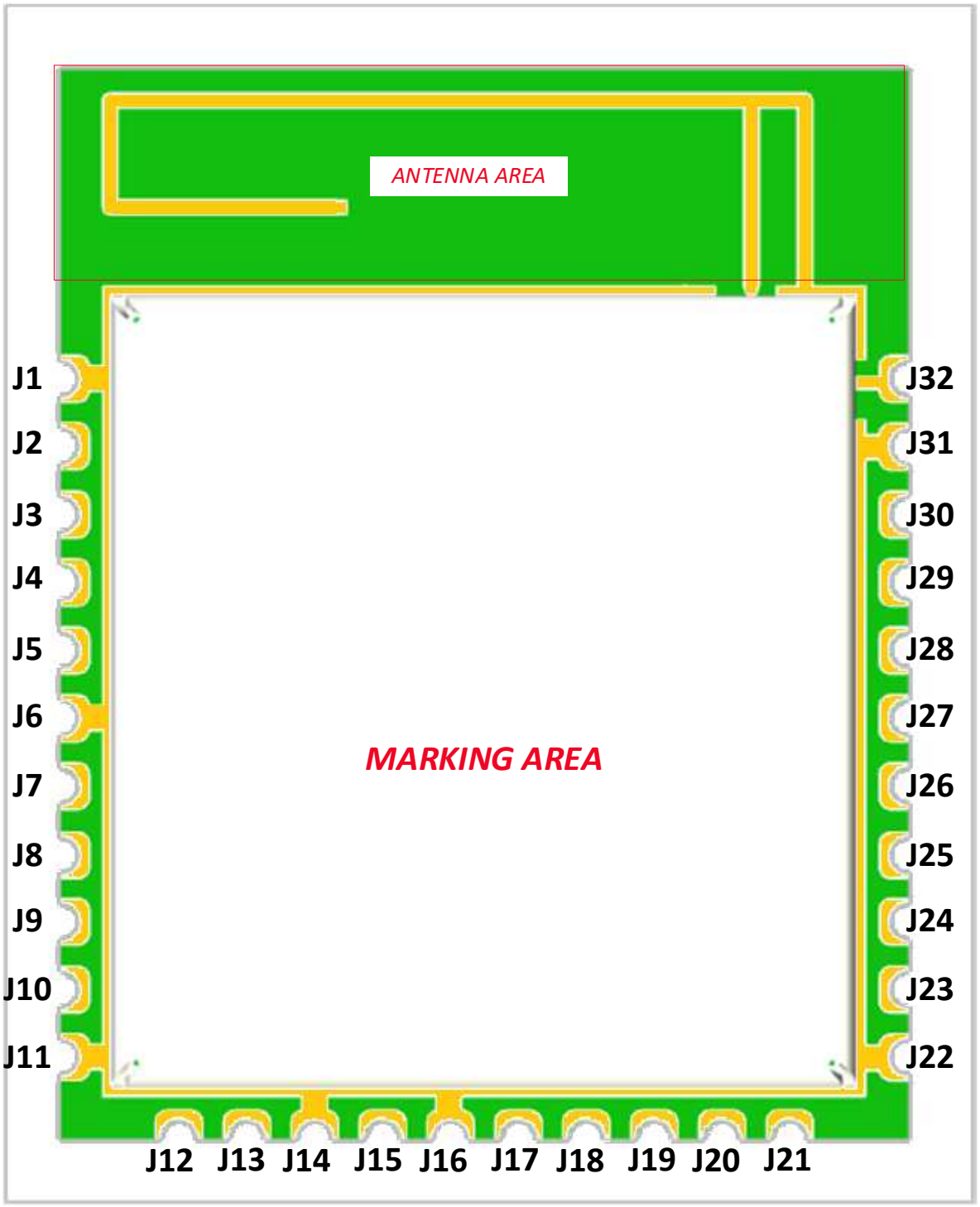

Figure 2: Pinout Diagram – Top View

Table 1: Edge Pins Description

Pin No	Pin Name	Type	Drive (mA)	Reset State	Description
J1	GND	-			Ground

Pin No	Pin Name	Type	Drive (mA)	Reset State	Description
J2	P0_13	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	CMAC_SWCLK	DI			INPUT. Arm Cortex-M0+ JTAG clock signal.
J3	P0_09	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC3	AI			INPUT. Analog to Digital Converter input 3.
	SDADC3	AI			INPUT. Analog input for the ΣΔ ADC, channel 3.
	UART Boot TX	DO			OUTPUT. UART Transmit data output during boot.
J4	P0_10	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	M33_SWDIO	DIO			INPUT/OUTPUT. Arm Cortex-M33 JTAG data I/O signal.
J5	P0_11	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	M33_SWCLK	DI			INPUT. Arm Cortex-M33 JTAG clock signal.
J6	GND	-			Ground
J7	P0_21	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J8	P1_03	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	SWDIO	DIO			INPUT/OUTPUT. JTAG Data input/output. Bidirectional data and control communication (by default).
J9	P0_28	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J10	V18	AIO			OUTPUT. 1.8 V power rail. Maximum current 50 mA.
J11	GND	-			Ground
J12	P1_08	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate

Pin No	Pin Name	Type	Drive (mA)	Reset State	Description
					function nodes. Contains state retention mechanism during power down.
J13	P1_04	DIO	4.8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J14	GND	-			Ground
J15	VBAT	AIO			INPUT. Battery connection.
J16	GND	-			Ground
J17	VBUS	AI			INPUT. USB bus voltage. INPUT. Battery charge voltage.
J18	P0_14	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	USBp	AIO			INPUT/OUTPUT. Analog USB Full Speed D+ signal.
	XTAL32k	DO			OUTPUT. XTAL32k clock signal output (square wave).
J19	P0_15	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	USBm	AIO			INPUT/OUTPUT. Analog USB Full Speed D- signal.
	DIVN	DO			OUTPUT. DIVN clock signal output (square wave).
J20	P1_06	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	Timer2.PWM	DO			OUTPUT. Timer2/PWM output (PWM2) in Sleep mode.
J21	P0_24	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J22	GND	-			Ground
J23	P0_25	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_1	AI			INPUT. Analog input for the general-purpose ADC, channel 1.
	SDADC_1	AI			INPUT. Analog input for the ΣΔ ADC, channel 1.

Pin No	Pin Name	Type	Drive (mA)	Reset State	Description
J24	P1_02	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J25	P1_07	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J26	P1_01	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	Timer.PWM	DO			OUTPUT. Timer/PWM output (PWM) in Sleep mode.
J27	P0_08	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_2	AI			INPUT. Analog input for the general-purpose ADC, channel 2.
	SDADC_2	AI			INPUT. Analog input for the ΣΔ ADC, channel 2.
	UART Boot RX	DI			INPUT. UART Receive data input during boot.
J28	P1_00	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J29	RSTn	AI			INPUT. Reset signal (active LOW).
J30	P0_07	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	NTC Input	AI			INPUT. Analog input for battery NTC (feedback).
J31	GND	-			Ground
J32	Not connected	-			Keep Floating

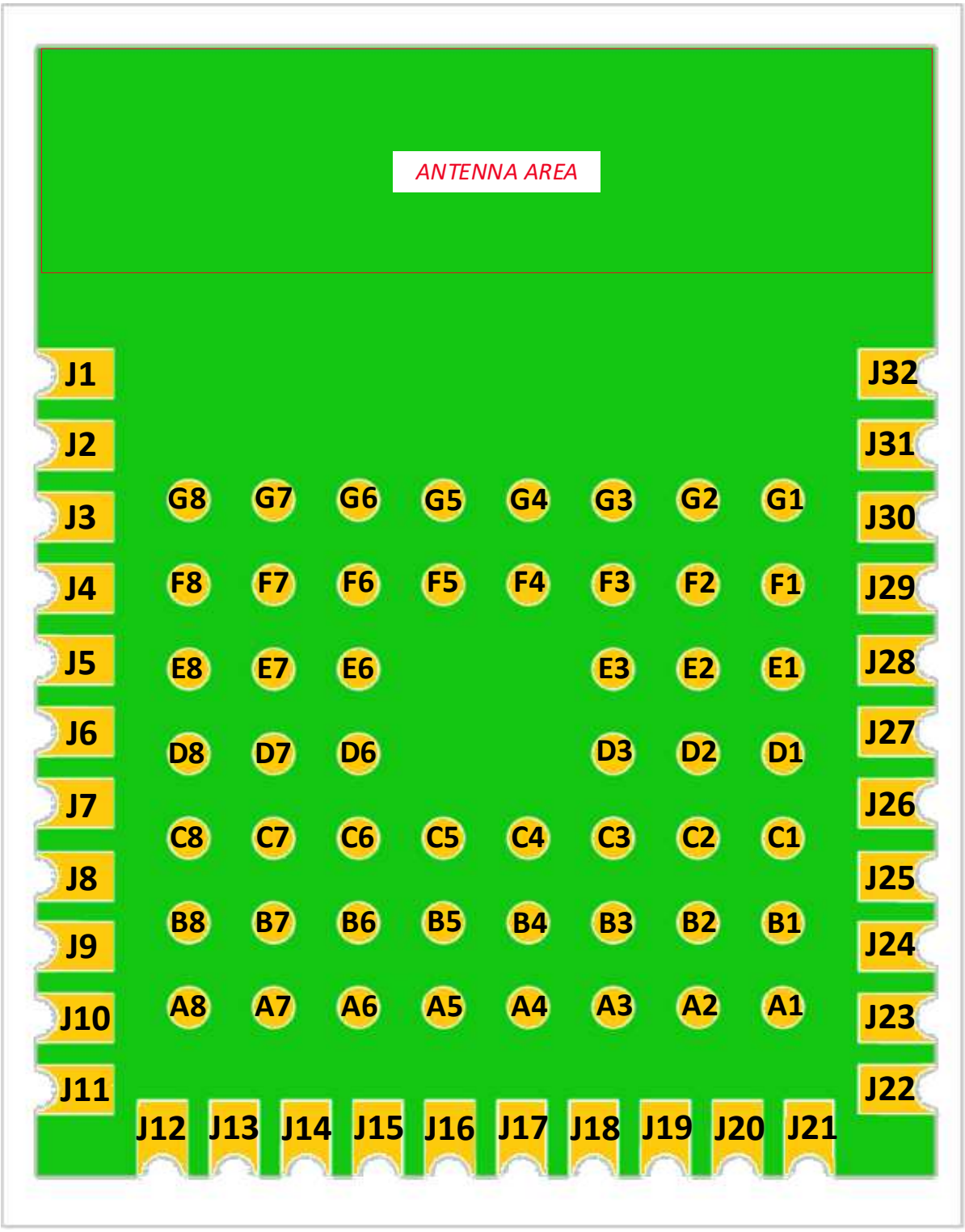

Figure 3: Pinout Diagram – Bottom Pads (Top View)

Table 2: Bottom Layer Pins Description

Ball No	Pin Name	Type	Drive (mA)	Reset State	Description
A1	GND	-			Ground
A7	GND	-			Ground

Ball No	Pin Name	Type	Drive (mA)	Reset State	Description
A8	GND	-			Ground
B1	GND	-			Ground
B3	GND	-			Ground
B4	GND	-			Ground
B8	GND	-			Ground
C1	GND	-			Ground
C7	GND	-			Ground
D2	GND	-			Ground
E1	GND	-			Ground
E2	GND	-			Ground
F3	GND	-			Ground
F4	GND	-			Ground
F8	GND	-			Ground
G3	GND	-			Ground
G4	GND	-			Ground
A2	P0_25	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_1	AI			INPUT. Analog input for the general-purpose ADC, channel 1.
	SDADC_1	AI			INPUT. Analog input for the ΣΔ ADC, channel 1.
A3	P1_10	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
A4	V30	AIO			OUTPUT. 3.0 V power rail. Maximum current 150 mA.
A5	VBUS	AI AI			INPUT. USB bus voltage. INPUT. Battery charge voltage.
A6	VBAT	AIO			INPUT. Battery connection
B2	P0_24	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
B5	P1_04	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor nd open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
B6	VBAT	AIO			INPUT. Battery connection
B7	V18	AIO			OUTPUT. 1.8 V power rail. Maximum current 50 mA.

Ball No	Pin Name	Type	Drive (mA)	Reset State	Description
C2	P1_09	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_0	AI			INPUT. Analog input for the general-purpose ADC, channel 0.
	SDADC_0	AI			INPUT. Analog input for the ΣΔ ADC, channel 0.
C3	P0_26	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
C4	P1_08	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
C5	P1_05	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
C6	P0_21	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
C8	P0_01	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPIR_D1	DIO			INPUT/OUTPUT. QSPI RAM data I/O 1.
D1	P0_18	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
D3	P0_20	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
D6	P0_02	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPIR_D2	DIO			INPUT/OUTPUT. QSPI RAM data I/O 2.
D7	V18P/V18F	AO			OUTPUT. 1.8 V power rail. Maximum current 50 mA.
D8	P0_04	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down

Ball No	Pin Name	Type	Drive (mA)	Reset State	Description
					enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPIR_CS	DIO			INPUT/OUTPUT. QSPI RAM data I/O 3.
E3	P0_16	DIO/ RDS	4.8/ 0.15	I-PD	INPUT / OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	SDADC_REF	AI			INPUT. Analog input for the ΣΔ ADC reference voltage.
	RCX	DO			OUTPUT. RC32k clock signal output (square wave).
E6	P0_31	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
E7	P0_00	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPIR_D0	DIO			INPUT/OUTPUT. QSPI RAM data I/O 0.
E8	P0_03	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPIR_D3	DIO			INPUT/OUTPUT. QSPI RAM data I/O 3.
F1	P0_07	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	NTC Input	AI			INPUT. Analog input for battery NTC (feedback).
F2	P0_06	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	SDADC_GND	AI			INPUT. Analog input for the ΣΔ ADC reference ground
F5	P0_19	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
F6	P0_29	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.

Ball No	Pin Name	Type	Drive (mA)	Reset State	Description
F7	P0_05	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPIR_CLK	DO			OUTPUT. QSPI RAM clock.
G1	P0_17	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	RC32k	DO			OUTPUT. RC32k clock signal output (square wave).
G2	P0_27	DIO/ RDS	4.8/ 0.15	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
G5	P0_13	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	CMAC_SWCLK	DI			INPUT. Arm Cortex-M0+ JTAG clock signal.
	RC32M	DO			OUTPUT. RC32M clock signal output (square wave).
G6	P0_11	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	M33_SWCLK	DI			INPUT. Arm Cortex-M33 JTAG clock signal.
G7	P0_12	DIO	4.8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	CMAC_SWDIO	DIO			INPUT/OUTPUT. Arm Cortex-M0+ JTAG data I/O signal.
	XTAL32M	DO			OUTPUT. XTAL32M clock signal output (square wave).
G8	V18F/V18P	AO			OUTPUT. 1.8 V power rail. Maximum current 50 mA.

Note 1 RDS = Reduced Driving Strength functionality (PAD_WEAK_CTRL_REG).

Note 2 I-PD is Input-Pulled Down.

Note 3 I-PU is Input-Pulled Up.

Note 4 DIO is Digital Input-Output.

Note 5 PWR is Power.

Note 6 GND is Ground.

5 Characteristics

All MIN/MAX specification limits are guaranteed by design, production testing and/or statistical characterization. Typical values are based on characterization results at default measurement conditions and are informative only.

Default measurement conditions (unless otherwise specified): V_{BAT}= 3.0 V, T_A = 25 °C. All radio measurements are done with standard RF measurement equipment.

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so the functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
$V_{PIN\_LIM\_DEF}$	Limiting voltage on a pin	Default, unless otherwise specified	-0.1	3.6	V
V_{BAT_LIM}	Limiting battery supply voltage	Pin V_{BAT}	0	6	V
V_{BUS_LIM}	Limiting bus supply voltage	Pin V_{BUS}	0	6.5	V
$V_{PIN\_LIM\_3V0}$	Limiting voltage on a pin	3.0 V I/O pins	0	3.45	V
$V_{PIN\_LIM\_1V8}$	Limiting voltage on a pin	1.8 V I/O pins	0	1.98	V
T_{STG}	Storage temperature		-50	150	°C

5.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BAT}	Battery supply voltage	Pin V_{BAT1} and V_{BAT2}	2.4		4.75	V
V_{BUS}	Bus supply voltage	Pin V_{BUS}	4.2		5.75	V
V_{PIN_3V0}	Voltage on a pin	3.0 V I/O pins	0		3	V
V_{PIN_1V8}	Voltage on a pin	1.8 V I/O pins	0		1.8	V
T_A	Ambient temperature		-40		85	°C

Table 5: DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{BAT_IDLE}	Battery supply current	CPU is idle (Wait for Interrupt - WFI); sys_clk = 32 MHz; pclk = 4 MHz; DC-DC on; FLASH off; peripherals on; V_{BAT} = 3 V.		0.8		mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{BAT\_ACTIVE\_32MHz}$	Battery supply current	CPU running CoreMark from RAM; sys_clk = 32 MHz; pclk = 4 MHz; DC-DC on; Peripherals off; V_{BAT} = 3 V.		1.8		mA
$I_{BAT\_ACTIVE\_48MHz}$	Battery supply current	CPU running CoreMark from RAM; hclk = 48 MHz; PLL on; pclk = 6 MHz; DC-DC on; Peripherals off; V_{BAT} = 3 V.		5		mA
$I_{BAT\_ACTIVE\_96MHz}$	Battery supply current	CPU running CoreMark from RAM; hclk = 96 MHz; PLL on; pclk = 12 MHz; DC-DC on; Peripherals off; V_{BAT} = 3 V.		7.8		mA
I_{BAT_HIBERN}	Battery supply current	Hibernation mode; no RAM retained; all clocks off; DC-DC off; VDD_clamp setting 0xD (0.83 V), FLASH off; V_{BAT} = 3 V. T_A 25 °C Note 1		6.8		µA
$I_{BAT\_DP\_SLP}$	Battery supply current	Deep Sleep mode; No RAM retained; XTAL32K on; RTC off; DC-DC off; VDD_RET = 0.75 V; FLASH off; V_{BAT} = 3 V. Bandgap Refresh rate = 0x80		10		µA
$I_{BAT\_EX\_SLP\_16K\_64K}$	Battery supply current	Extended Sleep mode; 16 kB (Cache) and 64 kB (data) RAM retained; XTAL32K on; DC-DC off; VDD_RET = 0.75 V; FLASH in Power Down mode; V_{BAT} = 3 V. Bandgap Refresh rate = 0x80; RTC off Note 2		12.3		µA
$I_{BAT\_EX\_SLP\_16K\_128K}$	Battery supply current	Extended Sleep mode; 16 kB (cache) and 128 kB (data) RAM retained; XTAL32K on; DC-DC off; VDD_RET = 0.75 V; FLASH in Power Down mode; V_{BAT} = 3 V. Bandgap Refresh rate = 0x80; RTC off Note 2		13.1		µA
$I_{BAT\_EX\_SLP\_16K\_256K}$	Battery supply current	Extended Sleep mode; 16 kB (cache) and 256 kB (data) RAM retained; XTAL32K on; DC-DC off; VDD_RET = 0.75 V; FLASH in Power Down mode; V_{BAT} = 3 V. Bandgap Refresh rate = 0x80; RTC off Note 2		14.9		µA
$I_{BAT\_EX\_SLP\_16K\_384K}$	Battery supply current	Extended Sleep mode; 16 kB (cache) and 384 kB (data) RAM retained; XTAL32K on; DC-DC off; VDD_RET = 0.75		16.7		µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
		V; FLASH in Power Down mode; V_{BAT} = 3 V. Bandgap Refresh rate = 0x80; RTC off Note 2				
$I_{BAT\_EX\_SLP\_16K\_512K}$	Battery supply current	Extended Sleep mode; 16 kB (cache) and 512 kB (data) RAM retained; XTAL32K on; DC-DC off; VDD_RET = 0.75 V; FLASH in Power Down mode; V_{BAT} = 3 V. Bandgap Refresh rate = 0x80;RTC off Note 2		18.4		µA
$I_{BAT\_BLE\_RX\_32M}$	Peak battery supply current	Bluetooth® LE receive mode; f_{CLK} = 32 MHz; CPU idle; DC-DC on; FLASH off; V_{BAT} = 3 V.		4.9		mA
$I_{BAT\_BLE\_TX\_32M}$	Peak battery supply current	Bluetooth® LE transmit mode @ 0dbm; f_{CLK} = 32 MHz; CPU idle; DC-DC on; FLASH off; V_{BAT} = 3 V.		5.8		mA
$I_{BAT\_BLE\_RX\_96M}$	Peak battery supply current	Bluetooth® LE receive mode; f_{CLK} = 96 MHz; CPU idle; DC-DC on; FLASH off; V_{BAT} = 3 V.		7		mA
$I_{BAT\_BLE\_TX\_96M}$	Peak battery supply current	Bluetooth® LE transmit mode @ 0dbm; f_{CLK} = 96 MHz; CPU idle; DC-DC on; FLASH off; V_{BAT} = 3 V.		7.8		mA

Note 1 At temperatures higher than 55 °C, a higher voltage setting (0xC) should be applied at the clamp to ensure proper hibernation operation.

Note 2 If RTC is on then 150 nA should be added.

5.3 Electrical Characteristics

Table 6: GPIO - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH level input current	V_I=V30 = 3.0 V	-10		10	µA
I_{IL}	LOW level input current	V_I=VSS = 0 V	-10		10	µA
$I_{IH\_PD\_3V0}$	HIGH level input current	V_I=V30 = 3.0 V	60		180	µA
$I_{IL\_PU\_3V0}$	LOW level input current	V_I=VSS = 0 V, V30 = 3.0 V	-180		-60	µA
$I_{IL\_PU\_1V8}$	LOW level input current	V_I=VSS = 0 V, V18P = 1.8 V	-110		-35	µA
V_{IH}	HIGH level input voltage	V12 = 1.2 V	0.7*V12			V
V_{IL}	LOW level input voltage	V12 = 1.2 V			0.3*V12	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OH_1V8}	HIGH level output voltage	I_O = 4.8 mA, V18P = 1.8 V	0.8*V18p			V
V_{OL_1V8}	LOW level output voltage	I_O = 4.8 mA, V18P = 1.8 V			0.2*V18P	V
V_{OH_3V0}	HIGH level output voltage	I_O = 4.8 mA, V30 = 3 V	0.8*V30			V
V_{OL_3V0}	LOW level output voltage	I_O = 4.8 mA, V30 = 3 V			0.2*V30	V

Table 7: GPIO - RDS - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OH\_1V8\_LOW\ DRV}$	HIGH level output voltage, limited drive	I_O = 150 µA, V18P = 1.8 V, low drive enabled Note 1	0.8*V18P			V
$V_{OL\_1V8\_LOW\ DRV}$	LOW level output voltage, limited drive	I_O = 150 µA, V18P = 1.8 V, low drive enabled			0.2*V18P	V

Note 1 Digital pad characteristics are equal to the standard GPIO pads unless overruled or added in this table.

Table 8: RCX - Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$\Delta f_{RC}/\Delta T$		For temperature ranging from -40 °C to 85 °C	-100		100	ppm/deg
f_{RCX}	RC oscillator frequency	At target fixed trim setting	13	15	18	kHz

Table 9: XTAL32K - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{XTAL_32K}	Crystal oscillator frequency			32.768		kHz
Δf_{XTAL_32K}	Crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is preferred.	-250		250	ppm

Table 10: XTAL32M - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{XTAL}(32M)	Crystal oscillator frequency			32		MHz

Parameter	Description	Conditions	Min	Typ	Max	Unit
$\Delta f_{XTAL}(32M)$	Crystal frequency tolerance	After optional trimming; including aging and temperature drift Note 1	-20		20	ppm

Note 1 Using the internal varicaps a wide range of crystals can be trimmed to the required tolerance.

Table 11: RADIO 1M - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_CLEAN}	Sensitivity level	Dirty Transmitter disabled; DC-DC converter disabled; PER = 30.8 % Note 1		-96		dBm
P_{SENS}	Sensitivity level	Dirty Transmitter enabled; DC-DC converter disabled; PER = 30.8 % Note 1		-95.5		dBm
$P_{SENS\_EPKT\_CLEAN}$	Sensitivity level	Dirty Transmitter disabled; DC-DC converter disabled; Extended packet size (255 octets) Note 1		-95		dBm
P_{SENS_EPKT}	Sensitivity level	Dirty Transmitter enabled; DC-DC converter disabled; Extended packet size (255 octets)		-93		dBm
P_O	Output power level	Power set to 6 dBm		6		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS.

Table 12: RADIO 2M - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_CLEAN}	Sensitivity level	Dirty Transmitter disabled; DC-DC converter disabled; PER = 30.8 % Note 1		-93.5		dBm
P_{SENS}	Sensitivity level	Dirty Transmitter enabled; DC-DC converter disabled; PER = 30.8 % Note 1		-93		dBm
$P_{SENS\_EPKT\_CLEAN}$	Sensitivity level	Dirty Transmitter disabled; DC-DC converter disabled; Extended packet size (255 octets) Note 1		-92		dBm

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_EPKT}	Sensitivity level	Dirty Transmitter enabled; DC-DC converter disabled; Extended packet size (255 octets)		-91.5		dBm
P_O	Output power level	Power set to 6 dBm		6		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS

6 Mechanical Specifications

6.1 Mechanical Dimensions and Land Pattern

The module's dimensions are accessible from the Renesas website – 84-Module.

6.2 Marking

The module's shield marking is shown in Figure 4.

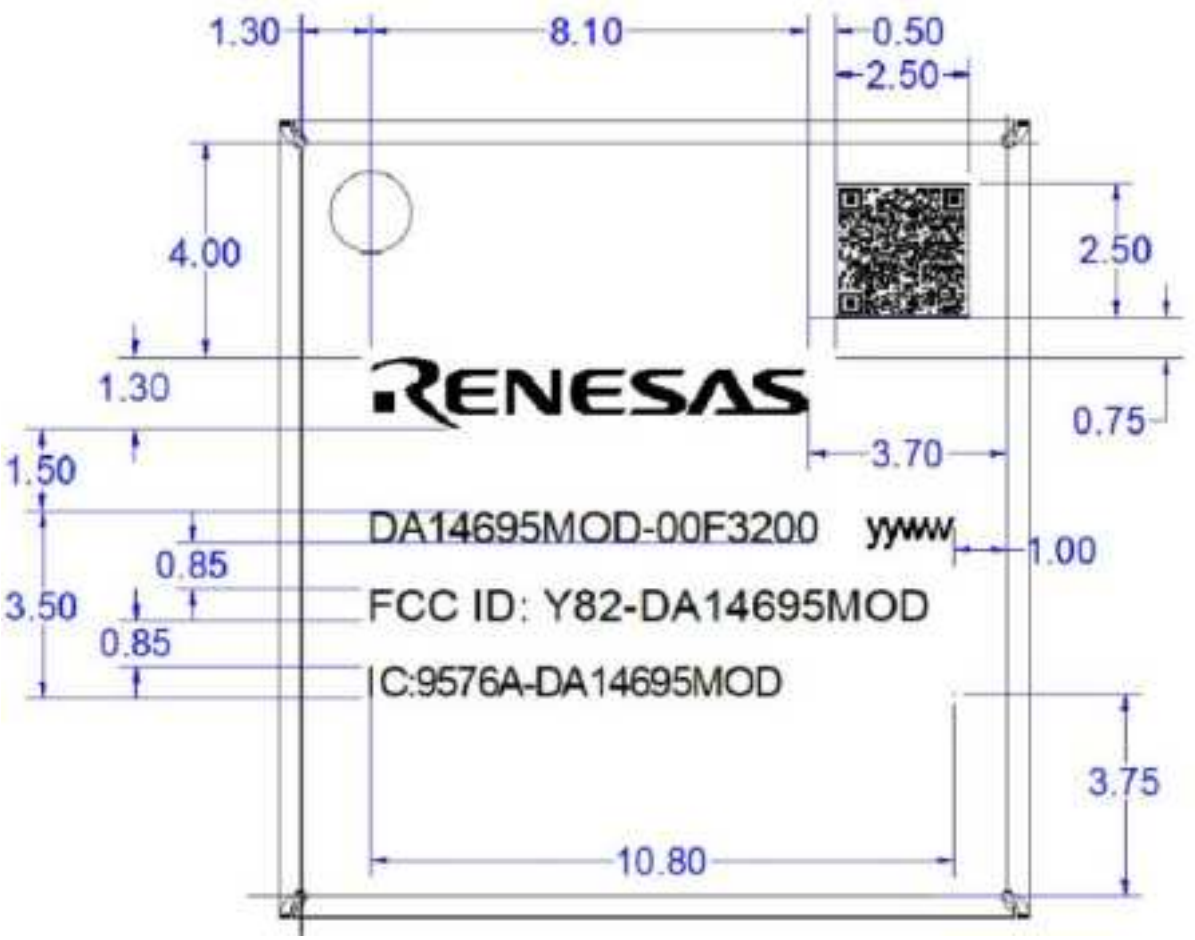

Figure 4: Module Shield Marking

Marking Legend:

DA14695MOD-00F3200 yyww

yy: production year

ww: production week

All dimension in mm. Tolerance: 0.4 mm

7 BOM

Table 13: Bill of Materials

#	Designator	Type	Value	Description	Manufacturer	MPN
1	C9, C15, C16	Capacitor	10uF	CAP CER 10UF 6.3 V X5R 0402	Murata	GRM155R60J106ME05D
2	C10	Capacitor	100nF	CAP CER 100n 25 V 10 % X7R 0402	Murata	GRM155R71E104KE14D
3	C11, C12, C17, C18	Capacitor	4.7uF	CAP CER 4.7UF 10 V X5R 0402	Murata	GRM155R61A475MEAAD
4	C13, C14	Capacitor	22uF	CAP CER 22UF 6.3 V X5R 0603	Murata	GRM188R60J226MEA0D
5	C22, C23	Capacitor	0.7pF	CAP CER 0.7±0.05pF 50V C0G/NP0 0201	Murata	GJM0335C1HR70WB01
6	C25	Capacitor	10pF	CAP CER 10PF 50 V 5 % NP0 0201	Murata	GRM0335C1H100JA01D
7	L2	Inductor	0.47uH	Shielded Wirewound Inductor 0.47uH 20 % 3600 mA 0.032 Ω 0806 (2016)	Murata Electronics	LQM21PNR47MG0D
	L3	Inductor	2.8nH	Inductor 2.8±0.1nH 450MA 250MOHM SM	Murata	LQP03TG2N8B02
8	R1	Resistor	10K	RES 10K OHM 5 % 1/20 W 0201	YAGEO	RC0201JR-0710KL
9	U1	IC	DA14695-00000HQ2	Renesas DA14695 BLE 5.2 SoC	Renesas Electronics	DA14695-00000HQ2
10	U2	NOR Flash	P25Q32SL-UXH-IR	FLASH 32MBIT SPI 104 MHZ 8USON 3x2x0.55 mm	Puya Semiconductor	P25Q32SL-UXH-IR
11	X1	Crystal Oscillator	32MHz 6pF 10ppm	2.0X1.6X0.65 MM 32 MHZ CRYSTAL XRCGB32M000F1S1AR0	Murata	XRCGB32M000F1S1AR0
12	X2	Crystal Oscillator	32.768 kHZ	CRYSTAL 32.768 kHZ SMD ±20 ppm 7pf 2,9x1.2 mm	TAI-SAW	TZ3158A

8 Design Guidelines

The DA14695MOD comes with an integrated PCB trace antenna. The antenna area is 15.85x4 mm. The antenna's Voltage Standing Wave Ratio (VSWR) and efficiency depend on the installation location.

The radiation performance of the PCB trace antenna depends on the host PCB layout. The maximum antenna gain is -0.2 dBi when installed on a 43x35 mm reference board, as shown in Figure 7. Antenna Radiation Efficiency is better than 40 % for all mounting positions. The radiation pattern is omnidirectional. The RF front end is optimized to achieve the maximum possible efficiency for various installation positions of the module on a host PCB. To obtain similar performance, follow the guidelines described in the following sections.

8.1 Installation Location

For optimum performance, install the module at the edge of a host PCB with the antenna edge facing out. The module can be located on either of the outer corners or in the middle of the host PCB with equivalent performance.

The antenna should have 4.0 mm free space in all directions. Copper or laminate in the proximity of the PCB trace antenna will affect the efficiency of the antenna. Laminate or copper under the antenna should be avoided as it severely affects the performance of the antenna. The antenna keep-out area is shown in Figure 6.

Metals close to the antenna will degrade the antenna's performance. The amount of degradation depends on the host system's characteristics.

Table 14 summarizes the antenna efficiency at different installation locations on a host PCB as shown in Figure 5.

Table 14: Antenna Efficiency vs DA14695MOD Module Positions

	Position # 1 (Left)		**Position # 2 (Middle)**		**Position # 3 (Right)**	
Freq	**Antenna efficiency**		**Antenna efficiency**		**Antenna efficiency**	
[MHz]	[%]	[dB]	[%]	[dB]	[%]	[dB]
2405	39	-4,1	46	-3,4	56	-2,5
2440	45	-3,5	48	-3,2	56	-2,5
2480	48	-3,2	49	-3,1	54	-2,7

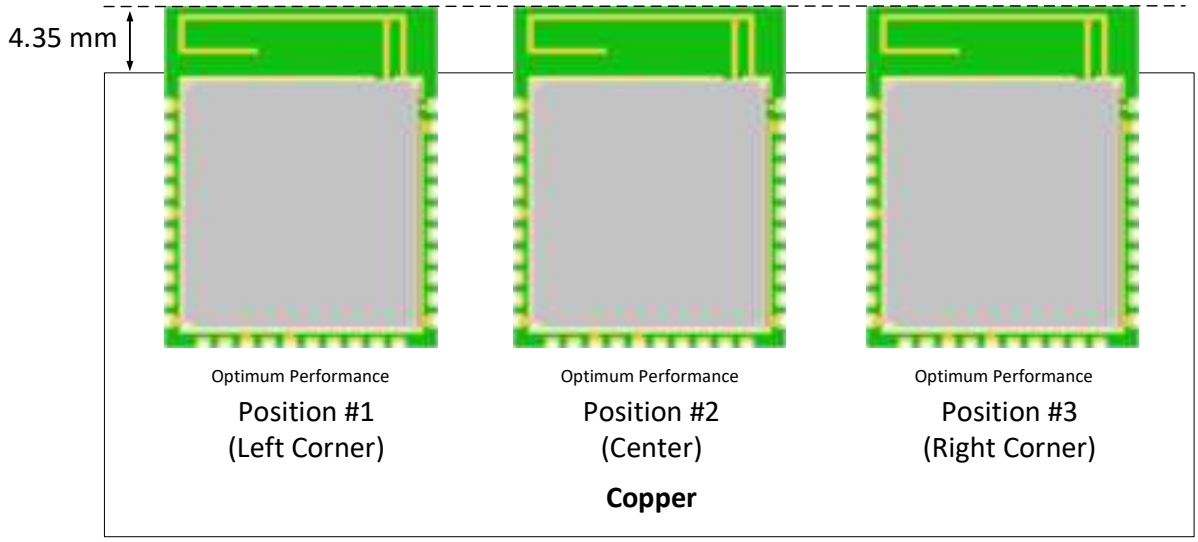

Figure 5: Installation Locations for Optimum Antenna Performance

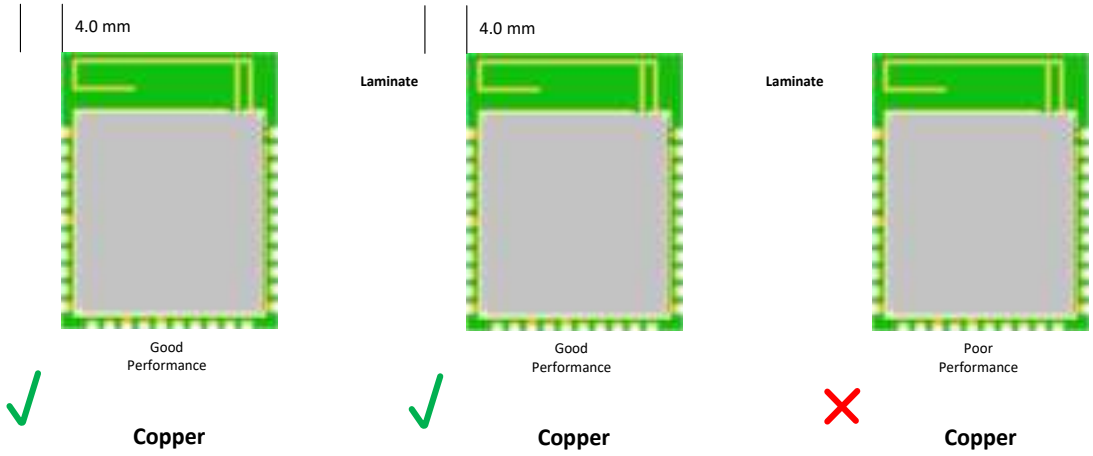

Figure 6: Antenna Performance in Proximity of Copper (Left), Laminate (Middle), and Laminate under Antenna (Right)

The actual DA14695MOD module evaluation board layout that has been used to conduct measurements is shown in Figure 7.

Figure 7: DA14695MOD Module Evaluation Board

8.2 Antenna Graphs

The antenna Voltage Standing Wave Ratio measurements for the three installation positions are shown in Figure 8, Figure 9, and Figure 10.

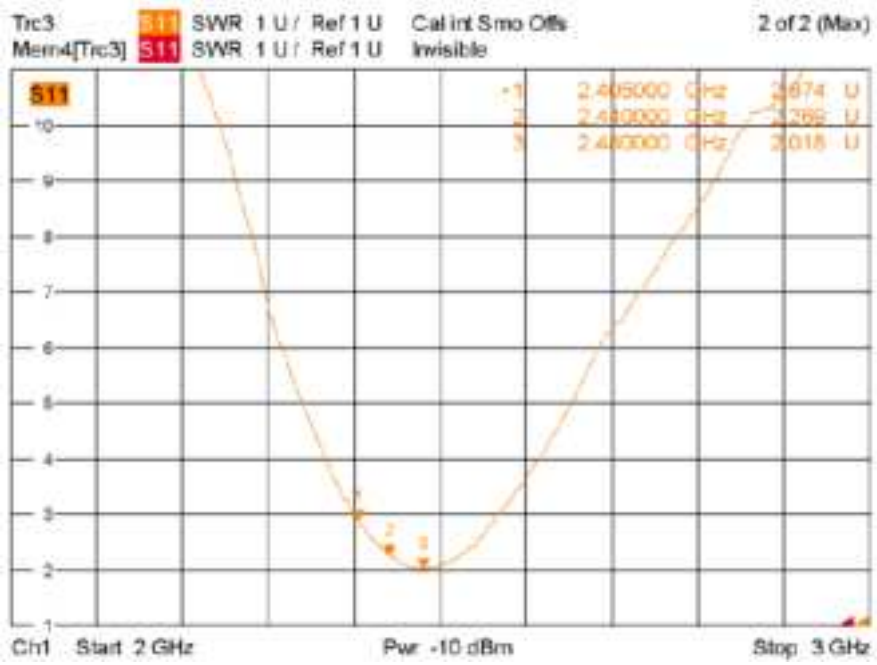

Figure 8: VSWR Installed in the Upper Left Corner (Position #1) of Evaluation Board

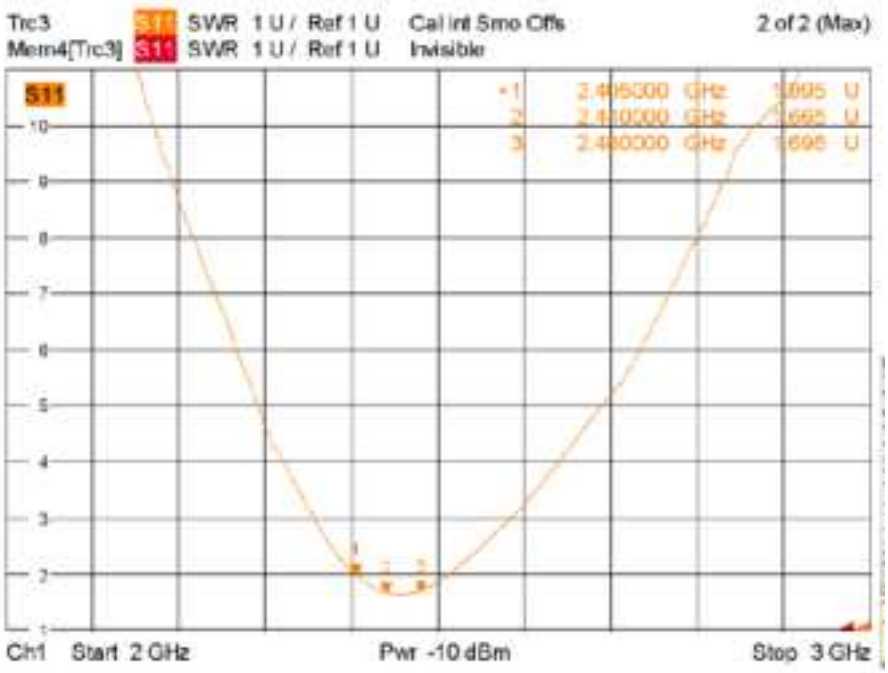

Figure 9: VSWR with Module Installed in Center (Position #2) of the Evaluation Board

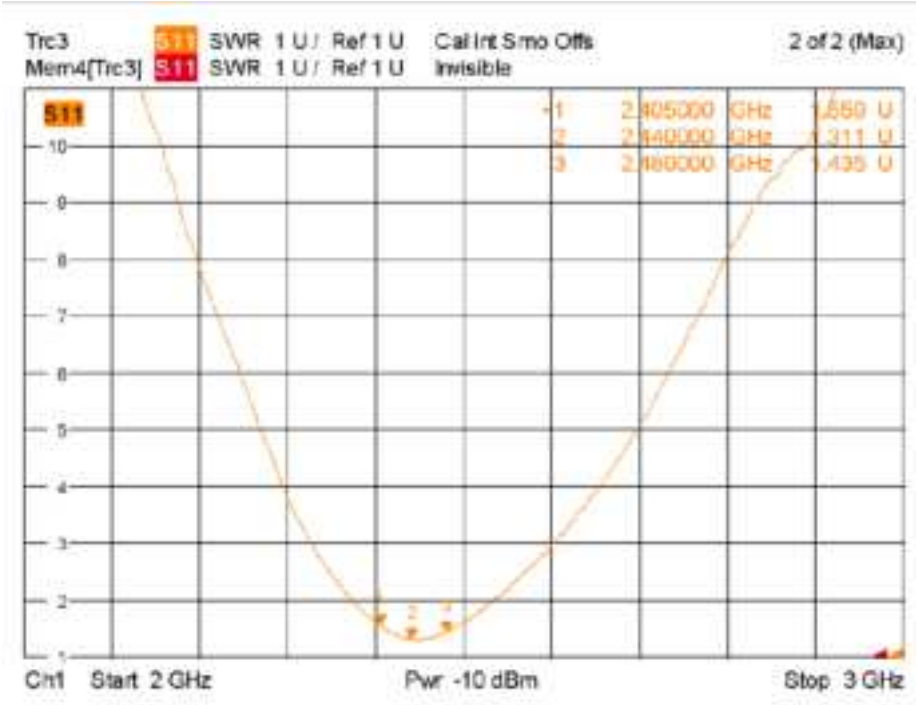

Figure 10: VSWR with Module Installed in the Upper Right Corner (Position #3) of the Evaluation Board

8.3 Radiation Pattern

The antenna radiation pattern measurements are carried out in an anechoic chamber. Radiation patterns are presented for three measurement planes: XY-, XZ-, and YZ- planes with horizontal and vertical polarization of the receiving antenna.

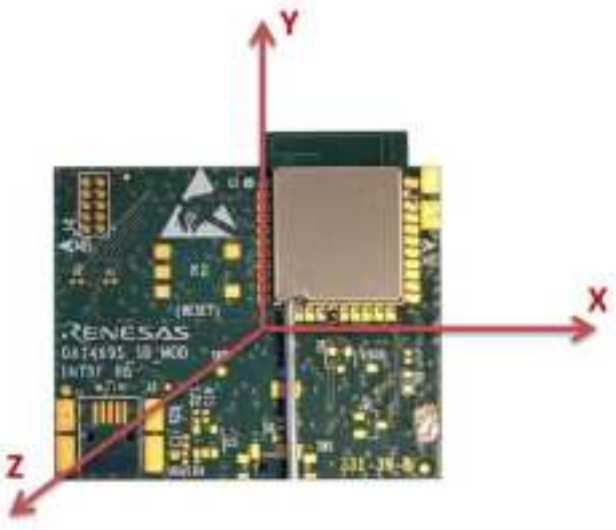

Figure 11: Measurement Plane Definition

Measurements are carried out for the module installed in the upper right corner on the reference board with no laminate below the antenna trace.

XY plane XZ plane YZ plane

Figure 12: Board Orientation at Different Planes

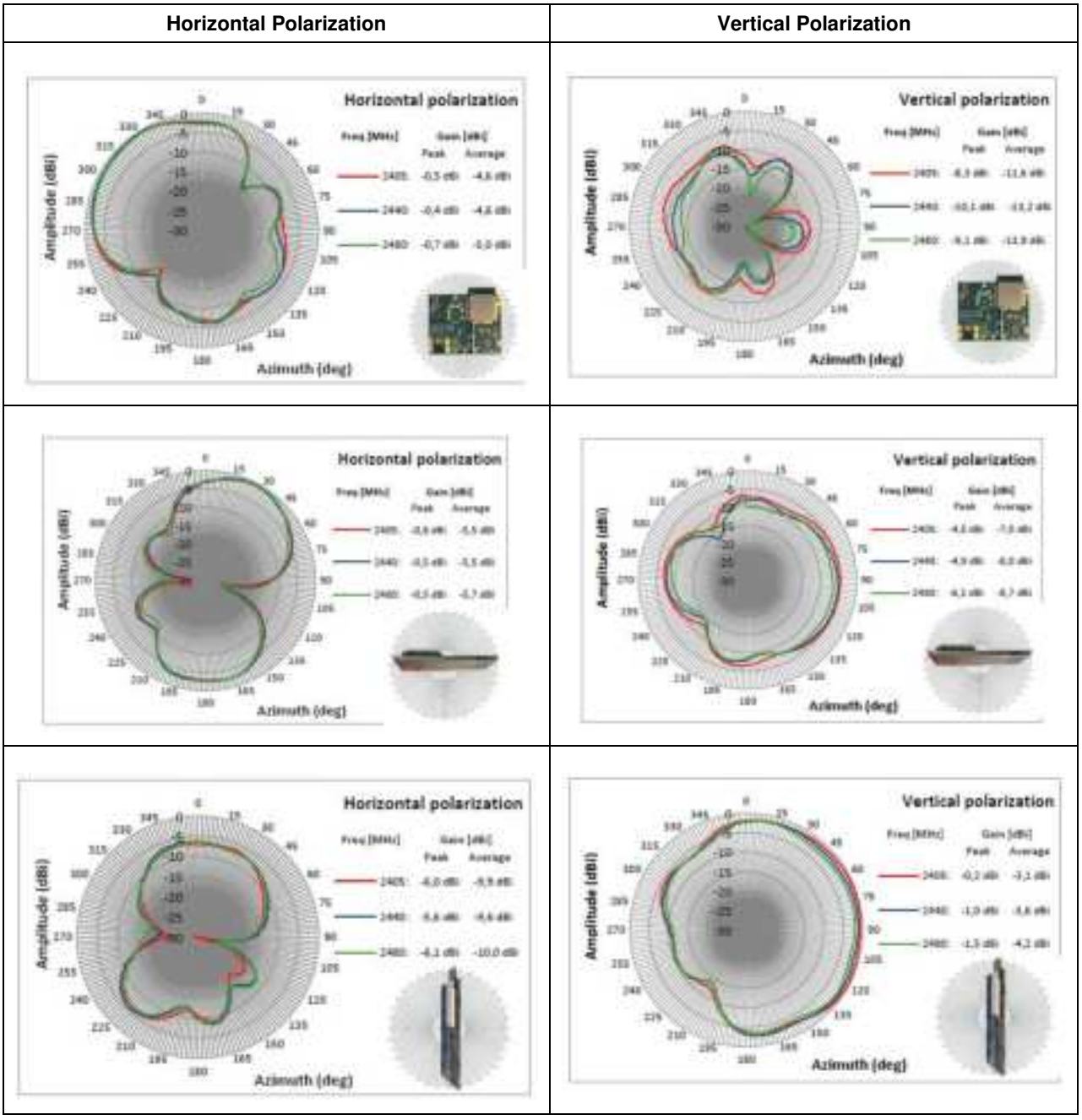

Figure 13: Radiation Pattern for Trace Antenna

Table 15 summarizes the antenna peak gain for the module mounted on the right corner position of the evaluation board.

Table 15: Antenna Peak Gain for 2.4 GHz Frequency Band

Frequency Band	XY-Plane		YZ-Plane		XZ-Plane	
	Peak gain [dBi]	Polarization	Peak gain [dBi]	Polarization	Peak gain [dBi]	Polarization
2.4 GHz	-0.4	Horizontal	-0.5	Horizontal	-0.2	Vertical

9 Soldering

The successful reflow soldering of the DA14695 Module on a PCB depends on several parameters such as the thickness of the stencil, the pads solder paste aperture, the solder paste characteristics, the reflow soldering profile, the size of the PCB, and so on.

The volume of solder paste applied to the board is mainly determined by the aperture size and stencil thickness. An initial solder paste aperture for the pads is provided on the solder paste layer of the PCB footprint. This aperture is modified by the assembly process experts according to stencil thickness, solder paste, and available assembly equipment.

The solder profile depends on the solder paste type used. For example, the soldering profile of a lead-free solder paste, Sn3Ag0.5Cu with no clean Flux (ROL0) and Solder Powder Type 4, is presented below.

No clean flux is recommended because washing must not be applied after assembly to avoid that moisture is trapped under the shield.

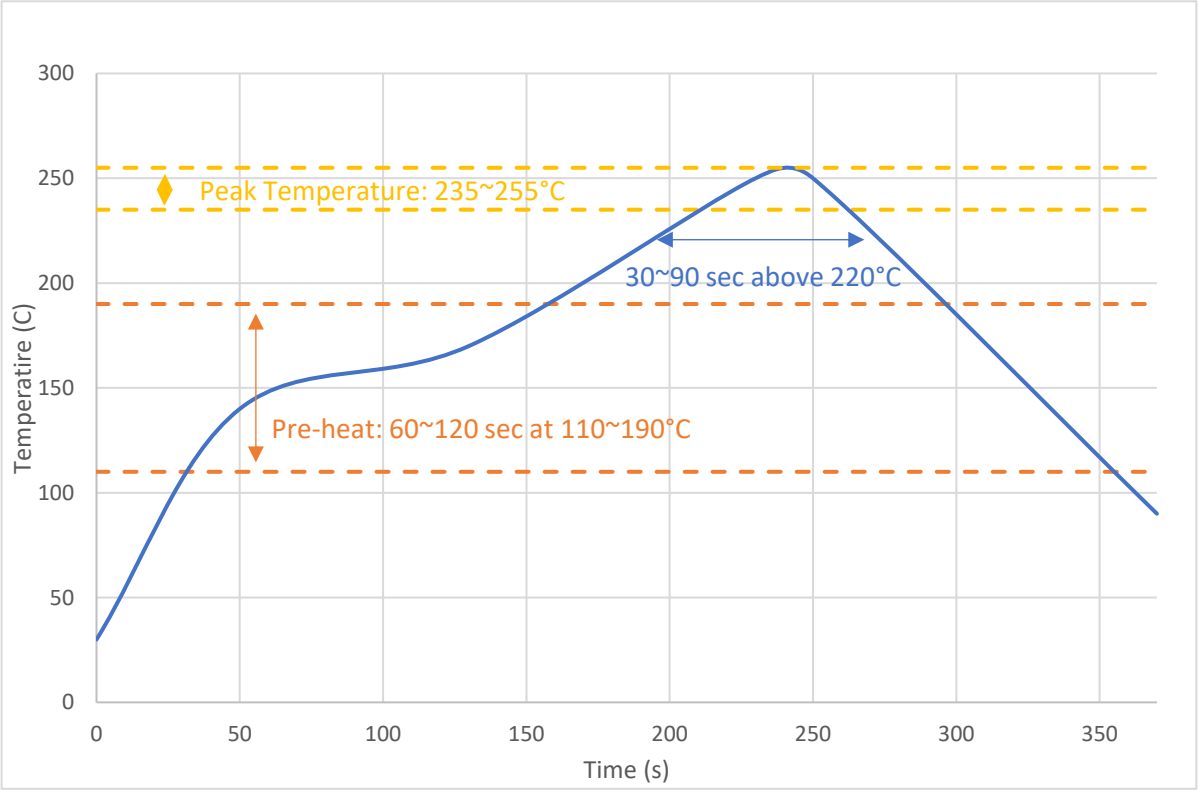

Figure 14: Recommended Reflow Profile for Lead Free Solder

Table 16: Reflow Profile Specification

Statistic Name	Low Limit	High Limit	Units
Slope1 (Target=2.0) Between 30.0 and 70.0	1	3	Degrees/Second
Slope2 (Target=2.0) Between 70.0 and 150.0	1	3	Degrees/Second
Slope3 (Target=-2.8) Between 220.0 and 150.0	-5	-0.5	Degrees/Second
Preheat time 110-190 °C	60	120	Seconds
Time above reflow @220 °C	30	90	Seconds
Peak temperature	235	255	Degrees Celsius
Total time above @235 °C	10	55	Second

Solderability reflow check of five cycles was performed, applying the procedures mentioned in JESD-A113E standard.

The MSL is an indicator for the maximum allowable time period (floor lifetime) in which a moisture-sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH before the solder reflow process.

DA14695 SmartBond™ Module is qualified for MSL 3.

Table 17: MSL Level vs Floor Lifetime

MSL Level	Floor Lifetime
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C/85% RH

10 Packaging Information

10.1 Tape and Reel

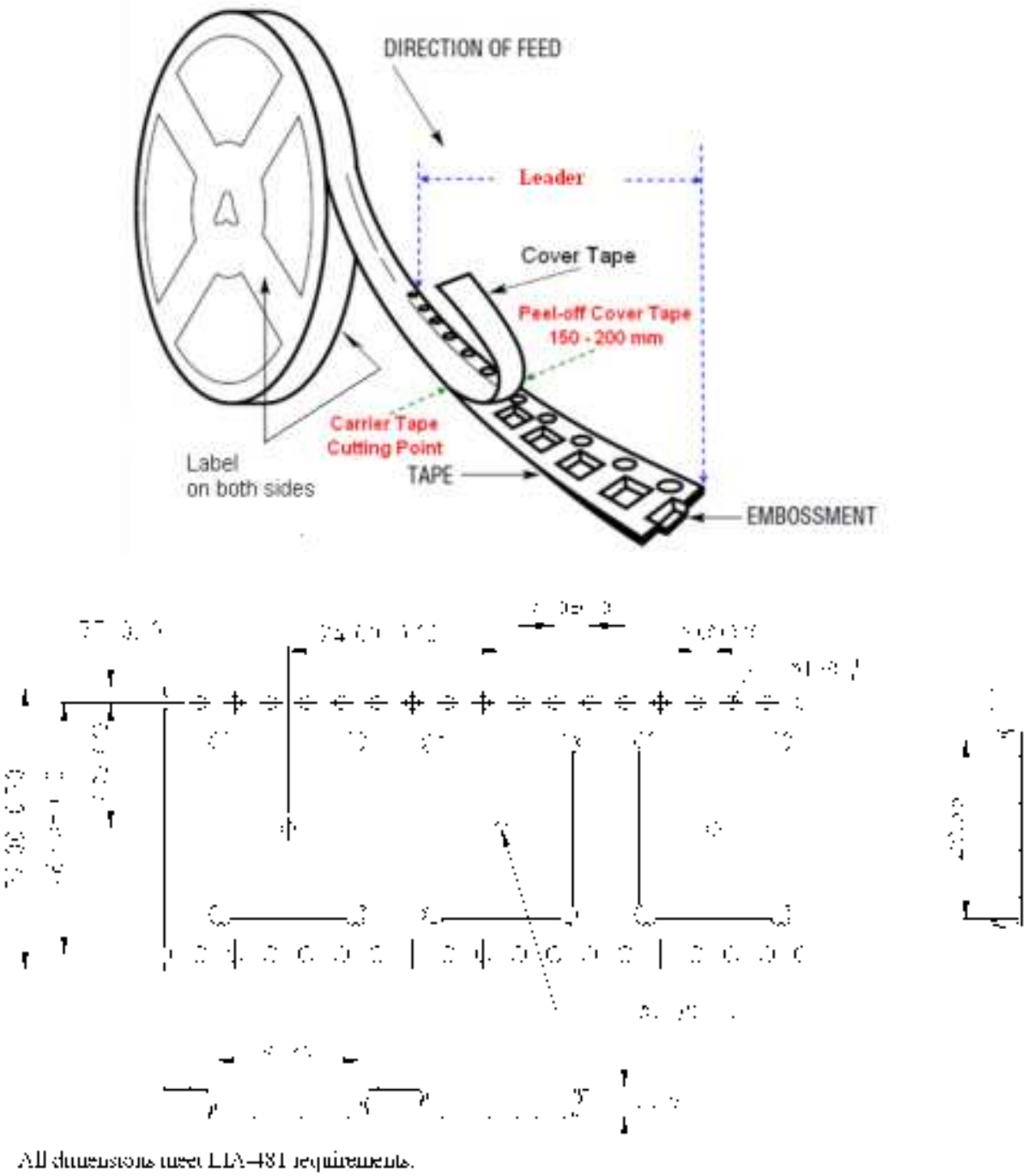

Figure 15: Tape and Reel

The reel specifications are presented in Table 18.

Table 18: Reel Specifications

Parameter	Value
Diameter	13 inches

Parameter	Value
Reel tape width	22 inches
Tape material	Static Dissipative Black Conductive Polystyrene Alloy
Qty/Reel	100/700pcs
Leader	400 mm + 10%
Trailer	160 mm + 10%
Round Sprocket Hole Diameter	1.50 ± 0.10 mm
Round Sprocket Hole Pitch	4.00 ± 0.10 mm

10.2 Labeling

On each reel, a set of labels are placed. The information label shows information regarding the batch number, date code, reel date and number, quantity, and part number as in Figure 16.

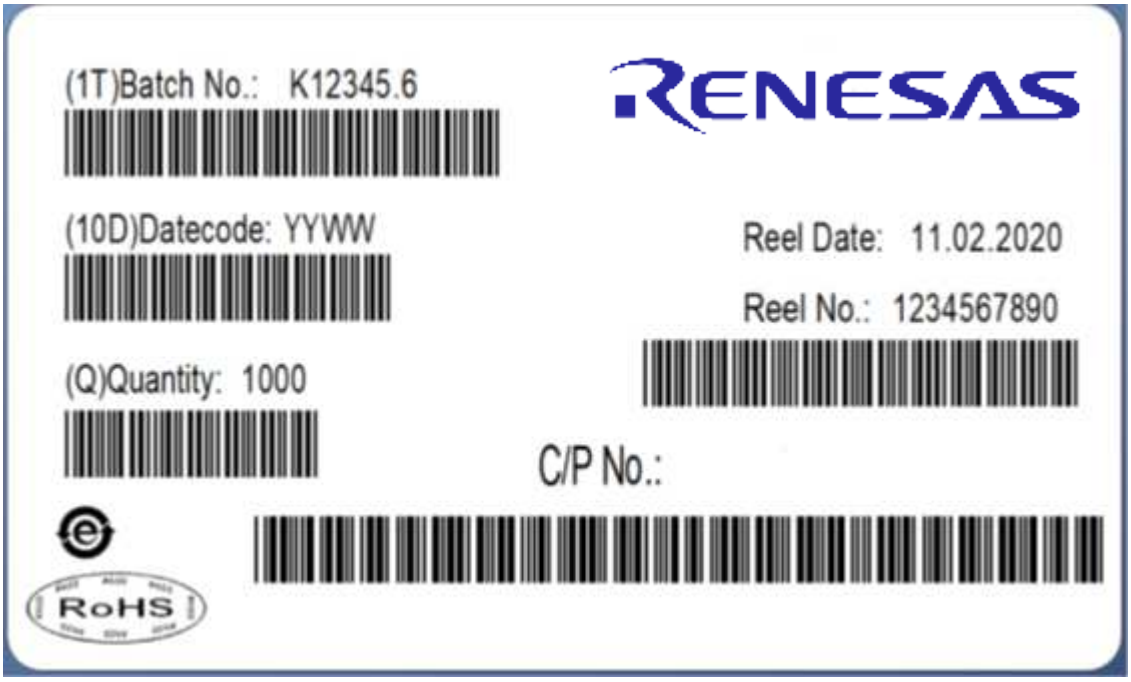

Figure 16: Reel Part Information Label

The directives label shows information regarding directives conformity as in Figure 17.

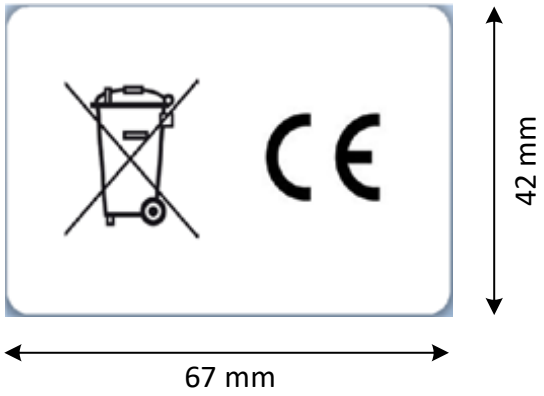

Figure 17: Reel Directives Conformity Label

11 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas Electronics Corporation local sales representative.

Table 19: Ordering Information (Samples)

Part Number	Size (mm)	Shipment Form	Pack Quantity	MOQ
DA14695MOD-00F3200C	15.85 x 20 x 2.5	Reel	100	1

Table 20: Ordering Information (Production)

Part Number	Size (mm)	Shipment Form	Pack Quantity	MOQ
DA14695MOD-00F32002	15.85 x 20 x 2.5	Reel	700	1

12 Regulatory Information

This section outlines the regulatory information for the DA14695 SmartBond™ Module. The module is certified for the global market. This facilitates the market entry of the end product. Note that the end product would need to apply for the end product certification, however, the module certification listed below will facilitate that procedure.

When the user sends the end product to those markets, the end product may need to follow additional requirements according to the specific market regulation.

For example, some markets have additional testing and/or certification like Korea EMC, South Africa SABS EMC and some have the requirement to put on the end product label a modular approval ID or mark that consists of an approved Bluetooth® Low Energy modular ID on host label directly, like Japan, Taiwan, Brazil.

A list of the Conformance Standards that the DA14695 SmartBond™ Module meets is shown in Table 21.

Table 21: Standards Conformance

Area	Item	Service	Standard	Certificate ID
Global	Safety for module	CB	IEC 62368-1:2018	CERTIFICATION PENDING Note 1
Europe	Wireless	RED	EN 300 328 v2.2.2 EN 62479:2010	CERTIFICATION PENDING
	Safety for module	CE	EN IEC 62368-1: 2020+A11: 2020	
	EMC	RED	EN 301 489-1 v2.2.3 EN 301 489-17 v3.2.4	
UK	Wireless	UKCA-RED	EN 300 328 v2.2.2 EN 62479:2010	CERTIFICATION PENDING
	Safety for module	UKCA-LVD	BS EN IEC 62368-1: 2020+A11: 2020	
	EMC	UKCA-RED	EN 301 489-1 V2.2.3 EN 301 489-17 V3.2.4	
US/CA	Wireless	FCC ID	47 CFR PART 15 Subpart C: 2021 section 15.247	Y82-DA14695MOD
		IC ID	RSS-247 Issue 2: February 2017 RSS-Gen Issue 4: November 2014	9576A-DA14695MOD
Japan	Wireless	MIC	JRL	012-230008
Taiwan	Wireless	NCC	LP0002	CERTIFICATION PENDING

Area	Item	Service	Standard	Certificate ID
South Korea	Wireless	MSIP	방송통신표준 KS X 3123 "무선 설비 적합성 평가 시험 방법" KN 301 489	R-R-8DL-DA14695MOD
South Africa	Wireless	ICASA	Based on RED	CERTIFICATION PENDING
Brazil	Wireless	Anatel	ATO No.14448/2017 Resolution No.680	CERTIFICATION PENDING
China	Wireless	SRRC	信部无【2002】353	CERTIFICATION PENDING
Thailand	Wireless	NBTC	NBTC TS 1035-2562	CERTIFICATION PENDING
India	Wireless	WPC	Based on RED	CERTIFICATION PENDING

Note 1 Include national differences of the US/Canada/Japan/China/Korea/Europe/Australia/South Africa/Taiwan/Brazil/Thailand.

12.1 CE (Radio Equipment Directive 2014/53/EU (RED)) – (Europe)

The DA14695 SmartBond™ Module is a Radio Equipment Directive (RED) assessed radio that is CE marked. The module has been manufactured and tested with the intention of being a subassembly to a final product. The module has been tested to RED 2014/53/EU Essential Requirements for Health, Safety, and Radio. The applicable standards are:

- **Radio: EN 300 328 V2.2.2 (2019-07)**
- **Health: (SAR) EN 62479:2010**
- **Safety: EN 62368-1**
- **EMC: EN 301 489-1 v2.1.1, EN 301 489 v3.1.1**

End product will need to perform the radio EMC tests according to EN 301 489. The conducted tests can be inherited from the module test report. It is recommended to repeat the EN 300 328 radiated testing with the end product assembly.

12.2 FCC – (U.S.A.)

FCC ID: **Y82-DA14695MOD**

12.2.1 List of Applicable FCC Rules

The module complies with FCC Part 15.247.

12.2.2 Summarize the Specific Operational Use Conditions

The module has been certified for Portable applications. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

12.2.3 Limited Module Procedures

Not applicable.

12.2.4 Trace Antenna Designs

Not applicable.

12.2.5 RF Exposure Considerations

This equipment complies with FCC's RF radiation exposure limits set forth for an uncontrolled environment. The antenna(s) used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter.

12.2.6 Antennas

Type	Gain	Impedance	Application
PCB Antenna	-0.2 dBi	50Ω	Fixed

The antenna is permanently attached, can't be replaced.

12.2.7 Label and Compliance Information

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference
2. This device must accept any interference received, including interference that may cause undesired operation.

Note
The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications or changes to this equipment. Such modifications or changes could void the user's authority to operate the equipment.

Warning
Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: • Reorient or relocate the receiving antenna. • Increase the separation between the equipment and receiver. • Connect the equipment into an outlet on a circuit different from that to which the receiver is connected. • Consult the dealer or an experienced radio/TV technician for help.

The system integrator must place an exterior label on the outside of the final product housing the DA14695MOD-00F3200 Module. Below are the contents that must be included on this label.

OEM Labeling Requirements:

Notice
The OEM must make sure that FCC labeling requirements are met. This includes a clearly visible exterior label on the outside of the final product housing that displays the contents shown in below:

Model: DA14695MOD-00F3200 Contains FCC ID: Y82-DA14695MOD

12.2.8 Information on test modes and additional testing requirements:

When testing host product, the host manufacture should follow FCC KDB Publication 996369 D04 Module Integration Guide for testing the host products. The host manufacturer may operate their product during the measurements. In setting up the configurations, if the pairing and call box options for testing does not work, then the host product manufacturer should coordinate with the module manufacturer for access to test mode software.

12.2.9 Additional testing, Part 15 Subpart B disclaimer:

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) list on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuity.

12.3 IC (Canada)

IC ID: 9576A-DA14695MOD

The DA14695 SmartBond™ Module is certified for the IC as a single-modular transmitter. The module meets IC modular approval and labeling requirements. The IC follows the same testing and rules as the FCC regarding certified modules in authorized equipment.

The module has been tested according to the following standards:

- Radio: RSS-247 Issue 2: February 2017, RSS-Gen Issue 4: November 2014
- Health: RSS-102 Issue 5:2015

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

RF Exposure Statement

This device complies with IC radiation exposure limits set forth for an uncontrolled environment and meets RSS-102 of the IC radio frequency (RF) Exposure rules. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Le présent appareil est conforme à l'exposition aux radiations IC définies pour un environnement non contrôlé et répond aux RSS-102 de la fréquence radio (RF) IC règles d'exposition. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

OEM Responsibilities to comply with IC Regulations

OEM integrator is responsible for testing their end product for any additional compliance requirements needed for the module installation like IC ES003 (EMC). This can be combined with the FCC Part 15B test.

End product labeling

The DA14695 SMARTBOND™ Module is labeled with its own IC ID: 9576A-DA14695MOD. If the IC ID is not visible when the module is installed inside another device, then the outside of the end product into which the module is installed must also display a label referring to the enclosed module. This exterior label can use the following or similar wording: “Contains IC ID: **9576A-DA14695MOD**”

12.4 UKCA (UK)

UKCA ID: CERTIFICATION PENDING

The module has been tested and found to comply with the standards harmonized with the regulations listed below according to UKCA-Radio Equipment Regulations 2017-CHAPTER 1 6(1)(a) Health, 6(1)(b) & 6(2).

The applicable standards are:

- **Radio: EN 300 328 V2.2.2 (2019-07)**
- **Health: (SAR) EN 62479:2010**
- **Safety: EN 62368-1:2018, BS EN IEC 62368-1: 2020+A11: 2020**
- **EMC: EN 301 489-1 v2.2.3, EN 301 489-17 v3.2.4**

End-product will need to perform the radio EMC tests according to EN 301 489. The conducted tests can be inherited from the module test report. It is recommended to repeat the EN 300 328 radiated testing with the end-product assembly.

12.5 NCC (Taiwan)

NCC ID: CERTIFICATION PENDING

The DA14695 SmartBond™ Module has received compliance approval in accordance with the Telecommunications Act. The module has been tested according to the following standard:

- Radio: Low Power Radio Frequency Devices Technical Regulations (LP0002)

End product may need to follow additional requirements according to the regulation EMC.

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。前述合法通信，指依電信管理法規定作業之無線電通信。低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

End product labeling

The NCC ID can be applied directly to the end product's label.

12.6 MSIP (South Korea)

MSIP ID: R-R-8DL-DA14695MOD

DA14695 SmartBond™ Module has received certification of conformity in accordance with Radio Waves Act. The module has been tested according to the following standard:

- Radio: Ministry of Science and ICT Notice No. 2019-105

For the end product wireless test, you can refer to Renesas' own certification report so that the lab knows the module itself has passed although it still needs to be tested.

Additionally, EMC for wireless (KN301489).

End product labeling

The MSIP ID can be applied directly to the end product's label. The ID should be clearly visible on the final end product. The integrator of the module should refer to the labeling requirements for Korea available on the Korea Communications Commission (KCC) website.

12.7 ICASA (South Africa)

South Africa certification is based on RED(CE) approval.

Approval is granted to print labels for the products as described below:

3. **For use as Label on the product size: 80 mm (W) X 40 mm (H). To be printed on the product.**
4. **For use as Label on the package size: 80 mm (W) X 40 mm (H). To be printed on the package.**

End product may need to follow additional requirements according to the regulation EMC.

12.8 ANATEL (Brazil)

Certification Pending

The module has been tested and found to be compliant according to the following Category II standards:

- ATO (Act) No 14448/2017

End product may need to follow additional requirements according to the regulation EMC.

“Este equipamento não tem direito à proteção contra interferência prejudicial e não pode causar interferência em sistemas devidamente autorizados.

Translation of the text:

"This equipment is not entitled to protection against harmful interference and must not cause interference in duly authorized systems."

12.9 SRRC (China)

Model no. DA14695MOD-00F3200

CMIIT ID: CERTIFICATION PENDING

The module has been tested and found to be compliant according to the following standards:

- 信部无【2002】353号

End product may need to follow additional requirements according to the regulation EMC.

12.10 MIC (Japan)

MIC ID: 012-230008

The DA14695 SmartBond™ Module has received type certification as required to conform to the technical standards regulated by the Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan.

The module has been tested according to the following standard:

- Radio: JRL “Article 49-20 and the relevant articles of the Ordinance Regulating Radio” Equipment

End product may need to follow additional requirements according to the regulation EMC.

End product labeling

The MIC ID can be applied directly to the end product's label. **The end product may bear the GITEKI mark and certification number so that is clear that the end product contains a certified radio module. The following note may be shown next to, below, or above the GITEKI mark and certification number in order to indicate the presence of a certified radio module:**

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

12.11 NBTC (Thailand)

Model no. DA14695MOD-00F3200

NBTC SDoC ID: CERTIFICATION PENDING

The DA14695 SmartBond™ Module is compliant with NBTC requirements in Thailand.

End product may need to follow additional requirements according to the regulation EMC.

End product labeling

End products will have their own ID and labeling requirements.

12.12 WPC (India)

Model no. DA14695MOD-00F3200

Registration No: CERTIFICATION PENDING

India certification is based on RED(CE) approval/reports. There are no **marking/labeling requirements.**

End product may need to follow additional requirements according to the regulation EMC.

13 Bluetooth SIG Qualification

The DA14695 SmartBondTM Module is listed on the Bluetooth® SIG Website as a qualified product. The customers can refer to the following QDIDs to qualify their product:

- QDID 152841 for Host Subsystem
- QDID 149229 for Controller Subsystem

Revision History

Revision	Date	Description
3.0	03-Aug-2023	Datasheet status: Final. Product status: Production

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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