GM500-U1G

Hardware Development Guide

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LTE Module Series

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Revision History

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1.0	2020-11-20	1st released version

About This Document

A. Application Range

This document is the Product Technical Specification for the GM500-U1G_AGSM/WCDMA/LTE-FDD module. It defines the high level product features and illustrates the interface for these features. This document is intended to cover the hardware aspects of the product, including electrical and mechanical.

B. Reading Note

The symbols below are the reading notes you should pay attention on:

⚠: **WARNING or ATTENTION** ▤: **NOTE or REMARK**

C. Purpose

This document provides the hardware solutions and development fundamentals for a product with the module. By reading this document, the user can have an overall knowledge of the module and a clear understanding of the technical parameters. With this document, the user can successfully fulfill the application and development of wireless Internet product or equipment.

Besides the product features and technical parameters, this document also provides the product reliability tests and related testing standards, RF performance indexes and a guide on the design of user circuits, to provide the user with a complete design reference.

▤**NOTE:**

To ensure the module manufacturing and welding quality, do as the chapter 7 of Manufacturing Guide in this document. The force on the squeegee should be adjusted so as to produce a clean stencil surface on a single pass and ensure the module soldering quality.

D. Abbreviations

Table below is a list of abbreviations involved in this document, as well as the English full names.

Abbreviations	Full Name
3GPP	Third Generation Partnership Project
AP	Another name of DTE
CHAP	Challenge Handshake Authentication Protocol
CE	European Conformity
CMOS	Complementary Metal Oxide Semiconductor
DCE	Data Communication Equipment
DL	Downlink
DTE	Data Terminal Equipment
EIA	Electronic Industries Association
EMC	Electromagnetic Compatibility
ESD	Electro-Static discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
GPIO	General-purpose I/O
LCC	Leadless Chip Carrier

LDO	Low-Dropout
LED	Light Emitting Diode
LTE	Long Term Evolution
ME	Mobile Equipment
MO	Mobile Origination Call
MT	Mobile Termination Call
MSB	Most Significant Bit
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PAP	Password Authentication Protocol
PPP	Point to Point Protocol
RTC	Real Time Clock
SMS	Short Messaging Service
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
TBD	To Be Determined
TCP	Transmission Control Protocol
TIS	Total Isotropic Sensitivity
TRP	Total Radiated Power
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UL	Up Link
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
URC	Unsolicited result code
VIH	Logic High level of input voltage
VIL	Logic Low level of input voltage
VOH	Logic High level of output voltage
VOL	Logic Low level of output voltage

Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating ME3610 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel and to incorporate these guidelines into all manuals supplied with the product. If not so, GOSUNCN does not take on any liability for customer failure to comply with these precautions.

🚚	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a hands free kit) cause distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.
✈	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers a Airplane Mode which must be enabled prior to boarding an aircraft.
⊕	Switch off your wireless device when in hospitals or clinics or other health care facilities. These requests are designed to prevent possible interference with sensitive medical equipment.
SOS	GSM cellular terminals or mobiles operate over radio frequency signal and cellular network and cannot be guaranteed to connect in all conditions, for example no mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
♥	Your cellular terminal or mobile contains a transmitter and receiver. When it is on, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
🔥	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres including fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

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1. Product Overview

1.1. General Description

GM500-U1G isaLTE/WCDMA wireless communication module with LCC+LGA interface. It is widely applied to but not limited to the various products and equipment such as laptops, vehicle-mounted terminals, and electric devices, by providing data services.

Customer can choose the dedicated type based on the wireless network configurationand using area. The following table shows the entire radio band configuration of GM500-U1G series.

Table 1-1 GM500-U1G Supported Band

PID	RF support	RF Band	Transmit Frequency (TX)	Receive Frequency (RX)
GM500-U1G(CAT4)	LTE FDD	B2	1850 to 1910 MHz	1930 to 1990 MHz
		B4	1710 to 1755 MHz	2110 to 2155 MHz
		B5	824 to 849 MHz	869 to 894 MHz
		B12	699 to 716 MHz	729 to 746 MHz
		B13	777 to 787 MHz	746 to 756 MHz
		B25	1850 to 1915 MHz	1930 to 1995 MHz
		B26	814 to 849 MHz	859 to 894 MHz
		B66	1710 to 1780 MHz	2110 to 2200 MHz
	WCDMA	B2	1850 to 1910 MHz	1930 to 1990 MHz
		B4	1710 to 1755 MHz	2110 to 2155 MHz
		B5	824 to 849 MHz	869 to 894 MHz

1.2. Key Features

The table below describes the detailed features of the GM500-U1G module.

Table 1-2 GM500-U1G Key Features

Feature	Description
Physical	Small form factor-30 mm × 30 mm × 2.4mm LCC+LGA interface
Power Supply	The range of voltage supply is 3.4V-4.2V, typical value is 3.8V
Transmission Rate	LTE FDD (CAT4): Max 150Mbps(DL)/Max 50Mbps(UL)
Network Protocols	Support TCP/PPP/UDP/FTP protocols Support PAP, CHAPprotocols used for PPP connection.
USIM Interface	1.8V/3V support SIM extraction/hot plug detection Support SIM and USIM
UART Interface	Support two UART interface: main UART interface and debug UART interface Main UART interface:

	Eight lines on main UART interface Support RTS and CTS hardware flow control Baud rate can reach up to 921600 bps,115200 bps by default Used for AT command, data transmission or firmware upgrade Debug UART interface: Two lines on debug UART interface, can be used for software debug, firmware upgrade
USB Interface	Compliant with USB 2.0 specification (slave only) Used for AT command communication, data transmission, software debug and firmware upgrade.
SDIO interface	1.8V, support (full speed) 4bits,SDIO compatible to WLAN (802.11)
Antenna Interface	Include main antenna ,diversity antenna and GNSS antenna
Rx-diversity	Support WCDMA/LTE Rx-diversity
Network Indication	Use LED_MODE to indicate network connectivity status
Temperature Range	Normal operation: -30°C to +75°C Restricted operation: -40°C~ -30°C and +75°C~ +85°C1) Storage temperature: -40°C to +85°C
Firmware Upgrade	USB interface or UART interface or OTA(WEFOTA)

1.3. Function Diagram

The figure below shows a block diagram of the GM500-U1G and illustrates the major functional parts.

- Power management
- Baseband
- Memory
- RF send-receive
- Peripheral interface
  --UART interface
  --USIM card interface
  --USB interface
  --SDIO interface
  --SPI interface
  --I2C interface
  --ADC interface
  --Status interface (LED)

1.4. Evaluation Board

In order to help you to develop applications with GM500-U1G, GOSUNCN supplies an evaluation board (G2000/GE2015), RS-232 to USB cable, USB data cable, power adapter, antenna and other peripherals to control or test the module. For details, please refer to the related document ***[GE2015 Dev Board User Guide].***

2. Application Interface

2.1. General Description

GM500-U1G is equipped with 80 LCC pads plus 16 ground pads and 22 LGA pads that connect to customer’s cellular application platform. Sub-interface included in these pads is described in detail in the following chapters:

- Pin assignment
- Pin description
- Power supply
- Turn on/off scenarios
- USIM interface
- USB interface
- UART interface
- Network status indication
- ADC interface
- WAKEUP_IN signal
- WAKEUP_OUT signal
- GPIO interface

2.2. Pin Assignment

The following figure shows the pin assignment of the GM500-U1G module.

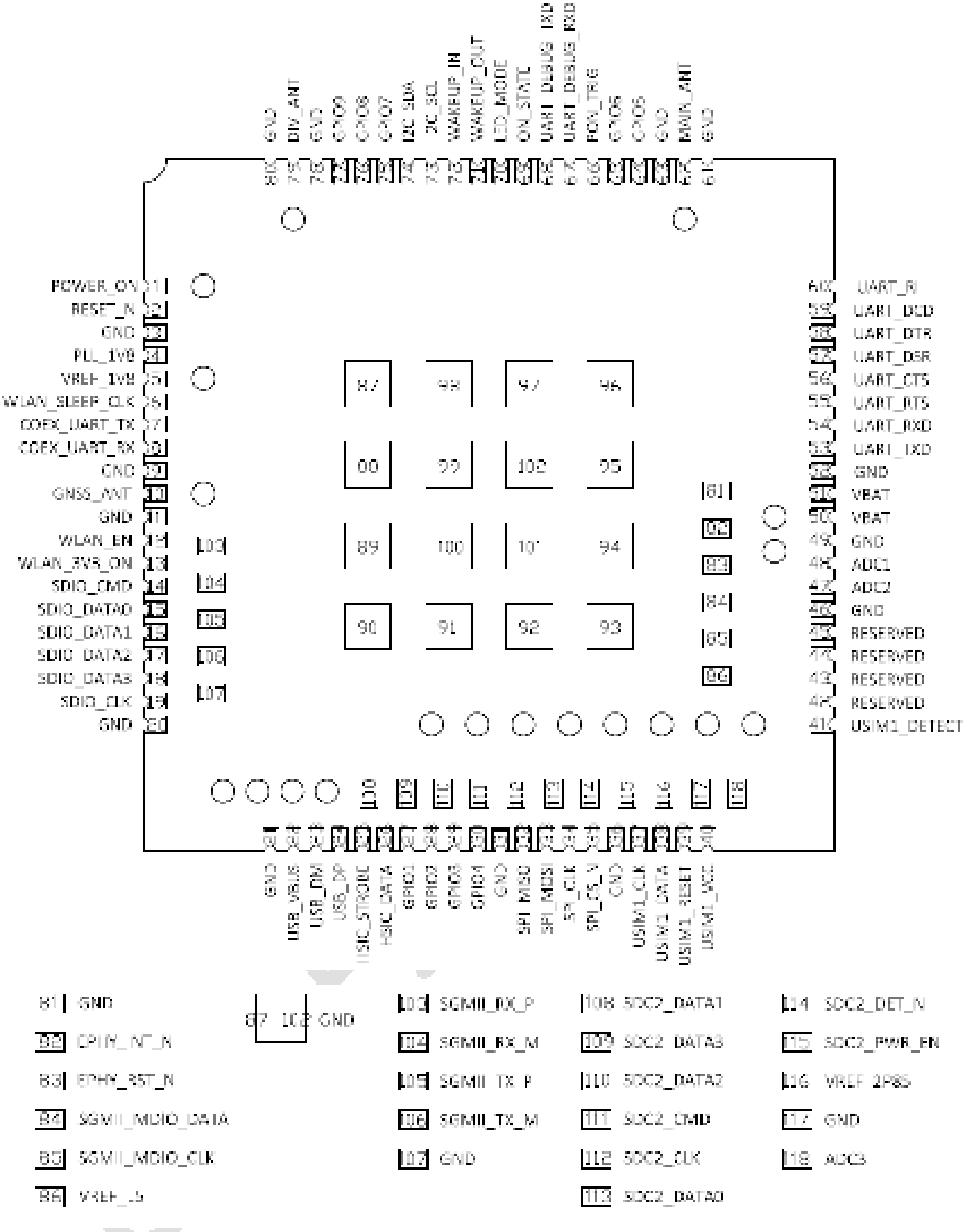


Figure 2–1 Pin Assignment

2.3. Pin Description

The following table shows the IO Parameters Definition.

Table 2-1 IO Parameters Definition

Type	Description
IO	Bidirectional input/output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

The logic levels are described in the following table.

Table 2-2 Logic levels Description

Parameter	Min	Max	Unit
VIH	0.65*VDD_IO	VDD_IO+0.3	V
VIL	-0.3	0.35* VDD_IO	V
VOH	VDD_IO-0.45	VDD_IO	V
VOL	0	0.45	V

NOTE:

VDD_IO is the voltage level of pins.

The following tables show the GM500-U1G's pin definition.

Table 2-3 Pin Description

Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
RF Interface					
MAIN_ANT	62	IO	Main antenna	50Ω impedance	
DIV_ANT	79	AI	Diversity antenna	50Ω impedance	
GNSS_ANT	10	IO	GNSS antenna	50Ω impedance	
Power Supply					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	50.51	PI	Power supply for module	Vmax = 4.2V Vmin = 3.4V Vnorm = 3.8V	It must be able to provide sufficient current in a transmitting burst which typically rises to 2.0A
VREF_1V8	5	PO	Provide 1.8V for external circuit	Vnorm = 1.8V Imax = 50mA	Power supply for external GPIO'S pull up circuits
PLL_1V8	4	PO	Provide 1.8V for external circuit	Vnorm = 1.8V Imax = 20mA	This pin can only be used for WiFi interface, and can left unconnected when not used.
GND	3,9,11,20,21,31,36, 46,49,52,61,63,78, 80,81,87~102,107,		Ground		

	117				
Turn On/Off					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
POWER_ON	1	DI	Turn on/off module,level trigger (active low)	V_{IH} max = 2.1V V_{IH} min = 1.17V V_{IL} max = 0.63V	Pull-up to 0.8V internally, active low
PON_TRIG	66	DI	Level high triggered power on input	V_{IH} max = 2.1V V_{IH} min = 1.17V V_{IL} max = 0.63V	
RESET_N	2	DI	Reset module	V_{IH} max = 2.1V V_{IH} min = 1.17V V_{IL} max = 0.63V	Active low
Status Indication					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ON_STATE	69	DO	Module power on/off status indicator	V_{OH} min = 1.35V V_{OL} max = 0.45V	1.8V power domain
LED_MODE	70	DO	Indicate the module network registration mode	V_{OH} min = 1.35V V_{OL} max = 0.45V	1.8V power domain
USB Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	24	IO	USB differential data bus		Compliant with USB 2.0 standard specification Require differential impedance of 90Ω
USB_DM	23	IO			
USB_VBUS	22	DI	USB plug detect pin, not USB power		USB plug detect
HSIC Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_STROBE	25	IO	HSIC strobe	InterChip USB(HSIC)	line impedance 50 ohm, isometric constraint is less than 2 mm, line length is less than 10 cm
USB_DATA	26	IO	HSIC data		
USIM Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VCC	40	PO	Power supply for USIM1 card	For 1.8V USIM: Vmax = 1.9V Vmin = 1.7V For 3.0V USIM: Vmax = 3.05V Vmin = 2.7V I_O max = 50mA	Either 1.8V or 3V is supported by the module automatically

USIM1_DATA	38	IO	Data signal of USIM1 card	For 1.8V USIM: V_{IL} max = 0.63V V_{IH} min = 1.17V V_{OL} max = 0.45V V_{OH} min = 1.35V For 3V USIM: V_{IL} max = 1.05V V_{IH} min = 1.95V V_{OL} max = 0.45V V_{OH} min = 2.6V	Pull-up to USIM1_VCC with 10k resistor internally
USIM1_CLK	37	DO	Clock signal of USIM1 card	For 1.8V USIM: V_{OL} max = 0.45V V_{OH} min = 1.35V For 3V USIM: V_{OL} max = 0.45V V_{OH} min = 2.6V	
USIM1_RST	39	DO	Reset signal of USIM1 card	For 1.8V USIM: V_{OL} max = 0.45V V_{OH} min = 1.35V For 3V USIM: V_{OL} max = 0.45V V_{OH} min = 2.6V	
USIM1_DETECT	41	DI	USIM1 card input detection	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V V_{IH} max = 2.1V	1.8V power domain.Active low. If do not need of USIM detect, leave this pin not connected.
ADC Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC1	48	AI	Analog to digital	0.05V to 4.15V	External sensor signal detection
ADC2	47	AI	Analog to digital	0.05V to 4.15V	External sensor signal detection
ADC3	108	AI	Analog to digital	0.05V to 4.15V	External sensor signal detection
Main UART Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART_TXD	53	DO	Transmit data	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain
UART_RXD	54	DI	Receive data	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V V_{IH} max = 2.1V	1.8V power domain
UART_RTS	55	DO	Request to send	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V	1.8V power domain

				V_{IH} max = 2.1V	
UART_CTS	56	DI	Clear to send	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain
UART_DSR	57	DO	Data set ready	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V V_{IH} max = 2.1V	1.8V power domain. DO not pull-up external.
UART_DTR	58	DI	Data terminal ready	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V V_{IH} max = 2.1V	1.8V power domain.
UART_DCD	59	DO	Data carrier detection	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain
UART_RI	60	DO	Ring indicator	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain
Debug UART Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART_DEBUG_TXD	68	DO	Transmit data	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain It is strongly recommended to add test point.
UART_DEBUG_RXD	67	DI	Receive data	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V V_{IH} max = 2.1V	1.8V power domain It is strongly recommended to add test point.
WLAN Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLEEP_CLK	6	DO	WLAN sleep clock	V_{OL} max = 0.45V V_{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC
COEX_UART_TX	7	DO	LTE transmitter sync for coexistence with UART	V_{OL} max = 0.45V V_{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC
COEX_UART_RX/USB_BOOT	8	DI	LTE receiver sync for coexistence with UART/Force boot from USB interface	V_{IL} max = 0.63V V_{IH} min = 1.17V	Only supported by firmware with WiFi. Pull-up this pin to VREF_1V8 and then power on the module, the module will enter emergency download mode. It is strongly recommended to add test point.
WLAN_EN	12	DO	WLAN enable	V_{OL} max = 0.45V V_{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC. DO not pull-up external.
WLAN_3V3_EN	13	DO	WLAN power enable	V_{OL} max = 0.45V V_{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC

SDIO_CMD	14	IO	Secure digital CMD	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V VIH max = 2.1V	Pull-up to 1.8V through external 10K resistance
SDIO_CLK	19	DO	Secure digital CLK	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain
SDIO_DATA0	15	IO	Secure digital IO data bit 0	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V VIH max = 2.1V	1.8V power domain
SDIO_DATA1	16	IO	Secure digital IO data bit 1	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V VIH max = 2.1V	1.8V power domain
SDIO_DATA2	17	IO	Secure digital IO data bit 2	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V VIH max = 2.1V	1.8V power domain
SDIO_DATA3	18	IO	Secure digital IO data bit 3	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V VIH max = 2.1V	1.8V power domain
SD card Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC2_DATA3	109	IO	Secure digital controller data bit 3	**1.8V:** V_{OL} max=0.45V V_{OH} min=1.4V V_{IL} min=-0.3V V_{IL} max=0.58V V_{IH} min=1.27V V_{IH} max=2.0V **3.0V:**	SDC signal level can be selected according to the signal level supported by SD card. Please refer to SD 3.0 protocol for details. If do not need SDC, leave this pin not connected.
SDC2_DATA2	110	IO	Secure digital controller 2 data bit 2		
SDC2_DATA1	108	IO	Secure digital controller 2 data bit 1		

				V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	
SDC2_DATA0	113	IO	Secure digital controller 2 data bit 0		
SDC2_CMD	111	IO	Secure digital controller 2 command		
SDC2_CLK	112	DO	Secure digital controller 2 clock	**1.8V**: V_{OL}max=0.45V V_{OH}min=1.4V **3.0V**: V_{OL}max=0.38V V_{OH}min=2.01V	
SDC2_DET_N	114	DI	Secure digital card detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain If do not need this, leave this pin not connected.
SDC2_PWR_EN	115	DO	Secure digital card power enable	V_{OL}max = 0.45V V_{OH}min = 1.35V	1.8V power domain If do not need this, leave this pin not connected.
VREF_2P85	116	PO	Secure digital card signal pull up power	Iomax=50mA	1.8V/2.85V Only used for SD card pull up If do not need this, leave this pin not connected.

SGMIIInterface

Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
EPHY_INT_N	82	DI	Ethernet PHY interrupt	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain If do not need this, leave this pin not connected.
EPHY_RST_N	83	DO	Ethernet PHY reset	**For 1.8V:** V_{OL}max=0.45V V_{OH}min=1.4V **For 2.85V:** V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain If do not need this, leave this pin not connected.
SGMII_MDIO_DATA	84	IO	Management data input output data	**For 1.8V:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}max=0.58V V_{IH}min=1.27V	1.8V/2.85V power domain If do not need this, leave this pin not connected.

				For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V V_{IL}max=0.71V V_{IH}min=1.78V	
SGMII_MDIO_CLK	85	DO	Management data input output clock	**For 1.8V:** V_{OL}max=0.45V V_{OH}min=1.4V **For 2.85V:** V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain If do not need this, leave this pin not connected.
SGMII_RX_P	103	AI	SGMII RX+		Use 0.1 µF AC coupled capacitor, and place closer to module. If do not need SGMII, leave this pin not connected.
SGMII_RX_M	104	AI	SGMII RX-		Use 0.1 µF AC coupled capacitor, and place closer to module. If do not need SGMII, leave this pin not connected.
SGMII_TX_P	105	AO	SGMII TX+		Use 0.1 µF AC coupled capacitor, and place closer to PHY. If do not need SGMII, leave this pin not connected.
SGMII_TX_M	106	AO	SGMII TX－		Use 0.1 µF AC coupled capacitor, and place closer to PHY. If do not need SGMII, leave this pin not connected.
VREF_L5	86	PO	SGMIIMDIO signal pull up power		1.8V/2.85V Only used for SGMII MDIO pull up If do not need this, leave this pin not connected.
I2C Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	73	DO	I2C serial clock	V_{OL} max = 0.45V V_{OH} min = 1.35V	Pull-up to 1.8V through external 2.2K resistance. If do not need I2C, leave this pin not connected.
I2C_SDA	74	IO	I2C serial data	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V	Pull-up to 1.8V through external 2.2K resistance. If do not need I2C, leave this pin not connected.

				V_{IH} max = 2.1V	
SPI Interface					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_MISO	32	IO	SPI main input slave output	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V VIH max = 2.1V	1.8V power domain
SPI_MOSI	33	IO	SPI main output slave input	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V VIH max = 2.1V	1.8V power domain
SPI_CLK	34	DO	SPI clock	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain
SPI_CS_N	35	DO	SPI segment	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain
Other Pins					
Pin Name	**Pin NO.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	72	DI	Sleep mode control, External device wakeup module	V_{IL} min = -0.3V V_{IL} max = 0.45V V_{IH} min = 1.53V V_{IH} max = 2.1V	1.8V power domain. Pull-down internally. Edge-triggered, Rising edgewake up module; Falling edge module can enter sleep. If use this signal, please add a pull-up resistor externally.
WAKEUP_OUT	71	DO	wakeup output signal,wake up the external devices	V_{OL} max = 0.8V V_{OH} min = 1.35V	Wakeup external circuits
GPIO	27, 28, 29, 30, 64, 65, 75, 76, 77	IO	General input/output	V_{OL} max = 0.45V V_{OH} min = 1.35V V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V VIH max = 2.1V	If unused, keep them floating. DO not pull-up PIN65 external DO not pull-up PIN77 external
RESERVED	42, 43, 44, 45		RESERVED		

2.4. Power Supply

2.4.1. Power Supply Pins

The GM500-U1G is supplied through the VBAT signal with the following characteristics.

Table 2-4Power Supply

Pin Name	Pin NO.	Description	Minimum	Typical	Maximum	Unit
VBAT	50,51	Power supply for module	3.4	3.8	4.2	V
GND	3,9,11,20,21,31,36,46,49,52,61,63,78,80,81,87~102,107,117	Ground	-		-	

GND signal is the power and signal ground of the module, which needs to be connected to the ground on the system board. If the GND signal is not connected completely, the performance of module will be affected.

2.4.2. Decrease Voltage Drop

The power supply range of the module is 3.4V~ 4.2V. So we recommended to add Energy storage capacitor (C6: 470µF). Filter capacitor(10µF, 0.1µF, 33pF) need to be added to reduce interference. The capacitors should be placed close to the GM500-U1G_A's VBAT pins. The following figure shows structure of the power supply.

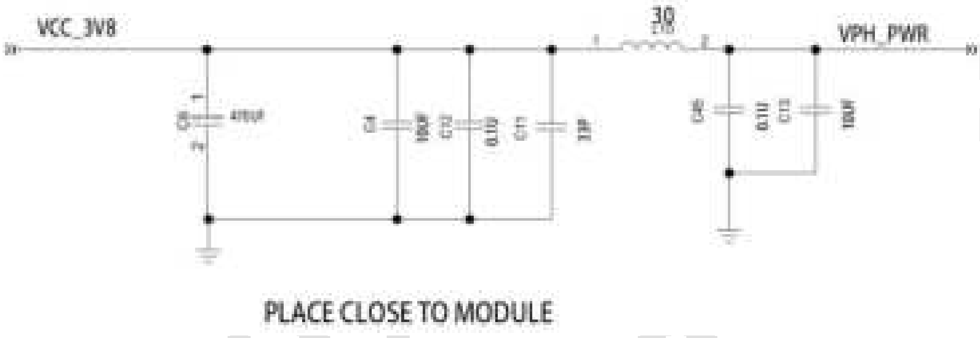


Figure 2–2 The input reference circuit of VBAT

In poor situation of the network, the antenna will transmit at the maximum power, so it's recommended that continuous power supply capacity is up to 2.5A when the module supports GSM mode, and it's up to 1.5A in other modes.

The PCB traces from the VBAT pins to the power source must be wide enough to ensure that there isn't too much voltage drop occurs in the transmitting procedure. The width of VBAT trace should be no less than 2mm, and the principle of the VBAT trace is the longer, the wider.

In addition, make the ground plane as complete as possible, and play more holes.

2.4.3. Reference Circuit of Power Supply

- **Option 1:DC-DC switching**

The over-current capability requirement of DC/DC switching power supply needs to be above 2.5A. When the input and output voltage difference is large, you need to select Buck circuit to improve translate efficiency.

The reference power supply circuit design with DC-DC is shown as figure below:

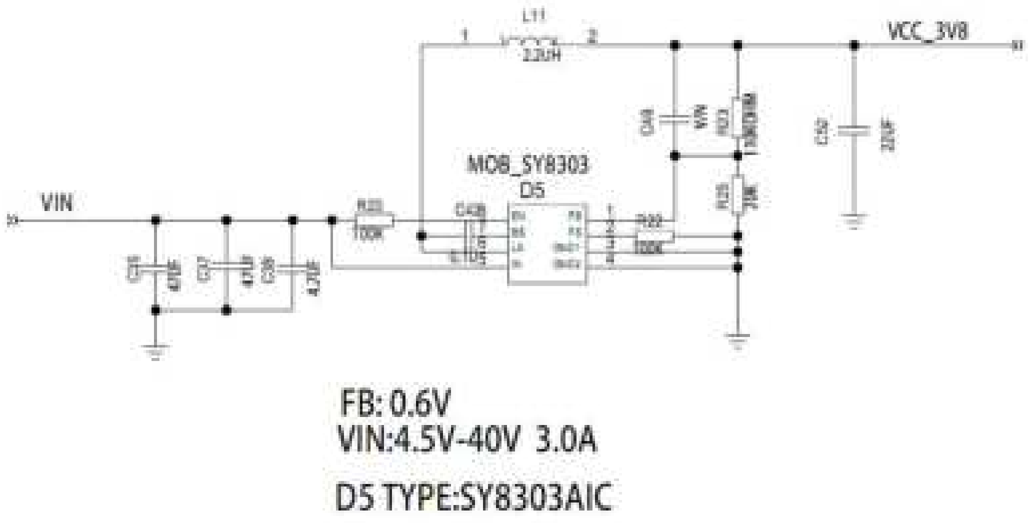


Figure 2–3 Reference circuit of DC-DC

- **Option 2:LDO**

  The over-current capability of LDO is above 2.5A. This LDO is apply to this situation: input and output voltage difference is small. The reference power supply circuit design with LDO is shown as figure below:

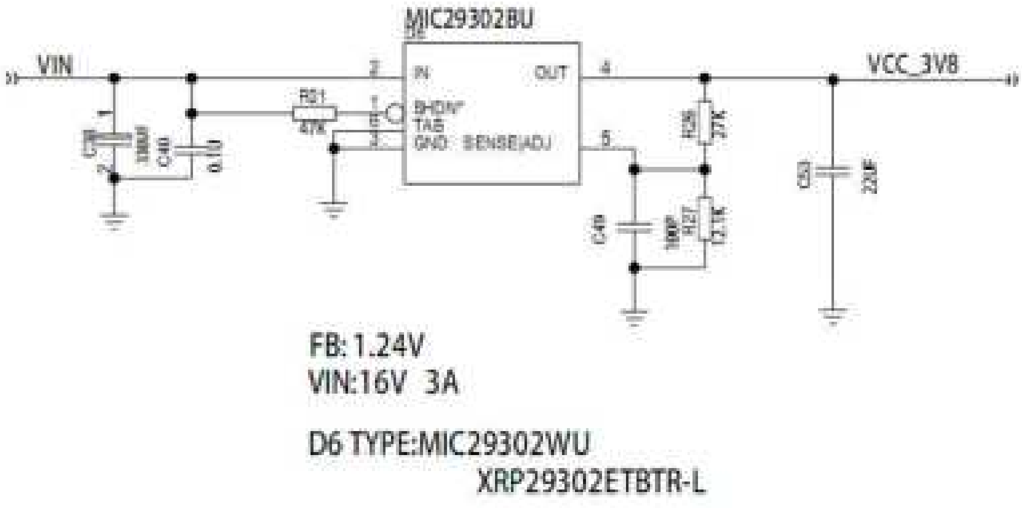


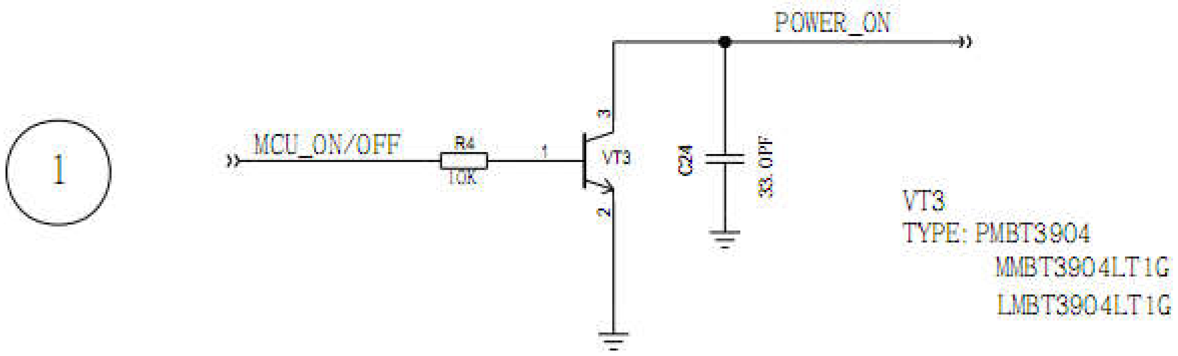
Figure 2–4 Reference circuit of LDO

2.5. Turn on Scenarios

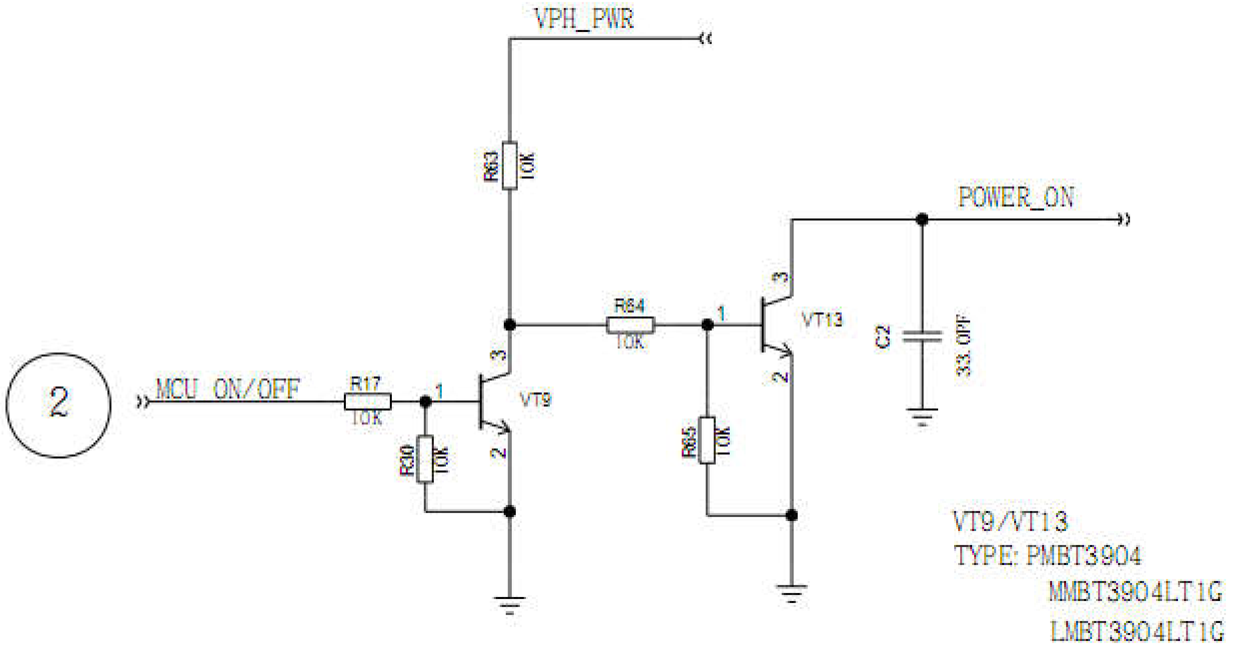
When MCU can provide high/low level pulse with adjustable length, the reference circuit to turn-on/off module is as shown in the following figure below.

The resistors in Figures below are only the recommended value and they need to adjust according to the actual situation.

Power-on by dynatron, the circuit ① connect ON/OFF to high level to power-on the module, the circuit ② can connect ON/OFF to low level to power-on the module



PULL ON/OFF HIGH TO POWER ON



PULL ON/OFF LOW TO POWER ON

Figure 2–5 Reference circuit of POWER_ON

The table below is the information of power-on/off pin

Table 2-5 Definition of POWER_ON

Pin Name	Pin NO.	I/O	Description	Comment
POWER_ON	1	DI	Turn on/off the module	low active. Pull-up to 0.8V internally

The power on scenarios is illustrated as the following figure, the module will power on and working when the POWER_ON pin keep in low level for T1, in this process , please ensure VBAT steady.

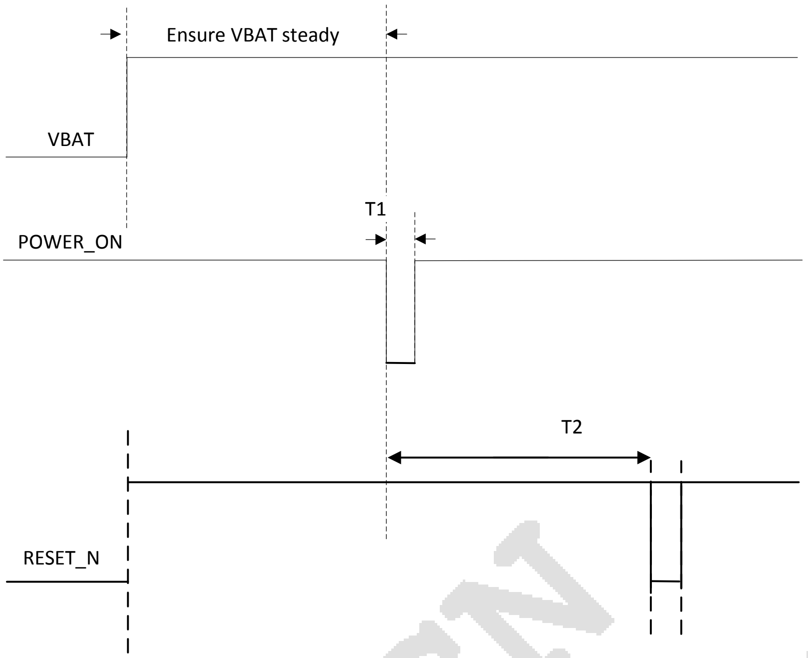


Figure 2–6 Timing of Turning on Mode

Table 2-6 Power-on Time

Parameter	Description	Min	Typical	Max	Unit
T1	The period that the Power-on signal for power on operation is kept on the low PWL	0.1	0.2	--	Second
T2	The minimum interval between the POWER_ON and RESET signals if you want to reset the module after power-on.	10	15	--	Second

2.6. Turn off Scenarios

The module supports two modes to turn off:

Mode 1:

Pull down pin1 (POWER_ON) for 2.5-3s will turn off the module. The power off process will take 22s at least. The reference circuit can refer to the figure 2-5.

Table 2-7Power-off Time

Parameter	Description	Min	Typical	Max	Unit
T2	The period that the POWER_ON signal for power off operation is kept on the low PWL	2.5	3	--	second
T3	The period that the VBAT signal should be kept after power off operation is down	22	--	--	second

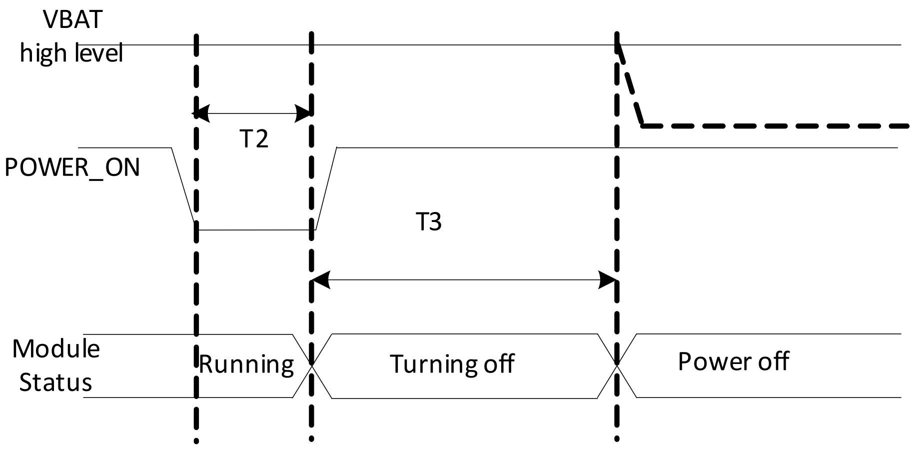


Figure 2–7Timing of Turning off Mode

Mode 2:

Send command of AT+ZTURNOFF, and the power off process will take 15s at least.

Note:when using modules, you need to avoid power off abnormally and frequently, as it will cause several risks shown as below:

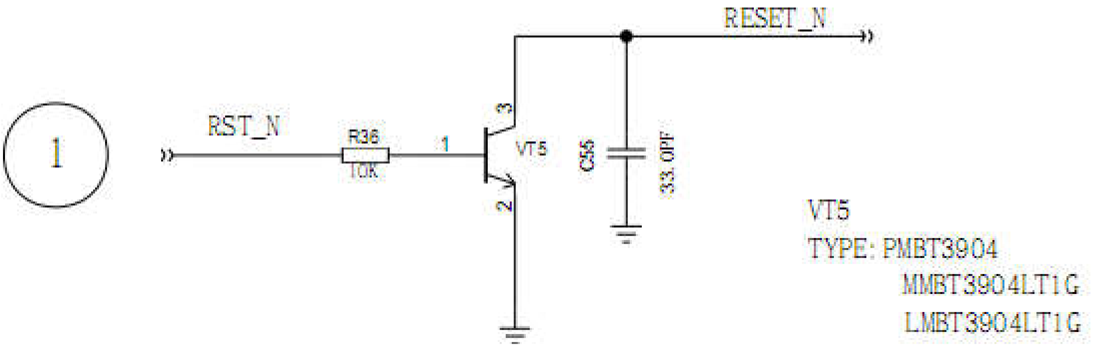
1. it will damage the flash permanently.

2. it can’t send deregister message to e-NodeB, and the MMS takes for the module is still registering to network, and it won’t remind "the user can’t reach" or "the user has turn down" when it’s called(MT).

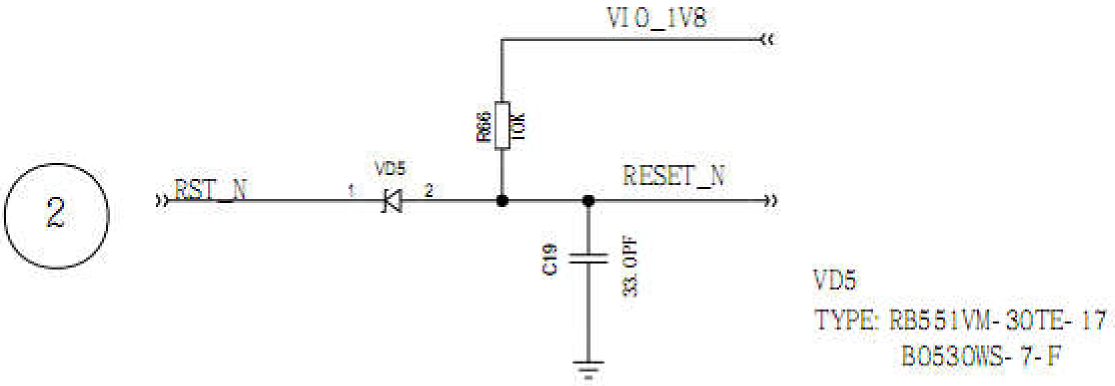
2.7. Reset Scenarios

When the software stops response, you can pulled down RESET_N pin(pin2) for 1 second to reset the module's system.

When MCU can provide high/low level pulse with 1 second, the reference circuit to reset module is as shown in the following figure below. The resistors in Figures below are only the recommended value and they need to adjust according to the actual situation.



PULL RST_N HIGH TO RESET



PULL RST_N LOW TO RESET

Figure 2–8reference circuit to reset module

The reset scenario is illustrated as the following figure,

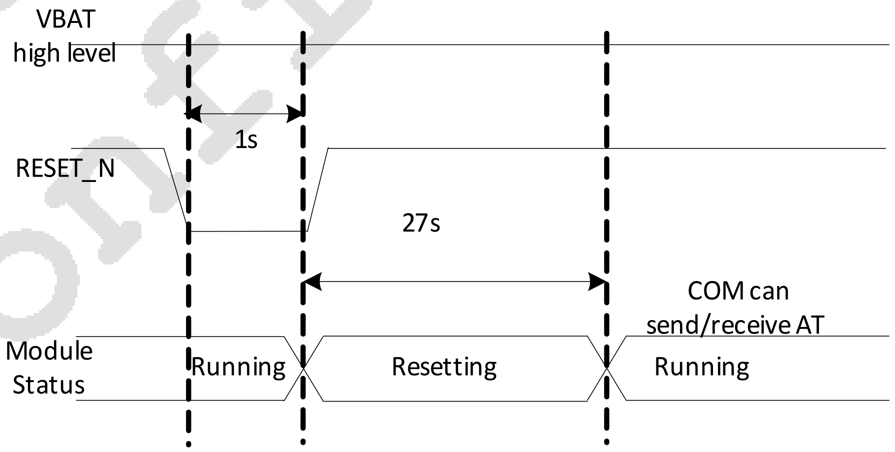


Figure 2–9Timing of Reset Mode

Mode 2:

Send command of AT+ZRST, and the RESET process until the AT port can communicate will take 27s at least.

2.8. USIM Card Interface

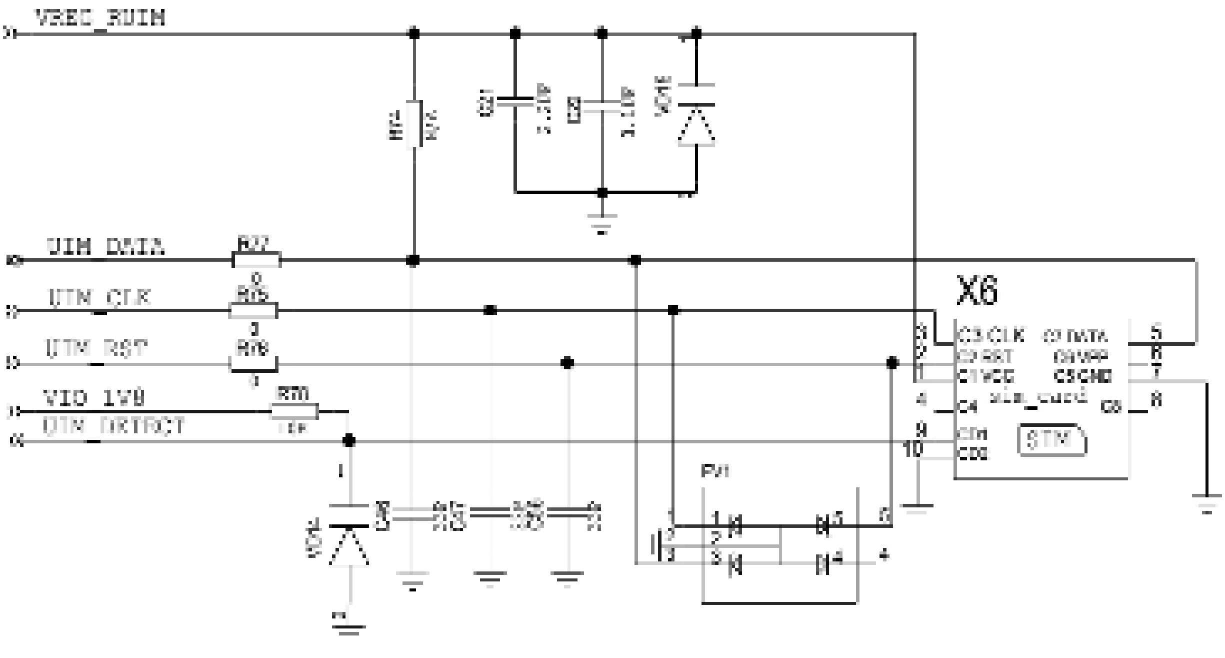
2.8.1. Description of USIM pins

The USIM card interface circuitry meets ETSI and IMT-2000 SIM interface requirements. Both 1.8V and 3.0V USIM cards are supported.

Table 2-8Pin Definition of the USIM Interface

Pin Name	Pin NO.	I/O	Description	Comment
USIM1_VCC	40	PO	Power supply for USIM1 card	Either 1.8V or 3V is supported by the module automatically
USIM1_DATA	38	IO	Data signal of USIM1 card	Pull-up to USIM1_VCC with 10k resistor internally
USIM1_CLK	37	DO	Clock signal of USIM1 card	
USIM1_RST	39	DO	Reset signal of USIM1 card	
USIM1_DETECT	41	DI	USIM1 card hot swap detection pin.	1.8V power domain. The signal is internally pulled up. Keep USIM1_DETECTnot connected, if it is not used.When USIM detect function is enable (send AT command AT+ZSDT=1), and if it is Low, USIM is present; if it is High, USIM is absent.
GND	36		Ground	

The following figure shows the reference design of the 8-pin USIM card.



NOTES:

1. FOR ME3630,R74 CAN BE NA, UIM_DATA PULL-UP HAS BEEN ADDED IN MODULE.

2.RECOMMENDED ADD AN ESD PROTECTION DEVICE FOR SIM PROTECTION.
PLEASE PLACE ESD NEAR THE SIM CARD AND LAYOUT FIRST THROUGH ESD DEVICE.

3.RECOMMENDED ADD 33PF BETWEEN UIM_CLK, UIM_DATA, UIM_RST AND GND TO FILTER RF SIGNAL INTERFERENCE.

4.RECOMMENDED ADD SERIES RESISTANCE IN UIM_DATA AND UIM_CLK SIGNAL.

5.UIM_DETECT IS THE INPUT SIGNAL OF THE MODULE, 1.8V.
RECOMMENDED PULL UP UIM_DETECT TO THE REFERENCE LEVEL (1.8V) BY 10K.
IT IS USED TO DETECT SIM CARD.
WHEN IT IS LOW, THERE IS A CARD, FOR HIGH, NO CARD.
PLEASE CONFIRM IF THE SIM CONNECTOR PLUG MEET THE HARDWARE REQUIREMENTS.

Figure 2–10Reference Circuit of the 8 Pin USIM Card

GM500-U1G supports USIM card hot-plugging via the USIM_ DETECT pin. For details, refer to document ***[AT Command Reference Guide of Module Product GM500-U1G_A]***. If you do not need the USIM card detect function, keep USIM_ DETECT unconnected.

The reference circuit for using a 6-pin USIM card socket is illustrated as the following figure.

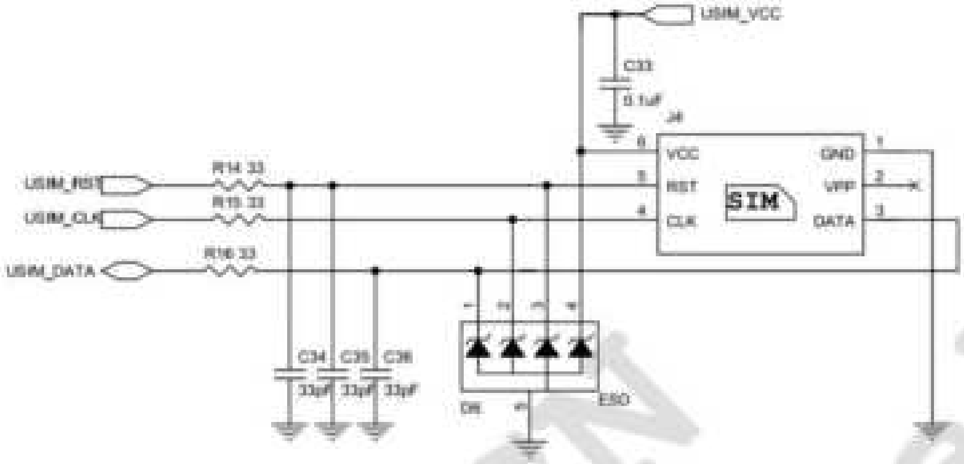


Figure 2–11Reference Circuit of the 6 Pin USIM Card

NOTE:

☑ **R14~R16 and D6 are applied to suppress the EMI spurious transmission and enhance the ESD protection.D6 should be closed to J4**

☑ **The value of C33 should be less than 1uF.**

In order to enhance the reliability and availability of the USIM card in customer's application, please follow the following criterion in the USIM circuit design:

- Keep layout of USIM card as close as possible to the module. Assure the possibility of the length of the trace is less than 50mm.
- Keep USIM card signal away from RF and VBAT alignment.
- Assure the ground between module and USIM cassette short and wide. Keep the width of ground and USIM_VCC no less than 0.5mm to maintain the same electric potential. The decouple capacitor of USIM_VCC should be less than 1uF and must be near to USIM cassette.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away with each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add TVS such as WILL (http://www.willsemi.com) ESDA6V8AV6. The 33Ω resistors should be added in series between the module and the USIM card so as to suppress the EMI spurious transmission and enhance the ESD protection. Please note that the USIM peripheral circuit should be close to the USIM card socket.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion is applied.

2.8.2. Design Considerations for USIM Card Holder

For 8-pin USIM card holder, it is recommended to use Molex 91228.

Please visit***http://www.molex.com*** for more information.

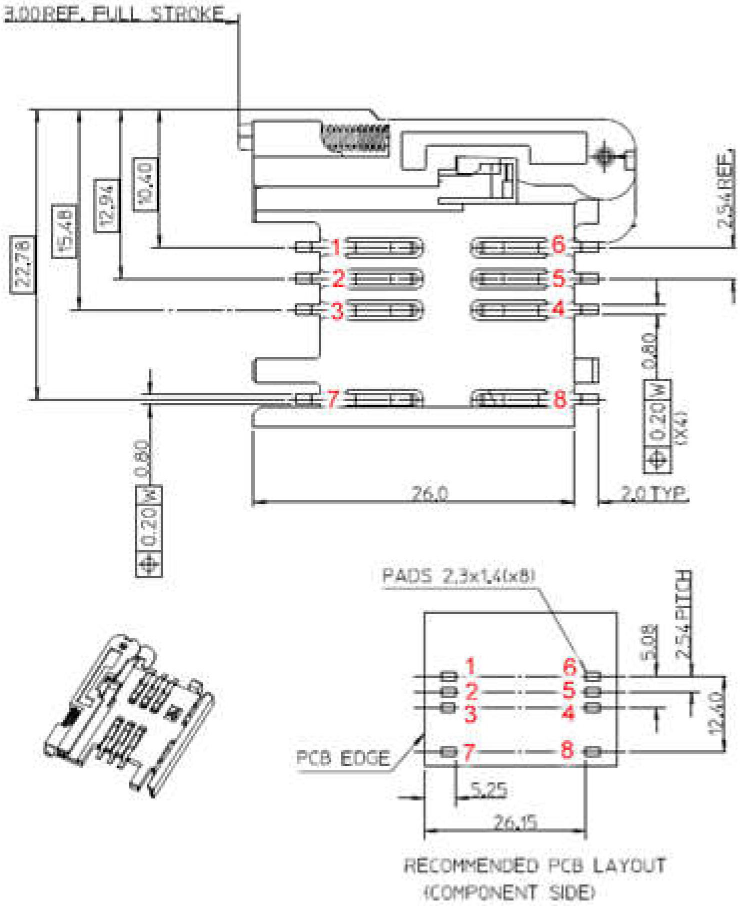


Figure 2–12Molex 91228 USIM Card Holder

Table 2-9Pin Description of Molex USIM Card Holder

Pin Name	Pin NO.	Function
GND	1	Ground
VPP	2	Not connected
DATA I/O	3	USIM card data
CLK	4	USIM card clock
RST	5	USIM card reset
VDD	6	USIM card power supply
DETECT	7	USIM card Detection
NC	8	Not defined, Connect to Ground

For 6-pin USIM card holder, it is recommended to use Amphenol C707 10M006 512 2.

Please visit ***http://www.amphenol.com***for more information.

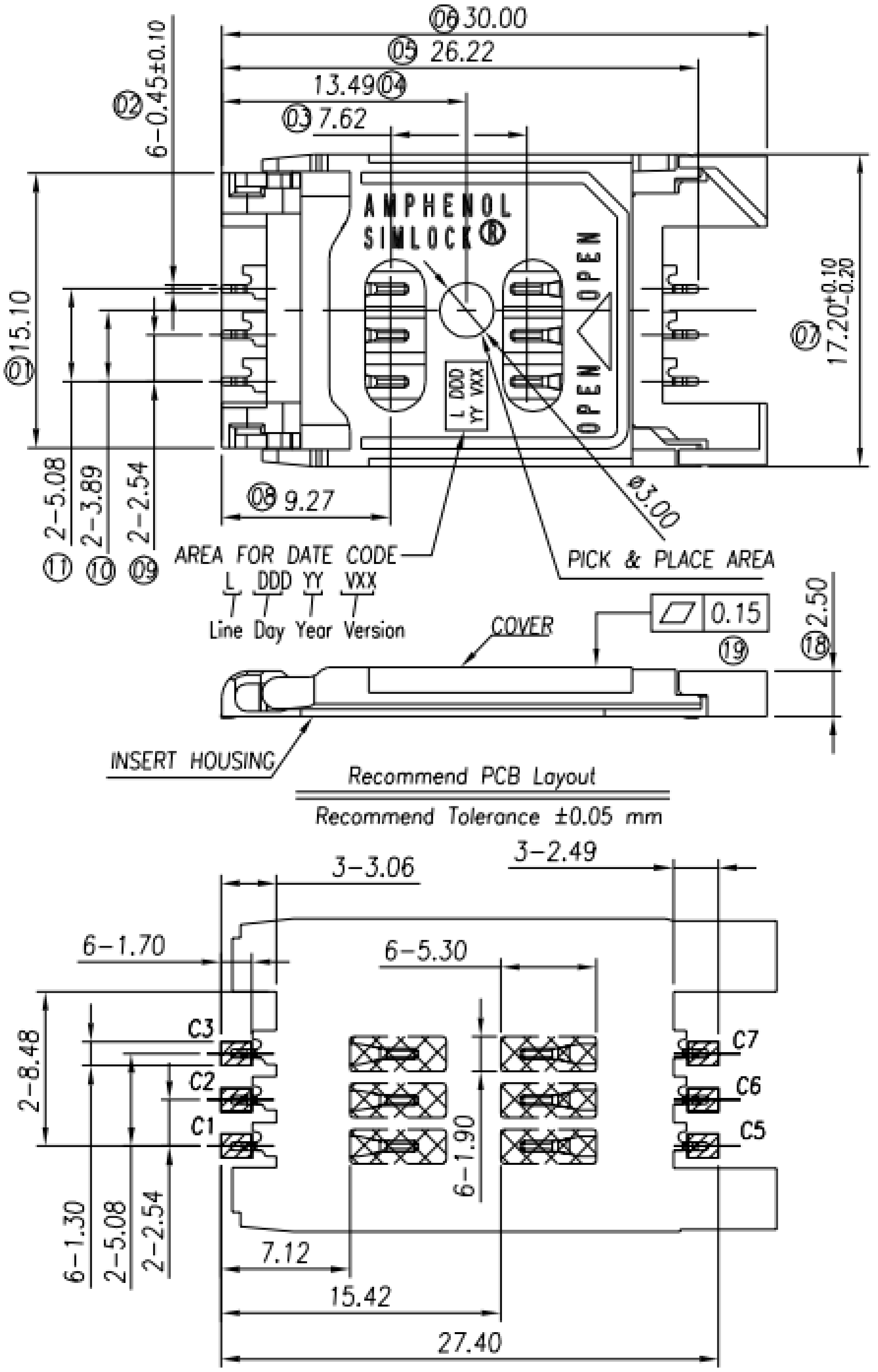


Figure 2–13Amphenol C707 10M006 512 2 USIM Card Holder

Table 2-10Pin Description of Amphenol USIM Card Holder

Pin Name	Pin NO.	Function
GND	1	Ground
VPP	2	Not connected
DATA I/O	3	USIM card data
CLK	4	USIM card clock

RST	5	USIM card reset
VDD	6	USIM card power supply

2.9. USB Interface

GM500-U1G contains one integrated USB transceiver which complies with the USB 2.0 specification and supports high speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) mode. The USB interface is primarily used for AT command, data transmission, software debug and firmware upgrade. The following table shows the pin definition of USB interface.

Table 2-11USB Pin Description

Pin Name	**Pin NO.**	**I/O**	**Description**	**Comment**
USB_DP	24	IO	USB differential data bus (positive)	Require differential impedance of 90Ω
USB_DM	23	IO	USB differential data bus (negative)	Require differential impedance of 90Ω
USB_VBUS	22	DI	USB plug detect pin, not USB power	USB plug detect
GND	21		Ground	

More details about the USB 2.0 specifications, please visit http://www.usb.org/home.

For different use purposes, different designs can be referred to:

- Connect USB interface to USB connector directly. The following figure shows the reference circuit of USB interface

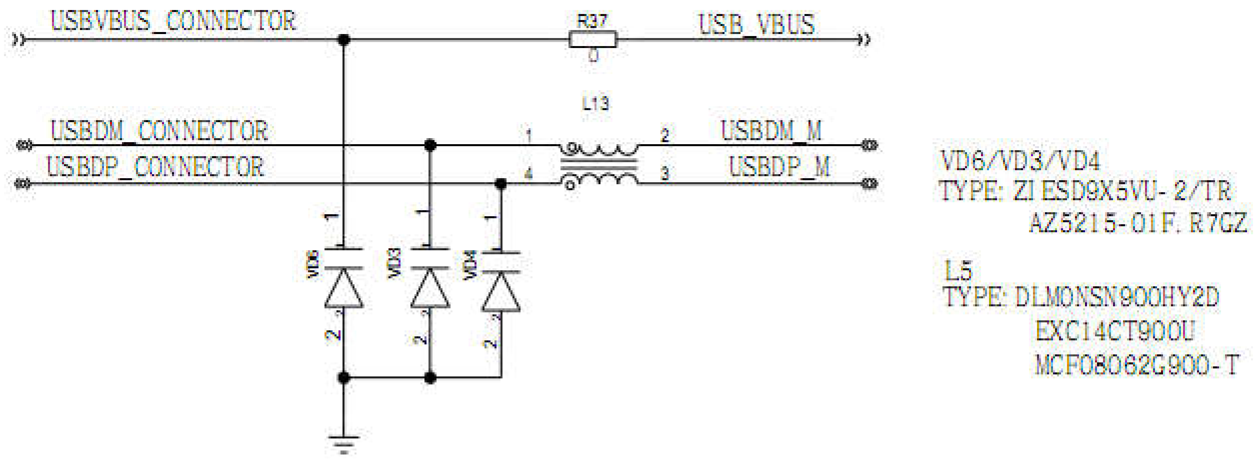


Figure 2–14Reference Circuit of USB Application

- Reference Circuit of USB Communication between module and AP is the one below. The 0Ω in the figure should be placed near pin.

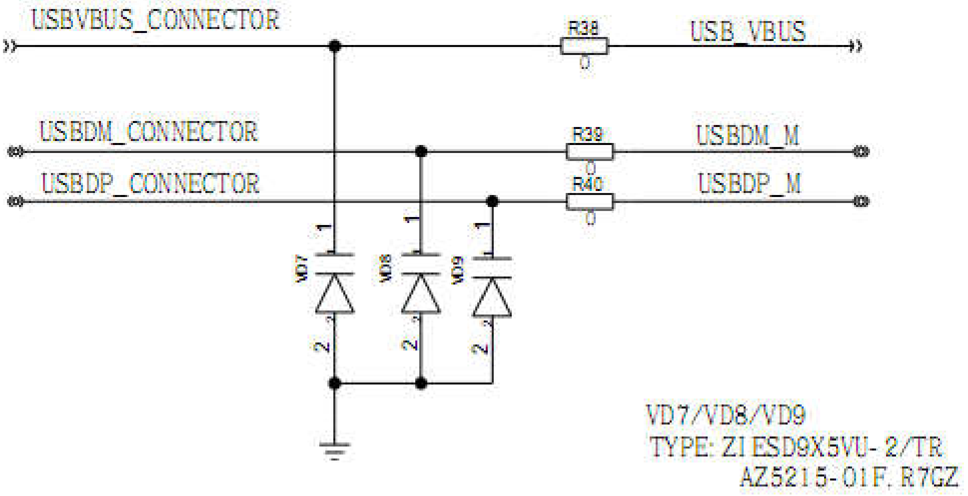


Figure 2–15Reference Circuit of USB Communication between module and AP

- When USB is not the desired function, connect differential signal, power and GND via test points. We recommend to connect these pins to the standard pin header in order to convenient for debugging and upgrading.

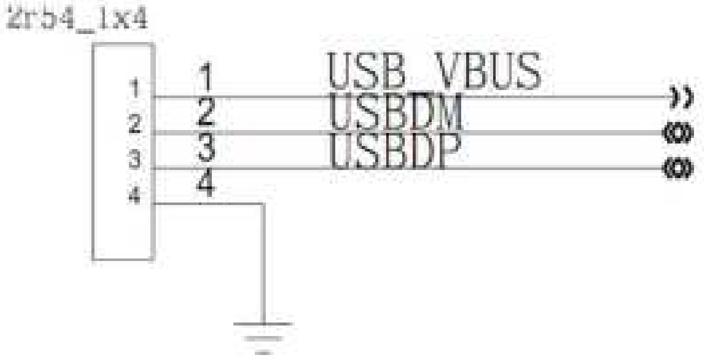


Figure 2–16 Reference circuit of USB when USB is not the desired function

Note:

we recommend connecting the USB interface for update and debugging the module.

we recommend connecting a 0 ohm resistor between module and AP, and placing 0 ohm close to the module pin.

In order to ensure the USB interface design corresponding with the USB 2.0 specification, please comply with the following principles.

It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90ohm.

Pay attention to the influence of junction capacitance of ESD component on USB data lines. Typically, the capacitance value should be less than 3pF.

Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding not only upper and lower layer but also right and left side.

Keep the ESD components as closer to the USB connector as possible.

2.10. UART Interface

The module provides two UART interfaces: Main UART Port and Debug UART Port. The Main UART Port can work in full function mode while the Debug UART Port is used for software debugging . The following show the different features.

Main UART interface support 1200 2400 4800 9600 19200 38400 57600 115200 230400 460800 921600 1000000 1500000 2000000 2500000 3000000 3500000bps baud rate, the default is 115200bps, This interface can be used for data transmission; AT communication or firmware upgrade (upgrade is not supported currently).

Debug UART interface supports 115200bps baud rate. It can be used for software debug and firmware upgrade. The module is designed as the DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection.

The following tables show the pin definition of these two UART interfaces.

Table 2-12Pin Definition of the Main UART Interface

Pin Name	Pin NO.	I/O	Description	Comment
UART_RI	60	DO	Ring indicator	1.8V power domain
UART_DCD	59	DO	Data carrier detection	1.8V power domain
UART_CTS	56	DI	Clear to send	1.8V power domain
UART_RTS	55	DO	Request to send	1.8V power domain
UART_DTR	58	DI	Data terminal ready	1.8V power domain.
UART_DSR	57	DO	Data set ready	1.8V power domain. DO not pull-up external.
UART_TXD	53	DO	Transmit data	1.8V power domain
UART_RXD	54	DI	Receive data	1.8V power domain

Table 2-13Pin Definition of the Debug UART Interface

Pin Name	Pin NO.	I/O	Description	Comment
UART_DEBUG_TXD	68	DO	Transmit data	1.8V power domain
UART_DEBUG_RXD	67	DI	Receive data	1.8V power domain

2.10.1. UART CONNECTION

Three normal connections for UART are shown in the figures below:

1. 8-wires UART connection mode, mainly used for MODEM mode(PPP dialing for example)

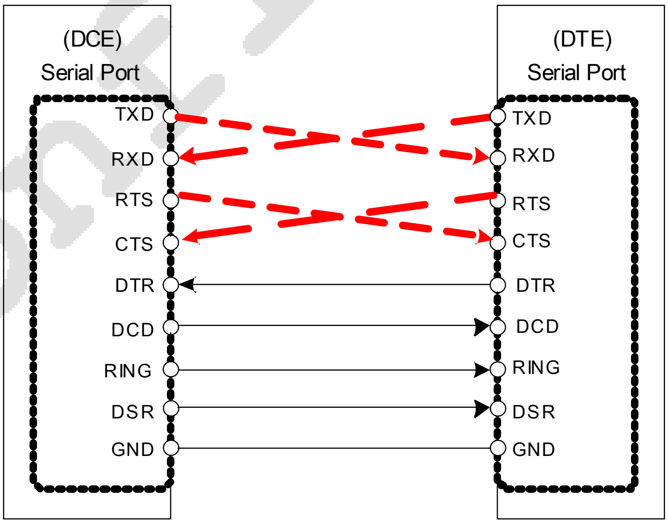


Figure 2–17Schematic of 8-wire UART Connection

2. 3-wire UART connection:

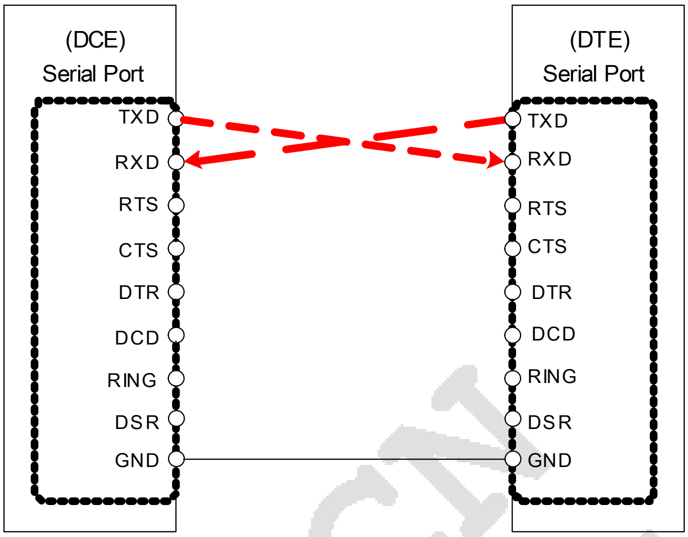


Figure 2–18 Schematic of 3-wire UART Connection

3. 4-wire UART connection, with hardware flow control:

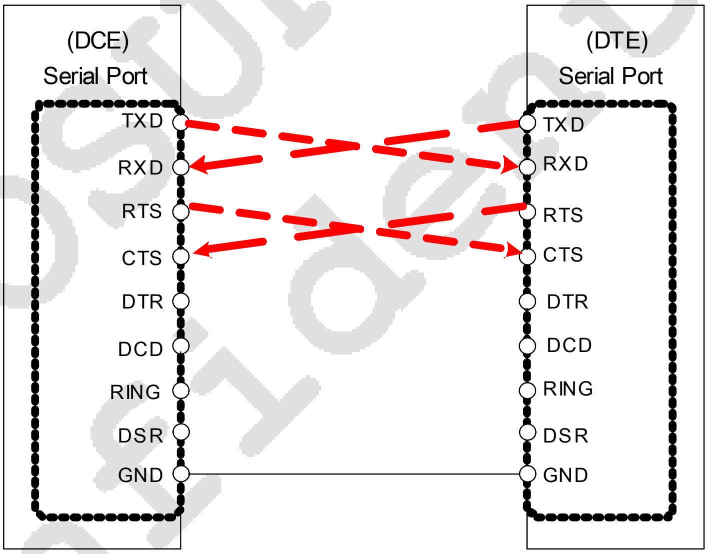


Figure 2–19 Schematic of 4-wire UART Connection

2.10.2. UART LEVEL MATCH

Notice the level match when connect module to external MCU. Level must be less than 3.0V under normal operation, and its default speed rate is 115200 bps.

We recommend to use audion or IC for UART level match circuit. The pictures below are the recommended level switch circuit for TXD, RXD, CTS, RTS. Each pin recommend two kinds of circuit, and you can select any one if necessarily.

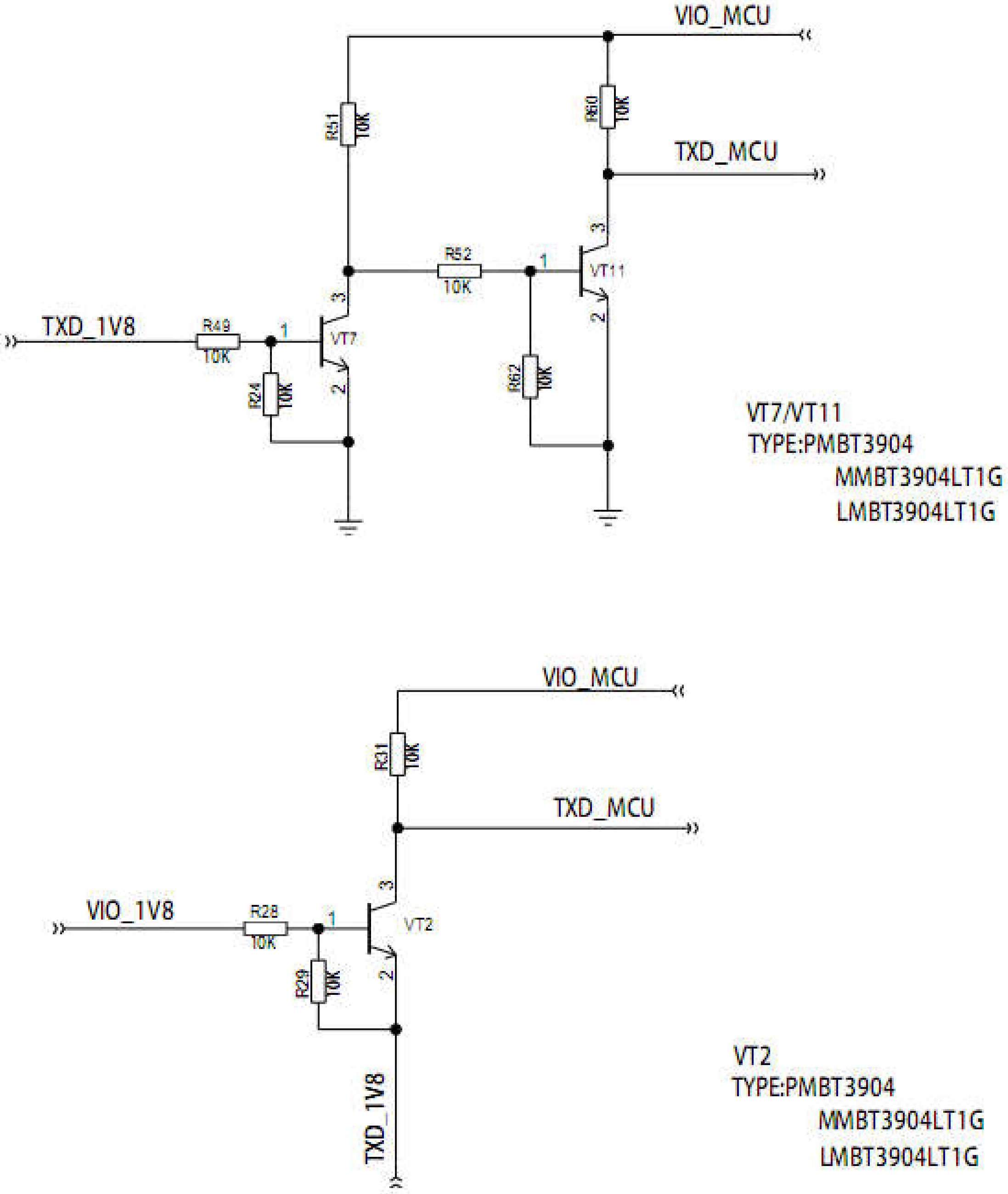
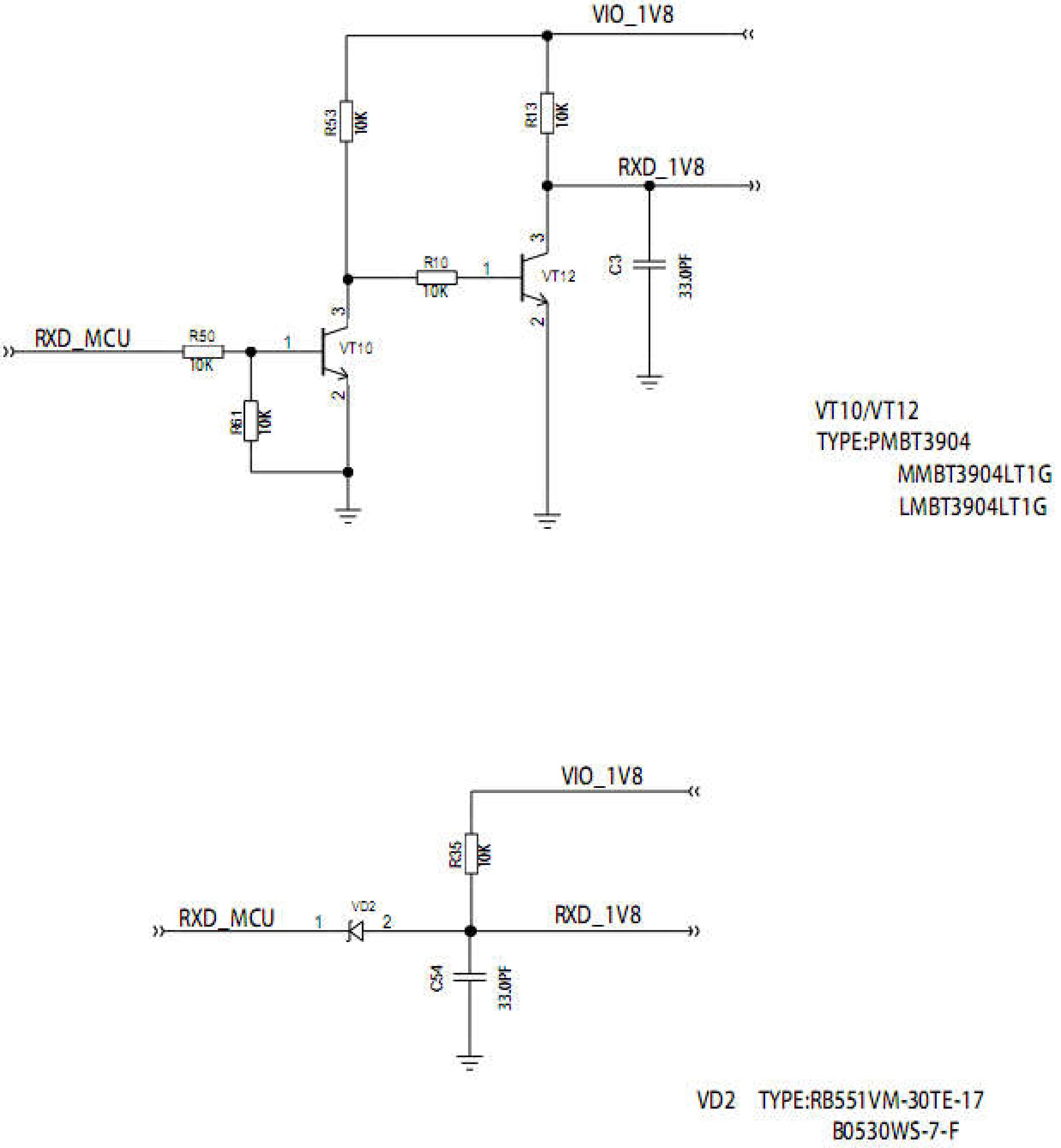


Figure 2–20Recommended TXD circuit



VT10/VT12
TYPE:PMBT3904
MMBT3904LT1G
LMBT3904LT1G

VD2 TYPE:RB551VM-30TE-17
B0530WS-7-F

Figure 2–21Recommended RXD circuit

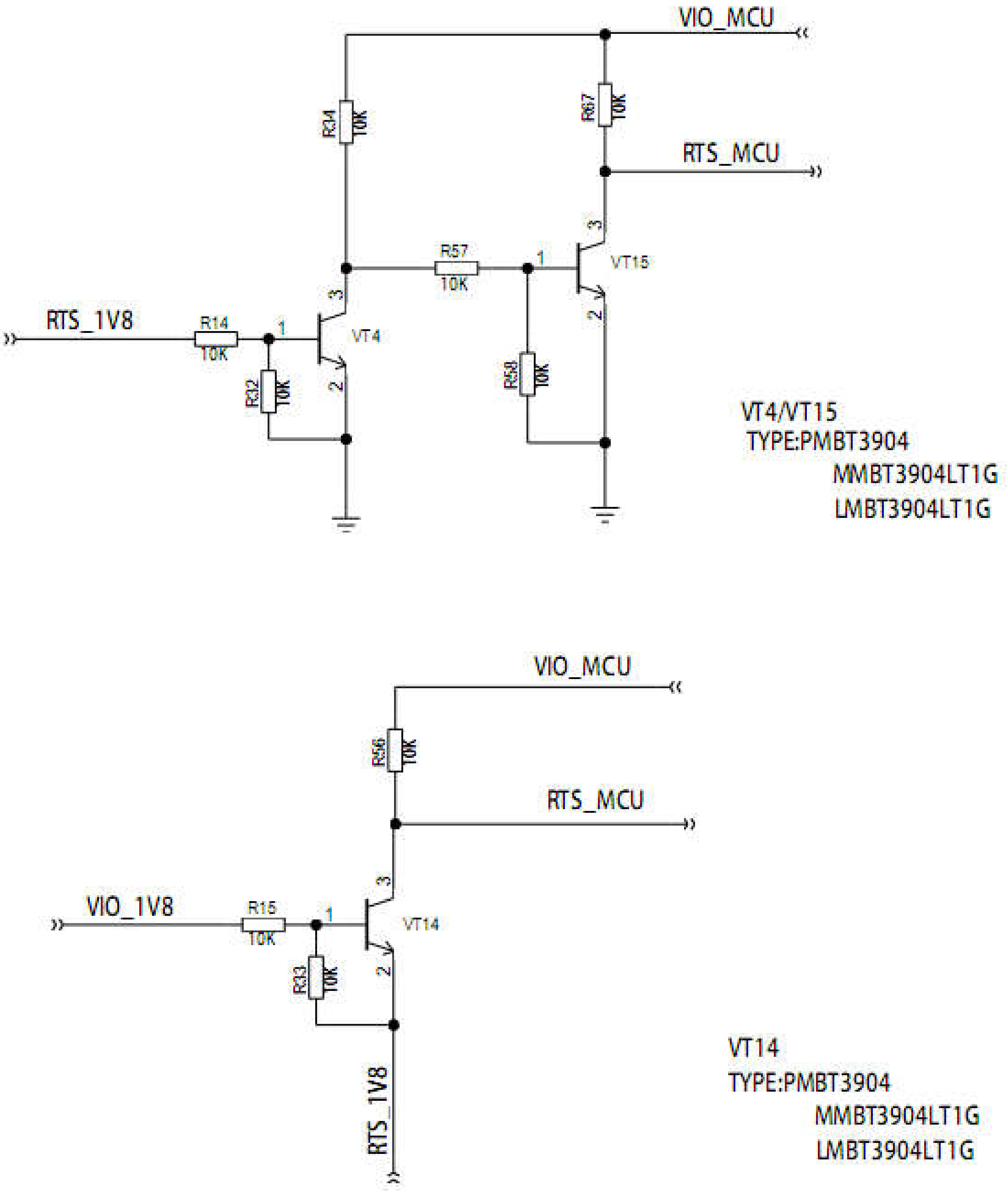


Figure 2–22Recommended RTS circuit

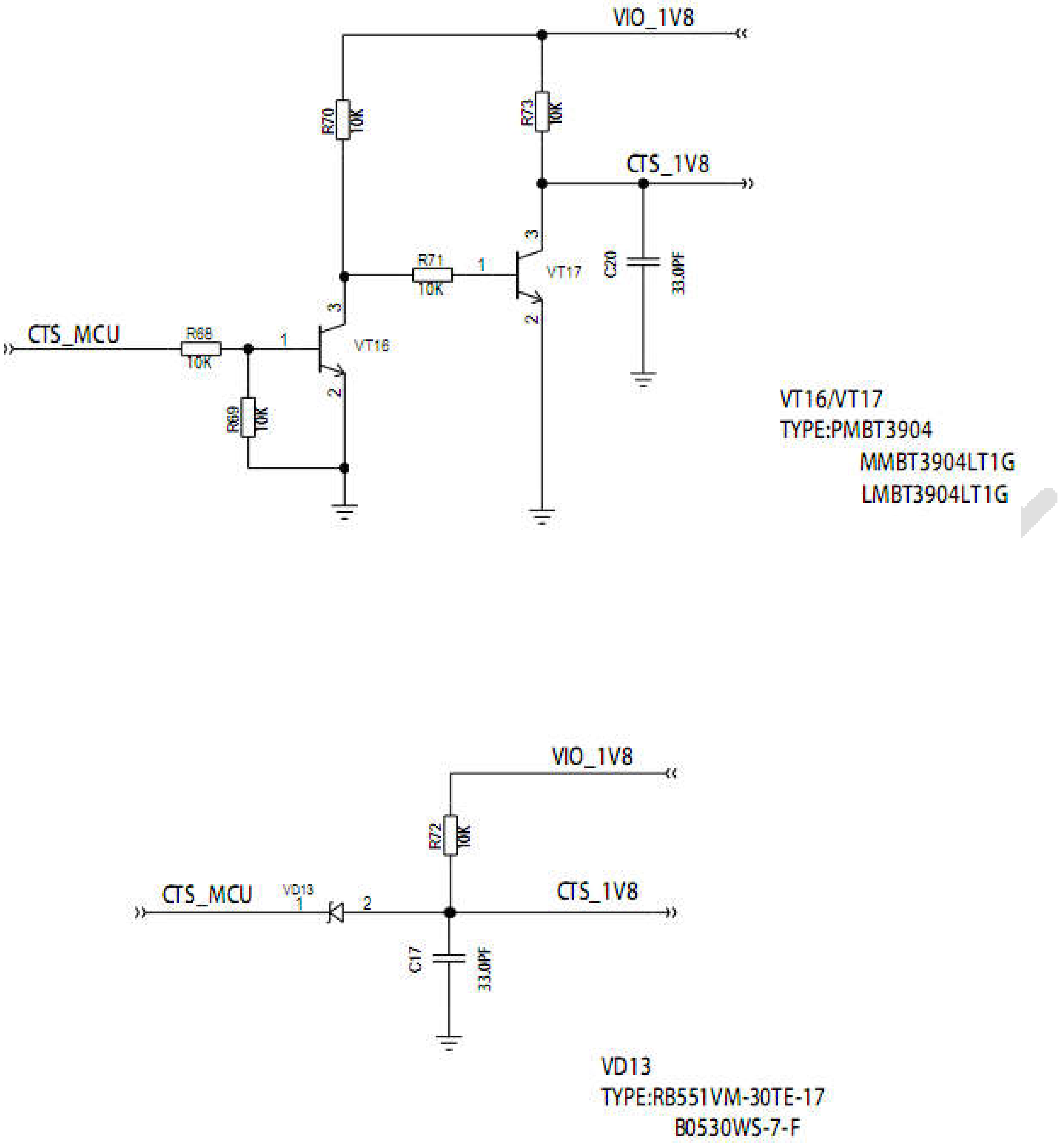
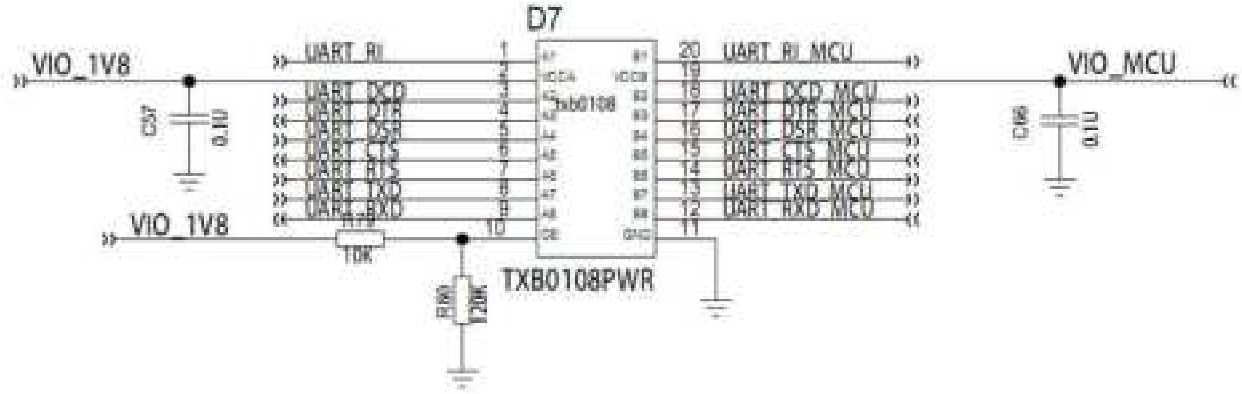


Figure 2–23Recommended CTS circuit

2.10.3. Use ic for level switch



NOTES:

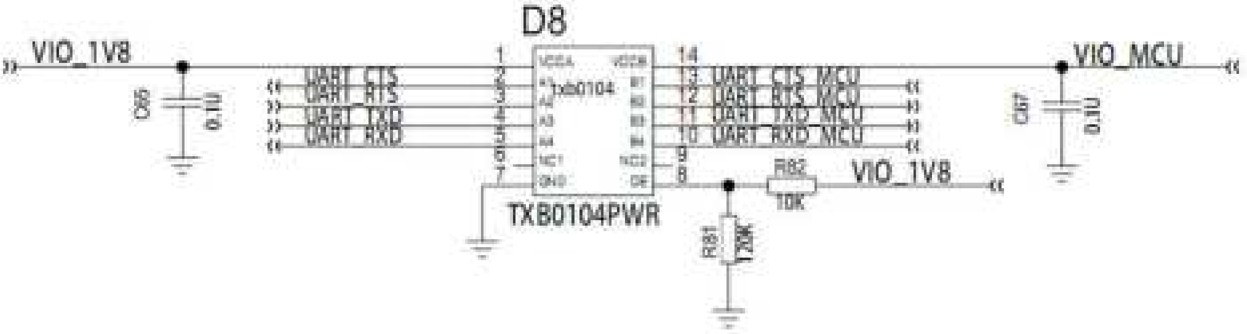
1.THE VOLTAGE DOMAIN OF UART IS 1.8V.

TXB0108 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.

2.VCCA SHOULD NOT EXCEED VCCB.

3.FOR MORE INFORMATION ABOUT TXB0108, PLEASE REFER TO THE DATASHEET.

Figure 2–24Recommended 8-wires UART level switch circuit



NOTES:

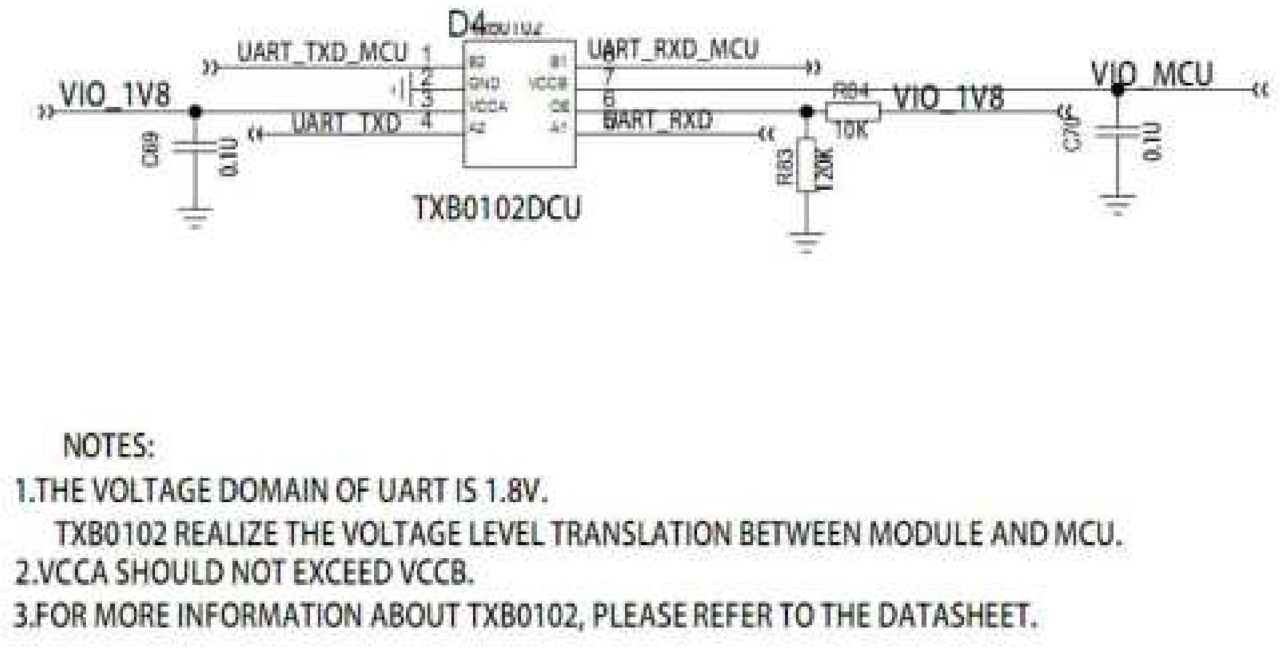
1.THE VOLTAGE DOMAIN OF UART IS 1.8V.

TXB0104 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.

2.VCCA SHOULD NOT EXCEED VCCB.

3.FOR MORE INFORMATION ABOUT TXB0104, PLEASE REFER TO THE DATASHEET.

Figure 2–25Recommended 4-wires UART level switch circuit

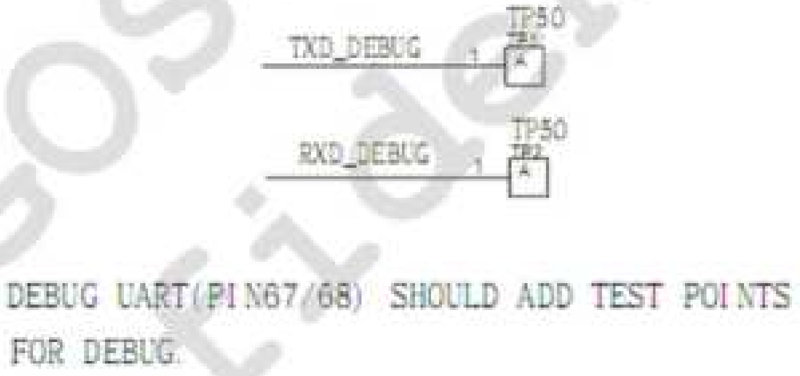


NOTES:
1.THE VOLTAGE DOMAIN OF UART IS 1.8V.
TXB0102 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.
2.VCCA SHOULD NOT EXCEED VCCB.
3.FOR MORE INFORMATION ABOUT TXB0102, PLEASE REFER TO THE DATASHEET.

Figure 2–26Recommended 2-wires UART level switch circuit

- **Debug UART Interface**

  Debug UART Interface is 2-wires interface, we recommend the use to connect this two pins to test points or jumper header.



DEBUG UART(PIN67/68) SHOULD ADD TEST POINTS FOR DEBUG.

Figure 2–27 The test point of debug UART

2.11. Network Status Indication

The network indication pin LED_MODE can be used to drive a network status indicator LED. The different modes of status indicator flashing indicate different network statuses. The following tables describe pin definition and logic level changes in different network status.

Table 2-14Pin Definition of Network Indicator

Pin Name	Pin NO.	I/O	Description	Comment
LED_MODE	70	DO	Indicate the module network registration mode	1.8V power domain

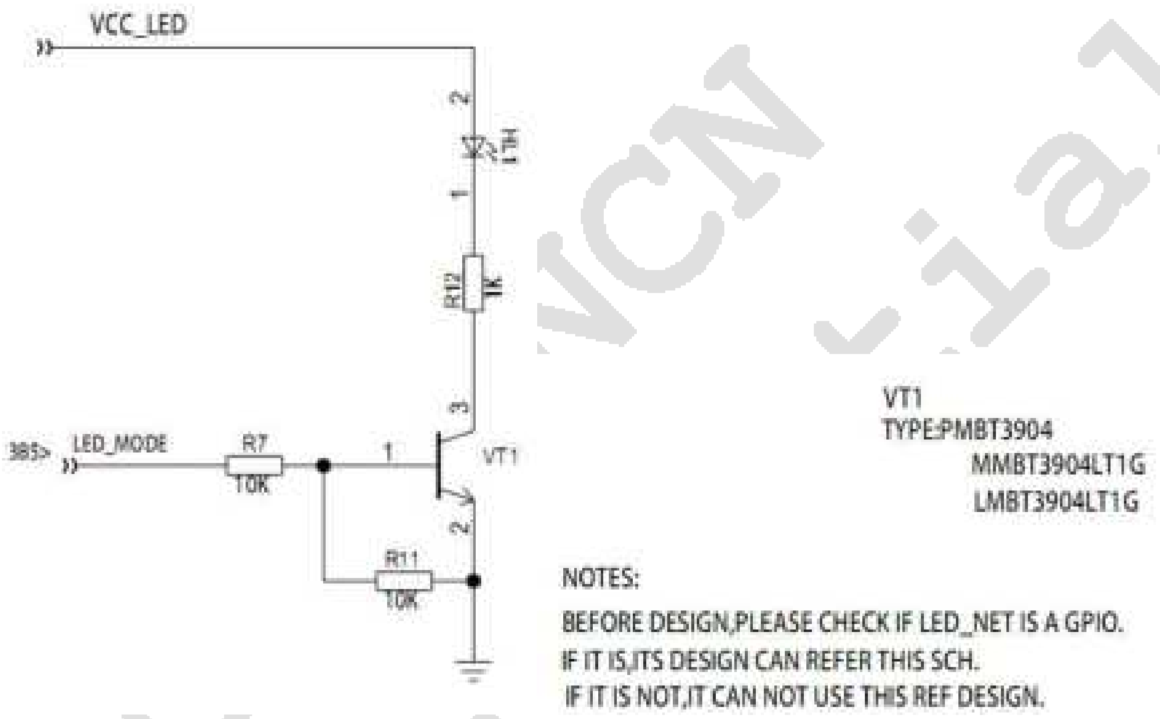
Table 2-15Working State of the Network Indicator

LED Status	Module status
High level, LED on	Module register to networksuccess
Low level, LED off	Module not register to network(module is in flight mode or power off)
Low level 1s(LED off), High level 1s(LED on)	PDP activated, and get the IP address or Socket established

Figure below is the reference circuit design diagram.

NOTE:

The resistors R11, R12 and R7 in Figures below are only the recommended value and they need to adjust according to the actual situation.



NOTES:
BEFORE DESIGN,PLEASE CHECK IF LED_NET IS A GPIO.
IF IT IS,ITS DESIGN CAN REFER THIS SCH.
IF IT IS NOT,IT CAN NOT USE THIS REF DESIGN.

Figure 2–28Reference Circuit of the Network Indicator

2.12. POWER_ON/OFF Status Indicator ON_STATE

PIN69(ON_STATE) is used to indicate the status of POWER_ON/OFF

Table 2-16Pin Definition of ON_STATE

Pin Name	Pin NO.	Description
ON_STATE	69	High level: module power on and ready, it can send/receive AT command. Low level: module power off/reset state, and can't send/receive AT command.

The recommend connection mode of this pin are shown as below, you can select one property mode according to you necessary:

Mode 1:this pin is used as GPIO output pin, the MCU can judge the state of module according to the high/low level.

Mode 2:connect this pin to LED to indicate the status of module, the reference circuit you can refer to chapter 2.11.

Mode 3:you can connect this pin to test point when in the development stage.

2.13. ADC Interface

The module provides 3 ADCs to digitize the analog signal to 15-bit digital data such as battery voltage, temperature and so on. Using AT commandcan read the voltage value on ADC pin. The read value is expressed in mV. For more details of these AT commands, please refer to document ***[AT Command Reference Guide of Module Product GM500-U1G_A]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 2-17 Pin Definition of the ADC

Pin Name	**Pin NO.**	**Description**
ADC1	48	General purpose analog to digital converter.
ADC2	47	General purpose analog to digital converter.
ADC3	108	General purpose analog to digital converter.

The following table describes the characteristic of the ADC function.

Table 2-18 Characteristic of the ADC

Item	**Min**	**Max**	**Unit**
ADC1 voltage range	0.05	4.15	V
ADC2 voltage range	0.05	4.15	V
ADC3 voltage range	0.05	4.15	V

ADC internal structure is shown in the figure below. It can be seen that after each ADC pin inputs the module, there are two conversion channels. You can select 1 / 3 scalingchannel to do ADC conversion, or directly send it to ADC converter. Since the internal reference voltage is 1.8V, the user can determine the channel according to the external voltage range to be converted. The channel selection can be programmed or customized by users 1 / 3 ADC channel configuration by default.

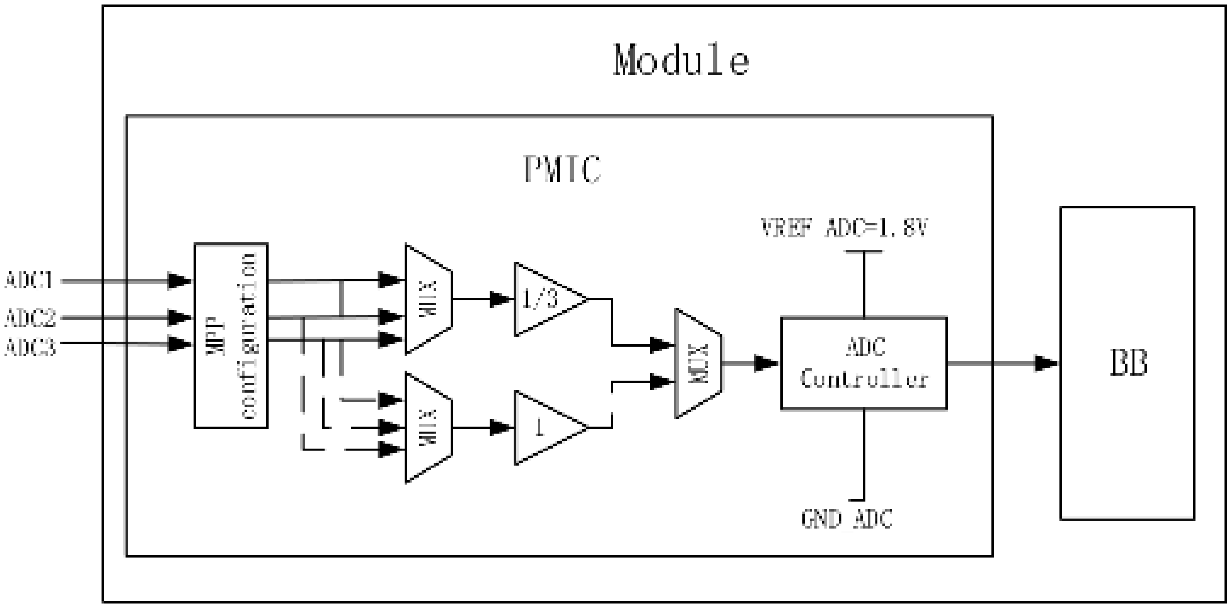


Figure 2–29 ADC internal structure

Table 2-19ADCinterface features(1/3 scaling)

Item	**VIN Min(V)**	**VIN Max(V)**	**ADC channel configuration**	**Minimum input resistance(MΩ)**	**Maximum input current**
ADC1	0.3	VBAT	1/3	1M	100 nA
ADC2	0.3	VBAT	1/3	1M	100 nA

ADC3	0.3	VBAT	1/3	1M	100 nA

Table 2-20ADC interface features(x1 scaling)

Item	VIN Min(V)	VIN Max(V)	ADC channel configuration	Minimum input resistance(MΩ)	Maximum input current
ADC1	0.1	1.7	1	10M	100 nA
ADC2	0.1	1.7	1	10M	100 nA
ADC3	0.1	1.7	1	10M	100 nA

NOTE:

ADC input voltage should not exceed VBAT;
The internal reference voltage of ADC is 1.8V;
When VBAT is not supplied, ADC1, ADC2 and ADC3 are forbidden to input current greater than 1uA.

2.14. WAKEUP_IN Signal

The module provides an AP control interface for communicating with external Application Processor including WAKEUP_IN. The following table shows the pin definition of AP control interface.

Table 2-21 Pin Definition of WAKEUP_IN

Pin Name	Pin NO.	I/O	Description	Comment
WAKEUP_IN	72	DI	Input control signal	1.8V power domain. Pull-down internally. Edge-triggered, Rising edgewake up module; Falling edge modules can enter sleep. If use this signal, please add a pull-up resistor externally.

When the module needs to be waken up, input a related signal via WAKEUP-IN. The following figure is the signal waveform:

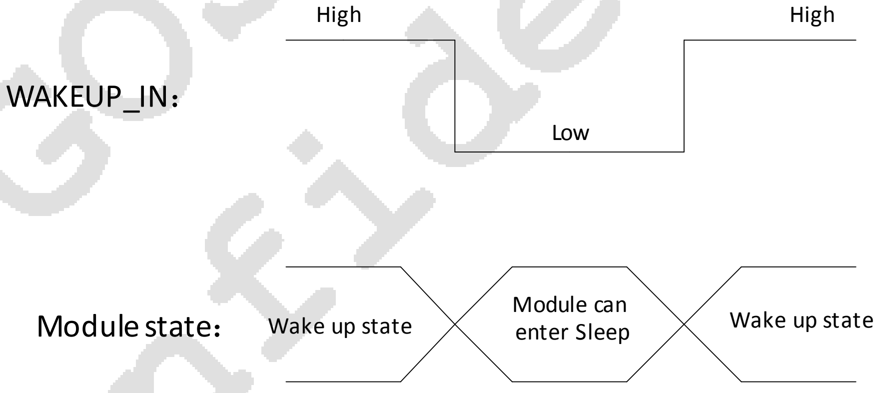


Figure 2–30 WAKEUP_IN input sequence

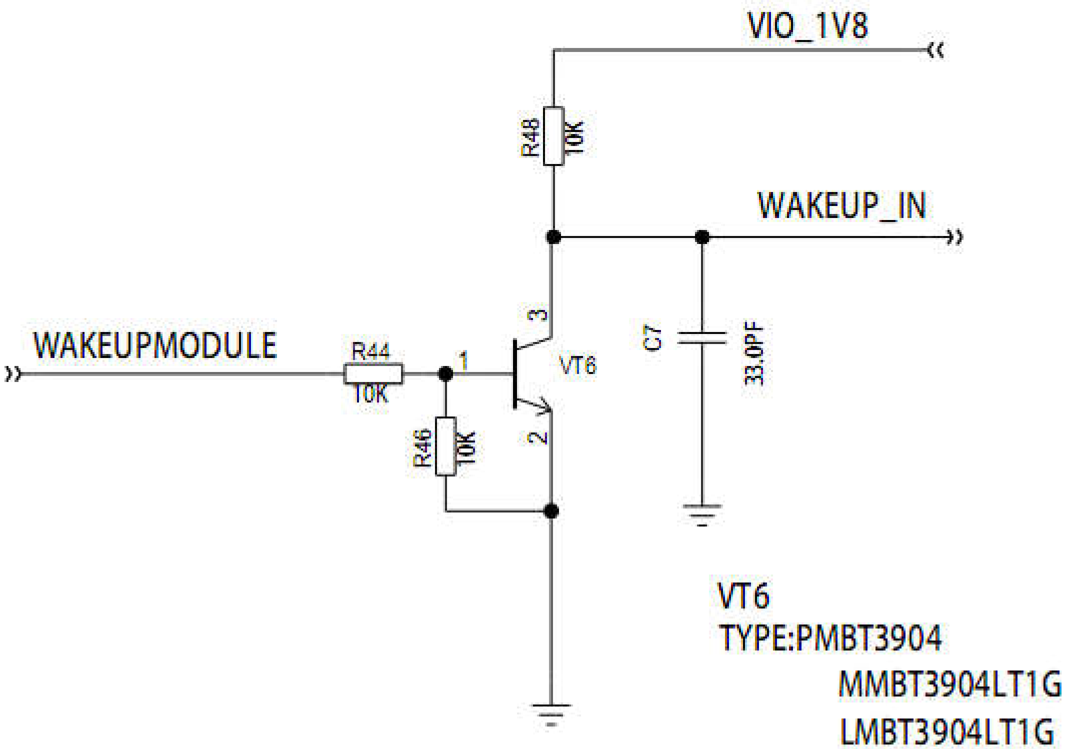


Figure 2–31 WAKEUP_IN reference design

NOTE:

There is Anti-shake design with WAKEUP_IN pin internal, when pull up or down this pin by external processor, the level must last more than 500ms.WAKEUP_IN Usage scenario you can refer to the document namedGOSUNCNGM500-U1G_AModule Power Management Design Guide.pdf

2.15. WAKEUP_OUT Signal

The module provides the WAKEUP_OUT pin which is used to wake up the external devices.

Table 2-22Pin Definition of WAKEUP_OUT

Pin Name	Pin NO.	I/O	Description	Comment
WAKEUP_OUT	71	DO	Output wakeup signal	1.8V power domain Thepin output a high-level voltage by default. When a wake-up source (such as new SMS receive, call, network data) arrives, the pin output a low-level-voltage pulse lasting for 1s

For instance, When a wake-up source arrives, the modulewill output the level shown as the figure below through pin 71.

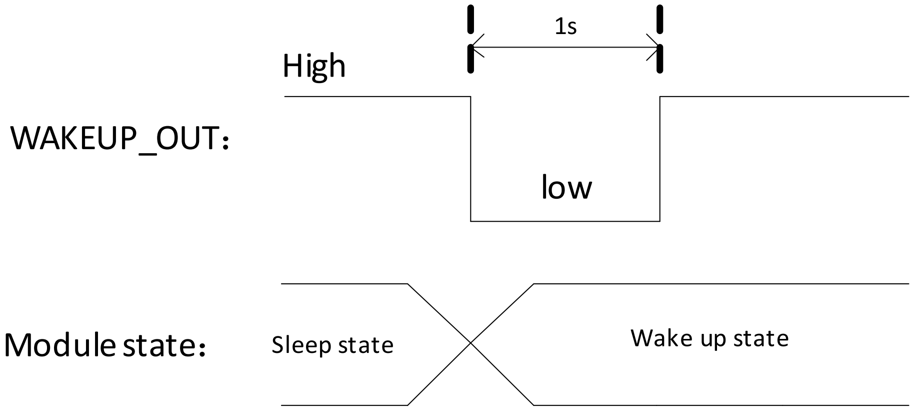


Figure 2–32 The output signal of WAKEUP_OUT

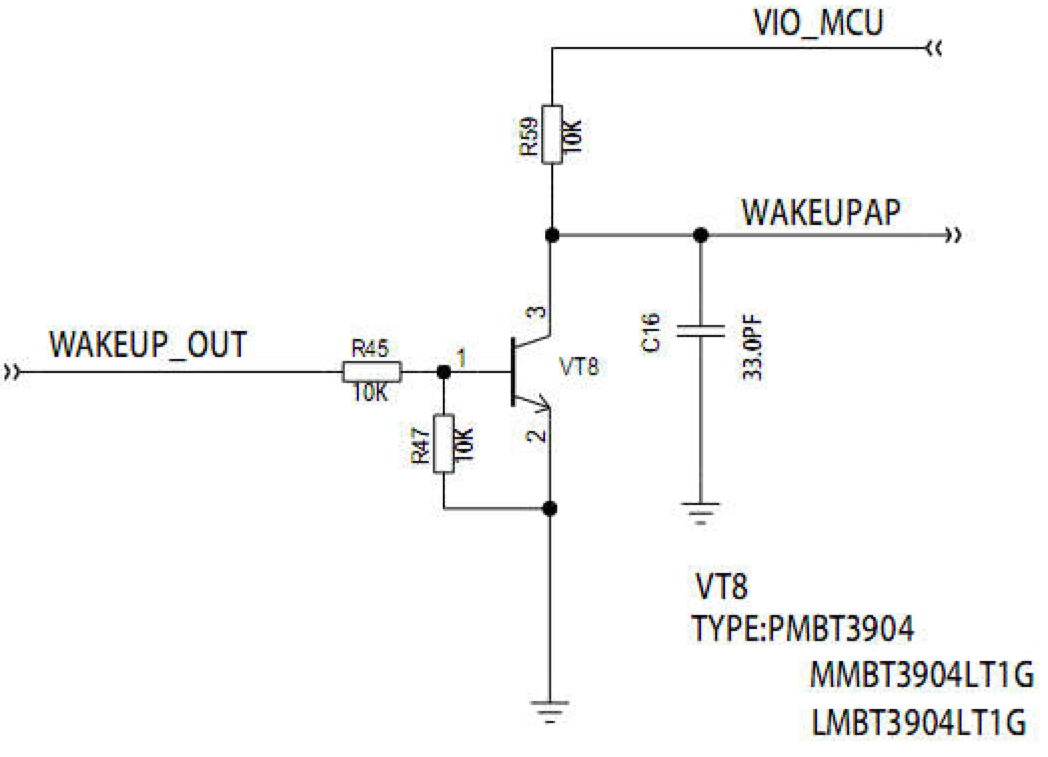


Figure 2–33 WAKEUP_OUTreference design

NOTE:

WAKEUP_OUT Usage scenario you can refer to the document namedGOSUNCNME3630Module Power Management Design Guide.pdf

2.16. GPIO Interface

Module provides 9 GPIO pins. The direction and output voltage level of the GPIO can be set by AT command "AT+ZGPIO". The input voltage level of the GPIO can also be read by AT command "AT+ZGPIO". For more details of these AT commands, please refer to document ***[AT Command Reference Guide of Module Product GM500-U1G_A].***

NOTE: All the GPIO pins are pull-down internally and are input pins in default.

Table 2-23Pin Definition of GPIO

Pin Name	Pin NO.	I/O	Description	Comment
GPIO1	27	IO	General input/output	1.8V power domain,
GPIO2	28	IO	General input/output	1.8V power domain
GPIO3	29	IO	General input/output	1.8V power domain
GPIO4	30	IO	General input/output	1.8V power domain
GPIO5	64	IO	General input/output	1.8V power domain
GPIO6	65	IO	General input/output	1.8V power domain DO not pull-up PIN65 external
GPIO7	75	IO	General input/output	1.8V power domain
GPIO8	76	IO	General input/output	1.8V power domain
GPIO9	77	IO	General input/output	1.8V power domain DO not pull-up PIN77 external

2.17. USB_BOOT

Table2-24 Pin Definition of USB_BOOT

Pin Name	Pin NO.	I/O	Description	Comment
COEX_UART_RX/USB_BOOT	8	DI	LTE receiver sync for coexistence with UART/Force boot from USB interface	Pull-up this pin to VREF_1V8 and then power on the module, the module will enter emergency download mode. It is strongly recommended to add test point.

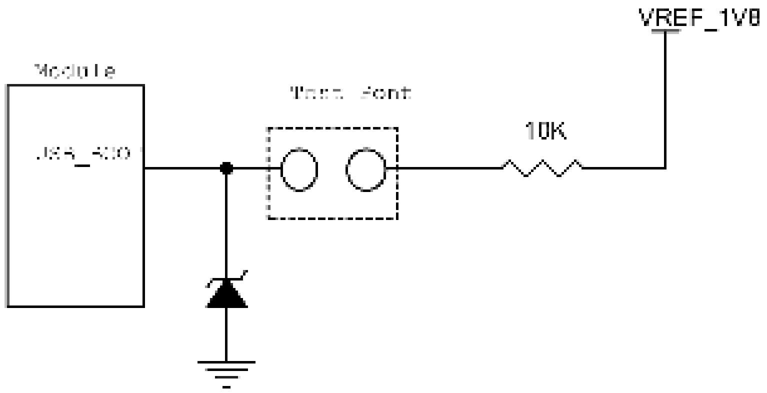


Figure 2–34 USB_BOOTreference design

2.18. SDCardInterface

Table 2-25 Pin Definition ofSD controller Interface

Pin Name	Pin NO.	I/O	Description	Comment
SDC2_DATA3	109	IO	Secure digital controller data bit 3	SDC signal level can be selected according to the signal level supported by SD card. Please refer to SD 3.0 protocol for details. If do not need SDC, leave this pin not connected.
SDC2_DATA2	110	IO	Secure digital controller 2 data bit 2	
SDC2_DATA1	108	IO	Secure digital controller 2 data bit 1	
SDC2_DATA0	113	IO	Secure digital controller 2 data bit 0	
SDC2_CMD	111	IO	Secure digital controller 2 command	

SDC2_CLK	112	DO	Secure digital controller 2 clock	
SDC2_DET_N	114	DI	Secure digital card detection	1.8V power domain If do not need this, leave this pin not connected.
SDC2_PWR_EN	115	DO	Secure digital card power enable	1.8V power domain If do not need this, leave this pin not connected.
VREF_2P85	116	PO	Secure digital card signal pull up power	1.8V/2.85V Iomax=50mA Only used for SD card pull up If do not need this, leave this pin not connected Additional LDO is required for SD card power supply (at least 800mA)

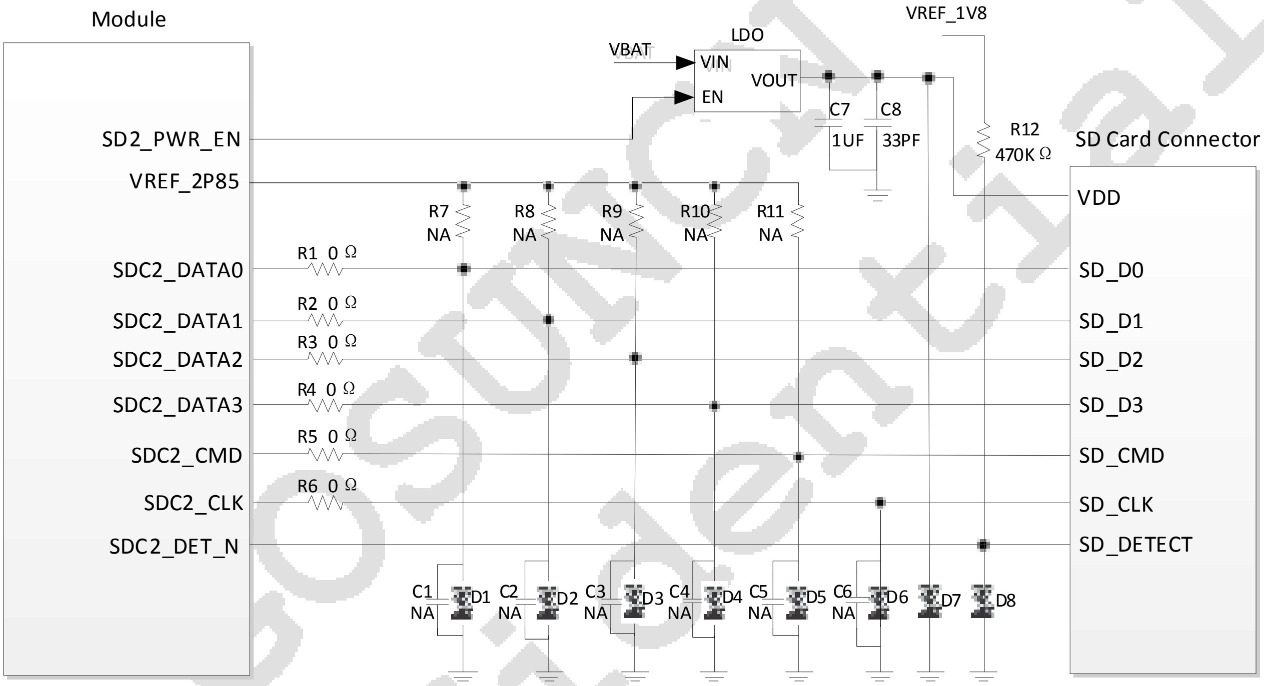


Figure 2–35 SD cardreference design

NOTE:

1) **The maximum output current of module output power VREF_2P85 is 50mA, which can only be used for pull-ups on the SDC2_DATA[0:3] and SDC2_CMD lines. The power supply of SD card needs to be provided from outside the module. Ensure the external LDO regulator for SD Card supports an output current of at least 800 mA to be compliant with the SD v3.0 specification;**
2) **In order to ensure good ESD performance, it is suggested to add TVSnear SD Card pins;**
3) **In order to adjust the signal quality, it is necessary to reserve the series resistance R1 ~ R6, the recommended value is 0 Ω, and reserve capacitance C1 ~ C6, which is NA by default;**
4) **The SD Card signal should be grounded and the impedance should be controlled at 50 Ω± 10%;**
5) **SDC2_CLK and SDC2_ DATA[0:3]/SDC2_CMD needs equal length (the difference is less than 1 mm), and the total length is less than 50 mm; because the internal wiring length of the module is about 7 mm, the external wiring length needs to be less than 43 mm;**

6) In order to ensure the signal quality, it is recommended to add pull-ups R7 ~ R11, default NA,on the SDC2_DATA_[0:3] and SDC2_CMD lines. The resistance range is 10 ~ 100k Ω, recommended 100k Ω.

2.19. SGMII Interface

Table 2-26 Pin Definition of SGMIIInterface

Pin Name	Pin NO.	I/O	Description	Comment
EPHY_INT_N	82	DI	Ethernet PHY interrupt	1.8V power domain If do not need this, leave this pin not connected.
EPHY_RST_N	83	DO	Ethernet PHY reset	1.8V/2.85V power domain If do not need this, leave this pin not connected.
SGMII_MDIO_DATA	84	IO	Management data input output data	1.8V/2.85V power domain If do not need this, leave this pin not connected.
SGMII_MDIO_CLK	85	DO	Management data input output clock	1.8V/2.85V power domain If do not need this, leave this pin not connected.
SGMII_RX_P	103	AI	SGMII RX+	Use 0.1 µF AC coupled capacitor, and place closer to module. If do not need SGMII, leave this pin not connected.
SGMII_RX_M	104	AI	SGMII RX-	Use 0.1 µF AC coupled capacitor, and place closer to module. If do not need SGMII, leave this pin not connected.
SGMII_TX_P	105	AO	SGMII TX+	Use 0.1 µF AC coupled capacitor, and place closer to PHY. If do not need SGMII, leave this pin not connected.
SGMII_TX_M	106	AO	SGMII TX－	Use 0.1 µF AC coupled capacitor, and place closer to PHY. If do not need SGMII, leave this pin not connected.
VREF_L5	86	PO	SGMIIMDIO signal pull up power	1.8V/2.85V Only used for SGMII MDIO pull up If do not need this, leave this pin not connected.

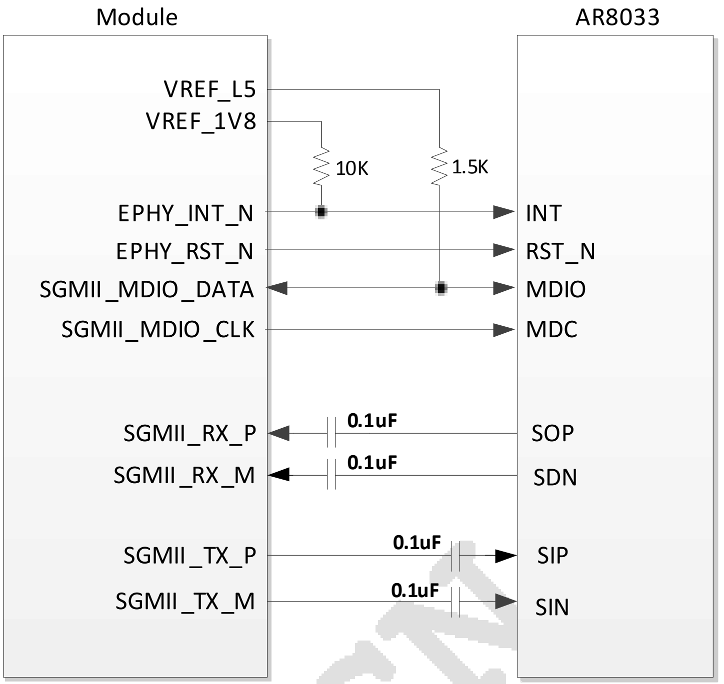


Figure 2–36 SGMII + AR8033typical connection

NOTE:

1) **Route SGMII differential signals with a controlled impedance of 100 Ω;**
2) **Keep SGMII away from other sensitive signals such as analog circuits, RF circuits, audio signals, etc., and away from noise sources such as DCDC and clock signals;**
3) **SGMII intrapair length match<0.5mm;**
4) **TX to RX lane spacing and SGMII to all other signals spacing 3x line width.**

3. Antenna Interface

GM500-U1G antenna interface includes a main antenna, an Rx-diversity antenna and a GNSS antenna to improve receiving performance. The antenna interface has an impedance of 50Ω.

3.1. Pin Definition

The main antenna and Rx-diversity antenna pins definition are shown below.

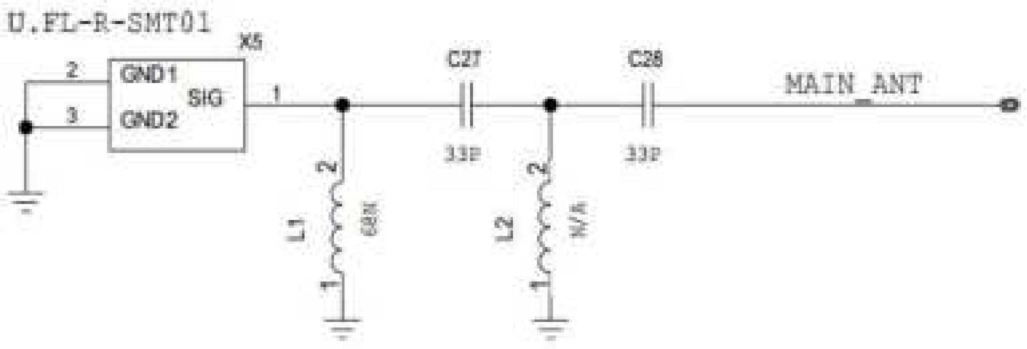
Table 3-1Pin Definition ofAntenna

Pin Name	Pin NO.	I/O	Description	Comment
MAIN_ANT	62	IO	Main antenna	50Ω impedance
DIV_ANT	79	AI	Diversity antenna	50Ω impedance
GNSS_ANT	10	IO	GNSS antenna	50Ω impedance

3.2. Reference Design

The antenna is a sensitive device and its performance is greatly affected by external environments. The radiation performance of the antenna is affected by the module dimensions, antenna position, occupied space size of the antenna, and the grounding of surrounding components of the antenna. Besides, the fixed assembly of the antenna, the wiring of RF cables on the antenna, and the fixed position of the antenna all affect the radiation performance of the antenna too.

The reference design of main antenna and Rx-diversity antenna is shown as below. It should reserve a double-L-type matching circuit for better RF performance, and place these components as close as possible to the module. The capacitors are not mounted by default.



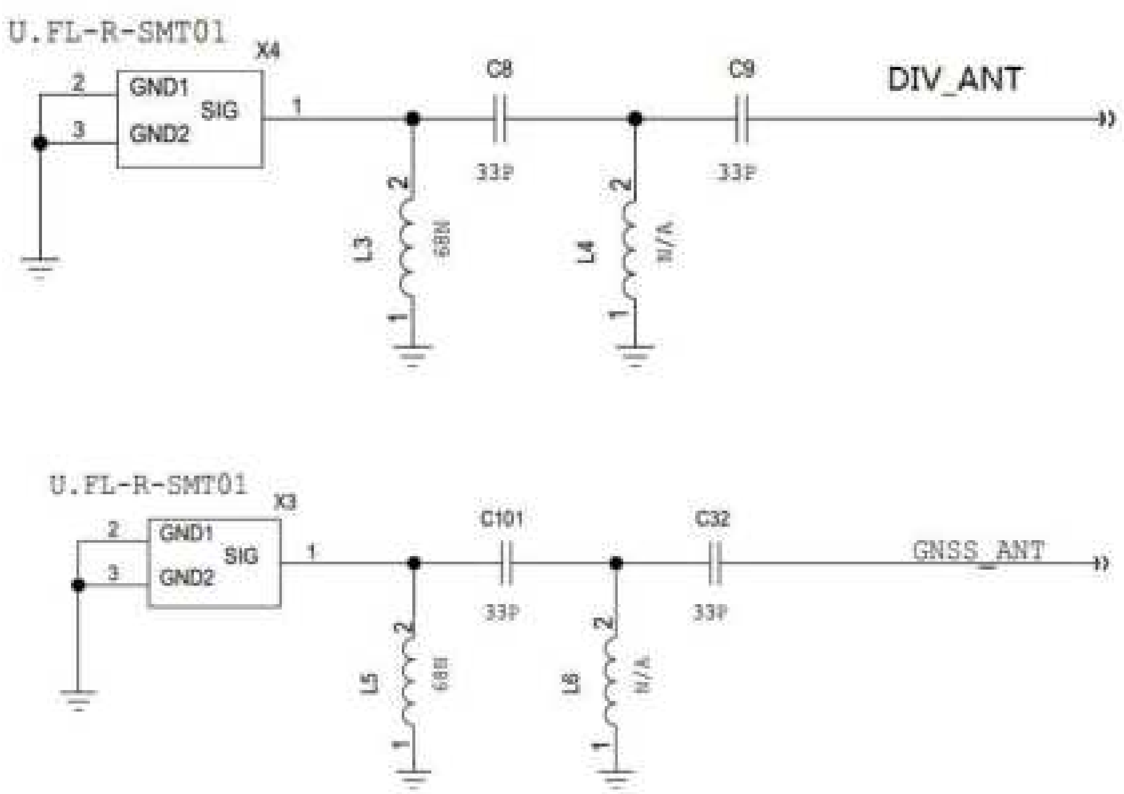


Figure 3–1Reference Circuit of Antenna Interface

The following picture is the reference of GNSS active antenna, VDD is its power, power supply should be designed by actual requirements.

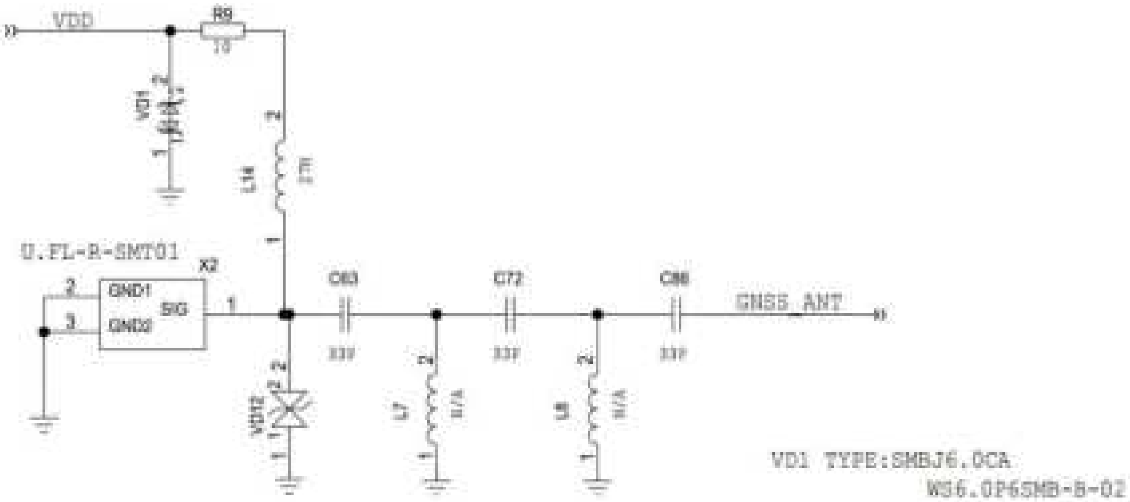


Figure 3–2Reference Circuit of GNSS Antenna

NOTE:

Keep a proper distance between main and diversity antenna to improve the receiving sensitivity.

3.3. Reference PCB Layout of Antenna

Please follow the following criterion in the process of antenna line PCB layout design:

Make sure that the transmission line’s characteristic impedance is 50ohm;

Keep line on the PCB as short as possible, since the antenna line loss shall be less than 0.3 dB;

Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves;

It is wise to surround the PCB transmission line with ground, avoid having other signal tracks facing directly the antenna line track.

Keep at least one layer of the PCB used only for the ground plane; and use this layer as reference ground plane for the transmission line;

- The ground surrounding the antenna line on PCB has to be strictly connected to the main Ground Plane by means of via holes (once per 2mm at least), placed close to the ground edges facing line track;
- Place EMI noisy devices as far as possible from modules antenna line;
- Keep the antenna line far away from the module power supply lines;

3.4. Suggestions for EMC & ESD Design

3.4.1. EMC Design Requirements

During the design of the whole device, the user needs to fully consider the EMC problem caused by the signal integrity and power integrity.

During the product design, it is better to separate the module from the mainboard PCB, instead of installing the module on the ground of the mainboard. If they cannot be separated, the module should be far from modules and components that might generate EMI, such as chip and memory, power interface, and data cable interface.

Because the mainboard of PAD, CPE, and Internet laptops does not have a shielding cover, as that of mobile terminals, to shield most circuits to avoid overflow of electromagnetic interference, you can spray conductive paint on the surface on non-antenna areas within the structural components above and below the mainboard, and the conductive paint should be connected to the ground on the mainboard by several points to shield electromagnetic interference.

Besides, data cables of the LCD and the camera might introduce interference signals, which affect the receiving performance of the antenna. Thus, it is necessary to wrap conductive cloth around the two data cables and connected them to the ground.

RF cables of the antenna should be far from modules and components that might generate EMI, such as chip and memory, power interface, and data cable interface. The wiring of RF cables should be close to the ground of the mainboard.

During the layout and wiring of peripheral circuits, for the wiring of power and signal cables, keep a distance of 2 times of the line width, so as to effectively reduce the coupling between signals and keep a clean reflux path for the signal.

During the design of peripheral power circuits, the de-coupled capacitor should be placed closed to the module power PIN, the high-frequency high-speed circuit and the sensitive circuit should be placed far away from the border of PCB. They should better be separated during layout, so as to reduce the interference between them and protect the sensitive signal.

For the circuit or device on the side of system board that might interfere with the module, it should be shielded during design.

3.4.2. ESD Design Requirements

Module is embedded on the side of system board, so the user needs to make the ESD protection during design. For the key input/output signal interface, such as the (U)SIM card signal interface, the ESD device should be placed closely for protection. Besides, on the side of main board, the user should reasonably design the structure and PCB layout, guarantee that the metallic shielding shell is fully grounded, so as to leave a smooth discharge channel for ESD.

3.5. Test Methods for Whole-Set Antenna OTA

Figure below is the diagram of OTA test system of CTIA. The system is mainly composed of test chamber, high-precision positioning system and its controller, Windows based PC running test software and RF test instruments with automatic test program. The main RF instruments are integrated RF test equipment, Spectrum Analyzer, Network Analyzer.

The radio equipments, Relay Switch Unit and PC with automatic test software are communicated via GPIB interface.

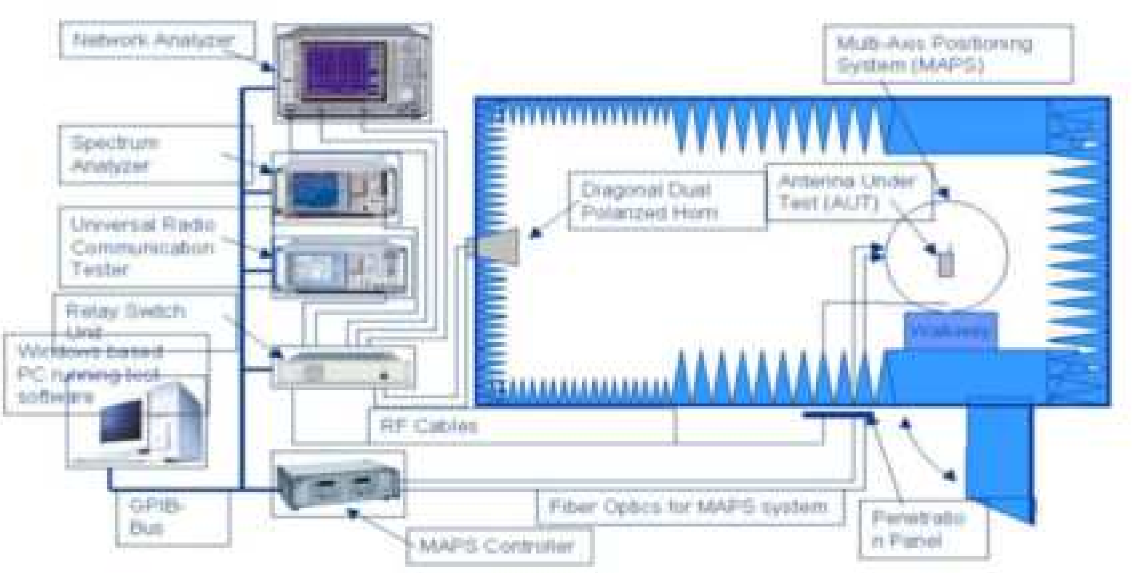


Figure 3–3 The OTA test system of CTIA

4. Electrical, Reliability and Radio Characteristics

4.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of module are listed in the following table:

Table 4-1Absolute Maximum Ratings

Parameter	**Min**	**Max**	**Unit**
VBAT	3.4	4.2	V
Peak current of VBAT	0	2	A
Voltage at digital pin	-0.3	2.1	V
Voltage at ADC1	0.05	4.15	V
Voltage at ADC2	0.05	4.15	V

4.2. Operating Temperature

The operating temperature is listed in the following table.

Table 4-2 Operating Temperature

Parameter	**Min**	**Typ.**	**Max**	**Unit**
Normal Temperature	-30	25	75	℃
Storage Temperature	-40	/	85	℃
Extreme Operating Temperature	-40°C~ -30°C	/	+75°C~ +85°C	℃

4.3. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatics discharge characteristics.

Table 4-3ESD characteristic

Tested Points	**Contact discharge**	**Air Discharge**	**Unit**
VBAT	± 5	± 10	kV
All antennainterfaces	±4	± 8	kV
Other interfaces	± 0.5	± 1	kV

4.4. GM500-U1G Test

4.4.1. Current Consumption

The values of current consumption in different operating mode are shown below.

Table 4-4 Averaged standby DC power consumption [1]

Parameter	**Condition**	**Typical Value**	**Unit**
OFF state	Power down	TBD	uA
Sleep state	Sleep mode (LTE)	TBD	mA
	Sleep mode (WCDMA)	TBD	mA
	Sleep mode (GSM)	TBD	mA

Table 4-5 Averaged working current [1]

Parameter	**Condition**	**Typical Value**（Bandwidth=10MHz）	**Unit**
LTE	LTE FDD Band 2, Pout=23dBm	575	mA
	LTE FDD Band 4, Pout=23dBm	530	mA
	LTE FDD Band 5 ,Pout=23dBm	610	mA
	LTE FDD Band 12,Pout=23dBm	630	mA
	LTE FDD Band 13,Pout=22dBm	720	mA
	LTE FDD Band 25, Pout=23dBm	650	mA
	LTE FDD Band 26, Pout=23dBm	700	mA
	LTE FDD Band 66, Pout=23dBm	720	mA

Table 4-6 Averaged working current [2]

Parameter	**Condition**	**Typical Value**	**Unit**
WCDMA	Band2, Pout=24dBm	532	mA
	Band4, Pout=24dBm	530	mA
	Band5, Pout=24dBm	526	mA

4.4.2. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity typical value of GM500-U1G module.

Table 4-7 Conducted RF Receiving Sensitivity Typical Value [1]

Band	**5 MHz(dBm)**	**10 MHz(dBm)**	**20 MHz(dBm)**
LTE FDD Band 2	-98 dBm	-95 dBm	-92 dBm
LTE FDD Band 4	-100 dBm	-97 dBm	-94 dBm
LTE FDD Band 5	-98 dBm	-95 dBm	/
LTE FDD Band 12	-97 dBm	-94 dBm	/
LTE FDD Band 13	-97 dBm	-94 dBm	/
LTE FDD Band 25	-97 dBm	-94 dBm	-91 dBm
LTE FDD Band 26	-98 dBm	-95 dBm	/
LTE FDD Band 66	-98 dBm	-95 dBm	/

Table 4-8 Conducted RF Receiving Sensitivity Typical Value [2]

Band	**Sensitivity**
WCDMA Band 2	-104.7 dBm
WCDMA Band 4	-104.7 dBm
WCDMA Band 5	-104.7 dBm

5. Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm.

5.1. Mechanical Dimensions of the Module

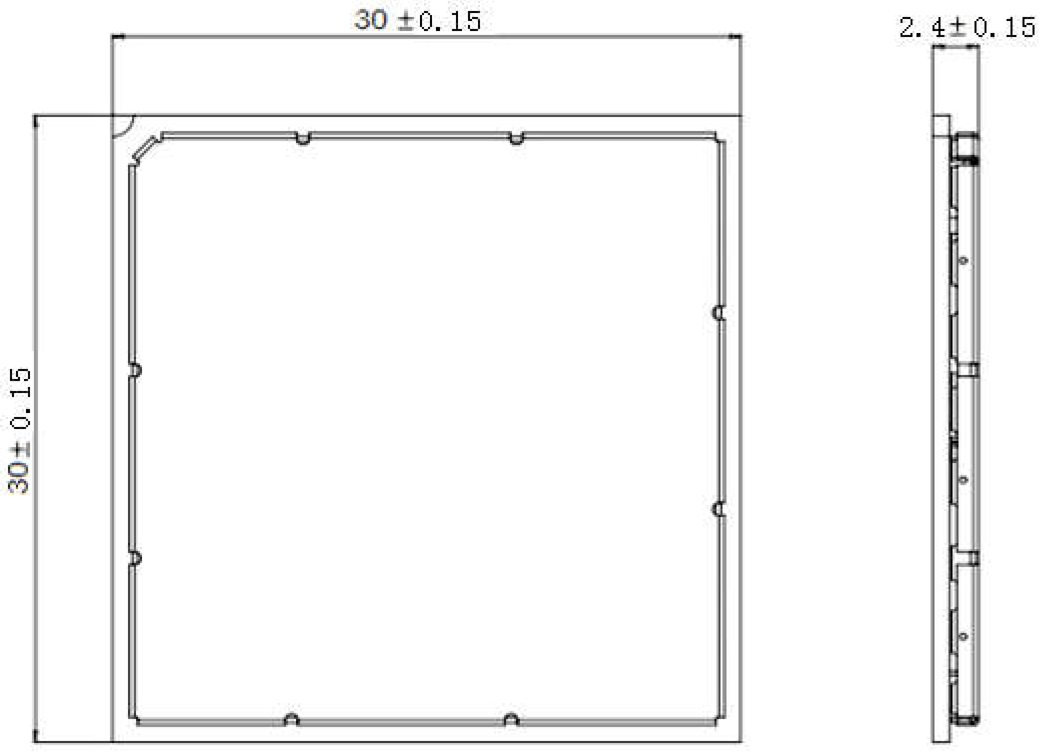


Figure 5–1GM500-U1G Top and Side Dimensions

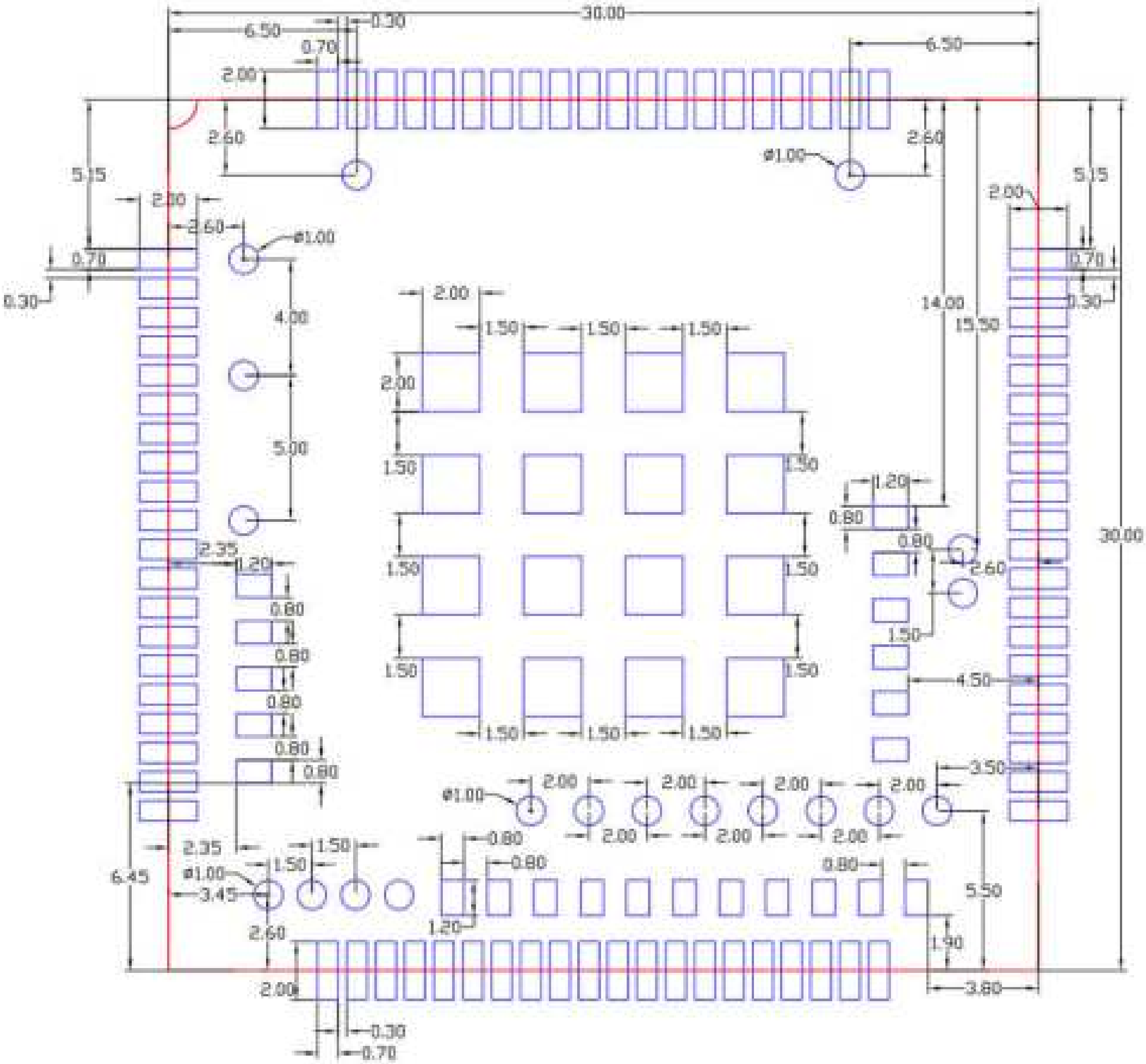


Figure 5–2GM500-U1G Bottom Dimensions (perspectiveview)

Note:

The diameter of test point is 1mm.

5.2. Footprint of Recommendation

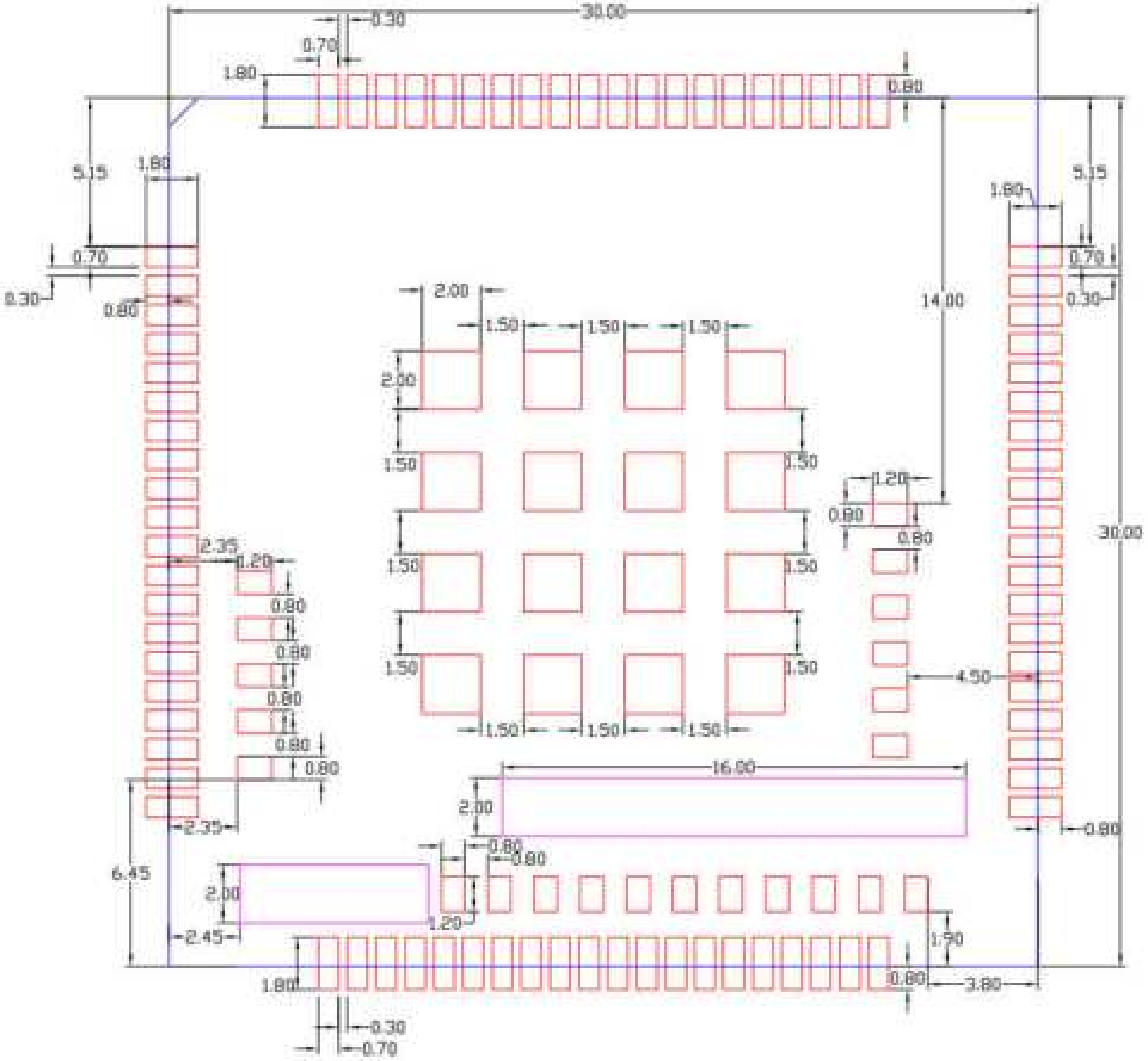


Figure 5–3 Recommended Footprint (perspectiveview)

NOTE:

☑ **Keep out the area below the test point (blue area on the above figure) in the host PCB.**

☑ **In order to maintain the module, keep about 3mm between the module and other components in the host PCB.**

6. Related Test & Test Standard

6.1. Testing Reference

The related tests of MODULE comply with the IEC standard, including the equipment running under high/low temperature, storage under high/low temperature, temperature shock and EMC. Table 6-1 is the list of testing standard, which includes the related testing standards for MODULE.

Table 6-1 Testing Standard

NOTE:

- ☑ **IEC: International Electro technical Commission;**
- ☑ **GB/T: Recommended national standard**

Test Standard	Document Reference
IEC6006826	Environmental testing-Part2.6: Test FC: Sinusoidal Vibration
IEC60068234	Basic environment testing procedures part2.
IEC60068264	Environmental testing-part2-64: Test FH: vibration, broadband random and guidance.
IEC60068214	Environmental testing-part 2-14: Test N: change of temperature
IEC60068229	Basic environmental testing procedures-part2: Test EB and guidance.
IEC6006822	Environmental testing-part2-2: Test B:dry heat
IEC6006821	Environment testing-part2-1: Test A: cold.
GB/T 15844.2	MS telecommunication RF wireless phone-set environment requirement & experimental method – part 4: Strict level of experimental condition
GB/T 2423.17	Basic environment experiment of electronic products-Experiment Ka: Salt mist experiment method
GB/T 2423.5	Basic environment experiment of electronic products-Part2: Experiment method Try Ea & Introduction: Shock
GB/T 2423.11	Basic environment experiment of electronic products-Part2: Experiment method Try Fd: Broad frequency band random vibration (General requirement)
TIA/EIA 603 3.3.5	TIA Standard-part3-5:Shock Stability

6.2. Description of Testing Environment

The working temperature range of MODULE is divided into the normal working temperature range and the extreme working temperature range. Under the normal working temperature range, the testing result of RF complies with the requirements of 3GPP specifications, and its function is normal. Under the extreme temperature range, the RF index basically complies with the 3GPP specifications, and the quality of data communication is affected to a certain extent, but its normal function is not affected. MODULE has passed the EMC test. Table 6-2 is the requirement for the testing environment, and Table 6-3 lists out the instruments and devices that might be used during the test.

⚠**WARNING:**

Table 6-2 lists the extreme working conditions for the Module. Using the Module beyond these conditions may result in permanent damage to the module.

Table 6-2 Testing Environment

Working Condition	Min Temperature	Max Temperature	Remark

Normal working condition	-30°C	75°C	All the indexes are good.
Extreme working condition	-40~ -30°C	75~85°C	Some indexes become poorer.
Storage	-40°C	85°C	Storage environment of module

Table 6-3 Testing Instrument & Device

Testing Item	**Instrument & Device**
RF test	Comprehensive testing device
	RF cable
	Tower antenna
	Microwave darkroom
High/Low-temperature running & storage test	High/Low-temperature experimental box
Temperature shock test	Temperature shock experimental box
Vibration test	Vibration console

6.3. Reliability Testing Environment

The reliability test includes the vibration test, high/low-temperature running, high/low-temperature storage and temperature shock experiment test. Refer to **Table 6-4** for the specific parameters.

Table 6-4 Reliability Features

Test Item	**Test Condition**	**Test Standard**
Random vibration	Frequency range: 5-20Hz, PSD: 1.0m2/s3 Frequency range: 20-200Hz, -3dB/oct 3 axis, 1 hour for each axis	IEC 68-2-6
Temperature shock	Low temperature: -40°C ± 2°C High temperature: +80°C ± 2°C Temperature changing period: less than 30s Test duration: 2 hours Cycle: 10	IEC 68-2-14 Na
High-temperature running	Normal high temperature: 75 °C Extreme high temperature: 85°C Duration: 24 hours	GOSUNCN standard
Low-temperature running	Normal low temperature: -30°C Extreme low temperature: -40°C Duration: 24 hours	GOSUNCN standard
High temperature & high humidity	Temperature: +60°C Humidity: 95% Duration: 48 hours	GOSUNCN standard
High temperature storage	Temperature: 85°C Duration: 24 hours	IEC 68-2-1 Ab
Low temperature storage	Temperature: -40°CDuration: 24 hours	IEC 68-2-2 Bb

7. SMT Process and Baking Guide

This chapter describes module’s storage, PAD design, SMT process parameters, baking requirements, etc., and it is applicable for the process guide to second-level assembly of LCC encapsulation module.

7.1. Storage Requirements

Storage conditions: temperature<40℃, relative humidity<90% (RH), 12 months weld ability guaranteed under this circumstances of excellent sealing package.

The Moisture sensitivity level for all modules is level 3 (Conforming to IPC/JEDEC J-STD-020). After opening the package, mount within 168 hours under the environment conditions of temperature<30℃, relative humidity<60% (RH). If it doesn’t meet the above requirements, perform the baking process. See the baking parameters in Table below:

Table 7-1Baking parameters

Temperature	Baking conditions	Baking time	Remarks
125± 5℃	Moisture: ≤60%RH	8 hours	The accumulated baking time must be less than 96 hours
45± 5℃	Moisture: ≤5%RH	192 hours	

The product’s transportation, storage and processing must conform to IPC/JEDEC J-STD-033

When in the process of PAD designing of module, refer to IPC-SM-782A and the chapter 6.2 below.

7.2. Module Plainness Standard

Plainness of the module is required to be less than 0.15mm.

Measurement method: put the module on the marble plane, use the feeler gage to measure the gap width at the position of maximum warp, and do not exert force on the module during the measurement.

7.3. Process Routing Selection

The modules are manufactured with the lead-free process and meet the ROHS requirements, therefore it’s recommended to follow the lead-free manufacturing process upon the selection of process routing for module board and main board.

7.3.1. Solder Paste Selection

The solder pastes with metal particle TYPE3 and TYPE4 can fulfill the welding requirements. It is accordingly recommended to use the no-clean solder paste. If the solder paste which needs cleaning is used, we cannot guarantee the components on the module board could withstand the washing of the cleaning solvents. This might cause the functional problems of such components and affect the appearance of the module. During the printing process, make sure the solder paste’s thickness at the position of module’s PAD is within 0.18mm~0.20mm.

7.3.2. Design of module PAD’s steel mesh opening on main board

The thickness of the steel mesh on main board is selected according to the encapsulation type of components on the main board. Pay attention to the following requirements:

Make sure to design the module PAD on main board according to chapter 5.

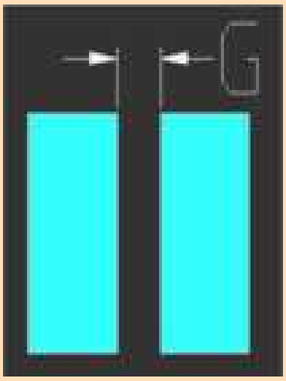
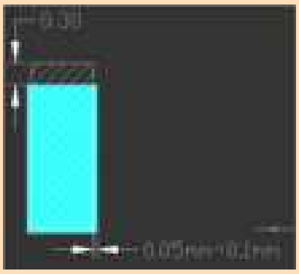
The thickness of steel mesh is 0.15mm or 0.18mm, but the thickness at the position of module pad can be increased to 0.18~0.20mm or the thickness of steel mesh is directly 0.18mm~0.20mm on main board.

Requirements on the thickness of solder paste: control the thickness between 0.18mm and 0.20mm.

See the LCC module PAD’s steel mesh opening in the following table:

Table 7-2LCC module PAD’s steel mesh opening

Module PAD GAP (G)=Center Distance (e) – PAD width (X)	Steel mesh opening

	G≥0.5mm	Drill holes at 100% scale in the direction of width; extend 0.3mm outward in the direction of length	
	G＜0.5mm	Contract 0.05~0.1mm in the direction of width; Contract 0.05~0.1mm inward in the direction of length, extend 0.5mm outward in the direction of length.	

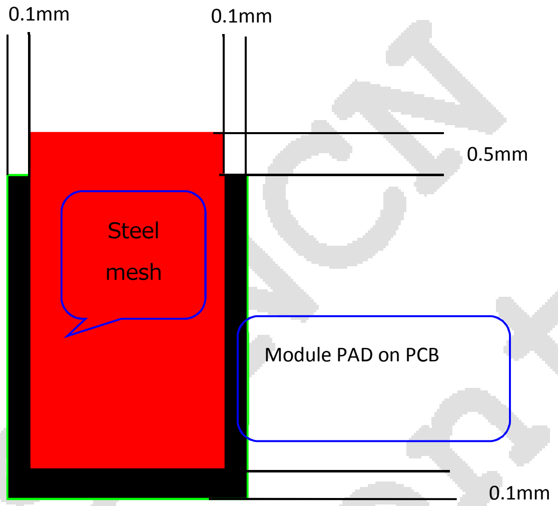


Figure 7–1 Module Board's Steel Mesh Diagram

7.3.3. Module Board's SMT process

1） **SMT Tape Reel:**

The tape reels, which are suitable for SMT, have been made for most GOSUNCN modules. If the module has provided the tape reel itself and meets the SMT requirements, customers can directly use it for module SMT.

Figure 7–2Material Module Pallet

NOTE:

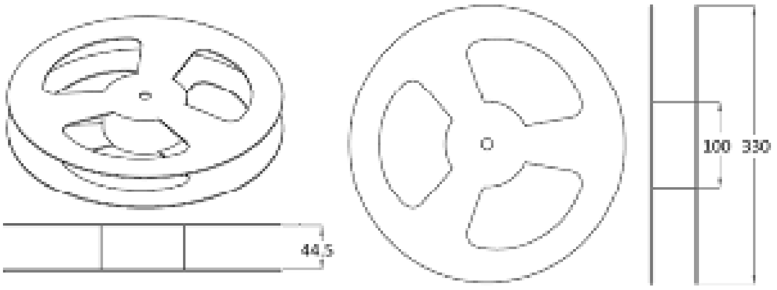
Figure7-2 is just for reference, it doesn't represent the actual Material Module Tape Reel.

Otherwise, customers need make a loading tool similar to the tape reel. Customers can take out the module from the packaging box, put them into the tape according to the sequence and direction, and then start SMT.

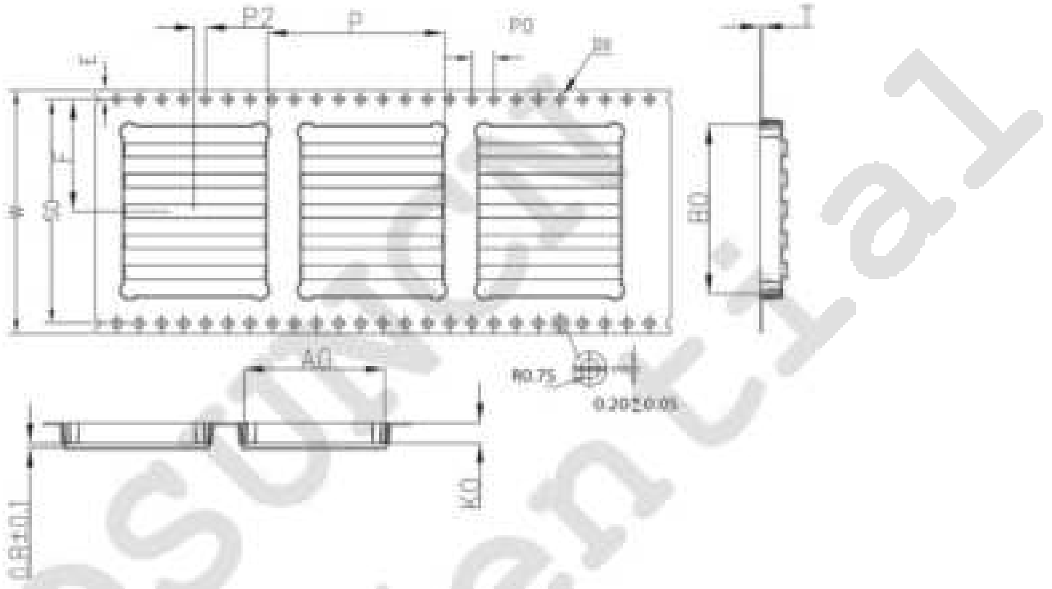
2） **Tape Reel Dimension (unit: mm):**

The following picture is the tape reel specific dimension for your reference:

A: Whole dimension:



B: Detailed dimension:



ITEM	W	A0	B0	K0	K1	P	F	E	S0	D0	D1	P0	P2	T
DIM	44.00 [illegible]	25.50 [illegible]	30.50 [illegible]	3.80 [illegible]	0.00 [illegible]	32.00 [illegible]	20.20 [illegible]	1.75 [illegible]	40.40 [illegible]	1.50 [illegible]	0.00 [illegible]	4.00 [illegible]	2.00 [illegible]	0.35 [illegible]
ALTERNATE														

Figure 7–3 Tape Reel Dimension

3） **Mounting Pressure:**

In order to ensure a good contact between the module and the solder paste on main board, the pressure of placing the module board on main board should be 2-5N according to our experiences. Different modules have different numbers of pads, therefore the pressure selected are different. Customers can select proper pressure based on their own situations to suppress the module paste as little as possible, in order to avoid the surface tension of the solder paste melts too much to drag the module during reflow.

7.3.4. Module Soldering Reflow Curve

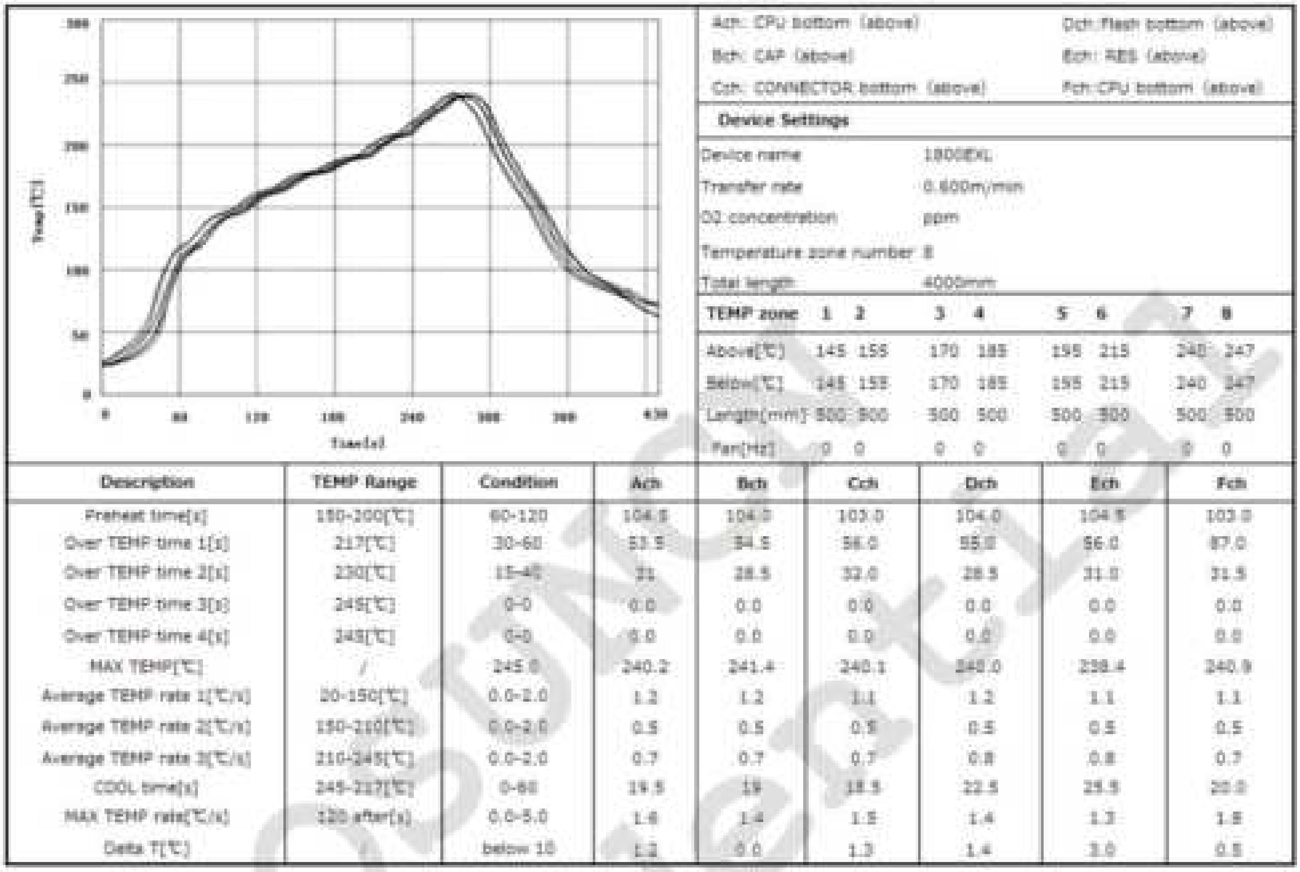
Module soldering furnace temperature curve is:

- Peak value: 245+0/-5℃
- ≥217℃: 30～～60S
- 150～200℃: 60～～120S
- Temperature rise slope: <3℃/S

- Temperature drop rate: －2～－4℃/S

NOTE:

The test board of furnace temperature must be the main board with the module board mounted on, and there must be testing points at the position of module board.



Ach: CPU bottom (above)
Bch: CAP (above)
Cch: CONNECTOR bottom (above)
Dch: Flash bottom (above)
Ech: RES (above)
Fch: CPU bottom (above)

Device Settings

Device name	1800EXL
Transfer rate	0.600m/min
O2 concentration	ppm
Temperature zone number	8
Total length	4000mm

TEMP zone	1	2	3	4	5	6	7	8
Above[℃]	145	155	170	185	195	215	240	247
Below[℃]	145	155	170	185	195	215	240	247
Length[mm]	500	500	500	500	500	500	500	500
Fan[Hz]	0	0	0	0	0	0	0	0

Description	TEMP Range	Condition	Ach	Bch	Cch	Dch	Ech	Fch
Preheat time[s]	150-200[℃]	60-120	104.5	104.0	103.0	104.0	104.5	103.0
Over TEMP time 1[s]	217[℃]	30-60	53.5	34.5	56.0	55.0	56.0	87.0
Over TEMP time 2[s]	230[℃]	15-40	31	28.5	32.0	28.5	31.0	31.5
Over TEMP time 3[s]	245[℃]	0-0	0.0	0.0	0.0	0.0	0.0	0.0
Over TEMP time 4[s]	245[℃]	0-0	0.0	0.0	0.0	0.0	0.0	0.0
MAX TEMP[℃]	/	245.0	240.2	241.4	240.1	240.0	238.4	240.9
Average TEMP rate 1[℃/s]	20-150[℃]	0.0-2.0	1.2	1.2	1.1	1.2	1.1	1.1
Average TEMP rate 2[℃/s]	150-210[℃]	0.0-2.0	0.5	0.5	0.5	0.5	0.5	0.5
Average TEMP rate 3[℃/s]	210-245[℃]	0.0-2.0	0.7	0.7	0.7	0.8	0.8	0.7
COOL time[s]	245-217[℃]	0-60	19.5	19	18.5	22.5	25.5	20.0
MAX TEMP rate[℃/s]	120 after[s]	0.0-5.0	1.6	1.4	1.5	1.4	1.3	1.8
Delta T[℃]	/	below 10	1.2	0.0	1.3	1.4	3.0	0.5

Figure 7–4Module Furnace Temperature Curve Reference Diagram

7.3.5. Reflow method

If the main board used by customers is a double-sided board, it is recommended to mount the module board at the second time. In addition, it is preferable for the main board to reflow on the mesh belt when mounting at the first time and the second time. If such failure is caused by any special reason, the fixture should be also used to make such main board reflow on the track so as to avoid the deformation of PCB during the reflow process.

7.3.6. Maintenance of defects

If poor welding occurs to the module board and main board, e.g., pseudo soldering of the module board and main board, the welder can directly use the soldering iron to repair welding according to the factory's normal welding parameters.

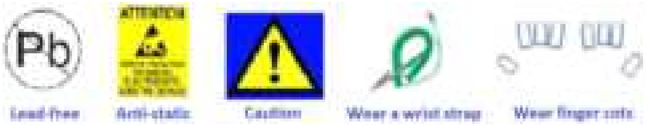
7.4. Module's Baking Requirements

The module must be baked prior to the second reflow.

7.4.1. Module's Baking Environment

The operators must wear dust-free finger cots and anti-static wrist strap under the lead-free and good static-resistant environment. Refer to the following environment requirements:

WARNING:



The product's transportation, storage and processing must conform to IPC/JEDEC J-STD-033.

7.4.2. Baking device and operation procedure

Baking device: Any oven where the temperature can rise up to 125°C or above.

Precautions regarding baking: during the baking process, the modules should be put in the high-temperature resistant pallet flatly and slightly to avoid the collisions and frictions between the modules. During the baking process, do not overlay the modules directly because it might cause damage to the module's chipset.

7.4.3. Module Baking Conditions

See the baking parameters in **Table 7-1.**

8. FEDERAL COMMUNICATION COMMISSION INTERFERENCE STATEMENT

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: 2APNR-GM500U1G1 The FCC ID can be used only when all FCC compliance requirements are met.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and and the maximum antenna gain allowed for use with this device as the bellow.

Band	Antenna Gain (dBi)
LTE FDD Band 2	2 dBi

LTE FDD Band 4	2 dBi
LTE FDD Band 5	2.5 dBi
LTE FDD Band 12	2 dBi
LTE FDD Band 13	3 dBi
LTE FDD Band 25	2.5 dBi
LTE FDD Band 26	2.5 dBi
LTE FDD Band 66	2 dBi
WCDMA Band 2	2 dBi
WCDMA Band 4	2 dBi
WCDMA Band 5	2.5 dBi

2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.