DT450 Mobile Data Radio Board Circuitry

The DT450 Mobile Data Radio works within a frequency range of 400 to 512 MHz.

The following section provides detail views and key areas on the DT450 Mobile Data Radio circuit board especially useful during troubleshooting.

Microcontroller

The microcontroller (U43) is a major component of the radio as it manages the operation of the radio loading the selected transmit/receive frequencies into the injection sythesizer. It also controls the operation of the modem, and determines which receiver provides a better signal from a given transmission. It provides transmit time-out protection in the event a fault causes the radio to halt in the transmit mode. It utilizes a Reduced Instruction Set Computer (RISC) architecture which provides low power operation and a powerful instruction set. Other features include a watchdog timer, serial UART, two 8-bit timers, and 2 kB of electrically erasable programmable read only memory (EEPROM) storage.

The EEPROM RAM stores the setup data entered by the technician even if there is a loss of power.

Support circuitry

The support circuitry consists of the following:

- A Supervisor Control Chip (U4) providing power-on reset.
- The clock controls microcontroller operation and is generated by crystal Y4 and a Pierce oscillator circuit (inside the U43-microcontroller).
- The latch (U40) decodes low order address bits (A0-A7) from the address/data bits (AD0-AD7). It enables Address Latch Enable (ALE) output of U43 and the bits are used by the modem and synthesizer circuitry.
- A 32Kx8 Static RAM Chip (U41) provides temporary storage of the radio's configuration data facilitating the technician with access to make changes.
- Glue logic is also an important part in the microcontroller section. The RAM chip select (CS) and modem chip select (MODEMCS*) command lines are created by U46. These gates decode four (4) high order address bits (A11-A15), plus the read (RD*) and write (WR*) command lines.

Input/Output

Input/output components convert serial and handshake data from the modem section to RS232 levels, and vice-versa. Chip U47 is an RS232 transmitter and receiver. It converts data in 5-volt logic form to data in +/-12-volt form, as required by the RS232 standard. A charge pump power supply on the chip converts the +5-volt DC logic power on pin 16 to the +12-volt and –12-volt levels required utilizing capacitors C199-C202 to generate these voltages.

Injection Synthesizer

The synthesizer chip (U3) is the major contributor of the injection synthesizer. This device contains the key components of a phase locked loop (PLL), including a 1.1 GHz prescaler, programmable divider, and phase detector. The selected frequencies are loaded into U3 as a clocked serial bit stream via the PLL DATA and PLL CLOCK inputs. The microcontroller provides the serial data.

A 10 MHz reference frequency is provided by voltage controlled, temperature compensated crystal oscillator module (VCTCXO)(Y3). This device has an input (REFMOD) that accepts transmit modulation and voltage from a RX FREQ ADJUST pot RV3. The pot allows the receiver to be fine-tuned to the exact operating frequency.

Diode (D1), capacitor (C34), and inverter (U44E) form a lock indication circuit. For troubleshooting, a green light emitting diode (LED) D5 glows and indicates the synthesizer is locked and working properly.

The UHF signal is generated by a wide-range voltage controlled oscillator (VCO) module VCO1. A voltage on the VT input determines the VCO frequency. The voltage is generated by the phase detector output (PDOUT) of U3 driving a loop filter consisting of R4, C33, C23, R3, and C32. It integrates the pulses that normally appear on PDOUT into a smooth DC control signal for the VCO. During transmit, the analog signal from the modem and transmit processing circuitry is applied to VCO1 via the VCOMOD input.

The output of VCO1 RFOUT goes to a two-way power divider (U30). One port of the U30 passes through a 3V attenuator (AT1) and provides the transmit injection (TXINJ) signal for the transmitter circuit while the other port drives another two-way power divider (U31). The first port of U30 provides the receive injection (RXINJ2) signal for Receiver 2, while the second port output is boosted by wide-band amplifier (U32). The amplifier output provides the receive injection (RXINJ1) signal for Receiver 1.

Transmitter

The transmitter section consists of an exciter, power amplifier, and power control circuitry. The exciter is built around an RF power amplifier chip (U28). To transmit, 5-volt power is applied to the 5VKEY line. This causes the U28 to power up and amplify the TXINJ signal. A gain control circuit inside of the U28 maintains the output power level to a constant value throughout the UHF spectrum. Simultaneously, the 12VKEY line is powered up. This causes power amplifier (U1) to boost the RF power to the desired level. Up to 40 watts are available from the transmitter.

The power amplifier modules are self-contained hybrid devices that contain both active and passive circuitry. There are five (5) modules available and each covers a 20-to-30 MHz portion of the UHF band. Should replacement of U1 be required, the exact replacement part must be used.

Receiver 1 Front-End

This section consists of the components that form Receiver 1 Front-End. These components include a T/R switch, bandpass filters, RF amplifiers, and a mixer circuit.

SW1 is a hybrid monolithic device that serves as the T/R switch and protects the Receiver from RF damage by isolating it from the transmitter output. SW1 is normally in the receive position. At the start of a transmission, a control voltage is applied to the TRSWCNTL input and SW1 transfers the antenna to the transmitter power amplifier.

Incoming signals pass through a double-tuned filter (FT4A) that selectively provides a high degree of out-of-band signal rejection. A low noise amplifier (U6A) amplifies the selected signals and a triple-tuned filter (FT3A) provides additional selectivity. An RF amplifier chip (Q6A) further amplifies the signal. The output from Q6A passes through another triple-tuned filter (FT2A) and it goes to the mixer (U29A). U29A is a double-balanced mixer which heterodynes the receive injection (RXINJ1) signal from the synthesizer with the RF amplifier output. The result is a 45 MHz IF signal. Spurious signals are filtered out by FL5A, a 4-pole bandpass filter, and the IF signal goes to the Receiver 1 IF section for further processing.

There are five (5) filter sets (FT2A, FT3A, and FT4A) available, and each one covers a 20-30 MHz portion of the UHF band. Should replacement of the filters be required, exact replacement parts must be used.

Receiver 1 IF

This section consists of Receiver 1 IF subsystem. The major contributor of the IF subsystem is a complete 45 MHz superheterodyne receiver chip that contains an RF amplifier, mixer, local oscillator, 455 KHz IF, quadrature detector, and received signal strength indication (RSSI) detector (U8A).

Incoming 45 MHz signals appearing at ISTIF pass through an amplifier and an LC matching circuit to a mixer. A crystal oscillator is controlled by crystal Y1A and provides the injection frequency for the mixer. This signal drives the oscillator in the Receiver 2 IF subsystem. The mixer output passes through a 455 KHz ceramic filter (FL6A). It is then amplified and passed through another ceramic filter (FL7A) to a second gain stage. The IF output drives a quadrature detector. The recovered audio appears at pin 9 of U8A. The RSSI detector converts the AGC voltage generated inside the chip into a DC level corresponding logarithmically to the signal strength. The Diversity Reception Controller uses RSSI to select the receiver with the best quality signal.

High frequency deemphasis is provided by a filter consisting of a resistor (R416) and a capacitor (C378). The audio is amplified by op amps (U9AC and U9AA) and delivered to the baseband routing circuitry via the BRXMOD1 output. Pot R19A is necessary to adjust the DC levels of U9AC and U9AA output.

Transmit Processing

The analog circuitry in this section modulates the Transmitter. There is also a fine-tuning frequency adjustment for the Receiver.

The data-bearing audio signal from the modem appears at TXMOD. The audio is amplified by op amp (U10A) and the DC output voltage of U10A is simultaneously biased to about half of the supply voltage by the VBIAS input. VBIAS biases the other op amps in the same manner so they operate in a linear region. This is necessary because these op amps operate from a single power supply. The output of U10A passes through a low pass filter (R31) and the signal drives two (2) amplifiers.

The upper amplifier (U39B) has adjustable gain. The output drives op amp (U39A), which inverts the phase of the signal allowing the modulated signal to pass through to the 10 MHz reference oscillator in the synthesizer. Some makes of 10 MHz oscillators do not require the modulation signal to be inverted and a jumper block (JMP1) is provided to accommodate the oscillators. The

lower op amp (U10B) amplifies the signal from the low pass filter and applies it to the VCO via the VCOMOD output.

Baseband Routing

This circuitry selects audio from the appropriate receiver to route to the modem for demodulation.

Power and Ground

Power from the vehicle's battery appears at the VBATT pad. The supply line powers a series of voltage regulators and the transmitter control circuitry, as follows:

- Voltage regulator VR3 provides a continuous 5-volts for the microcontroller, RS232 interface, and modem circuitry. This power supply is always live allowing user-defined parameters to be stored in the radio.
- Voltage regulator VR5 provides switched 8-volt power for most other sections in the radio. VR1 is switched on by the microcontroller.
- Voltage regulator VR6 powers the analog circuitry in the radio.

In the transmit control circuitry, to transmit, the microcontroller makes TXKEYOUT* low. This causes Q5 to conduct, grounding the gate terminal of Q2. This forces the P-channel device to conduct, applying 5-volts via 5VKEY to the transmitter exciter. At the same time Q4 conducts, grounding the gate terminal of Q7. This forces the P-channel device to conduct, applying 12-volts via 12VKEY to the transmitter power amplifier.

Transmitter over-temperature protection is provided by a temperature sensor (U18). When the heatsink becomes too hot, U18 shunts the bias from transistors Q5 and Q4 to ground, turning off Q2 and Q7. This shuts down the transmitter. After the heatsink cools off, the shunt is removed and transmission can resume.

Receiver 2 Front-End

The circuitry for Receiver 2 is identical to Receiver 1 with the exception of the T/R switch and an additional amplifier (U33).

Incoming signals pass through a filter (FT4B). The filter is a double-tuned device that provides a high degree of selectivity. Selected signals are amplified by a low noise amplifier (U6B). A triple-tuned filter (FT3B) provides additional selectivity and the signal is further amplified by an RF amplifier chip (Q6B).

The output from Q6B passes through another triple-tuned filter (FT2B) and it goes to a double-balanced mixer (U29B), which heterodynes the amplified signal from U33. The result is a 45 MHz IF signal. Spurious signals are filtered out by a 4-pole bandpass filter (FL5B). The IF signal goes to Receiver 2 IF for further processing.

There are five (5) filter sets (FT2B, FT3B, and FT4B) available and each one covers a 20-30 MHz portion of the UHF band. Should replacement of the filters be required, exact replacement parts must be used.

Receiver 2 IF

This section is identical to the Receiver 1 IF with the exception of the local oscillator circuitry.

Incoming 45 MHz signals appearing at 2NDIF pass through an amplifier and an LC matching circuit mixer. Local oscillator injection is provided by the Receiver 1 IF subsystem. The mixer output passes through a 455 KHz ceramic filter (FL6B). It is then amplified and passed through another ceramic filter (FL7B) to a second gain stage. The IF output drives a quadrature detector. The recovered audio appears at pin 9 of U8B. The RSSI detector converts if the amplifier current is generated inside the chip into a DC level corresponding logarithmically to the signal strength. RSSI is used by the Diversity Reception Controller to select the Receiver with the better quality signal.

Modem

The IP uses a single-chip modem circuit (U49) that converts parallel data to an analog audio waveform for transmission and analog audio from a receiver to serial data. In addition to the modem functions, U49 provides forward error correction and detection, bit interleaving for more robust data communications, and third generation collision detection and correction capabilities.

The microcontroller section controls the Modem operation. Address bus (A0 and A1), address/data bus (A0-A7), and control lines (RD*, WR*, MODEMCS*) operate the Modem chip. The Modem circuitry requires a crystal-controlled clock, consisting of crystal Y5 and an internal Pierce oscillator.

Incoming audio from the baseband routing circuit appears on the DISCAUD input. The audio signal is demodulated into digital data appearing on the AD0-AD7 lines when the MODEMCS* and RD* lines are low. The data goes to the microcontroller section for further processing, and then to the input/output section for conversion to RS232 signal levels. At this point, the received data is available to the user's MDC and VIU.

During a transmission, outgoing data appearing on the AD0-AD7 lines is converted into a 4-level FSK audio signal by the modem chip. This operation takes place when the MODEMCS* and WR* lines are low. Data from the user's MDC or VIU passes through the input/output section and microcontroller section to the AD0-AD7 bus.

This modem supports 115.2 KBPS (serial port) and 19.2 KBPS or 9600 KBPS (over-the-air) data transmission rates.