

## General Description

The CYBT-243053-02 is a dual-mode Bluetooth® BR/EDR and Low Energy (BLE) wireless module solution. The CYBT-243053-02 includes an onboard crystal oscillator, passive components, and the Cypress CYW20820 silicon device.

The CYBT-243053-02 supports a number of peripheral functions (ADC, PWM), as well as multiple serial communication protocols (UART, SPI, I<sup>2</sup>C, I<sup>2</sup>S/PCM). The CYBT-243053-02 includes a royalty-free stack compatible with Bluetooth 5.0 in a 12.0 × 16.61 × 1.70 mm module form-factor.

The CYBT-243053-02 includes 256 KB of on-chip flash memory and is designed for standalone operation. The CYBT-243053-02 uses an integrated power amplifier to achieve Class I or Class II output power capability.

The CYBT-243053-02 includes an integrated PCB trace antenna, is qualified by Bluetooth SIG, and includes regulatory certification approval for FCC, ISCED, MIC, and CE.

### Module Description

- Module size: 12.00 mm × 16.61 mm × 1.70 mm
- Complies with Bluetooth Core Specification version 5.0 and includes support for BR, EDR 2/3 Mbps, eSCO, BLE, LE 2 Mbps, as well as Bluetooth Mesh.
  - QDID: TBD
  - Declaration ID: TBD
- Certified to FCC, ISCED, MIC, and CE standards
- 256-KB on-chip Flash, 176-KB on-chip RAM
- Industrial temperature range: –30 °C to +85 °C
- Integrated Arm® Cortex®-M4 microprocessor core with floating point unit (FPU)

### RF Characteristics

- Maximum TX output power: +10.5 dBm
- BLE RX Receive Sensitivity: –94.5 dBm

### Power Consumption

- TX current consumption
  - BLE silicon: 22 mA (radio only, 10.5 dBm)
- RX current consumption
  - Bluetooth silicon: 5.9 mA (radio only)
- Cypress CYW20820 silicon low power mode support
  - PDS: 16.5 µA with 176 KB RAM retention
  - ePDS: 8.7 µA
  - HIDEOFF (wake on external or timed interrupt): 1.75 µA

### Functional Capabilities

- Up to 22 GPIOs
- I<sup>2</sup>C, I2S, UART, and PCM interfaces
- Two Quad-SPI interfaces
- Auxiliary ADC with up to 15 analog channels
- Programmable key scan 20 × 8 matrix
- General-purpose timers and six PWMs
- Real-time clock (RTC) and watchdog timers (WDT)
- Bluetooth Basic Rate (BR) and Enhanced Data Rate (EDR) Support
- BLE protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles

### Benefits

CYBT-243053-02 is fully integrated and certified solution that provides all necessary components required to operate Bluetooth communication standards.

- Proven hardware design ready to use
- Ultra-flexible supermux I/O design allows maximum flexibility for GPIO function assignment
- Over-the-air update capable for development or field updates
- Bluetooth SIG qualified.
- ModusToolbox™ provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test your Bluetooth application

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

## References

- Overview: [EZ-BLE/EZ-BT Module Portfolio](#), [Module Roadmap](#)
- Development Kits:
  - CYBT-213043-EVAL, CYBT-243053-02 Evaluation Board
  - [CYW920820EVB-TBD](#), Evaluation Kit for CYW20820 silicon device
- Test and Debug Tools:
  - [CYSmart](#), Bluetooth® LE Test and Debug Tool (Windows)
  - [CYSmart Mobile](#), Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)
- Knowledge Base Article
  - [KBA97095](#) - EZ-BLE™ Module Placement
  - RF Regulatory Certifications for CYBT-213034-02 EZ-BT WICED Modules (TBD)
  - [KBA213976](#) - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - [KBA210802](#) - Queries on BLE Qualification and Declaration Processes
  - [KBA218122](#) - 3D Model Files for EZ-BLE/EZ-BT Modules
  - [KBA223428](#) - Programming an EZ-BT WICED Module
  - [KBA225450](#) - Putting 2073x, 2070x, and 20719 Based Devices or Modules in HCI Mode

## Development Environments

*ModusToolbox Integrated Development Environment (IDE)*

[ModusToolbox](#) simplifies development for IoT designers. It delivers easy-to-use tools and a familiar microcontroller (MCU) integrated development environment (IDE) for Windows®, macOS®, and Linux®. It provides a sophisticated environment for system setup, wireless connectivity libraries, power analysis, application-specific configurators for Bluetooth® Low Energy (BLE), CapSense®, as well as other peripherals.

In addition, code examples, documentation, technical support and community forums are available to help your IoT development process along. These tools and features enable an IoT designer to develop innovative IoT applications efficiently and with ease.

## Technical Support

- [Cypress Community](#): Whether you are a customer, partner, or a developer interested in the latest Cypress innovations, the Cypress Developer Community offers you a place to learn, share, and engage with both Cypress experts and other embedded engineers around the world.
- [Frequently Asked Questions \(FAQs\)](#): Learn more about our Bluetooth ecosystem.
- Visit our [support](#) page and create a [technical support case](#) or contact a [local sales representatives](#). If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

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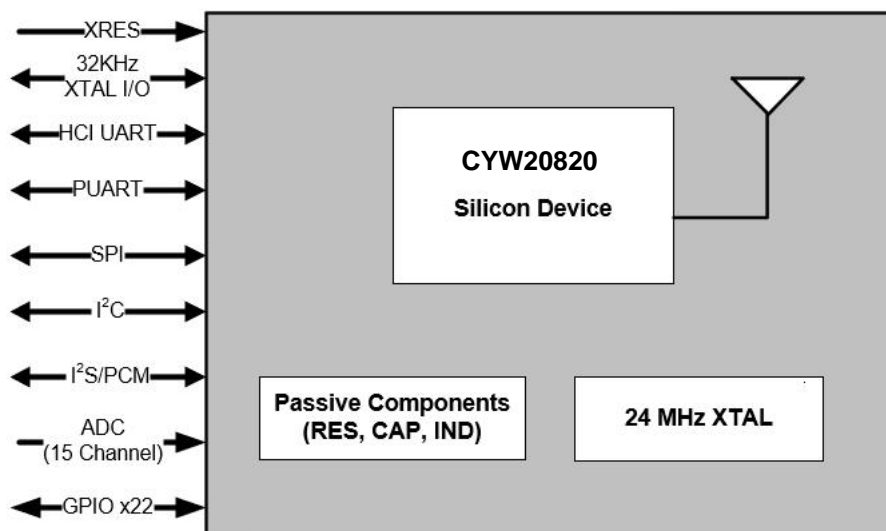
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## Overview

### Functional Block Diagram

Figure 1 illustrates the CYBT-243053-02 functional block diagram.

**Figure 1. Functional Block Diagram**



**Note:** General Purpose Input/Output pins shown in Figure 1 are configurable to any specified input or output function in the SuperMux table detailed in Table 5 in the [Module Connections](#) section.

**Note:** The total number of GPIOs available on the CYBT-243053-02 is 22. Peripheral and/or Serial communication functions are implemented using these 22 GPIOs.

### Module Description

The CYBT-243053-02 module is a complete module designed to be soldered to the applications main board.

#### Module Dimensions and Drawing

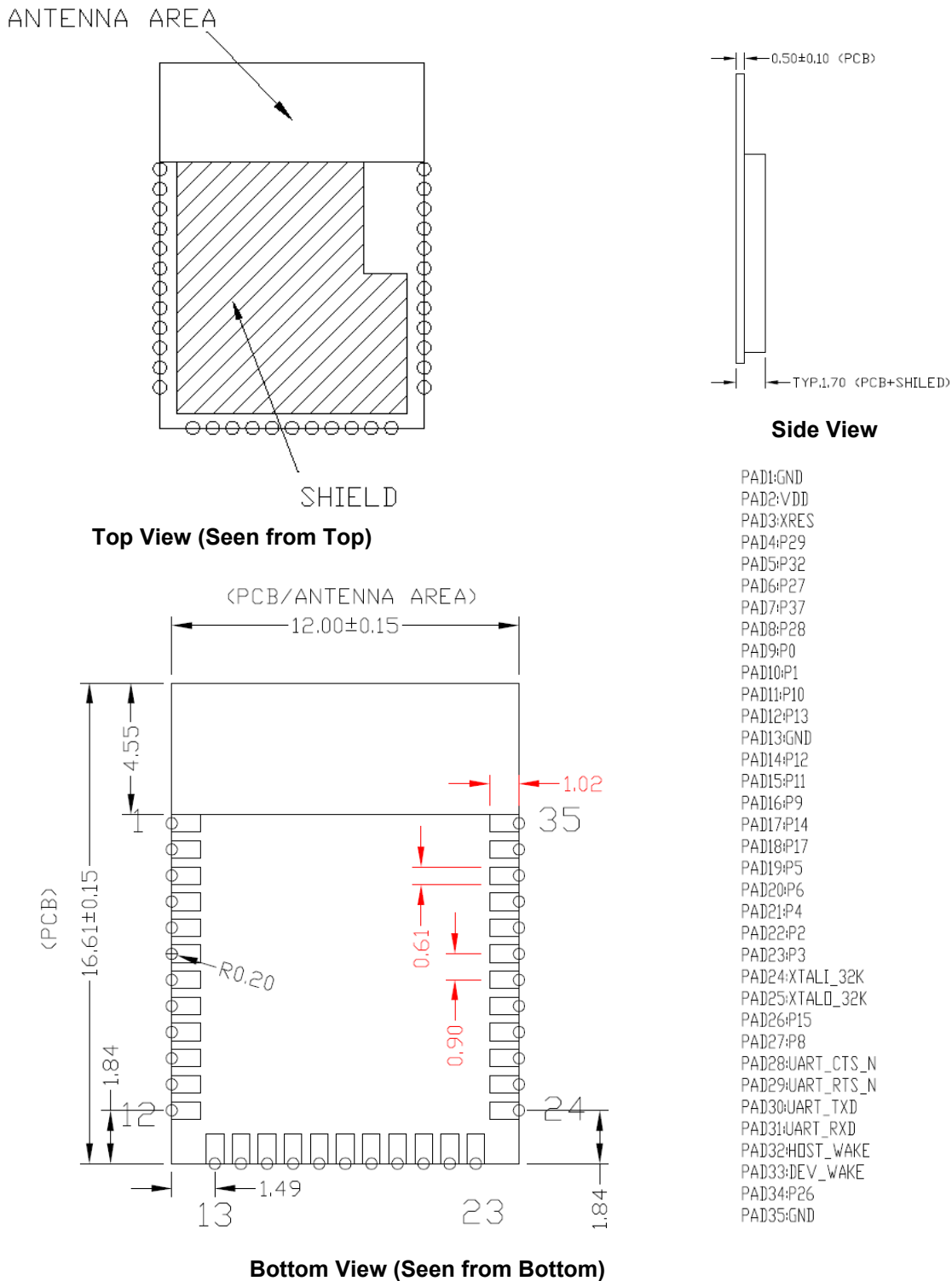
Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. The CYBT-243053-02 will be held within the physical dimensions shown in the mechanical drawings in [Figure 2 on page 5](#). All dimensions are in millimeters (mm).

**Table 1. Module Design Dimensions**

| Dimension Item   |            | Specification   |
|--|------------|-----------------|
| Module dimensions  | Length (X) | 12.00 ± 0.15 mm |
|  | Width (Y)  | 16.61 ± 0.15 mm |
| Antenna location dimensions                                | Length (X) | 12.00 mm        |
|  | Width (Y)  | 4.55 mm         |
| PCB thickness  | Height (H) | 0.50 ± 0.10 mm  |
| Shield height  | Height (H) | 1.20 mm typical |
| Maximum component height                                   | Height (H) | 0.80 mm typical |
| Total module thickness (bottom of module to top of shield) | Height (H) | 1.70 mm typical |

See [Figure 2](#) for the mechanical reference drawing for CYBT-243053-02.

**Figure 2. Module Mechanical Drawing**



**Note**

1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on the recommended host PCB layout, see ["Recommended Host PCB Layout"](#) on page 7.

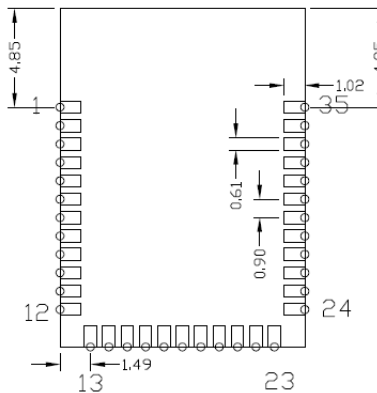
## Pad Connection Interface

As shown in the bottom view of [Figure 2 on page 5](#), the CYBT-243053-02 has 35 connections to a host board via solder pads (SP). [Table 2](#) and [Figure 3](#) detail the solder pad length, width, and pitch dimensions of the CYBT-243053-02 module.

**Table 2. Connection Description**

| Name | Connections | Connection Type | Pad Length Dimension | Pad Width Dimension | Pad Pitch |
|------|-------------|-----------------|----------------------|---------------------|-----------|
| SP   | 35          | Solder Pad      | 1.02 mm              | 0.61 mm             | 0.90 mm   |

**Figure 3. Solder Pad Dimensions (Seen from Bottom)**



**Solder Pad Connections (Seen from Bottom)**

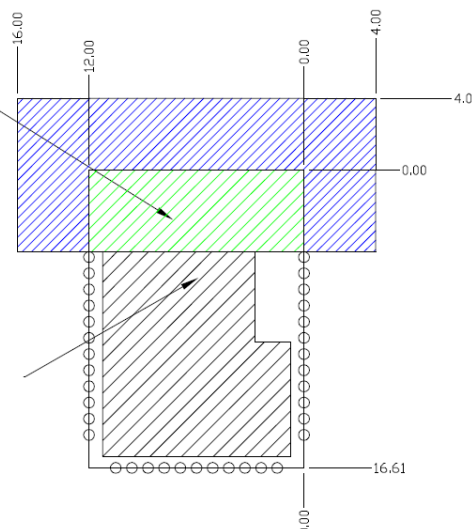
To maximize RF performance, the host layout should follow these recommendations:

1. **Antenna Area Keepout:** The host board directly below the antenna area of the Cypress module (see [Figure 2 on page 5](#)) must contain no ground or signal traces. This keep out area requirement applies to all layers of the host board.
2. **Module Placement:** The ideal placement of the Cypress Bluetooth module is in a corner of the host board with the PCB antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 3 below. Refer to [AN96841](#) for module placement best practices.
3. **Optional Keepout:** To maximize RF performance, the area immediately around the Cypress Bluetooth module PCB antenna may contain an additional keep out area, where there are no grounding or signal traces. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in [Figure 4](#) (dimensions are in mm).

**Figure 4. Optional Additional Host PCB Keep Out Area Around the CYBT-243053-02 PCB Antenna**

1. FOR BEST RF PERFORMANCE, ADDITIONAL KEEPOUT IN BLUE HATCHED AREA ON THE HOST BOARD ON ALL LAYERS.
2. RECOMMENDATION IS TO PLACE THE BLE MODULE IN THE CORNER OF THE HOST BOARD.

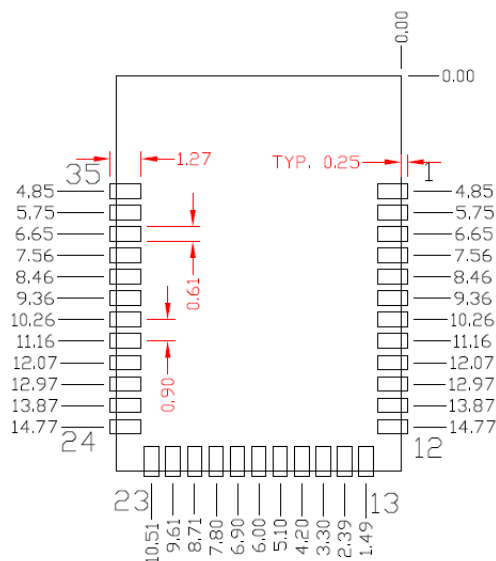
ANTENNA KEEPOUT AREA ONLY BARE PCB/SUBSTRATE



**Optional Host PCB Keep Out Area Around PCB Antenna (Seen from Bottom)**

Figure 5, Figure 6, Figure 7, and Table provide details that can be used for the recommended host PCB layout pattern for the CYBT-243053-02. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.633 mm from center of the pad on either side) shown in Figure 7 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 5, Figure 6, or Figure 7. It is not necessary to use all figures to complete the host PCB layout pattern.

**Figure 6. CYBT-243053-02 Host Layout (Relative to Origin)**



### Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBT-243053-02. All dimensions are referenced to the center of the solder pad. Refer to Figure 7 for the location of each module solder pad.

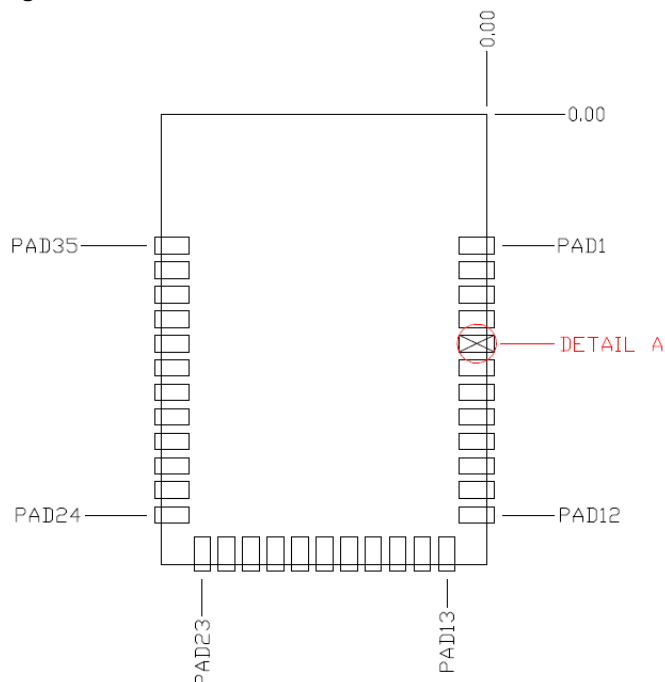
**Table 3. Module Solder Pad Location**

| Solder Pad<br>(Center of Pad) | Location (X,Y) from<br>Origin (mm) | Dimension from<br>Origin (mils) |
|-------------------------------|------------------------------------|---------------------------------|
| 1                             | (0.38, 4.85)                       | (14.96, 190.94)                 |
| 2                             | (0.38, 5.75)                       | (14.96, 226.38)                 |
| 3                             | (0.38, 6.65)                       | (14.96, 261.81)                 |
| 4                             | (0.38, 7.56)                       | (14.96, 297.64)                 |
| 5                             | (0.38, 8.46)                       | (14.96, 333.07)                 |
| 6                             | (0.38, 9.36)                       | (14.96, 368.50)                 |
| 7                             | (0.38, 10.26)                      | (14.96, 403.94)                 |
| 8                             | (0.38, 11.16)                      | (14.96, 439.37)                 |
| 9                             | (0.38, 12.07)                      | (14.96, 475.20)                 |
| 10                            | (0.38, 12.97)                      | (14.96, 510.63)                 |
| 11                            | (0.38, 13.87)                      | (14.96, 546.06)                 |
| 12                            | (0.38, 14.77)                      | (14.96, 581.49)                 |
| 13                            | (1.49, 16.23)                      | (58.66, 638.98)                 |
| 14                            | (2.39, 16.23)                      | (94.09, 638.98)                 |
| 15                            | (3.30, 16.23)                      | (129.92, 638.98)                |
| 16                            | (4.20, 16.23)                      | (165.35, 638.98)                |
| 17                            | (5.10, 16.23)                      | (200.79, 638.98)                |
| 18                            | (6.00, 16.23)                      | (236.22, 638.98)                |
| 19                            | (6.90, 16.23)                      | (271.65, 638.98)                |
| 20                            | (7.80, 16.23)                      | (307.09, 638.98)                |
| 21                            | (8.71, 16.23)                      | (342.91, 638.98)                |
| 22                            | (9.61, 16.23)                      | (378.35, 638.98)                |
| 23                            | (10.51, 16.23)                     | (413.78, 638.98)                |
| 24                            | (11.62, 14.47)                     | (457.48, 581.49)                |
| 25                            | (11.62, 13.87)                     | (457.48, 546.06)                |
| 26                            | (11.62, 12.97)                     | (457.48, 510.63)                |
| 27                            | (11.62, 12.07)                     | (457.48, 475.20)                |
| 28                            | (11.62, 11.16)                     | (457.48, 439.37)                |
| 29                            | (11.62, 10.26)                     | (457.48, 403.94)                |
| 30                            | (11.62, 9.36)                      | (457.48, 368.50)                |
| 31                            | (11.62, 8.46)                      | (457.48, 333.07)                |
| 32                            | (11.62, 7.56)                      | (457.48, 297.64)                |
| 33                            | (11.62, 6.65)                      | (457.48, 261.81)                |

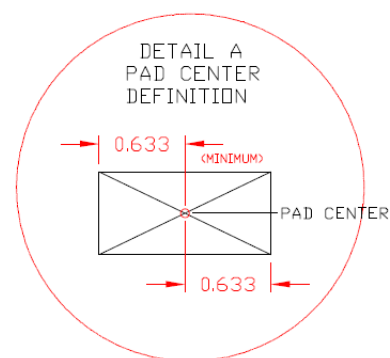
**Table 3. Module Solder Pad Location** (continued)

| Solder Pad<br>(Center of Pad) | Location (X,Y) from<br>Origin (mm) | Dimension from<br>Origin (mils) |
|-------------------------------|------------------------------------|---------------------------------|
| 34                            | (11.62, 5.75)                      | (457.48, 226.38)                |
| 35                            | (11.62, 4.85)                      | (457.48, 190.94)                |

**Figure 7. Solder Pad Reference Location**



**Top View (Seen on Host PCB)**





## Module Connections

Table 4 details the solder pad connection definitions and available functions for each connection pad. The GPIO connections available on the CYBT-243053-02 can be configured to any of the input or output functions listed in Table 5. Table 4 specifies any function that is required to be used on a specific solder pad, and also identifies SuperMux capable GPIOs that can be configured using the ModusToolbox device configurator.

**Table 4. CYBT-243053-02 Solder Pad Connection Definitions**

| Pad | Pad Name   | Silicon Pin Name | XTALI/O  | ADC  | GPIO | SuperMux Capable <sup>[2]</sup> |
|-----|------------|------------------|--|------|------|---------------------------------|
| 1   | GND        | GND              | Ground   |      |      |                                 |
| 2   | VDD        | VDDIO            | Power Supply Input (2.6V ~ 3.63V)  |      |      |                                 |
| 3   | XRES       | RST_N            | External Reset (Active Low)  |      |      |                                 |
| 4   | P29        | P29              | -  | IN10 | ✓    | ✓ see Table                     |
| 5   | P32        | P32              | -  | IN7  | ✓    | ✓ see Table                     |
| 6   | P27        | P27              | -  | -    | ✓    | ✓ see Table                     |
| 7   | P37        | P37              | -  | IN2  | ✓    | ✓ see Table                     |
| 8   | P28        | P28              | -  | IN11 | ✓    | ✓ see Table                     |
| 9   | P0         | P0               | -  | IN29 | ✓    | ✓ see Table                     |
| 10  | P1         | P1               | -  | IN28 | ✓    | ✓ see Table                     |
| 11  | P10        | P10              | -  | IN25 | ✓    | ✓ see Table                     |
| 12  | P13        | P13              | -  | IN22 | ✓    | ✓ see Table                     |
| 13  | GND        | GND              | Ground   |      |      |                                 |
| 14  | P12        | P12              | -  | IN23 | ✓    | ✓ see Table                     |
| 15  | P11        | P11              | -  | IN24 | ✓    | ✓ see Table                     |
| 16  | P9         | P9               | -  | IN26 | ✓    | ✓ see Table                     |
| 17  | P14        | P14              | -  | IN21 | ✓    | ✓ see Table                     |
| 18  | P17        | P17              | -  | IN18 | ✓    | ✓, see Table                    |
| 19  | P5         | P5               | -  | -    | ✓    | ✓ see Table                     |
| 20  | P6         | P6               | -  | -    | ✓    | ✓ see Table                     |
| 21  | P4         | P4               | -  | -    | ✓    | ✓ see Table                     |
| 22  | P2         | P2               | -  | -    | ✓    | ✓ see Table                     |
| 23  | P3         | P3               | -  | -    | ✓    | ✓ see Table                     |
| 24  | XTALI_32K  | XTALI_32K        | External Oscillator Input (32KHz)  | -    | -    | -                               |
| 25  | XTALO_32K  | XTALO_32K        | External Oscillator Output (32KHz)   | -    | -    | -                               |
| 26  | P15        | P15              | -  | IN20 | ✓    | ✓ see Table                     |
| 27  | P8         | P8               | -  | IN27 | ✓    | ✓ see Table                     |
| 28  | UART_CTS_N | UART_CTS_N       | UART (HCI UART) Clear To Send Input Only   |      |      |                                 |
| 29  | UART_RTS_N | UART_RTS_N       | UART (HCI UART) Request To Send Output Only  |      |      |                                 |
| 30  | UART_TXD   | UART_TXD         | UART (HCI UART) Transmit Data Only   |      |      |                                 |
| 31  | UART_RXD   | UART_RXD         | UART (HCI UART) Receive Data Only  |      |      |                                 |
| 32  | HOST_WAKE  | HOST_WAKE        | A signal from the CYBT-243043-02 module to the host indicating that the Bluetooth device requires attention. |      |      |                                 |
| 33  | DEV_WAKE   | DEV_WAKE         | A signal from the host to the CYBT-243043-02 module indicating that the host requires attention.             |      |      |                                 |
| 34  | P26        | P26              | -  | -    | ✓    | ✓ see Table                     |
| 35  | GND        | GND              | Ground   |      |      |                                 |

**Note**

2. The CYBT-243053-02 can configure GPIO connections to any Input/Output function described in Table using the ModusToolbox Device Configurator.

Table 5 details the available Input and Output functions that are configurable to any solder pad in Table that are marked as SuperMux capable.

**Table 5. GPIO SuperMux Input and Output Functions**

| Function             | Input or Output | Function Type                             | GPIOs Required | Function Connection Description |
|----------------------|-----------------|---|----------------|---------------------------------|
| SPI 1                | Input/Output    | Serial Communication<br>(Master or Slave) | 4 ~ 7          | SPI 1 Clock                     |
|                      |                 |   |                | SPI 1 Chip Select               |
|                      |                 |   |                | SPI 1 MOSI                      |
|                      |                 |   |                | SPI 1 MISO                      |
|                      |                 |   |                | SPI 1 I/O 2 (Quad SPI)          |
|                      |                 |   |                | SPI 1 I/O 3 (Quad SPI)          |
|                      |                 |   |                | SPI 1 Interrupt                 |
| SPI 2                | Input/Output    | Serial Communication<br>(Master or Slave) | 4 ~ 7          | SPI 2 Clock                     |
|                      |                 |   |                | SPI 2 Chip Select               |
|                      |                 |   |                | SPI 2 MOSI                      |
|                      |                 |   |                | SPI 2 MISO                      |
|                      |                 |   |                | SPI 2 I/O 2 (Quad SPI)          |
|                      |                 |   |                | SPI 2 I/O 3 (Quad SPI)          |
|                      |                 |   |                | SPI 2 Interrupt                 |
| PUART                | Input           | Serial Communication Input                | 4              | Peripheral UART RX              |
|                      | Output          | Serial Communication Output               |                | Peripheral UART CTS             |
|                      |                 |   |                | Peripheral UART TX              |
|                      |                 |   |                | Peripheral UART RTS             |
| I <sup>2</sup> C     | Input/Output    | Serial Communication<br>(Master or Slave) | 2              | I2C Clock                       |
|                      |                 |   |                | I2C Data                        |
| PCM In               | Input           | Audio Input Communication                 | 3              | PCM Input                       |
|                      |                 |   |                | PCM Clock                       |
|                      |                 |   |                | PCM Sync                        |
| PCM Out              | Output          | Audio Output<br>Communication             | 3              | PCM Output                      |
|                      |                 |   |                | PCM Clock                       |
|                      |                 |   |                | PCM Sync                        |
| I <sup>2</sup> S In  | Input           | Audio Input Communication                 | 3              | I2S DI, Data Input              |
|                      |                 |   |                | I2S WS, Word Select             |
|                      |                 |   |                | I2S Clock                       |
| I <sup>2</sup> S Out | Output          | Audio Output<br>Communication             | 3              | I2S DO, Data Output             |
|                      |                 |   |                | I2S WS, Word Select             |
|                      |                 |   |                | I2S Clock                       |
| PDM                  | Input           | Microphone                                | 1 ~ 2          | PDM Input Channel 1             |
|                      |                 |   |                | PDM Input Channel 2             |
| PWM                  | Output          | Pulse Width Modulator                     | 1 ~ 6          | PWM Channel 0                   |
|                      |                 |   |                | PWM Channel 1                   |
|                      |                 |   |                | PWM Channel 2                   |
|                      |                 |   |                | PWM Channel 3                   |
|                      |                 |   |                | PWM Channel 4                   |
|                      |                 |   |                | PWM Channel 5                   |

## Connections and Optional External Components

### Power Connections (VDD)

The CYBT-243053-02 contains one power supply connection, VDD. VDD accepts a supply input of 2.6 V to 3.63 V. Table 12 provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 12.

### External Reset (XRES)

The CYBT-243053-02 has an integrated power-on reset circuit which completely resets all circuits to a known power-on state. This action can also be invoked by an external reset signal, forcing it into a power-on reset state. XRES is an active-low input signal on the CYBT-243053-02 module (solder pad 3). The CYBT-243053-02 does not require external pull-up resistors on the XRES input. Refer to Figure 10 on page 15 for Power On and XRES operation and timing requirements during power on events.

### HCI UART Connections

The recommendations in this section apply to the HCI UART (Solder Pads 28, 29, 30, and 31). For full UART functionality, all UART signals must be connected to the Host device. If full UART functionality is not being used, and only UART RXD and TXD are desired or capable, then the following connection considerations should be followed for UART RTS and CTS:

- UART RTS: Can be left floating, pulled low, or pulled high. RTS is not critical for initial firmware uploading at power on.
- UART CTS: Must be pulled low to bypass flow control and to ensure that continuous data transfers are made from the host to the module.

### External Component Recommendation

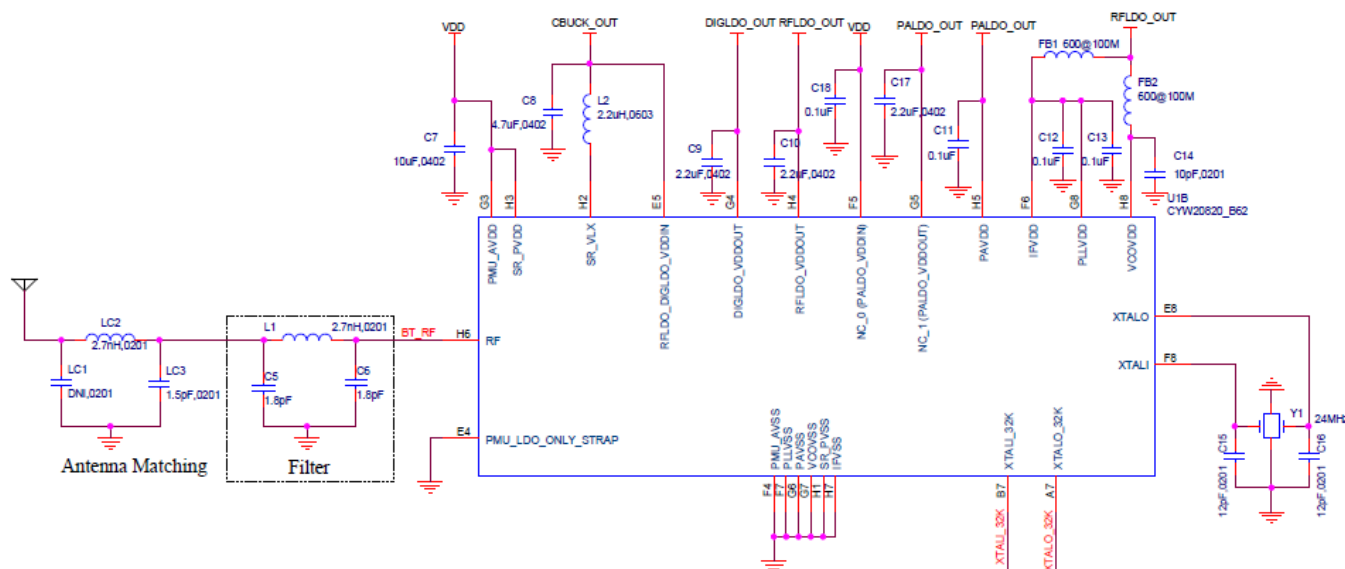
#### Power Supply Circuitry

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included. The ferrite bead should be positioned as close as possible to the module pad connection.

If used, the recommended ferrite bead value is 330  $\Omega$ , 100 MHz. (Murata BLM21PG331SN1D).

Figure 8 illustrates the CYBT-243053-02 schematic.

**Figure 8. CYBT-243053-02 Schematic Diagram**



## Critical Components List

Table 6 details the critical components used in the CYBT-243053-02 module.

**Table 6. Critical Component List**

| Component | Reference Designator | Description                                    |
|-----------|----------------------|--|
| Silicon   | U1                   | 62-pin QFN Bluetooth Silicon Device - CYW20820 |
| Crystal   | Y1                   | 24.000 MHz, 8PF                                |

## Antenna Design

Table 7 details the PCB trace antenna used in the CYBT-243053-02 module.

**Table 7. PCB Antenna Specifications**

| Item            | Description      |
|-----------------|------------------|
| Frequency Range | 2400–2500 MHz    |
| Peak Gain       | –0.5 dBi typical |
| Return Loss     | 10 dB minimum    |

## Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It prioritizes and schedules all RX/TX activities including adv, paging, scanning, and servicing of connections. In addition to these functions, it independently handles the host controller interface (HCI) including all commands, events, and data flowing over HCI. The core also handles symbol timing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), authentication, data encryption/decryption, and data whitening/dewhitening.

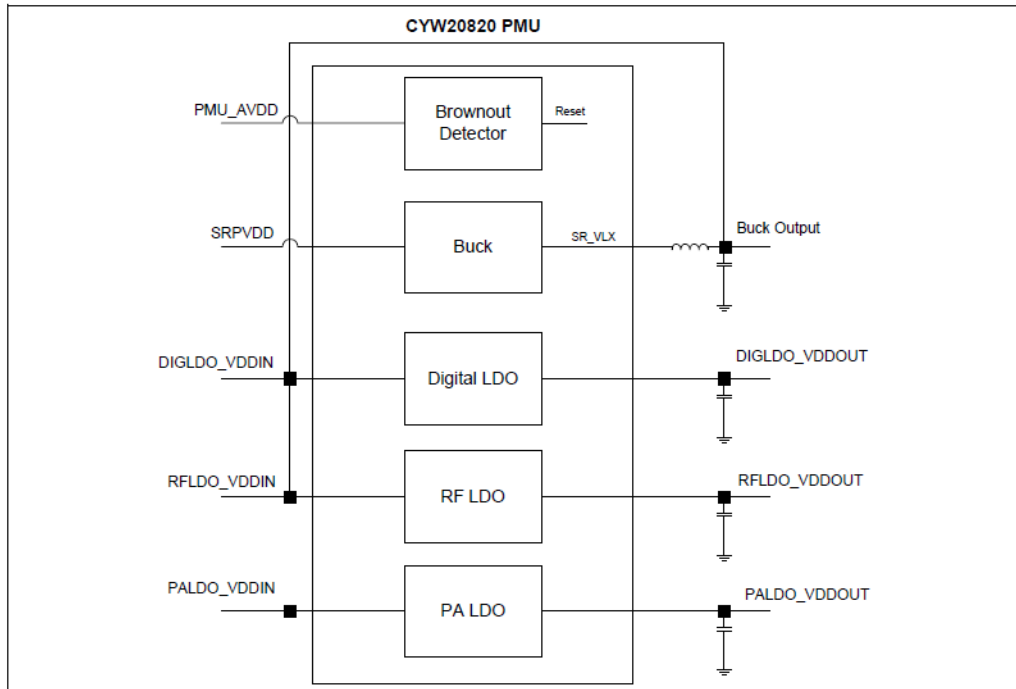
**Table 8. Bluetooth Features**

| Bluetooth 1.0              | Bluetooth 1.2                | Bluetooth 2.0               |
|----------------------------|------------------------------|-----------------------------|
| Basic Rate                 | Interlaced Scans             | EDR 2 Mbps and 3 Mbps       |
| SCO                        | Adaptive Frequency Hopping   | –                           |
| Paging and Inquiry         | eSCO                         | –                           |
| Page and Inquiry Scan      | –                            | –                           |
| Sniff                      | –                            | –                           |
| Bluetooth 2.1              | Bluetooth 3.0                | Bluetooth 4.0               |
| Secure Simple Pairing      | Unicast Connectionless Data  | Bluetooth Low Energy        |
| Enhanced Inquiry Response  | Enhanced Power Control       | –                           |
| Sniff Subrating            | eSCO                         | –                           |
| Bluetooth 4.1              | Bluetooth 4.2                | Bluetooth 5.0               |
| Low Duty Cycle Advertising | Data Packet Length Extension | LE 2 Mbps                   |
| Dual Mode                  | LE Secure Connection         | Slot Availability Mask      |
| LE Link Layer Topology     | Link Layer Privacy           | High Duty Cycle Advertising |

## Power Management Unit

Figure 9 shows the CYW20820 power management unit (PMU) block diagram. The CYW20820 includes an integrated buck regulator, a digital LDO for the digital core, and an RF LDO for the Radio. The PMU also includes a brownout detector which places the part in shutdown when input voltage is below a certain threshold.

**Figure 9. Default Usage Mode**



## **Integrated Radio Transceiver**

The CYBT-243053-02 has an integrated radio transceiver that has been designed to provide low power operation in the globally available 2.4 GHz unlicensed ISM band.

### **Transmitter Path**

CYBT-243053-02 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

#### *Digital Modulator*

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

#### *Power Amplifier*

The CYBT-243053-02 has an integrated power amplifier (PA) that can transmit up to +10.5 dBm for class 1 operation.

### **Receiver Path**

The receiver path uses a low IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYBT-243053-02 to be used in most applications without off-chip filtering.

#### *Digital Demodulator and Bit Synchronizer*

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

#### *Receiver Signal Strength Indicator*

The radio portion of the CYBT-243053-02 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

### **Local Oscillator**

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the band. The CYBT-243053-02 uses an internal loop filter.

## Microcontroller Unit

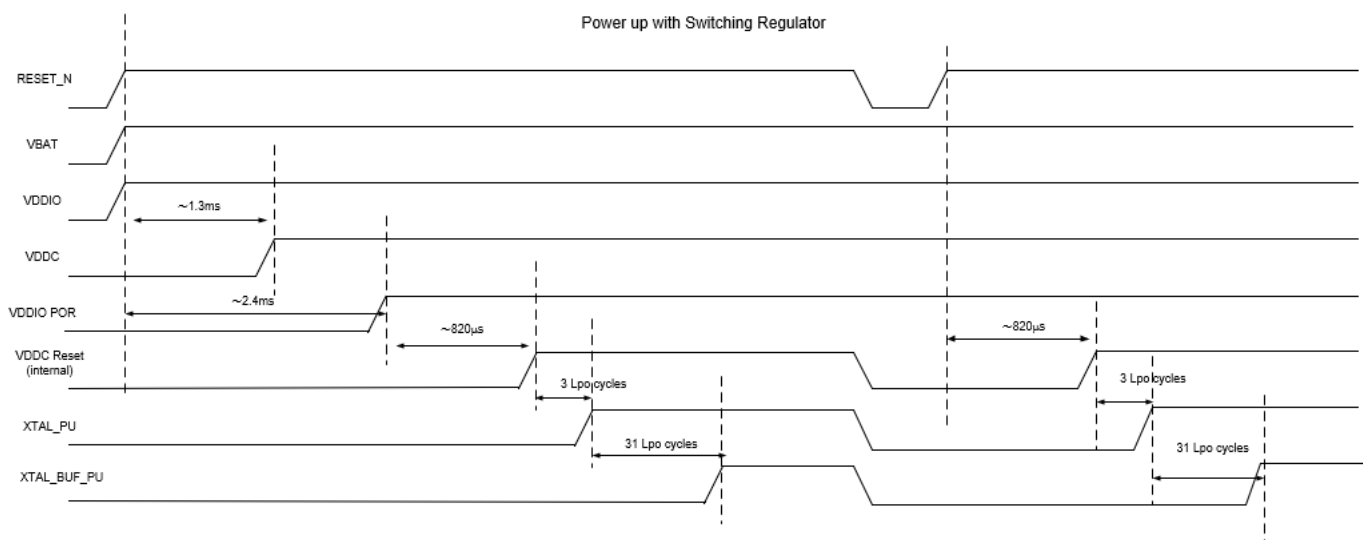
The CYBT-243053-02 includes a Cortex-M4 processor with 1 MB of program ROM, 176 KB of RAM, and 256 KB of flash. The CM4 has a maximum speed of 96 MHz. The 256 KB of flash is supported by an 8 KB cache allowing direct code execution from flash at near maximum speed and low power consumption.

The CM4 runs all the BT layers as well as application code. The ROM includes LMAC, HCI, L2CAP, GATT, as well as other stack layers freeing up most of the flash for application usage. A standard serial wire debug (SWD) interface provides debugging support.

## External Reset

Figure 10 shows power on and reset timing of the CYBT-243053-02. After VBAT is applied and reset is inactive, the internal buck turns on, followed by the RF and Digital LDOs. Once the LDO outputs have stabilized, the PMU allows the digital core to come out of reset. As shown in the figure, external reset can be applied at any time subsequent to power up.

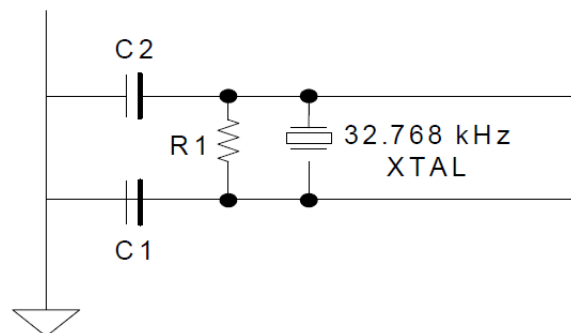
**Figure 10. Reset Timing**



## 32-kHz Crystal Oscillator

The CYBT-243053-02 includes connections for an external 32-kHz oscillator to provide accurate timing during low power operations. Figure 11 shows the 32-kHz XTAL oscillator with external components and Table 9 lists the oscillator characteristics. This oscillator can be operated with a 32 kHz or 32.768-kHz crystal oscillator or be driven with a clock input at similar frequency. The XTAL must have an accuracy of  $\pm 250$  ppm or better per the BT spec over temperature and including aging. The external component values should be:  $R1 = 10\text{ M}\Omega$  and  $C1 = C2 = 6\text{ pF}$ . The values of  $C1$  and  $C2$  are used to fine-tune the oscillator. A XTAL meeting the  $C1$  and  $C2$  values should be used.

**Figure 11. 32 kHz Oscillator Block Diagram**



**Table 9. XTAL Oscillator Characteristics**

| Parameter              | Symbol              | Conditions                 | Min | Typ    | Max | Unit             |
|------------------------|---------------------|----------------------------|-----|--------|-----|------------------|
| Output frequency       | $F_{\text{oscout}}$ | –                          | –   | 32.768 | –   | kHz              |
| Frequency tolerance    | –                   | Over temperature and aging | –   | –      | 250 | ppm              |
| XTAL drive level       | $P_{\text{drv}}$    | For crystal selection      | –   | –      | 0.5 | $\mu\text{W}$    |
| XTAL series resistance | $R_{\text{series}}$ | For crystal selection      | –   | –      | 70  | $\text{k}\Omega$ |
| XTAL shunt capacitance | $C_{\text{shunt}}$  | For crystal selection      | –   | –      | 2.2 | pF               |
| Load capacitance       | $C_l$               | For crystal selection      | –   | 6      | –   | pF               |

## Power Modes

The CYBT-243053-02 support the following HW power modes are supported:

- **Active mode** - Normal operating mode in which all peripherals are available and the CPU is active.
- **Idle mode** - CPU is paused.
- **Sleep mode** - All system clocks are idle except for the LPO. The device can wake up either after a programmed period of time has expired or if an external event is received via one of the GPIOs. In Sleep mode, the CPU is in WFI (wait for interrupt) and the HCLK is not running. The PMU determines if the other clocks can be turned off and does accordingly. The state of the device is retained, the internal LDOs run at a lower voltage (voltage is managed by the PMU), and SRAM is retained.
- **Power Down Sleep (PDS) mode** - Radio powered down and digital core mostly powered down except for RAM, registers, and some core logic. CYBT-243053-02 can wake up either after a programmed period of time has expired or if an external event is received via one of the GPIO.
- **Extended PDS (ePDS)** - This is an extension of PDS Mode. In this mode, only the main RAM and ePDS control circuitry retains power. As in other modes, the CYBT-243053-02 can wake up either after a programmed period or upon receiving an external event.
- **HID-OFF (Deep Sleep) mode** - Core, radio, and regulators powered down. Only the GPIO domain is powered. In this mode, the CYBT-243053-02 can be woken up either by an external event on one of the GPIOs or after a programmed period of time has expired. The lowest power option for HID-Off mode is to wake by external event, allowing all clocking sources to remain off. If a timed wake HID-Off state is desired, this is accomplished by powering the external or internal LPO. Current consumption will increase slightly in timed wake HID-Off mode to account for the LPO power. After wakeup, the part will go through full FW initialization although it will retain enough information to determine that it came out of HID-Off and the event that caused the wake up.

Transition between power modes is handled by the on-chip firmware with host/application involvement. In general, ePDS is the most power-efficient mode for active use cases. HID-Off is preferable for non-connectable beacon use cases (long advertisement intervals).

## Firmware

The CYBT-243053-02 ROM firmware runs on a real time operating system and handles the programming and configuration of all on-chip hardware functions as well as the BT/LE baseband, LM, HCI, GATT, ATT, L2CAP, and SDP layers. The ROM also includes drivers for on-chip peripherals as well as handling on-chip power management functions including transitions between different power modes. The ROM also supports OTA firmware update.

The CYBT-243053-02 is fully supported by the Cypress ModusToolbox IDE. ModusToolbox releases provide latest ROM patches, drivers, and sample applications allowing customized applications using the CYBT-243053-02 to be built quickly and efficiently.

## Watchdog

CYBT-243053-02 includes an onboard watchdog with a period of approximately 4 seconds. The watchdog generates an interrupt to the Firmware after 2 seconds of inactivity and resets the device after 4 seconds.

## Lockout Functionality

The CYBT-243053-02 powers up with SWD access to flash and RAM is disabled. After reset, FW checks OCF for the presence of a security lockout field. If present, FW leaves SWD Flash and RAM access disabled and also blocks any HCI commands from reading the raw contents of the RAM or Flash. This provides an effective way of protection against tampering, dumping, probing, or reverse engineering of the user application stored in the on-chip flash. The only firmware upgrade path in this scenario is secure over-the-air (OTA) update. The security field can be programmed in the factory after all programming and testing has been done.

## True Random Number Generator

The CYBT-243053-02 includes a hardware TRNG (True Random Number Generator). Applications can access the random number generator via firmware APIs.



## Peripherals and Communication Interfaces

### I<sup>2</sup>C

The CYBT-243053-02 provides a 2-pin I<sup>2</sup>C master/slave interface to communicate with I<sup>2</sup>C compatible peripherals. The following transfer clock rates are supported:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I<sup>2</sup>C-compatible speed)
- 1 MHz (Compatibility with high-speed I<sup>2</sup>C-compatible devices is not guaranteed)

The I<sup>2</sup>C compatible master is capable for doing read, write, write followed by read, and read followed by write operations where read/write can be up to 64 bytes.

SCL and SDA lines can be routed to any of the configurable GPIOs (as indicated in [Table](#) ), allowing for flexible system configuration. When used as SCL/SDA the GPIOs go into open drain mode and require an external pull-up for proper operation. I<sup>2</sup>C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

### HCI UART Interface

CYBT-243053-02 includes a UART interface for factory programming as well as when operating as a BT HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 3 Mbps. Typical rates are 115200, 921600, 1500000, and 3,000,000 bps although intermediate speeds are also available. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command. The CYBT-243053-02 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 5\%$ . The UART interface CYBT-243053-02 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

During HCI Mode, the DEV\_WAKE signal can be programmed to wake up the CYBT-243053-02 or allow the CYBT-243053-02 to sleep when radio activities permit. The CYBT-243053-02 can also wake up the host as needed or allow the host to sleep via the HOST\_WAKE signal. Combined, the two signals allow the host and the CYBT-243053-02 to optimize system power consumption by allowing independent control of low power modes. DEV\_WAKE and HOST\_WAKE signals can be enabled via a vendor-specific command.

The FW UART driver allows applications to select different baud rates.

### Peripheral UART Interface

The CYBT-243053-02 has a second UART that may be used to interface to peripherals. Functionally, the peripheral UART is the same as the HCI UART except for 256-byte TX/RX FIFOs. The peripheral UART is accessed through the I/O ports, which can be configured individually and separately for each functional pin. The CYBT-243053-02 can map the peripheral UART to any GPIO.

### Serial Peripheral Interface

The CYBT-243053-02 has two independent SPI interfaces. Both interfaces support single, dual, and Quad Mode SPI operations. Either interface can be a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYBT-243053-02 has optional I/O ports that can be configured individually and separately for each functional pin.

SPI IO voltage depends on VDDO.

### Keyboard Scanner

The CYBT-243053-02 includes a HW key scanner that supports a maximum matrix size of  $20 \times 8$ . The scanner has eight inputs (also referred to as rows) and 20 outputs (also referred to as columns). Keys are detected by driving the columns down sequentially and sampling the rows. The HW scanner includes support for ghost key detection and debouncing. The scanner can also operate in Sleep and PDS modes allowing low power operation while continuing to detect/store all key strokes, up or down. In other low power modes, the scanner can continue to monitor the matrix and initiate exit to Active Mode upon detecting a change of state.

The application can access the key scanner via the associated firmware driver. Refer to the [Firmware](#) section for more details.

### Mouse Quadrature Signal Decoder

The CYBT-243053-02 includes one double-axis and one single axis quadrature decoders. There are two input lines for each axis and a programmable control signal that can be active high or low.

The application can access the quadrature interface via the driver included in the firmware.

## ADC Port

The CYBT-243053-02 includes a  $\Sigma$ - $\Delta$  ADC designed for audio and DC measurements. The ADC can measure the voltage on 15 GPIOs (P0, P1, P8-P15, P17, P28, P29, P32, P37). When used for analog inputs, the GPIOs must be placed in digital input disable mode to disconnect the digital circuit from the pin and avoid leakage. The internal bandgap reference has  $\pm 5\%$  accuracy without calibration. Calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in Direct Current (DC) Mode.

The application can access the ADC through the ADC driver included in the firmware.

The following CYBT-243053-02 module solder pads can be used as ADC inputs:

- Pad 4: P29, ADC Input Channel 10
- Pad 5: P32, ADC Input Channel 7
- Pad 7: P37, ADC Input Channel 2
- Pad 8: P28, ADC Input Channel 11
- Pad 9: P0, ADC Input Channel 29
- Pad 10: P13, ADC Input Channels 28
- Pad 11: P10, ADC Input Channel 25
- Pad 12: P13, ADC Input Channel 22
- Pad 14: P12, ADC Input Channel 23
- Pad 15: P11, ADC Input Channels 24
- Pad 16: P9, ADC Input Channels 26
- Pad 17: P14, ADC Input Channels 21
- Pad 18: P17, ADC Input Channels 18
- Pad 26: P15, ADC Input Channels 20
- Pad 27: P8, ADC Input Channels 27

## GPIO Port

The CYBT-243053-02 has a maximum of 22 GPIOs. All GPIOs support the following:

- Programmable pull-up/down of approximately 45 k $\Omega$ .
- Input disable mode, allowing pins to be left floating or analog signals connected without risk of leakage.
- Source/sink 8 mA at 3.3 V and 4 mA at 1.8 V.
- P26/P27/P28/P29 can sink/source 16 mA at 3.3 V and 8 mA at 1.8 V.

Most peripheral functions can be assigned to any GPIO using the ModusToolbox Device Configurator. For details on the functions that are assignable via the ModusToolbox Device Configurator, refer to [Table](#) .

The following list details the GPIOs that are available on the CYBT-243053-02 module:

- P0-P6, P8-P15, P17, P26-P29, P32, and P37

## PWM

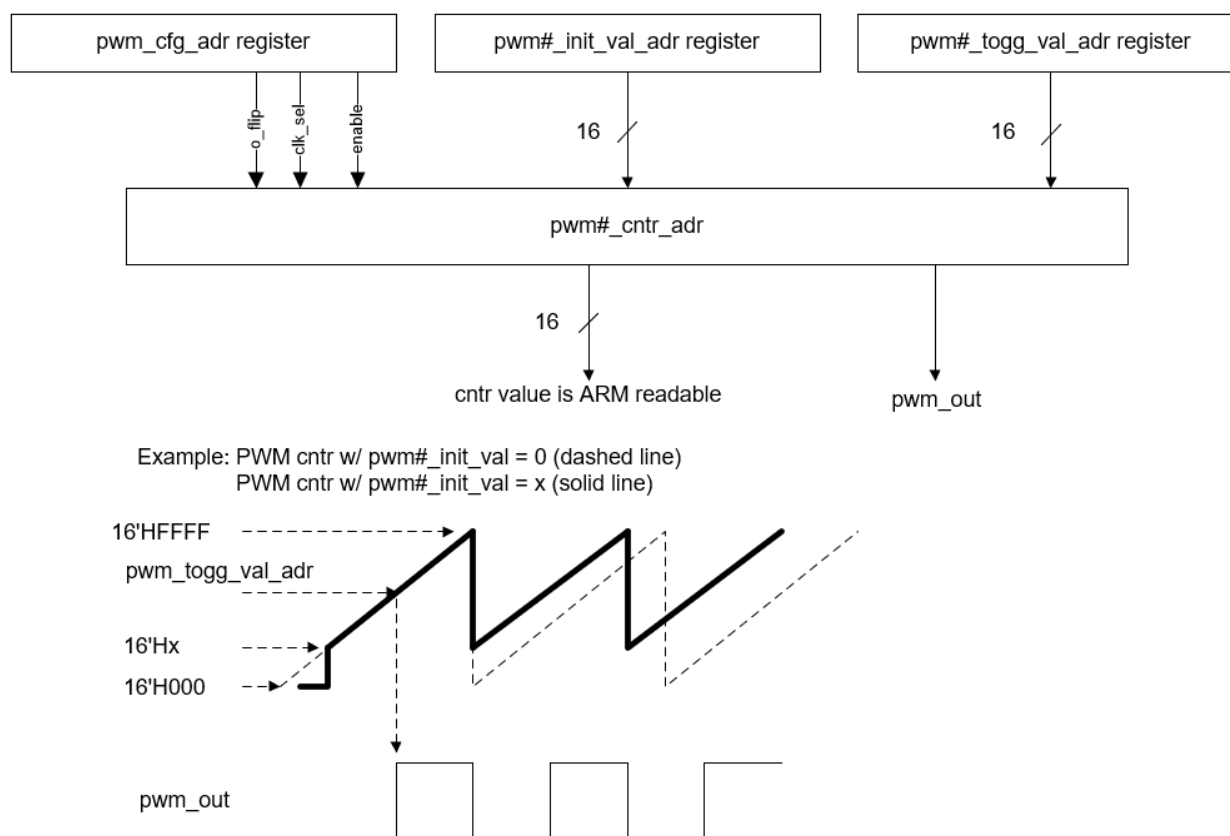
The CYBT-243053-02 has six internal PWMs, labeled PWM0-5. The PWM module consists of the following:

- Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0-5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

The application can access the PWM module through the FW driver.

Figure 12 shows the structure of one PWM channel.

**Figure 12. PWM Block Diagram**



## PDM Microphone

The CYBT-243053-02 accepts a  $\Sigma\Delta$ -based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The PDM input shares the filter path with the auxADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone takes in a 2.4-MHz clock generated by the CYBT-243053-02 and outputs a PDM signal, which is registered by the PDM interface with either the rising or falling edge of the 2.4-MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

## I<sup>2</sup>S Interface

The CYBT-243053-02 supports a single I<sup>2</sup>S digital audio port. with both master and slave modes. The I<sup>2</sup>S signals are:

- I<sup>2</sup>S Clock: I<sup>2</sup>S SCK
- I<sup>2</sup>S Word Select: I<sup>2</sup>S WS
- I<sup>2</sup>S Data Out: I<sup>2</sup>S DO
- I<sup>2</sup>S Data In: I<sup>2</sup>S DI

I<sup>2</sup>S SCK and I<sup>2</sup>S WS become outputs in master mode and inputs in slave mode, while I<sup>2</sup>S DO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSN of the left-channel data is aligned with the MSB of the I<sup>2</sup>S bus, per I<sup>2</sup>S Specifications. The MSB of each data word is transmitted one bit clock cycle after the I<sup>2</sup>S WS transition, synchronous with the falling edge of bit clock. Left Channel data is transmitted when I<sup>2</sup>S WS is low, and right-channel data is transmitted when I<sup>2</sup>S WS is high. Data bits sent by the CYBT-243053-02 are synchronized with the falling edge of I<sup>2</sup>S SCK and should be sampled by the receiver on the rising edge of the I<sup>2</sup>S SCK.

The clock rate in master mode is either one of the following:

- 32 kHz × 32 bits per frame = 1024 kHz
- 32 kHz × 50 bits per frame = 1600 kHz

The master clock is generated from the reference clock using an N/M clock divider. In the slave mode, any clock rate is supported up to a maximum of 3.072 MHz.

**Note:** The PCM interface shares HW with the I<sup>2</sup>S interface and only one can be used at a given time.

## PCM Interface

The CYBT-243053-02 includes a PCM interface that can connect to linear PCM codec devices in master or slave mode. In master mode, the CYBT-243053-02 generates the PCM\_CLK and PCM\_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYBT-243053-02. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

**Note:** The PCM interface shares HW with the I<sup>2</sup>S interface and only one can be used at a given time.

**Note:** Only audio source (other than SCO) use cases are supported on 20819 at this time.

### Slot Mapping

The CYBT-243053-02 supports up to three simultaneous full-duplex channels through the PCM Interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rates is 1, 2, 4, 8, and 16, respectively. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

### Frame Synchronization

The CYBT-243053-02 supports both short- and long-frame synchronization in both master and slave modes. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCGM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

### Data Formatting

The CYBT-243053-02 may be configured to generate and accept several different data formats. For conventional narrow band speech mode, the CYBT-243053-02 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

## Electrical Characteristics

The absolute maximum ratings in the following table indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

**Table 10. Silicon Absolute Maximum Ratings**

| Requirement Parameter        | Specification |     |       | Unit |
|------------------------------|---------------|-----|-------|------|
|                              | Min           | Nom | Max   |      |
| Maximum Junction Temperature | TBD           | TBD | –     | °C   |
| VDDO1/VDDO2                  | –0.5          | –   | 3.795 | V    |
| IFVDD/PLLVDD/VCOVDD/VDDC     | –0.5          | –   | 1.38  | V    |
| PMUAVDD/SR_PVDD              | –0.5          | –   | 3.795 | V    |
| DIGLDO_VDDIN                 | –0.5          | –   | 1.65  | V    |
| RFLDO_VDDIN                  | –0.5          | –   | 1.65  | V    |
| MIC_AVDD                     | –0.5          | –   | 3.795 | V    |
| PALDO_VDDIN                  | –0.5          | –   | 3.79  | V    |
| PAVDD                        | –0.5          | –   | 2.75  | V    |

**Table 11. ESD/Latch-up**

| Requirement Parameter       | Specification |     |      | Unit |
|-----------------------------|---------------|-----|------|------|
|                             | Min           | Nom | Max  |      |
| ESD Tolerance HBM (Silicon) | –2000         | –   | 2000 | V    |
| ESD Tolerance CDM (Silicon) | –500          | –   | 500  | V    |
| Latch-up                    | –             | 200 | –    | mA   |

**Table 12. Power Supply Specifications**

| Parameter  | Conditions                | Min | Typ | Max  | Unit |
|------------|---------------------------|-----|-----|------|------|
| VDD input  | Module Input              | 2.6 | 3.0 | 3.63 | V    |
| VDD Ripple | Module Input Ripple (VDD) | –   | –   | 100  | mV   |

**Table 13. Shutdown Voltage (Brown Out)**

| Parameter         | Specification |      |     | Unit |
|-------------------|---------------|------|-----|------|
|                   | Min           | Typ  | Max |      |
| V <sub>SHUT</sub> | 1.5           | 1.56 | 1.7 | V    |

The CYBT-243053-02 uses an onboard low voltage detector to shut down the device when supply voltage (VBAT) drops below the operating range.

## Current Consumption

Table 14 provides the current consumption measurements taken at the input of LDOIN and VDDIO combined (LDOIN = VDDIO = 3.0 V).

**Table 14. Current Consumption**

| Operational Mode | Conditions               | Typical | Unit |
|------------------|--------------------------|---------|------|
| HCI              | 48 MHz with Pause        | 1.3     | mA   |
|                  | 48 MHz without Pause     | 2.55    | mA   |
| RX               | Continuous RX            | 5.9     | mA   |
| TX               | Continuous TX - 10.5 dBm | 22.0    | mA   |
| PDS              | —                        | 16.5    | μA   |
| ePDS             | All RAM retained         | 8.7     | μA   |
| HID-Off (SDS)    | 32 kHz XTAL on           | 1.75    | μA   |

## Silicon Core Buck Regulator

**Table 15. Core Buck Regulator**

| Parameter                          | Conditions  | Min                | Typ      | Max  | Unit |
|------------------------------------|---|--------------------|----------|------|------|
| Input Supply, VBAT                 | DC Range  | 1.71               | 3.0      | 3.63 | V    |
| Output Current                     | Active Mode   | —                  | < 60     | 100  | mA   |
|                                    | PDS Mode  | —                  | < 60     | 70   |      |
| Output Voltage                     | Active Mode   | 1.1                | 1.26     | 1.4  | V    |
|                                    | PDS Mode, 40 mV min regulation window.  | 0.76               | 0.94 Avg | 1.4  |      |
| Output Voltage Accuracy            | Active Mode, includes line and load regulation.<br>Before trim:                                       | −4                 | —        | +4   | %    |
| Ripple Voltage                     | Active Mode<br>2.2 μH ± 25% inductor, DCR = 114 mΩ ± 20%<br>4.7 μF ± 10% capacitor, Total ESR < 20 mΩ | —                  | 3        | —    | mV   |
|                                    | PDS Mode  | —                  | —        | —    |      |
| Output Inductor, L                 | Refer to the Recommended Component section for more details.  | 1.6 <sup>[3]</sup> | 2.2      | —    | μH   |
| Output Capacitor, C <sub>OUT</sub> |   | 3.0 <sup>[3]</sup> | 4.7      | —    | μF   |
| Input Capacitor, C <sub>IN</sub>   |   | 4.0 <sup>[3]</sup> | 10       | —    |      |
| Input Supply Voltage Ramp Time     | 0 to 3.3 V  | 40                 | —        | —    | μs   |

**Note**

3. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

## Digital LDO

**Table 16. Digital LDO**

| Parameter                        | Conditions  | Min                       | Typ  | Max   | Unit          |
|----------------------------------|---|---------------------------|------|-------|---------------|
| Input Supply, DIGLDO_VDDIN       | Min must be met for correct operation   | $V_{OUT} + 20 \text{ mV}$ | 1.26 | 1.4   | V             |
| Output Voltage, DIGLDO_VDDOUT    | Range   | 0.9                       | 1.2  | 1.275 | V             |
|                                  | Step  | –                         | 25   | –     | mV            |
|                                  | Accuracy after trimming   | –2                        | –    | +2    | %             |
| Dropout Voltage                  | At max load current   | –                         | –    | 20    | mV            |
| Output Current                   | DC Load   | 0.075                     | 40   | 60    | mA            |
| Quiescent Current                | At $T \leq 85^\circ\text{C}$ , $V_{IN} = 1.4 \text{ V}$   | –                         | –    | 40    | $\mu\text{A}$ |
| Output Load Capacitor, $C_{OUT}$ | Total trace + cap ESR must be $< 80 \text{ m}\Omega$  | 1.55 <sup>[4]</sup>       | 2.2  | –     | $\mu\text{F}$ |
| Line Regulation                  | $1.235 \text{ V} \leq V_{IN} \leq 1.4 \text{ V}$  | –                         | 5    | 10    | mV/V          |
| Load Regulation                  | $V_{OUT} = 1.2 \text{ V}$ , $V_{IN} = 1.26 \text{ V}$ , $1 \text{ mA} \leq I_{OUT} \leq 25 \text{ mA}$  | –                         | –    | 0.44  | mV/mA         |
| Load Step Error                  | $I_{OUT}$ step $1 \text{ mA} \leftrightarrow 20 \text{ mA}$ @ $1 \mu\text{s}$ rise/fall, $C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.235 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$ | –24                       | –    | +24   | mV            |
| Leakage Current                  | Power down Mode, $V_{IN} = 1.4 \text{ V}$ , Temp = $25^\circ\text{C}$   | –                         | –    | 50    | nA            |
|                                  | Power down Mode, $V_{IN} = 1.4 \text{ V}$ , Temp = $125^\circ\text{C}$  | –                         | –    | 2     | $\mu\text{A}$ |
| In-rush Current                  | $C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.4 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$  | –                         | –    | 100   | mA            |
| LDO Turn On Time                 | $C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.4 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$ , $I_{OUT} = 20 \text{ mA}$  | –                         | –    | 120   | $\mu\text{s}$ |
| PSRR                             | $C_{OUT} = 2.2 \mu\text{F}$ , $1.235 \text{ V} \leq V_{IN} \leq 1.4 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$ , $I_{OUT} = 20 \text{ mA}$<br>$f = 1 \text{ kHz}$                 | 25                        | –    | –     | dB            |
|                                  | $f = 100 \text{ kHz}$   | 13                        | –    | –     | dB            |

## RF LDO

**Table 17. RF LDO**

| Parameter                        | Conditions  | Min                       | Typ  | Max   | Unit          |
|----------------------------------|---|---------------------------|------|-------|---------------|
| Input Supply, RFLDO_VDDIN        | Min must be met for correct operation   | $V_{OUT} + 20 \text{ mV}$ | 1.26 | 1.4   | V             |
| Output Voltage, RFLDO_VDDOUT     | Range   | 1.1                       | 1.2  | 1.275 | V             |
|                                  | Step  | –                         | 25   | –     | mV            |
|                                  | Accuracy  | –4                        | –    | +4    | %             |
| Dropout Voltage                  | At max load current   | –                         | –    | 20    | mV            |
| Output Current                   | DC Load   | –                         | 20   | 60    | mA            |
| Quiescent Current                | At $T \leq 85^\circ\text{C}$ , $V_{IN} = 1.4 \text{ V}$   | –                         | –    | 50    | $\mu\text{A}$ |
| Output Load Capacitor, $C_{OUT}$ | Total trace + cap ESR must be $< 80 \text{ m}\Omega$  | 1.55 <sup>[4]</sup>       | 2.2  | –     | $\mu\text{F}$ |
| Line Regulation                  | $1.235 \text{ V} \leq V_{IN} \leq 1.4 \text{ V}$  | –                         | –    | 10    | mV/V          |
| Load Regulation                  | $V_{OUT} = 1.2 \text{ V}$ , $V_{IN} = 1.26 \text{ V}$ , $1 \text{ mA} \leq I_{OUT} \leq 25 \text{ mA}$  | –                         | –    | 1     | mV/mA         |
| Load Step Error                  | $I_{OUT}$ step $1 \text{ mA} \leftrightarrow 20 \text{ mA}$ @ $1 \mu\text{s}$ rise/fall, $C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.235 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$ | –24                       | –    | +24   | mV            |
| Leakage Current                  | Power down Mode, $V_{IN} = 1.4 \text{ V}$ , Temp = $25^\circ\text{C}$   | –                         | –    | 50    | nA            |
|                                  | Power down Mode, $V_{IN} = 1.4 \text{ V}$ , Temp = $125^\circ\text{C}$  | –                         | –    | 2     | $\mu\text{A}$ |
| In-rush Current                  | $C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.4 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$  | –                         | –    | 100   | mA            |
| LDO Turn On Time                 | $C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.4 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$ , $I_{OUT} = 20 \text{ mA}$  | –                         | –    | 120   | $\mu\text{s}$ |

**Note**

4. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

**Table 17. RF LDO (continued)**

| Parameter | Conditions  | Min      | Typ | Max | Unit     |
|-----------|---|----------|-----|-----|----------|
| PSRR      | $C_{OUT} = 2.2 \mu F$ , $1.235 V \leq V_{IN} \leq 1.4 V$ , $V_{OUT} = 1.2 V$ ,<br>$I_{OUT} = 20 mA$<br>$f = 1 kHz$<br>$f = 100 kHz$ | 25<br>13 | –   | –   | dB<br>dB |

## Digital I/O Characteristics

**Table 18. Digital I/O Characteristics**

| Characteristics                                      | Symbol   | Min          | Typ | Max | Unit    |
|--|----------|--------------|-----|-----|---------|
| Input low voltage (VDD = 3 V)                        | $V_{IL}$ | –            | –   | 0.8 | V       |
| Input high voltage (VDD = 3 V)                       | $V_{IH}$ | 2.4          | –   | –   | V       |
| Input low voltage (VDD = 1.8 V)                      | $V_{IL}$ | –            | –   | 0.4 | V       |
| Input high voltage (VDD = 1.8 V)                     | $V_{IH}$ | 1.4          | –   | –   | V       |
| Output low voltage                                   | $V_{OL}$ | –            | –   | 0.4 | V       |
| Output high voltage                                  | $V_{OH}$ | VDDO – 0.4 V | –   | –   | V       |
| Input low current                                    | $I_{IL}$ | –            | –   | 1.0 | $\mu A$ |
| Input high current                                   | $I_{IH}$ | –            | –   | 1.0 | $\mu A$ |
| Output low current (VDD = 3 V, $V_{OL} = 0.4 V$ )    | $I_{OL}$ | –            | –   | 4.0 | mA      |
| Output low current (VDD = 3 V, $V_{OL} = 1.8 V$ )    | $I_{OL}$ | –            | –   | 2.0 | mA      |
| Output high current (VDD = 3 V, $V_{OH} = 2.6 V$ )   | $I_{OH}$ | –            | –   | 8.0 | mA      |
| Output high current (VDD = 1.8 V, $V_{OH} = 1.4 V$ ) | $I_{OH}$ | –            | –   | 4.0 | mA      |
| Input capacitance                                    | $C_{IN}$ | –            | –   | 0.4 | pF      |

## ADC Characteristics

**Table 19. Electrical Characteristics**

| Parameter                     | Symbol    | Conditions/Comments  | Min | Typ  | Max | Unit    |
|-------------------------------|-----------|--|-----|------|-----|---------|
| Current consumption           | $I_{TOT}$ | –  | –   | 2    | 3   | mA      |
| Power down current            | –         | At room temperature  | –   | 1    | –   | $\mu A$ |
| <b>ADC Core Specification</b> |           |  |     |      |     |         |
| ADC reference voltage         | VREF      | From BG with $\pm 3\%$ accuracy  | –   | 0.85 | –   | V       |
| ADC sampling clock            | –         | –  | –   | 12   | –   | MHz     |
| Absolute error                | –         | Includes gain error, offset and distortion. Without factory calibration. | –   | –    | 5   | %       |
|                               |           | Includes gain error, offset and distortion. After factory calibration.   | –   | –    | 2   | %       |
| ENOB                          | –         | For audio application  | 12  | 13   | –   | Bit     |
|                               |           | For static measurement   | 10  | –    | –   |         |
| ADC input full scale          | FS        | For audio application  | –   | 1.6  | –   |         |
|                               |           | For static measurement   | 1.8 | –    | 3.6 |         |
| Conversion rate               | –         | For audio application  | 8   | 16   | –   | kHz     |
| Signal bandwidth              | –         | For audio application  | 20  | –    | 8K  | Hz      |
|                               |           | For static measurement   | –   | DC   | –   |         |



**Table 19. Electrical Characteristics** (continued)

| Parameter                            | Symbol          | Conditions/Comments                              | Min | Typ | Max | Unit |
|--------------------------------------|-----------------|--|-----|-----|-----|------|
| Input impedance                      | R <sub>IN</sub> | For audio application                            | 10  | –   | –   | KΩ   |
|                                      |                 | For static measurement                           | 500 | –   | –   |      |
| Startup time                         | –               | For audio application                            | –   | 10  | –   | ms   |
|                                      |                 | For static measurement                           | –   | 20  | –   | μs   |
| MIC PGA Specifications               |                 |  |     |     |     |      |
| MIC PGA gain range                   | –               | –  | 0   | –   | 42  | dB   |
| MIC PGA gain step                    | –               | –  | –   | 1   | –   | dB   |
| PGA input referred noise             | –               | At 42 dB PGA gain A-weighted                     | –   | –   | 4   | μV   |
| MIC Bias Specifications              |                 |  |     |     |     |      |
| MIC bias output voltage              | –               | At 3-V supply, 25 °C, default settings           | –   | 2.4 | –   | V    |
| MIC bias loading current             | –               | –  | –   | –   | 3   | mA   |
| MIC bias noise                       | –               | Refers to PGA input 20 Hz to 8 kHz, A-weighted   | –   | –   | 3   | μV   |
| MIC bias PSRR                        | –               | At 1 kHz   | 40  | –   | –   | dB   |
| ADC SNR                              | –               | A-weighted 0 dB PGA gain, Temperature = 25 °C    | –   | 78  | –   | dB   |
| ADC THD + N                          | –               | –3 dBFS input 0 dB PGA gain, Temperature = 25 °C | –   | 70  | –   | dB   |
| GPIO input voltage                   |                 | Always lower than avddBAT                        | –   | –   | 3.6 | V    |
| GPIO source impedance <sup>[5]</sup> | –               | Resistance                                       | –   | –   | 1   | kΩ   |
|                                      |                 | Capacitance                                      | –   | –   | 10  | pF   |

**Note**

 5. Conditional requirement for the measurement time of 10  $\mu s$ . Relaxed with longer measurement time for each GPIO input channel.

## Chipset RF Specifications

Table 20, Table 21, Table 22, and Table 23 apply to single-ended industrial temperatures. Unused inputs are left open.

**Table 20. BR/EDR - Receiver RF Specifications**

| Parameter  | Mode and Conditions                    | Min  | Typ                | Max   | Unit |
|--|--|------|--------------------|-------|------|
| Receiver Section                                     |  |      |                    |       |      |
| Frequency range                                      | —                                      | 2402 | —                  | 2480  | MHz  |
| RX sensitivity                                       | GFSK, BDR GFSK 0.1% BER, 1 Mbps        | —    | −91 <sup>[6]</sup> | —     | dBm  |
|  | EDR 2M                                 | —    | −93.5              | —     | dB   |
|  | EDR 3M                                 | —    | −87.5              | —     | dB   |
| Maximum input  | —                                      | −20  | —                  | —     | dBm  |
| Interference Performance                             |  |      |                    |       |      |
| C/I cochannel  | GFSK, BDR GFSK 0.1% BER <sup>[7]</sup> | —    | —                  | —     | dB   |
| C/I 1 MHz adjacent channel                           |  | —    | —                  | —     | dB   |
| C/I 2 MHz adjacent channel                           |  | —    | —                  | —     | dB   |
| C/I ≥ 3 MHz adjacent channel                         |  | —    | —                  | —     | dB   |
| C/I image channel                                    |  | —    | —                  | —     | dB   |
| C/I 1 MHz adjacent to image channel                  |  | —    | —                  | —     | dB   |
| Out-of-Band Blocking Performance (CW) <sup>[8]</sup> |  |      |                    |       |      |
| 30 MHz to 2000 MHz                                   | BDR GFSK 0.1% BER                      | —    | −10.0              | —     | dBm  |
| 2000 MHz to 2399 MHz                                 |  | —    | −27                | —     | dBm  |
| 2498 MHz to 3000 MHz                                 |  | —    | −27                | —     | dBm  |
| 3000 MHz to 12.75 GHz                                |  | —    | −10.0              | —     | dBm  |
| Intermodulation Performance <sup>[7]</sup>           |  |      |                    |       |      |
| BT, interferer signal level                          | BR GFSK 0.1% BER                       | —    | —                  | −39.0 | dBm  |
| Spurious Emissions                                   |  |      |                    |       |      |
| 30 MHz to 1 GHz                                      | —                                      | —    | —                  | −57.0 | dBm  |
| 1 GHz to 12.75 GHz                                   | —                                      | —    | —                  | −55.0 | dBm  |

**Table 21. BR/EDR - Transmitter RF Specifications**

| Parameter                       | Min  | Typ  | Max  | Unit |
|---------------------------------|------|------|------|------|
| <b>Transmitter Section</b>      |      |      |      |      |
| Frequency range                 | 2402 | —    | 2480 | MHz  |
| Class 1: BR TX power            | —    | 10.5 | —    | dBm  |
| Class 1: EDR 2M and 3M TX power | —    | 4    | —    | dBm  |

### Notes

6. The receiver sensitivity is measured at BER of 0.1% on the device interface with dirty TX Off.
7. Desired signal is 10 dB above the reference sensitivity level (defined as −70 dBm).
8. Desired signal is 3 dB above the reference sensitivity level (defined as −70 dBm).

**Table 21. BR/EDR - Transmitter RF Specifications (continued)**

| Parameter  | Min | Typ | Max   | Unit           |
|--|-----|-----|-------|----------------|
| 20 dB bandwidth  | –   | 930 | 1000  | kHz            |
| <b>Adjacent Channel Power</b>                            |     |     |       |                |
| $ M - N  = 2$  | –   | –   | –20   | dBm            |
| $ M - N  \geq 3$ [9]                                     | –   | –   | –40   | dBm            |
| <b>Out-of-Band Spurious Emission</b>                     |     |     |       |                |
| 30 MHz to 1 GHz  | –   | –   | –36.0 | dBm            |
| 1 GHz to 12.75 GHz                                       | –   | –   | –30.0 | dBm            |
| 1.8 GHz to 1.9 GHz                                       | –   | –   | –47.0 | dBm            |
| 5.15 GHz to 5.3 GHz                                      | –   | –   | –47.0 | dBm            |
| <b>LO Performance</b>                                    |     |     |       |                |
| Initial carrier frequency tolerance                      | –75 | –   | +75   | kHz            |
| <b>Frequency Drift</b>                                   |     |     |       |                |
| DH1 packet   | –25 | –   | +25   | kHz            |
| DH3 packet   | –40 | –   | +40   | kHz            |
| DH5 packet   | –40 | –   | +40   | kHz            |
| Drift rate   | –20 | –   | 20    | kHz/50 $\mu$ s |
| <b>Frequency Deviation</b>                               |     |     |       |                |
| Average deviation in payload (sequence used is 00001111) | 140 | –   | 175   | kHz            |
| Maximum deviation in payload (sequence used is 10101010) | 115 | –   | –     | kHz            |
| Channel spacing  | –   | 1   | –     | MHz            |

**Table 22. BLE RF Specifications**

| Parameter                              | Conditions                               | Min  | Typ   | Max  | Unit |
|--|--|------|-------|------|------|
| Frequency range                        | N/A                                      | 2402 | –     | 2480 | MHz  |
| RX sensitivity <sup>[10]</sup>         | GFSK, BDR GFSK 0.1% BER 0.1% BER, 1 Mbps | –    | –94.5 | –    | dBm  |
| TX power                               | N/A                                      | –    | 10.5  | –    | dBm  |
| Mod Char: Delta F1 average             | N/A                                      | 225  | 255   | 275  | kHz  |
| Mod Char: Delta F2 max <sup>[11]</sup> | N/A                                      | 99.9 | –     | –    | %    |
| Mod Char: Ratio                        | N/A                                      | 0.8  | –     | –    | %    |

**Table 23. BLE2 RF Specifications**

| Parameter                      | Conditions | Min | Typ   | Max | Unit |
|--------------------------------|------------|-----|-------|-----|------|
| RX sensitivity <sup>[12]</sup> | –          | –   | –89.5 | –   | dBm  |
| TX power                       | –          | –   | 10.5  | –   | dBm  |

**Notes**

9. Meets SIG Specification.

10. Dirty TX is Off.

11. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

12. 255 byte packet.

## Timing and AC Characteristics

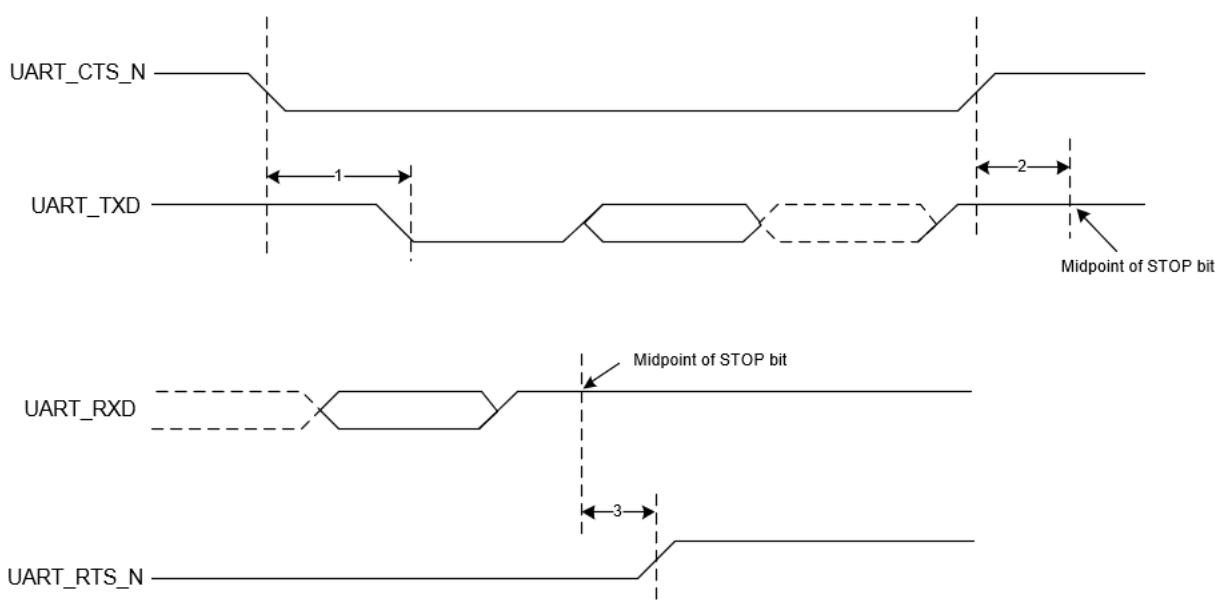
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

### UART Timing

**Table 24. UART Timing Specifications**

| Reference | Characteristics  | Min | Typ | Max  | Unit        |
|-----------|--|-----|-----|------|-------------|
| 1         | Delay time, UART_CTS_N low to UART_TXD valid.            | –   | –   | 1.50 | Bit periods |
| 2         | Setup time, UART_CTS_N high before midpoint of stop bit. | –   | –   | 0.67 | Bit periods |
| 3         | Delay time, midpoint of stop bit to UART_RTS_N high.     | –   | –   | 1.33 | Bit periods |

**Figure 13. UART Timing**



### SPI Timing

The SPI interface can be clocked up to 24 MHz.

Table 25 and Figure 14 show the timing requirements when operating in SPI Mode 0 and 2.

**Table 25. SPI Mode 0 and 2**

| Reference | Characteristics                                     | Min   | Max               | Unit |
|-----------|---|-------|-------------------|------|
| 1         | Time from master assert SPI_CSN to first clock edge | 45    | –                 | ns   |
| 2         | Setup time for MOSI data lines                      | 6     | $\frac{3}{4}$ SCK | ns   |
| 3         | Idle time between subsequent SPI transactions       | 1 SCK | –                 | ns   |

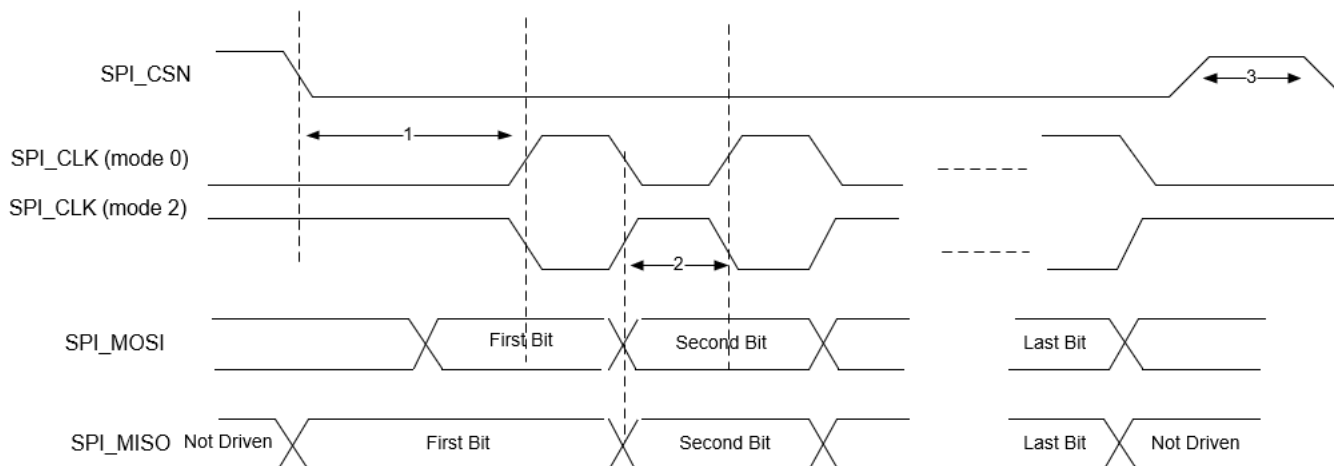
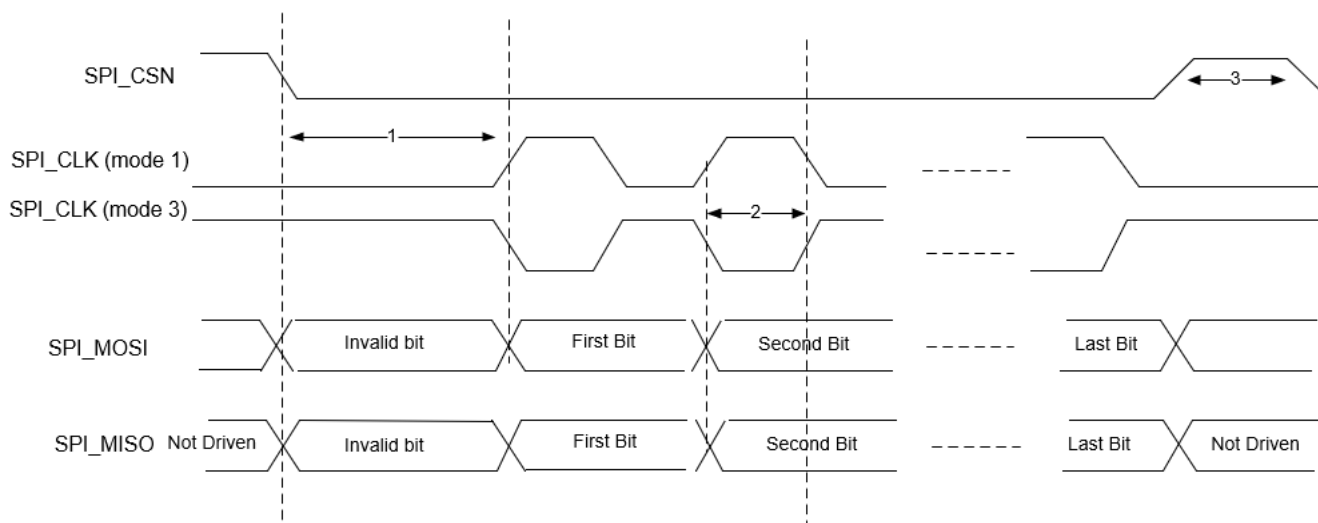
**Figure 14. SPI Timing, Mode 0 and 2**


Table 26 and Figure 15 show the timing requirements when operating in SPI Mode 1 and 3.

**Table 26. SPI Mode 1 and 3**

| Reference | Characteristics                                     | Min   | Max               | Unit |
|-----------|---|-------|-------------------|------|
| 1         | Time from master assert SPI_CSN to first clock edge | 45    | –                 | ns   |
| 2         | Setup time for MOSI data lines                      | 6     | $\frac{3}{4}$ SCK | ns   |
| 3         | Idle time between subsequent SPI transactions       | 1 SCK | –                 | ns   |

**Figure 15. SPI Timing, Mode 1 and 3**


## I<sup>2</sup>C Compatible Interface Timing

The specifications in [Table 26](#) references [Figure](#) .

**Table 27. I<sup>2</sup>C Interface Timing Specifications (up to 1 MHz)**

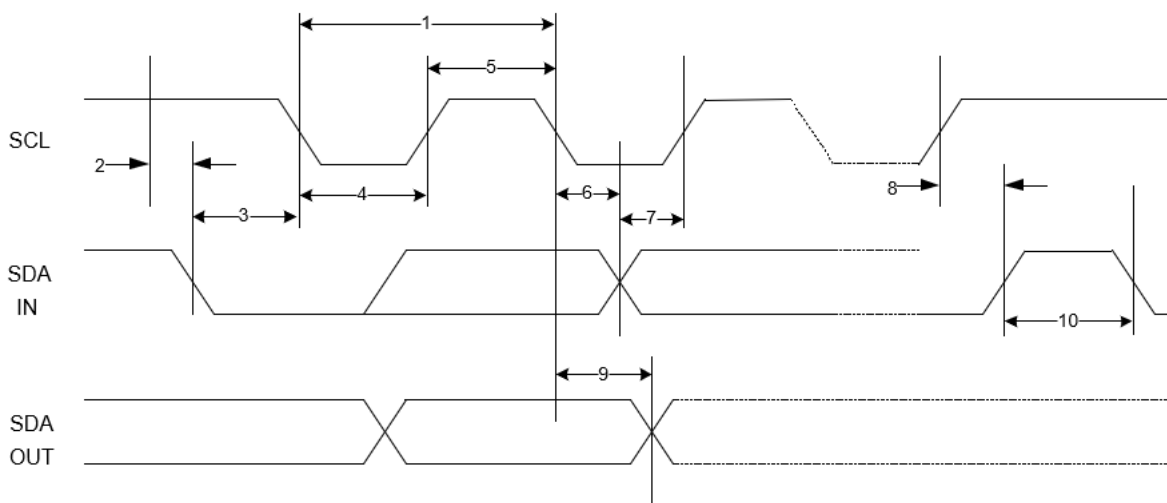
| Reference | Characteristics                      | Min | Max  | Unit |
|-----------|--------------------------------------|-----|------|------|
| 1         | Clock frequency                      | –   | 100  | kHz  |
|           |                                      |     | 400  | kHz  |
|           |                                      |     | 800  | kHz  |
|           |                                      |     | 1000 | kHz  |
| 2         | START condition setup time           | 650 | –    | ns   |
| 3         | START condition hold time            | 280 | –    | ns   |
| 4         | Clock low time                       | 650 | –    | ns   |
| 5         | Clock high time                      | 280 | –    | ns   |
| 6         | Data input hold time <sup>[13]</sup> | 0   | –    | ns   |
| 7         | Data input setup time                | 100 | –    | ns   |
| 8         | STOP condition setup time            | 280 | –    | ns   |
| 9         | Output valid from clock              | –   | 400  | ns   |
| 10        | Bus free time <sup>[14]</sup>        | 650 | –    | ns   |

### Notes

13. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

14. Time that the CBUS must be free before a new transaction can start.

**Figure 16. I<sup>2</sup>C Interface Timing Diagram**



## I<sup>2</sup>S Interface Timing

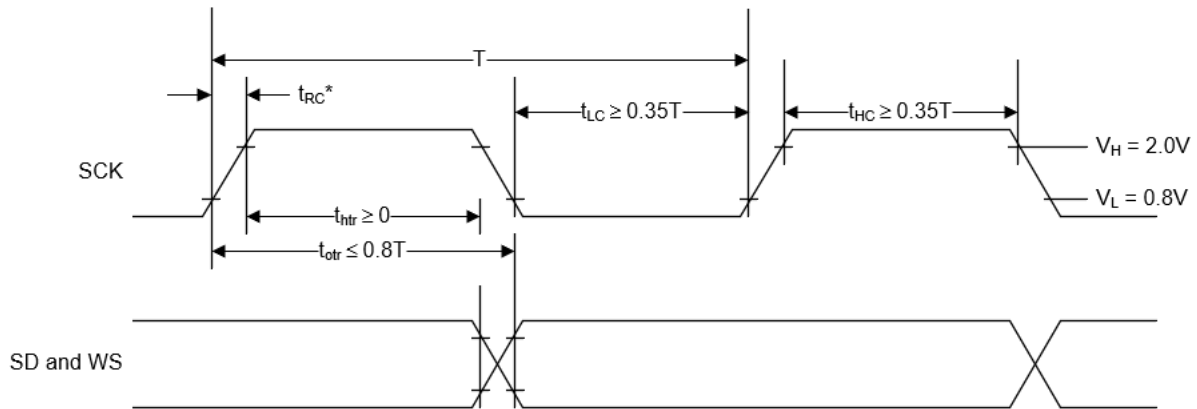
I<sup>2</sup>S timing is shown below in Table 28, Figure 17, and Figure 18.

**Table 28. Timing for I<sup>2</sup>S Transmitters and Receivers**

|   | Transmitter         |                     |                     |      | Receiver            |                     |             |     | Notes |
|---|---------------------|---------------------|---------------------|------|---------------------|---------------------|-------------|-----|-------|
|   | Lower Limit         |                     | Upper Limit         |      | Lower Limit         |                     | Upper Limit |     |       |
|   | Min                 | Max                 | Min                 | Max  | Min                 | Max                 | Min         | Max |       |
| Clock Period T  | T <sub>tr</sub>     | —                   | —                   | —    | T <sub>r</sub>      | —                   | —           | —   | [15]  |
| Master Mode: Clock generated by transmitter or receiver |                     |                     |                     |      |                     |                     |             |     |       |
| HIGH t <sub>HC</sub>                                    | 0.35T <sub>tr</sub> | —                   | —                   | —    | 0.35T <sub>tr</sub> | —                   | —           | —   | [16]  |
| LOWt <sub>LC</sub>                                      | 0.35T <sub>tr</sub> | —                   | —                   | —    | 0.35T <sub>tr</sub> | —                   | —           | —   | [16]  |
| Slave Mode: Clock accepted by transmitter or receiver   |                     |                     |                     |      |                     |                     |             |     |       |
| HIGH t <sub>HC</sub>                                    | —                   | 0.35T <sub>tr</sub> | —                   | —    | —                   | 0.35T <sub>tr</sub> | —           | —   | [15]  |
| LOW t <sub>LC</sub>                                     | —                   | 0.35T <sub>tr</sub> | —                   | —    | —                   | 0.35T <sub>tr</sub> | —           | —   | [15]  |
| Rise time t <sub>RC</sub>                               | —                   | —                   | 0.15T <sub>tr</sub> | —    | —                   | —                   |             | —   | [16]  |
| Transmitter   |                     |                     |                     |      |                     |                     |             |     |       |
| Delay t <sub>dtr</sub>                                  | —                   | —                   | —                   | 0.8T | —                   | —                   | —           | —   | [17]  |
| Hold time t <sub>htr</sub>                              | 0                   | —                   | —                   | —    | —                   | —                   | —           | —   | [16]  |
| Receiver  |                     |                     |                     |      |                     |                     |             |     |       |
| Setup time t <sub>sr</sub>                              | —                   | —                   | —                   | —    | 0.2T <sub>tr</sub>  | —                   | —           | —   | [18]  |
| Hold time t <sub>hr</sub>                               | —                   | —                   | —                   | —    | 0.2T <sub>tr</sub>  | —                   | —           | —   | [18]  |

### Notes

15. The system clock period T must be greater than  $T_{tr}$  and  $T_r$  because both the transmitter and receiver have to be able to handle the data transfer rate.
16. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason,  $t_{HC}$  and  $t_{LC}$  are specified with respect to T.
17. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than  $0.35T_r$ , any clock that meets the requirements can be used.
18. Because the delay ( $t_{dtr}$ ) and the maximum transmitter speed (defined by  $T_{tr}$ ) are related, a fast transmitter driven by a slow clock edge can result in  $t_{dtr}$  not exceeding  $t_{RC}$  which means  $t_{htr}$  becomes zero or negative. Therefore, the transmitter has to guarantee that  $t_{htr}$  is greater than or equal to zero, so long as the clock rise-time  $t_{RC}$  is not more than  $t_{RCmax}$ , where  $t_{RCmax}$  is not less than  $0.15T_{tr}$ .
19. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
20. The data setup and hold time must not be less than the specified receiver setup and hold time.

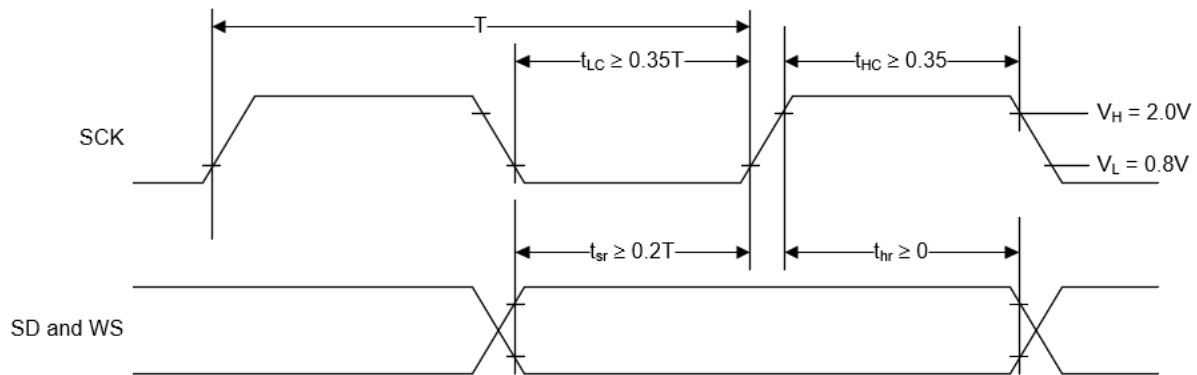
**Figure 17. I<sup>2</sup>S Transmitter Timing**


$T$  = Clock period

$T_{tr}$  = Minimum allowed clock period for transmitter

$T = T_{tr}$

\*  $t_{RC}$  is only relevant for transmitters in slave mode.

**Figure 18. I<sup>2</sup>S Receiver Timing**


$T$  = Clock period

$T_r$  = Minimum allowed clock period for transmitter

$T > T_r$



## Environmental Specifications

### Environmental Compliance

This Cypress BLE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen-Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

### RF Certification

The CYBT-243053-02 module is certified under the following RF certification standards:

- FCC: WAP3053
- ISSED: 7922A-3053
- MIC: TBD
- CE

### Safety Certification

The CYBT-243053-02 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

### Environmental Conditions

Table 29 describes the operating and storage conditions for the Cypress Bluetooth module.

**Table 29. Environmental Conditions for CYBT-243053-02**

| Description   | Minimum Specification | Maximum Specification       |
|---|-----------------------|-----------------------------|
| Operating temperature   | −30 °C                | 85 °C                       |
| Operating humidity (relative, non-condensation)               | 5%                    | 85%                         |
| Thermal ramp rate   | –                     | 10 °C/minute                |
| Storage temperature   | −40 °C                | 85 °C                       |
| Storage temperature and humidity                              | –                     | 85 °C at 85%                |
| ESD: Module integrated into system Components <sup>[21]</sup> | –                     | 15 kV Air<br>2.0 kV Contact |

### ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

**Device Handling:** Proper ESD protocol must be followed in manufacturing to ensure component reliability.

#### Note

21. This does not apply to the RF pins (ANT).

## Regulatory Information

### FCC

#### FCC NOTICE:

The device CYBT-243053-02 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. Transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

#### CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

#### LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP3053.

In any case the end product must be labeled exterior with **"Contains FCC ID: WAP3053"**.

#### ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antenna listed in [Table on page 12](#). When integrated in the OEM's product, this fixed antenna requires installation preventing end-users from replacing them with non-approved antennas. Any antenna not in [Table on page 12](#) must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

#### RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antenna in [Table on page 12](#), to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBT-243053-02 with the integrated PCB trace antenna (FCC ID: WAP3053) is far below the FCC radiofrequency exposure limits. Nevertheless, use CYBT-243053-02 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

**ISED****Innovation, Science and Economic Development (ISED) Canada Certification**

CYBT-243053-02 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development (ISED) Canada.

License: IC: 7922A-3053

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from [www.ic.gc.ca](http://www.ic.gc.ca).

This device has been designed to operate with the antenna listed in [Table on page 12](#), having a maximum gain of -0.5 dBi. Antennas not included in [Table on page 12](#) or having a gain greater than -0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

**ISED NOTICE:**

The device CYBT-243053-02 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYBT-243053-02, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

**ISED INTERFERENCE STATEMENT FOR CANADA**

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**ISED RADIATION EXPOSURE STATEMENT FOR CANADA**

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé.

**LABELING REQUIREMENTS:**

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the ISED Notices above. The IC identifier is 7922A-3053. In any case, the end product must be labeled in its exterior with **"Contains IC: 7922A-3053"**.

Le fabricant d'équipement d'origine (OEM) doit s'assurer que les exigences d'étiquetage ISED sont respectées. Cela comprend une étiquette clairement visible à l'extérieur de l'enceinte OEM spécifiant l'identifiant Cypress Semiconductor IC approprié pour ce produit ainsi que l'avis ISED ci-dessus. L'identificateur IC est TBD. En tout cas, le produit final doit être étiqueté dans son extérieur avec **"Contient IC: 7922A-3053"**.

**European Declaration of Conformity**

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBT-243053-02 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:



All versions of the CYBT-243053-02 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

**MIC Japan**

CYBT-243053-02 is certified as a module with certification number **TBD**. End products that integrate CYBT-243053-02 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

**TBD**

## Packaging

**Table 30. Solder Reflow Peak Temperature**

| Module Part Number | Package    | Maximum Peak Temperature | Maximum Time at Peak Temperature | No. of Cycles |
|--------------------|------------|--------------------------|----------------------------------|---------------|
| CYBT-243053-02     | 35-pad SMT | 260 °C                   | 30 seconds                       | 2             |

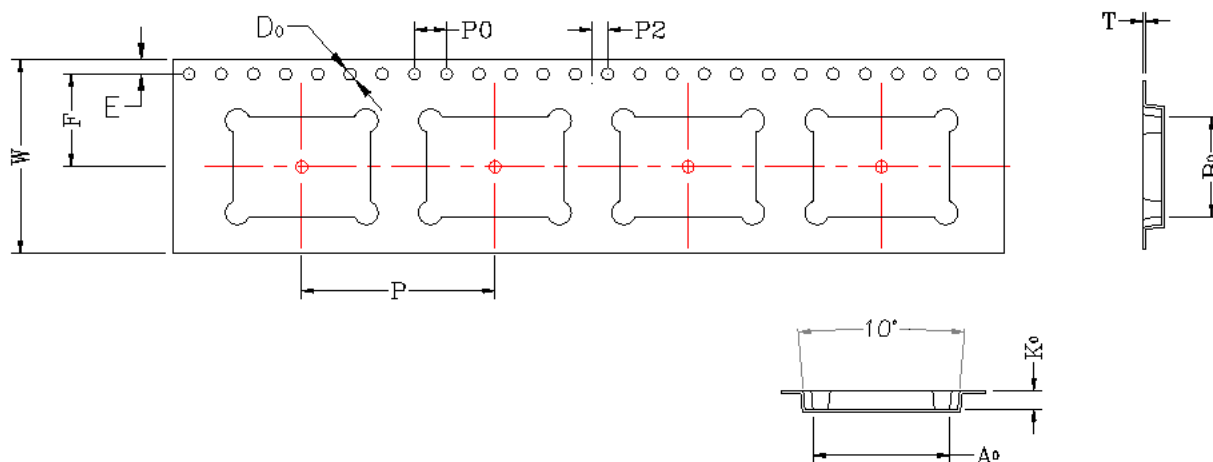
**Table 31. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Module Part Number | Package    | MSL   |
|--------------------|------------|-------|
| CYBT-243053-02     | 35-pad SMT | MSL 3 |

The CYBT-243053-02 is offered in tape and reel packaging. [Figure 19](#) details the tape dimensions used for the CYBT-243053-02.

**Figure 19. CYBT-243053-02 Tape Dimensions**

| Item        | W                                      | A <sub>0</sub>                         | B <sub>0</sub>                         | K <sub>0</sub>                        | P                                      | F                                      | E                                      | D <sub>0</sub>                         | D <sub>1</sub>                         | P <sub>0</sub>                         | P <sub>2</sub>                         | T                                     |
|-------------|--|--|--|---------------------------------------|--|--|--|--|--|--|--|---------------------------------------|
| Measurement | 24.0 <sup>+0.30</sup> <sub>-0.30</sub> | 17.0 <sup>+0.10</sup> <sub>-0.10</sub> | 12.4 <sup>+0.10</sup> <sub>-0.10</sub> | 2.3 <sup>+0.10</sup> <sub>-0.10</sub> | 24.0 <sup>+0.10</sup> <sub>-0.10</sub> | 11.5 <sup>+0.10</sup> <sub>-0.10</sub> | 1.75 <sup>+0.10</sup> <sub>-0.10</sub> | 1.50 <sup>+0.10</sup> <sub>-0.00</sub> | 1.50 <sup>+0.10</sup> <sub>-0.10</sub> | 4.00 <sup>+0.10</sup> <sub>-0.10</sub> | 2.00 <sup>+0.10</sup> <sub>-0.10</sub> | 0.3 <sup>+0.05</sup> <sub>-0.05</sub> |



[Figure 20](#) details the orientation of the CYBT-243053-02 in the tape as well as the direction for unreeling.

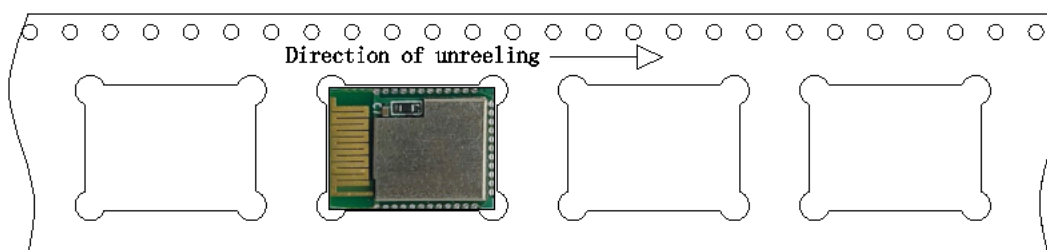
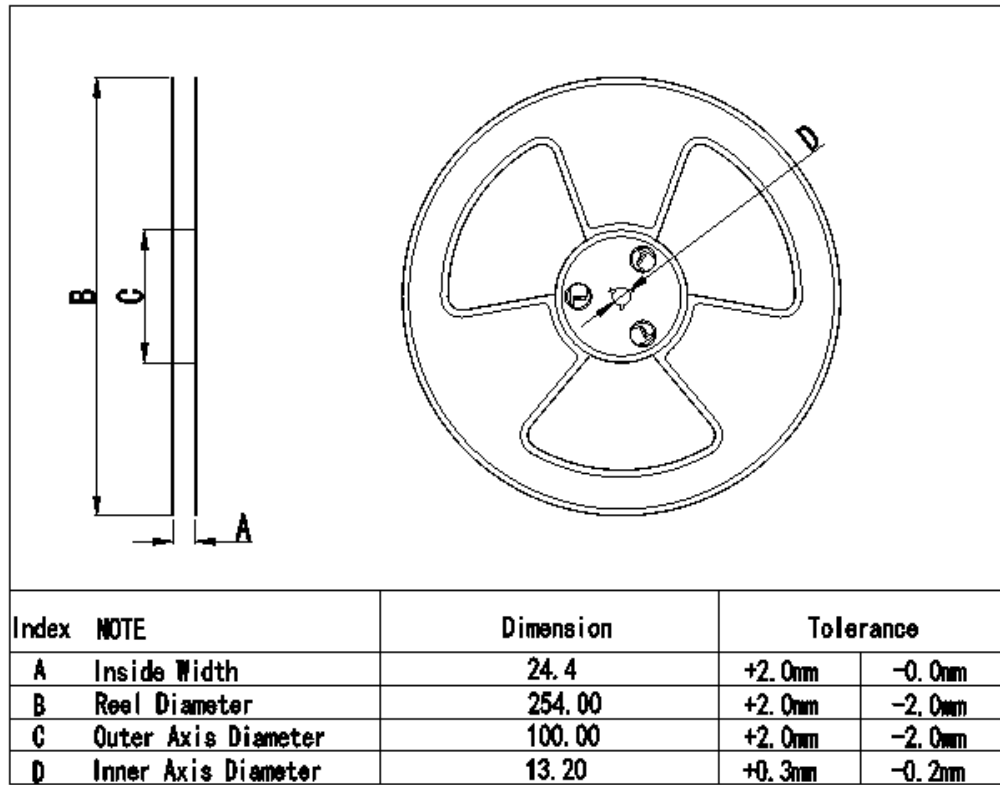
**Figure 20. Component Orientation in Tape and Unreeling Direction**


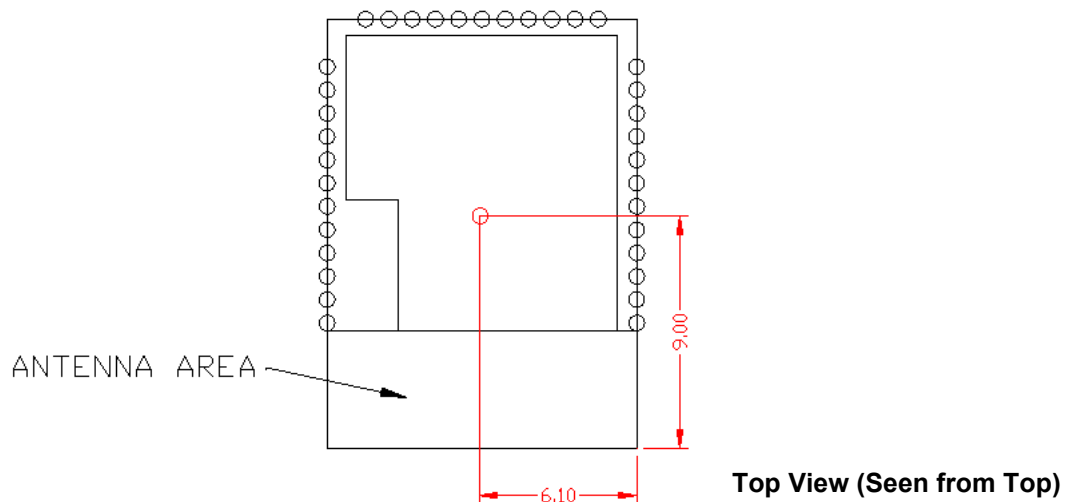
Figure 21 details reel dimensions used for the CYBT-243053-02.

**Figure 21. Reel Dimensions**



The CYBT-243053-02 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBT-243053-02 is detailed in Figure 22.

**Figure 22. CYBT-243053-02 Center of Mass**



## Ordering Information

Table 32 lists the CYBT-243053-02 part number and features. Table 32 also lists the target program for the respective module ordering codes. Table 33 lists the reel shipment quantities for the CYBT-243053-02.

**Table 32. Ordering Information**

| Ordering Part Number | Max CPU Speed (MHz) | Flash Size (KB) | RAM Size (KB) | UART | I <sup>2</sup> C | SPI | I <sup>2</sup> S | PCM | PWM | ADC Inputs | GPIOs | Package | Packaging     |
|----------------------|---------------------|-----------------|---------------|------|------------------|-----|------------------|-----|-----|------------|-------|---------|---------------|
| CYBT-243053-02       | 96                  | 256             | 176           | Yes  | Yes              | Yes | Yes              | Yes | 6   | 15         | 22    | 35-SMT  | Tape and Reel |

**Table 33. Tape and Reel Package Quantity and Minimum Order Amount**

| Description                  | Minimum Reel Quantity | Maximum Reel Quantity | Comments                           |
|------------------------------|-----------------------|-----------------------|------------------------------------|
| Reel Quantity                | 500                   | 500                   | Ships in 500 unit reel quantities. |
| Minimum Order Quantity (MOQ) | 500                   | –                     | –                                  |
| Order Increment (OI)         | 500                   | –                     | –                                  |

The CYBT-243053-02 is offered in tape and reel packaging. The CYBT-243053-02 ships in a reel size of 500 units.

For additional information and a complete list of Cypress Semiconductor Bluetooth products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

|                                       |   |
|---------------------------------------|---|
| U.S. Cypress Headquarters Address     | 198 Champion Court, San Jose, CA 95134                      |
| U.S. Cypress Headquarter Contact Info | (408) 943-2600  |
| Cypress website address               | <a href="http://www.cypress.com">http://www.cypress.com</a> |

## Acronyms

**Table 34. Acronyms Used in this Document**

| Acronym       | Description  |
|---------------|--|
| BLE           | Bluetooth Low Energy   |
| Bluetooth SIG | Bluetooth Special Interest Group   |
| CE            | European Conformity  |
| CSA           | Canadian Standards Association   |
| EMI           | electromagnetic interference   |
| ESD           | electrostatic discharge  |
| FCC           | Federal Communications Commission  |
| GPIO          | general-purpose input/output   |
| ISED          | Innovation, Science and Economic Development (Canada)  |
| IDE           | integrated design environment  |
| KC            | Korea Certification  |
| MIC           | Ministry of Internal Affairs and Communications (Japan)  |
| PCB           | printed circuit board  |
| RX            | receive  |
| QDID          | qualification design ID  |
| SMT           | surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs |
| TCPWM         | timer, counter, pulse width modulator (PWM)  |
| TUV           | Germany: Technischer Überwachungs-Verein (Technical Inspection Association)  |
| TX            | transmit   |

## Document Conventions

### Units of Measure

**Table 35. Units of Measure**

| Symbol | Unit of Measure                |
|--------|--------------------------------|
| °C     | degree Celsius                 |
| dB     | decibel                        |
| dBi    | decibels relative to isotropic |
| dBm    | decibel-milliwatts             |
| kV     | kilovolt                       |
| mA     | milliamperes                   |
| mm     | millimeters                    |
| mV     | millivolt                      |
| μA     | microamperes                   |
| μm     | micrometers                    |
| MHz    | megahertz                      |
| GHz    | gigahertz                      |
| V      | volt                           |



## Document History Page

| Document Title: CYBT-243053-02, EZ-BT™ Module<br>Document Number: 002-28015 |     |                 |  |
|---|-----|-----------------|--|
| Revision  | ECN | Submission Date | Description of Change                            |
| **  |     | 08/01/2019      | Preliminary datasheet for CYBT-243053-02 module. |

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