

The receiver section configuration is shown as Fig. 1.

is mixed with the second local oscillator signal □50.4MHz□to create a 450KHz second IF signal. The second IF signal is then fed to a ceramic filter (N□CF101□CF103□W□CF102□CF104) to eliminate unwanted signals. The resulting signal is detected by IC119 and output from Pin9 as an AF signal.

## 2.4 AF Amplifier

The AF signal from IC119 is amplified by IC109 before being filtered. The resulting AF signal passes through Q108□AF MUTE□and IC121(electronic switch) , then is amplified by IC106 ( the received signaling is inputted into CPU for decoding) and IC104. The amplified signal is fed to IC125 (volume control) and Q114 (SP MUTE) before entering AF AMP (IC126). The outputted AF signal is then delivered to the speaker through control panel.

## 2.5 Squelch

The AF signal from IC119 is amplified by IC109 again, then filtered to remove noise signals. The noise signal is amplified by Q121 and rectified by D110 to produce an ASQ level. The ASQ level is then compared in CPU (IC120) to generate a level which controls AF MUTE and SP MUTE. IC120 determines whether to output sounds from the speaker by controlling Q108, Q114.

## 3. Transmitter

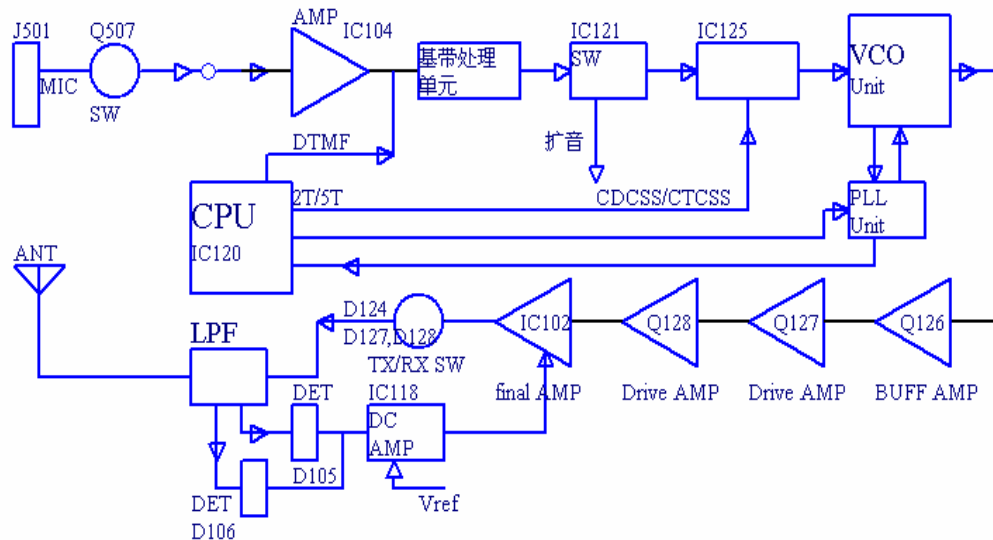


Figure 2 Transmitter Section Configuration

### 3.1 MIC Circuit and Modulation Circuit

The AF signal from MIC is amplified by IC204 after passing through the MIC control switch (Q507). The resulting signal is then amplified by IC106 and pre-emphasized, encoded. It is passed to IC121 (electronic switch) before reaching IC125. The signaling is inputted into IC125 and enters VCO for modulation.

### **3.2 Power AMP and Post AMP**

TX-RF signal is outputted from Q703 in VCO circuit and amplified by Q126, Q127 and Q128. The amplified signal is then fed to IC102 and passes through LPF before reaching the antenna terminal.

### **3.3 APC**

The APC is used to keep the power output at a constant preset value. D105 and D106 transform the signal from detector into DC voltage which is then compared with the reference voltage from CPU in IC118 and outputted as DC control voltage. The DC control voltage controls the output power by controlling the grid of IC102.

## **4. PLL**

PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission. PLL circuit consists of TX frequency oscillator (Q701), RX frequency oscillator (Q702), buffer amplifier (Q703), RF amplifier (Q124), PLL IC (IC801), LPF (Q804, Q805) and TX/RX VCO control switch (Q704, Q706).

In transmit mode, IC120 transmits the frequency data to PLL IC. Q704 is turned on to activate TX VCO. The outputted signal is amplified by Q703, Q124, then divided by PLL IC into 2.5KHz, 5KHz or 6.25KHz signal. The divided signal is compared with 2.5KHz, 5KHz or 6.25KHz reference signal from 16.8MHz crystal oscillator (2.5 PPM frequency stability) in the phase comparator. The frequency control voltage outputted from the phase comparator is sent to TX VCO after passing through LPF (Q804, Q805). In the meantime, modulation signal (TX) is passed to TX VCO for frequency modulation.

The working principle in receive mode is similar to that in transmit mode.