Circuit Description

1. Frequency Configuration

The receiver utilizes double conversion super heterodyne. The first IF is 21.7 MHz and the second is 450KHz. The first local oscillator signal is supplied from PLL circuit. PLL circuit in the transmitter generates the necessary frequencies. Figure 1 shows the frequency configuration.

Frequency range: 460—470MHz

(For the detail, please refer to the Appendix I: TC-1600 Frequency Table)

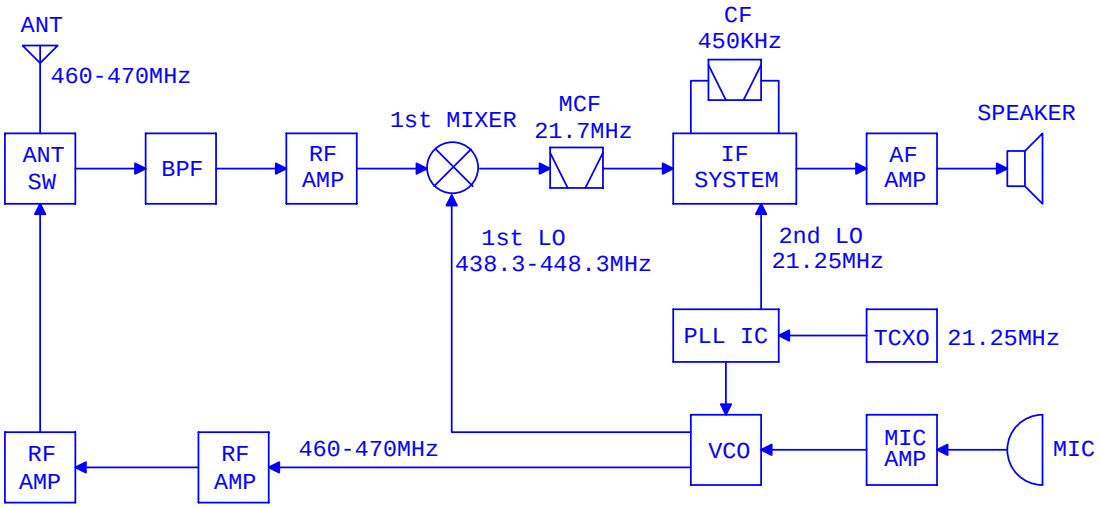


Fig1. Frequency Configuration

2. Receiver

The receiver utilizes double conversion super heterodyne.

1) Front-end RF Amplifier

The signal from the antenna passes through a transmit/receive switch circuit before entering the SAW filter Z501 to eliminate unwanted signals, and then is amplified at RF amplifier Q501. The processed amplified signal then goes to the first mixer.

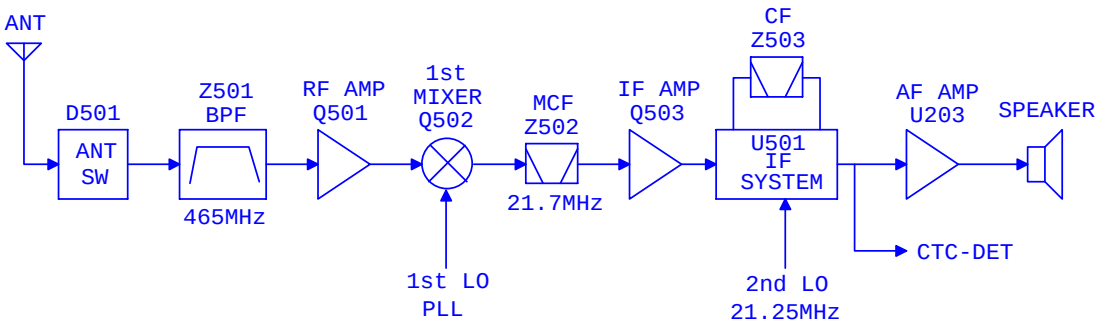


Fig.2 Receiver Section Configuration

2） First Mixer

The signal from RF amplifier is mixed with the first local oscillator signal from PLL frequency synthesizer in the first mixer Q502 to generate a 21.7 MHz first IF signal. The first IF signal is then fed through the 21.7MHz crystal filter Z502 to remove spurious signals from adjacent channel.

3) IF Amplifier

The first IF signal is amplified at Q503, which then enters the IF processing chip U501. The signal is mixed with the second local oscillator signal to generate a 450KHz second IF signal. The second IF signal is then fed to a 450KHz ceramic filter Z503 to eliminate unwanted signals before it is amplified and detected at U501.

4) AF Amplifier

The AF signal obtained from U501 is filtered in U301A, and then amplified in Q207. Then the processed

AF signal passes through an AF squelch switch U202 and a volume control circuit and then is amplified in an AF power amplifier U203to drive the speaker.

5) Squelch

Part of the AF signal from U501 enters U501 again and the noise component is amplified by a filter and an amplifier, and then enters Q206 to amplify the noise further. After rectified and filtered by D203 and C331, the DC signals goes to the analog port U604 of the microprocessor. U604 determines whether to output sounds from the speaker by detecting whether the input voltage is higher or lower than the preset value.

To output sounds from the speaker, U604 sends a mute and an AF control signal APA-EN to U203. (See figure 3)

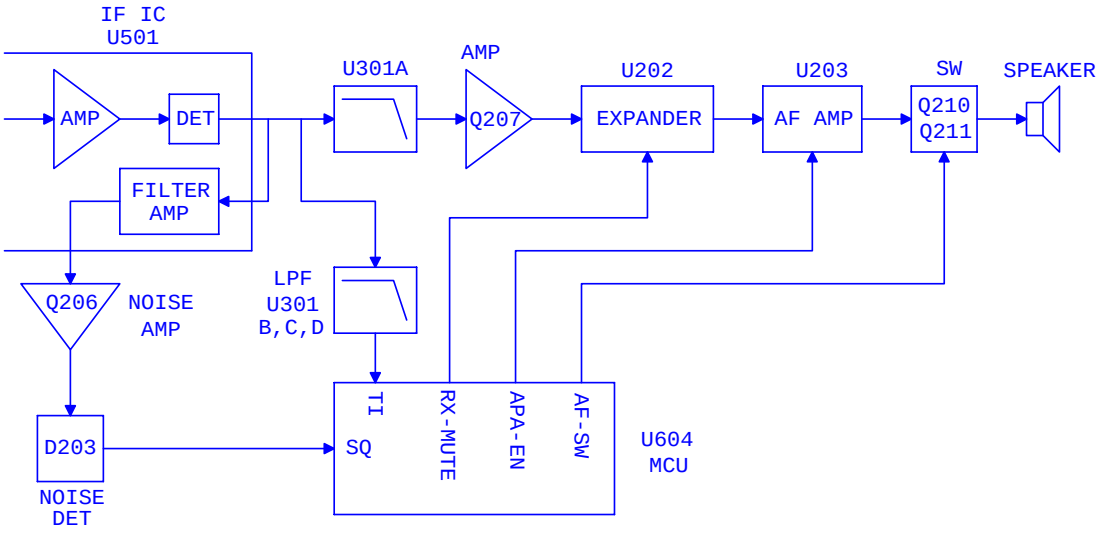


Fig. 3 AF Amplifier & Squelch Circuit

6) Receiving CTCSS/CDCSS signal

The 300Hz-and-higher audio frequency of the signal output from U501 is filtered by low-pass filter U301-B, C, D. The processed signal enters the microprocessor U604 which determines whether the CTCSS/ CDCSS matches the pre-set value, and controls the RX-MUTE, APA and the speaker output sounds according to the squelch result.

3. PLL Synthesizer

PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

1) PLL Circuit

The step frequency of PLL circuit is 6.25KHz, 10 KHz or 12.5 KHz. A 21.25MHz reference oscillator signal is divided at U101 by a mixed counter to create a 6.25KHz, 10 KHz or 12.5 KHz reference frequency. Output signal from VCO enters the 16 pin of U101 and is divided at U101 by a programmable pulse swallow counter. The divided signal is compared in the phase comparator U101 with a 6.25KHz, 10 KHz or 12.5 KHz reference signal. The signal from phase comparator is filtered through a low-pass filter and generates a VCO voltage added to varactor diodes D102 and D103 to control the oscillator frequency. (See Figure 4)

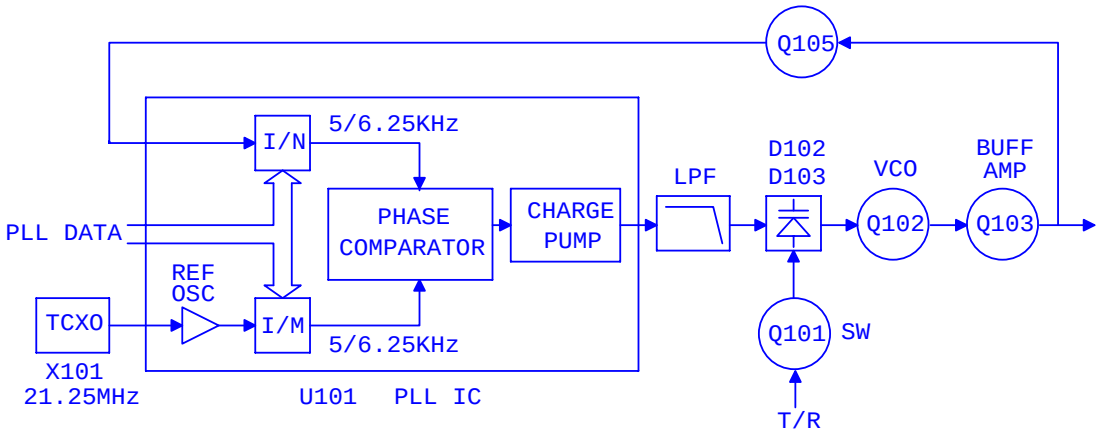


Fig.4 PLL Circuit

2）**VCO**

Q102 composes Colpitts oscillator circuit together with the peripheral circuit. The oscillator frequency is controlled by PLL. In receive mode, the oscillator frequency is the first local oscillator frequency for reception. In transmit mode, the oscillator frequency is the RF frequency for transmission.

4. Transmitter

1) Transmitting AF

The AF signal from the microphone passes through a pre-emphasis circuit, is amplified and filtered by a low-pass filter at U202-A, B and Q204, Q205. The processed signal enters VCO for direct modulation. (See figure 5)

2) CTCSS/CDCSS Encoder

The necessary signal for 38 groups of CTCSS and 83 groups of CDCSS encoder is generated and outputted by TO pin of U604 to adjust the reference frequency of PLL circuit. Because the reference oscillator is unable to modulate the frequency outside PLL feature, it is modulated by the distributor at one side of the VCO. (See fig.5)

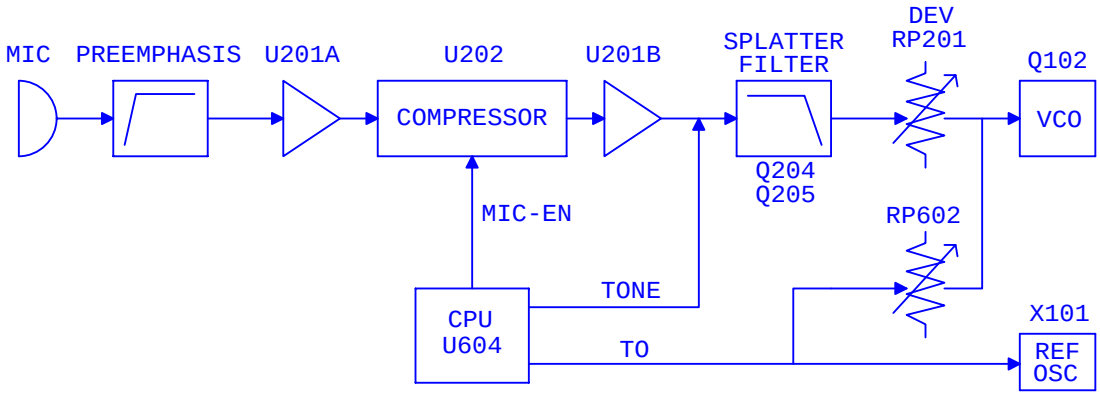


Fig 5.Transmit AF and CTCSS/CDCSS

3) RF Amplifier

The RF signal obtained from VCO buffer amplifier is amplified by Q104. The amplified signal is amplified by power amplifier Q401, Q402 and Q403 to generate RF power. (See Fig.6)

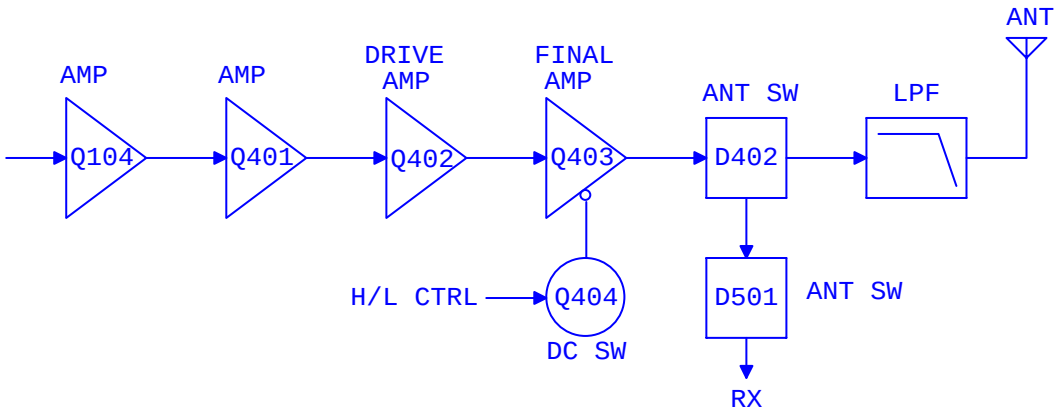


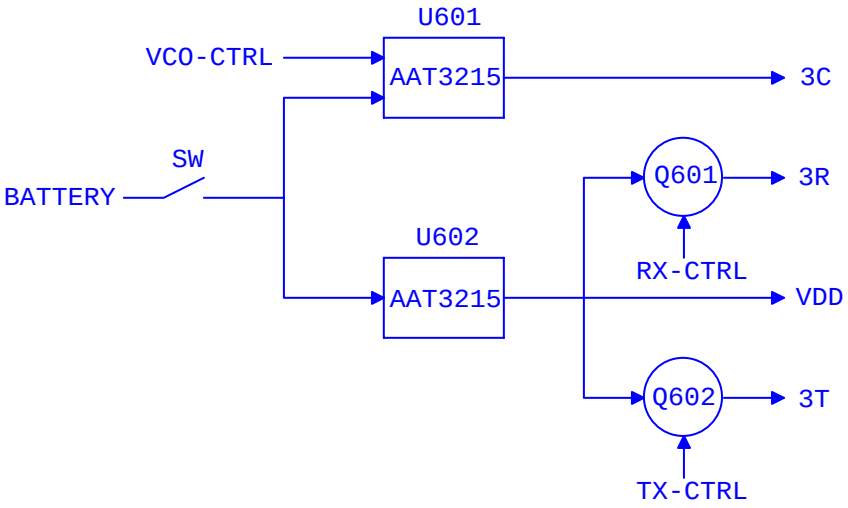
Fig.6 Transmit Module

4）Antenna Switch and LPF

The RF signal is passed through a low-pass filter network and a transmit/receive switch (D402 and D501) before it is passed to the antenna terminal. D402 is turned on in transmit mode and off in receive mode.

5．Power Supply

U602 supplies stabilized power for the control circuit. In transmit mode, U601 is turned on and supplies voltage for the transmit VCO; Q602 is turned on and supplies operation voltage for the transmitting front-end amplifier. In receiving mode, U601 is turned on and supplies voltage for the receive VCO high-frequency amplified circuit; Q601 is turned on and supplies operation voltage for the receiving circuit.



6．Control System

The U604 CPU operates at 4.9152MHz and supplies control signal voltage for the control circuit.