DS720i TECHNICAL DESCRIPTION
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The DS720i is a long range dual PIR/Microwave motion detector. The detection coverage consists of a standard 300' x 10.5' pattern or an optional 90' x 70' pattern. The enclosure design is similar to the DS794z and uses the existing DS794z optics. Feature set will include the following:

- MW and PIR Noise Voltage Output
- Form C Relay
- Input power from 6-15 VDC
- Cover Tamper
- PIR and MW Self Test
- Trouble Output Relay
- MW Range Adjust
- Antimask Delay Processing
- Optional Active IR Antimask
- MW Frequencies
  - 9.900GHz (DS720i-A and DS720ia-A only for United Kingdom)
  - 10.525 GHz (DS720I and DS720IA)
  - 10.687GHz (DS720i-B and DS720ia-B only for France)
- Unit Sensitivity High/Int
- Antimask On/Off
- Antimask Sensitivity High/Low
- Motion Monitor Off/1 Day/4 Day/30 Day
- Memory On/Off

+5V Regulator

The 5V regulator (U1) consists of an LM2931 voltage regulator. RV3 protects the voltage regulator from harmful voltage spikes. The UNREG line is used to drive all high current loads through emitter followers to prevent noise spikes from entering the amplifiers.

PIR Amplifier

The PIR amplifier utilizes a LM358 (U3). The DET is AC coupled to the first amp stage via a non-polar capacitor (C31). The gain of the first amp is determined by the ratio of R24 to R36. The bandwidth of the first stage is limited by the values of C21 and C22. The gain of the second stage is determined by the ratio of R26 to R37. The bandwidth is limited by C24 and C30. The amplified signal is coupled to one of the analog inputs of the microprocessor (U4) where signal processing is performed.

Microwave Subsystem

The MW subsystem utilizes a micro-strip Microwave Transceiver. The transmitter consists of a FET oscillator (Q99) biased through R99. The frequency of oscillation is determined by the electrical/physical properties of the ceramic resonator Y99. Fine tuning of the transmitter is accomplished by adjusting the position of the tuning screw located in the back of the plastic back shield. The transmit and receive antenna consist of patch antenna design. The antenna is located on top of the PIR focusing mirror. The transmitter drive pulse is generated by microprocessor U4. The drive pulses are applied to Q99 by Q10through P3, and are 20 microseconds on-time, and 1 millisecond off-time. The receiver incorporates a balanced mixer design consisting of two diodes present in D99. Equal amounts of RF energy are applied to each diode, one from the transmitter and one from the receiver section. This balancing of the RF energy should produce a nominal pulse voltage on the IF output (MW2) of 0Vp, and should always be less than +/- 0.2Vp. The IF output is fed to a sample-and-hold circuit Q1 via AC coupling cap C20. The sample pulse is generated by the microprocessor and should be 10 microseconds long and centered in the middle of the drive pulse. The signal is fed to two stages of amplification U2-1 and U2-4. The MW range is adjusted by potentiometer R31. This amplified signal is fed into one of the analog inputs of the microprocessor where the rest of the signal processing is done (see software spec.).

Microprocessor Functions

See DS720i Software Specification.