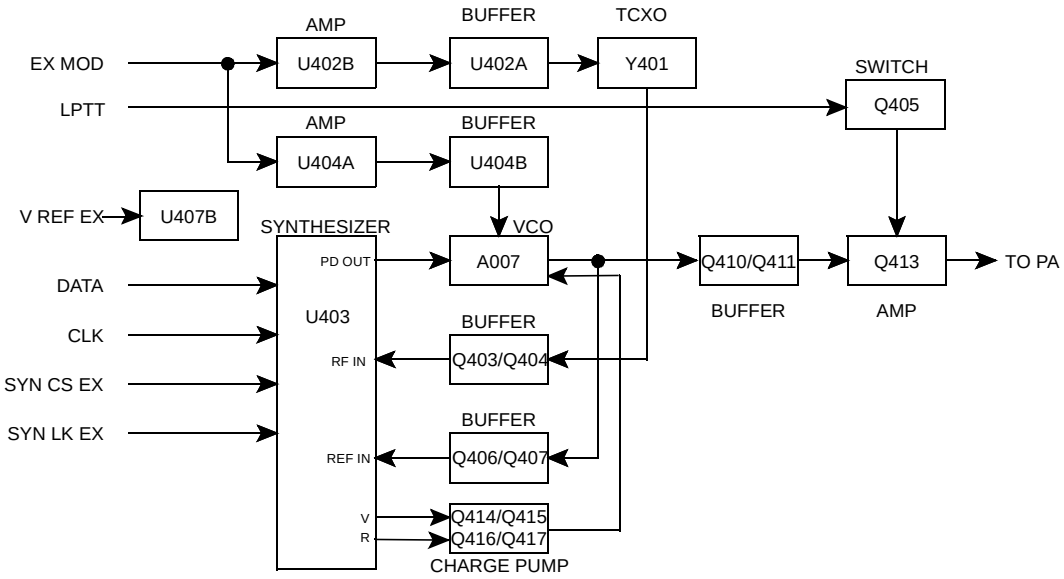

Figure 1 EXCITER BLOCK DIAGRAM

SYNTHESIZER

The synthesizer inputs/outputs are shown in Figure 1. The synthesizer output signal is the transmit frequency. This signal is produced by a VCO (voltage-controller oscillator) that is frequency controlled by a DC voltage produced by synthesizer chip U403. This DC voltage is filtered by a loop filter made up of C805, C806 and R804 in the VCO circuitry.

Frequencies are selected by programming counters in U403 to divide by a certain number. This programming is provided through J401, pins 12, 19 and 20. The frequency stability of the synthesizer is established by the ±1.0 PPM stability of TCXO Y401. This oscillator is stable from -30°C to +60°C (-22°F to +140°F).

The VCO frequency of A007 is controlled by a DC voltage produced by the phase detector in U403. The phase detector senses the phase and frequency of the two input signals and causes the VCO control voltage to increase or decrease if they are not the same. When the frequencies are the same, the VCO is then “locked” on frequency.

The synthesizer contains the R (reference), N, and A counters, phase and lock detectors and counter programming circuitry.

One input signal to the phase detector in U403 is the reference frequency (f_R). This frequency is the 17.5 MHz TCXO frequency divided by the reference counter to the frequency step or 6.25 kHz. The other input signal (f_V) is the VCO frequency divided by the “N” counter in U403. The counters are programmed through the synthesizer data line on J401, pin 20. Each channel is programmed by a divide number so that the phase detector input is identical to the reference frequency (f_R) when the VCO is locked on the correct frequency.

Frequencies are selected by programming the three counters in U403 to divide by assigned numbers. The programming of these counters is performed by circuitry in the Main Processor Card (MPC), buffered and latched through the Interface Alarm Card (IAC) and fed into the synthesizer on J401, pin 20 to Data input port U403, pin 19.

Data is loaded into U403 serially on the Data input port U403, pin 19 when U403, pin 17 is low. Data is clocked into the shift registers a bit at a time by a low to high transition on the Clock input port U403, pin 18. The Clock pulses come from the MPC via the IAC to J401, pin 19.

As previously stated, the counter divide numbers are chosen so that when the VCO is operating on the correct frequency, the VCO-derived input to the phase detector (f_V) is the same frequency as the TCXO-derived input (f_R). The f_R input is produced by dividing the 17.5 MHz TCXO frequency by 2800. This produces a reference frequency (f_R) of 6.25 kHz. Since the VCO is on frequency and no multiplication is used, the frequencies are changed in 6.25 kHz steps. The reference frequency is 6.25 kHz for all frequencies selected by this Exciter.

The f_V input is produced by dividing the VCO frequency using the prescaler and N counter in U403. The prescaler divides by 64 or 65. The divide number of the prescaler is controlled by the N and A counters in U403. The N and A counters function as follows:

Both the N and A counters begin counting down from their programmed number. When the A counter reaches zero, it halts until the N counter reaches zero. Both counters then reset and the cycle repeats. The A counter is always programmed with a smaller number than the N counter. While the A counter is counting down, the prescaler divides by 65. Then when the A counter is halted, the prescaler divides by 64.

Example: To illustrate the operation of these counters, assume a transmit frequency of 150.250 MHz. Since the VCO is the channel frequency for transmit this frequency is used. To produce this frequency, the N and A counters are programmed as follows:

N = 375 **A = 40**

To determine the overall divide number of the prescaler and N counter, the number of VCO output pulses required to produce one N counter output pulse can be counted. In this example, the prescaler divides by 65 for 65 x 40 or 2,600 input pulses. It then divides by 64 for 64 x (375 - 40) or 21,440 input pulses. The overall divide number K is therefore (21,440 + 2,600) or 24,040. The VCO frequency of 150.250 MHz divided by 24,040 equals 6.25 kHz which is the f_R input to the phase detector. The overall divide number K can also be determined by the following formula:

$$K = 64N + A$$

Where,

N = N counter divide number and

A = A counter divide number.

BUFFER AMPLIFIER

A cascode amplifier formed by Q403 and Q404 provides amplification and isolation between the TCXO and Synthesizer U403. A cascode amplifier is used because it provides high gain, high reverse isolation and consumes only a small amount of power. The input signal to this amplifier is coupled from TCXO Y401, pin 5 by C420. C420 also provides DC blocking. Bias for the amplifier is provided by R430, R431, R432, R433 and R428. L402 is an RF choke. RF bypass is provided by C416, C418 and C419. The output of Q403/Q404 is coupled to U403, pin 20 by C417.

BUFFER AMPLIFIER

A cascode amplifier formed by Q406 and Q407 provides amplification and also isolation between the VCO and Synthesizer U403. A cascode amplifier is used because it provides high gain, high isolation and consumes only a small amount of power. The input signal to this amplifier is coupled from VCO A007, pin 6 by C433. C433 also provides DC blocking. Bias for the amplifier is provided by R450, R451, R453, R454 and R455. L403 is an RF choke. RF bypass is provided by C430, C431 and C479. The output of Q406/Q407 is coupled to U403, pin 11 by a non-polarized capacitor formed by C429/C499.

LOCK DETECT

When the synthesizer is locked on frequency, the Lock Detect output on U403, pin 2 is a high voltage with narrow negative-going pulses. When the synthesizer is unlocked, the negative-going pulses are much wider, the width may vary at a rate determined by the frequency difference of f_V/f_R.

The locked or unlocked condition of the synthesizer is filtered by R440/C423 and applied to J401, pin 16, then sent to the RF Interface on J102, pin 16 for detection.

CHARGE PUMP, LOOP FILTER

The charge pump circuit charges and discharges C519, C520 and C521 in the loop filter to provide the 12V VCO control voltage. Pulses which control the charge pump are fed out of U403, pins 3/4. When both phase detector inputs are in phase, these output signals are high except for a very short period when both pulse low in phase. If the frequency of the f_R input to the phase detector is higher than that of the f_V input (or if the phase of f_R leads f_V), the VCO frequency is too low. The negative-going pulses on the f_V output (pin 4) then become much wider and the f_R output (pin 3) stays essentially high. If the frequency of the f_V input is greater than f_R (VCO frequency too high), the opposite occurs.

Q414 and Q415 are drivers which make the 5V levels and polarity of U403 phase detector outputs compatible with the high voltage supply to Q416 and Q417. Capacitors C523 and C517 momentarily bypass R494 and R498 when negative-going pulses occur. This speeds up the turn-off time of Q414 and Q415 by minimizing the effect of the base charge.

When a negative-going pulse occurs on pin 4, Q414 turns on which turns on Q416. Q416 sources current to charge up the loop filter capacitors C519/C520, thereby increasing the VCO control line voltage. When a negative-going pulse occurs on pin 3, Q415 turns on which turns on Q417. Q417 sinks current to discharge the loop filter capacitors C519/C520 thereby decreasing the VCO control line voltage. The source current from Q416, when it is on, equals the sink current from Q417, when it is on.

BUFFER AMPLIFIER

A cascode amplifier formed by Q410/Q411 provides amplification and also isolation between the VCO and exciter RF stages. A cascode amplifier is used because it provides high gain, high isolation and consumes only a small amount of power. The input signal to this amplifier is tapped from VCO A007, pin 4 by C441. C441 also provides DC blocking. Bias for the amplifier is provided by R464, R465, R466, R467 and R468. L406 is an RF choke and R483 lowers the Q of the coil. RF bypass is provided by C434, C442, C445, C443, C444 and C480. The output of Q410/Q411 is matched to the Exciter RF stages by a section of microstrip, C446, signal pad R459/R460/R461, C498, C450 and L408.

RF AMPLIFIERS

RF amplifier Q413 is biased by CR403, R477, R478, R479 and R480. C508 provides RF bypass from the DC line and R479/R480 provide supply voltage isolation. L 411 is an RF choke to the supply line. Q413 is matched to 50 ohms by low pass filter C509/L412/C510 and C465 provides DC blocking. The RF output of the Exciter is on coaxial connector J402 to the Power Amplifier.

125W POWER AMPLIFIER

AMPLIFIER/PREDRIVER

RF input to the PA from the Exciter is through a coaxial cable and connector to WO511. C501 couples the RF to signal pad R501/R502/R503 that connects the input to 0.3W pre-driver Q501. R504, R505 and R506 provide DC bias to the gate of Q501. C506, C507 and C508 provide RF bypass from the DC supply line. L503 is an RF choke. C510 and C522 provide RF bypass. C511/L504/C512/C513 match Q501 output impedance to U501 input impedance. U502 provides Q501 with DC voltage regulated at 8V.

DRIVER

U501 is a 12W amplifier operating in the 132-178 MHz range. The RF is applied to the input of the splitter and to the finals. U509 is used to monitor the current supply to U501 by software through the RF Interface board. U509 also prevents over-driving the final amplifiers.

Power control is connected to WO505 from the RF Interface board (RFIB). RF is filtered from the control voltage line by various capacitors to U501, pin 2. This control voltage regulates the RF output of the amplifier on U501, pin 5 to approximately 10W.

FINAL AMPLIFIERS

Q502 and Q503 are combined 60W amplifiers. The 10W RF input from the driver U501 is applied to a 70.7 ohm Wilkinson splitter and then to the gate of each MOSFET amplifier. The 60W outputs on the drain of the amplifiers are combined using a Wilkinson combiner. Q502 has a half-wave transmission line on the input and Q503 has a half-wave on the output. These T-lines are used to drive the 60W amplifiers out of phase. The output of the combiner is fed from WO513 directly to the forward/reverse power detect board.

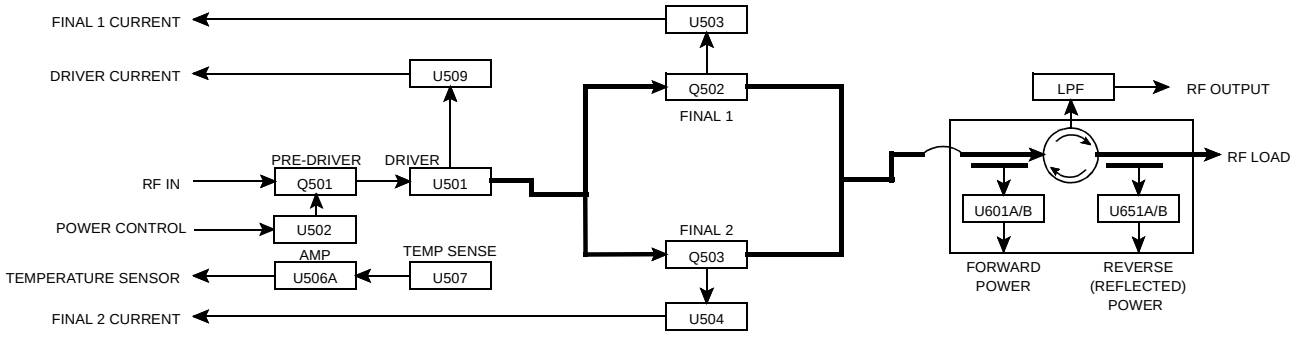

Figure 2 125W POWER AMPLIFIER BLOCK DIAGRAM

The Wilkinson splitter and combiner provide the capability to split the drive input and combine the final outputs while maintaining isolation between the two final amplifiers. The combiner consists of two quarter-wave transmission lines and a balancing resistor. During normal operation, a signal of relatively equal phase and amplitude is present on both ends of the balancing resistor. Therefore, no current flows and no power is dissipated in the balance resistor. If one final failed, the other final of a pair would continue to function.

POWER DETECTORS

The supply current is monitored through a resistor that creates a current output level indicative of the power output. The outputs of U503 and U504 are monitored by software through the RF Interface Board. If a final amplifier fails, the software will reduce the output power to prevent over-driving the remaining final amplifier.

THERMAL SENSOR

Thermal protection is provided by temperature sensor U507. The operating range of the sensor is from -30° C to 100° C (-22° F to 212° F). Amplifier U506A sends the output of U507 through WO509 to the RF Interface Board. The RF Interface Board reduces the power amplifier to half power (via the MPC) if the temperature reading is too high and turns the fan on and off (not via the MPC). The fan is turned on at approximately 50°C and off again at 42°C.

FORWARD/REVERSE POWER DETECT, CIRCULATOR, LOW-PASS FILTER

The power amplifier output is directly coupled to the forward/reverse power detect board via a jumper. The output then enters the circulator and exits to the low-pass filter board and the antenna jack for a minimum power output of 125W. The low-pass filter board provides rejection of harmonics of the fundamental transmitter frequency and spurious signals to ensure that the equipment meets emission specifications. If an antenna is not connected, the circulator connects the output power to R668.

Forward and reverse power are electromagnetically coupled from the input and reflected ports of the circulator. RV601/RV602 calibrate the forward and reverse sense levels. The sensed levels are coupled to the RF Interface Board and software.