Raymarine

RAY101 THEORY OF OPERATIO, Ver 1.0

This PLL - controlled VHF marine transceiver provides an accurate and stable multi-channel operation.

The transceiver consists of 6 main sections:

- **Transmitter**
- **Receiver**
- **Low voltage detection**
- **Weather alert**
- **Local Oscillator PLL (Phase Lock Loop) Circuit**
- **Memory backup**

- **Transmitter**

  The audio is picked up from the internal MIC. The audio signal is then amplified by Audio Amplifier, IC7 LM324 (4/4), IC7 (3/4) and filtered by a low pass filter IC7 (2/4). The audio is adjusted with VR3 to obtain a suitable Audio frequency response, and then modulated with the carrier by VCO, through Varicap (D8).

  The modulated signal output from the VCO is pre-amplified by Q3, Q4 and Q2. Then it is amplified by Q19, Q20 .The amplified signal then passes through a low -pass filter network which consists of L3, L6, C19, C91, C98 filters out spurious emission, and the antenna switching circuit, D1, D2. The signal is filtered by another low-pass filter circuit which is consists of C1, C4, C5, C11, C16, L1, L2. These low pass filters are necessary to suppress the second and third harmonics. The signal is then fed into the antenna input and radiated out. The signal is also fed into another path consisting of C88, D5, R47 for sampling, and is converted into a direct current voltage for the Automatic power control (APC) circuit IC1, Q6, Q9, VR1, VR5.

  When the unit is transmitting, the audio signal is added to the TX VCO Varicap D8. The capacitance of D8 is varied following the audio signal and when mixed with the carrier to form the modulated signal.

- **Receiver**

  The receiver uses a double frequency super-heterodyne circuit. The first Immediate Frequency (IF) is 21.4 MHz and the second is 450 kHz.

The RF signal is received by the antenna, and passes through a low-pass filter network C1, C4, C5, C10, C11, C16, L1, L2, L5 to filter out the unwanted signals, the antenna switching circuit D1 switching circuit to receive. The received RF signal then passes through a SAW filter F4. And is amplified by RF amplifier Q5. The amplified RF signal passes through another SAW filter F5. The RF signal then is mixed with the local oscillation frequency by the mixer Q18. A first IF (Immediate Frequency) 21.4 MHz is produced. The IF is passed through a pair of crystal filter F1 (1/2), F2 (2/2) to further filter other unwanted signals. The first IF then is amplified by Q1 and the IF amplifier IC3 (BA4116). IC3 is a integrated RF amplifier which is consists of a local oscillator, a demodulator, a second mixer, squelch control circuit, and RF amplifier. The 21.4 MHz IF then is mixed here with second mixer and converted into 2nd Immediate Frequency (IF) 450 kHz. The 2nd IF passes through a ceramic filter F3 to filter out the residue unwanted signal at pin 5 of IC4 (BA4116) output this final IF signal and the Audio signal is output at pin 9 of IC3 (BA4116).

The audio signal is fed through a volume control VR6 and finally amplified by Audio amplifier IC2 (NJM2070) and heard in the speaker.

The squelch control is also controlled by IC3 (BA4116). The second IF passes through IC3 (BA4116) internal squelch control R114, C164, C165 to form a squelch amplifier. The ceramic filter produces a squelch signal (RF noise). Pin 14 of IC3 sends the digital squelch control signal to the CPU to mute the audio speaker path. Pin 12 of IC3 outputs a RSSI level to the CPU.

- **Low Voltage Detection**

  The battery voltage, divided by R21 and R22 is input to IC5 Pin 41 for voltage level sample.

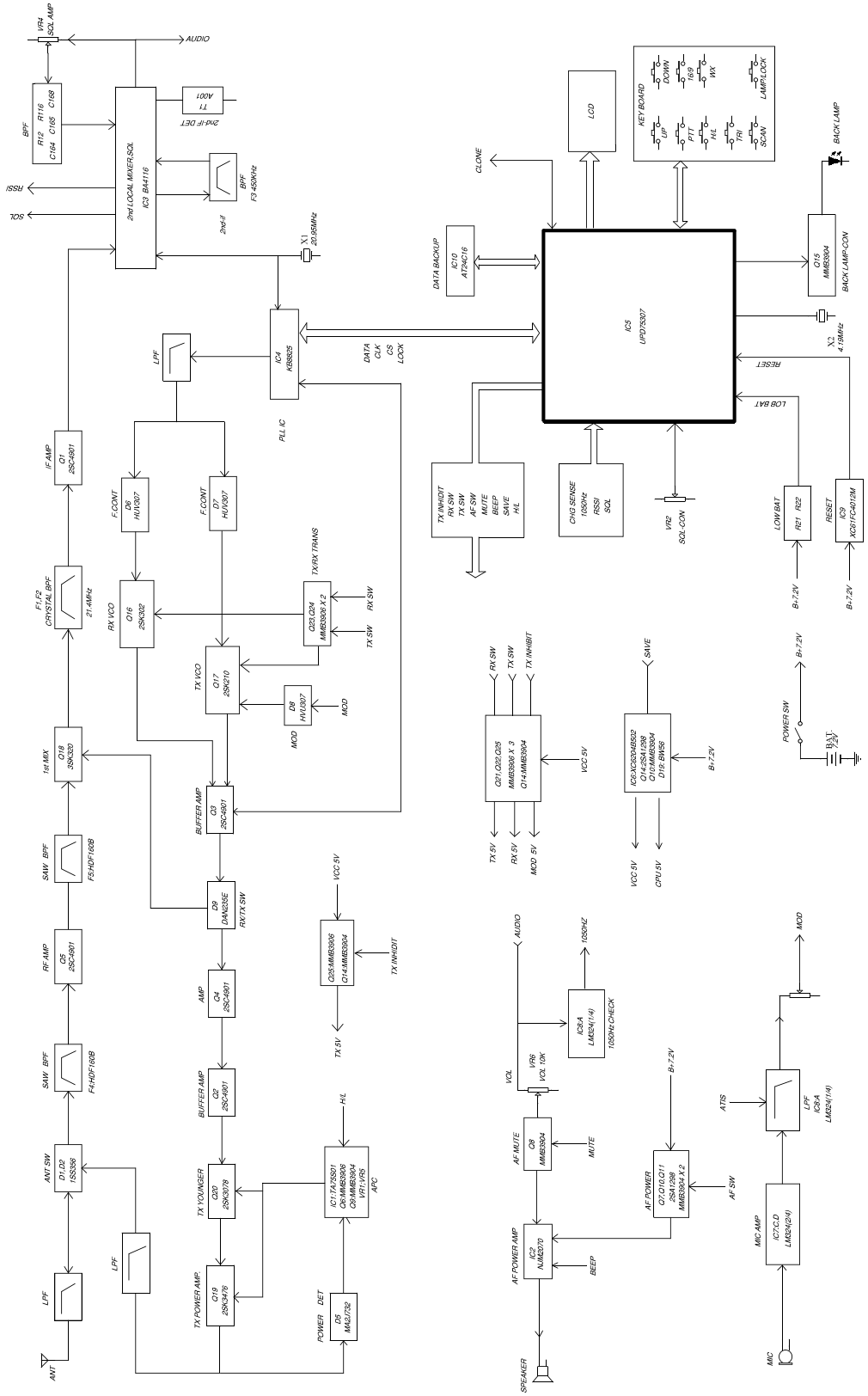
- **Weather alert**

  The weather signal pass through a band pass filter which is consist of IC8(B,C,D) LM324, and is reshaped by IC8A LM324, Then, it is detected by IC5 UPD789407.

- **PLL (Phase Lock Loop) Circuit:**

  The receiver and transmitter both share the same PLL (Phase Lock Loop) Circuit to produce the carrier or the receive frequency. The local oscillator consists of a fundamental frequency oscillator X1 20.95MHz and IC4 (KB8825). A phase Lock Loop (PLL) IC4 (KB8825), TX VCO Q17 and RX VCO Q16. The fundamental frequency is frequency divided by IC4 and a 25 kHz signal is produced. When the VCO frequency applied to and frequency divided by IC4 produces a frequency comparable to 25 kHz, PLL will

BLOCK DIAGRAM



control the VCO. When these two frequencies are matched, a constant control voltage is output from PLL to lock VCO in desired frequency. The PLL will also output a lock indication to CPU to indicate the PLL is in frequency lock state.

- **Memory Backup**

  IC10 is an EEPROM AT24C16 which acts as a memory backup for the working channel code and the system parameters. Every time when the unit is switched on, the CPU will reset the system, clear the RAM, and recall in the memory from the EEPROM to refresh the RAM in MCU .