ALARM DEVICE MANUFACTURING COMPANY
160 Eileen Way Syosset, N.Y. 11791

EXHIBIT 2

Technical Description

Block Diagrams

Schematics

Para. 2.1033 (b) (4) and (5)

SPREAD SPECTRUM TRANSMITTER

TRANE WIRELESS ZONE SENSOR

MODEL 7722TX

BLOCK DIAGRAM DESCRIPTION

BATTERY (BAT)

Two 3 volt, 2/3 lithium batteries are used to provide 6.0 volts to the transmitter.

ELECTRONIC ERASABLE PROGRAMABLE READ ONLY MEMORY (EE PROM)

The EE PROM is a 256 x 8 memory unit used to store calibration values, frequency modulation values and temperature data processing algorithms.

4 VOLT REGULATORS (x 2 4V REG)

Two 4 v linear regulators are used to provide the necessary regulated voltage to all circuits. Mainly, one is dedicated to power the RF circuitry and the other to power digital and analog circuitry.

ANALOG CIRCUITRY

The analog circuitry provides the initial processing functions for the temperature data. It consists basically of three operational amplifiers, one to provide buffering and gain and the other two are used as a fine and coarse channel for the analog to digital converter.

COMPLEX PROGRAMABLE LOGIC DEVICE (CPLD)

The CPLD provides the PN sequence to the BPSK MODULATOR for carrier signal spreading and the data to be transmitted in digital form to the digital to analog converter.

MICROPROCESSOR (MICRO)

The micro initiates control signals, processes temperature data and user requests. I/O is typically 0 to 6 volts.

DIGITAL TO ANALOG CONVERTER AND LOW PASS FILTER (D TO A & L.P.F.)

The D TO A & L.P.F. is used to convert the digital data out of the CPLD to analog form which is then used to steer and frequency modulate the reference oscillator. An active low pass filter follows the output of the D TO A to prevent any high frequency noise out of the CPLD from getting to the reference oscillator.

CRYSTAL REFERENCE OSCILLATOR (XTAL REF OSC)

The reference oscillator provides a 7.12 MHz signal which is used by the phase locked loop circuit as a stable reference frequency source. It is also used by the CPLD as a clock source to generate the PN SEQUENCE.

PHASE LOCKED LOOP (PLL)

The PLL is an integrated circuit containing all the basic functions required to form a phase locked loop circuit (vco, phase detector/charge pump, modulus prescaler).

HARMONIC LOW PASS FILTER (HARM. L.P.F.)

The harmonic low pass filter is a three element pi configuration used to remove unwanted harmonic signals from the synthesized carrier signal.

BI-PHASE SHIFT-KEYED MODULATOR (BPSK MOD)

The BPSK MODULATOR is an integrated Gilbert cell multiplier used to combine the digital PN SEQUENCE code from the CPLD with the 9 11.36/9 18.537 MHz FM signals from the PLL to produce a spread spectrum waveform.

PRE AMPLIFIER (PRE AMP)

The pre amp is used to provide 15 dB gain to drive the power amplifier.

POWER AMPLIFIER (POWER AMP)

The power amplifier provides an additional 8 dB gain to increase the transmitted power to approximately +21 dbm.

LOW PASS FILTER (L.P.F.)

The low pass filter is a three element pi configuration used to remove unwanted harmonic signals from the final carrier signal before reaching the antenna.

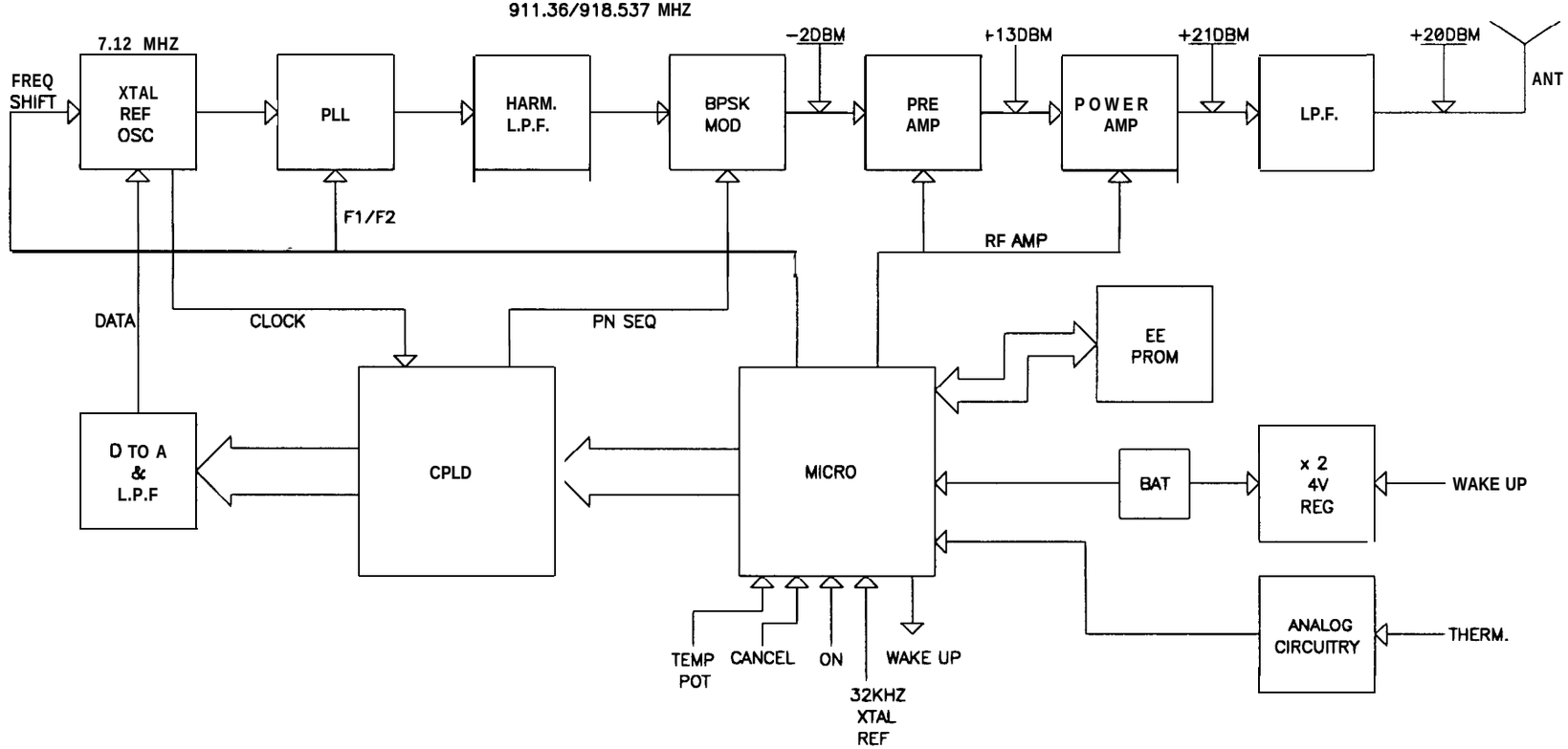
ANTENNA (ANT)

The antenna used is a simple ¼ wavelength monopole which has been folded so as to achieve a nearly omnidirectional pattern in a minimum space. The antenna works in conjunction with the printed circuit board ground plane, having particular dimensions and orientation. The antenna is printed directly on the board and is not removable. Use of this antenna and ground plane produces vertical RF propagation from a horizontally mounted antenna, provides a nearly 50 ohm input impedance around the 902-928 MHz operating frequency, and significantly attenuates signal propagation for frequencies below 700 MHz.

ASSY REV	DESCRIPTION	APPROMD	DATE

TRANE TRANSMITTER

911.36/918.537 MHZ



APPROVALS	DATE
DRAWN BY G.B.	11/4/99
CHECKED BY D.O.	11/4/99
APPROVED BY D.O.	11/4/99

ADEMCO [illegible] E N W A Y
SYOSSET, NEW YORK 11791

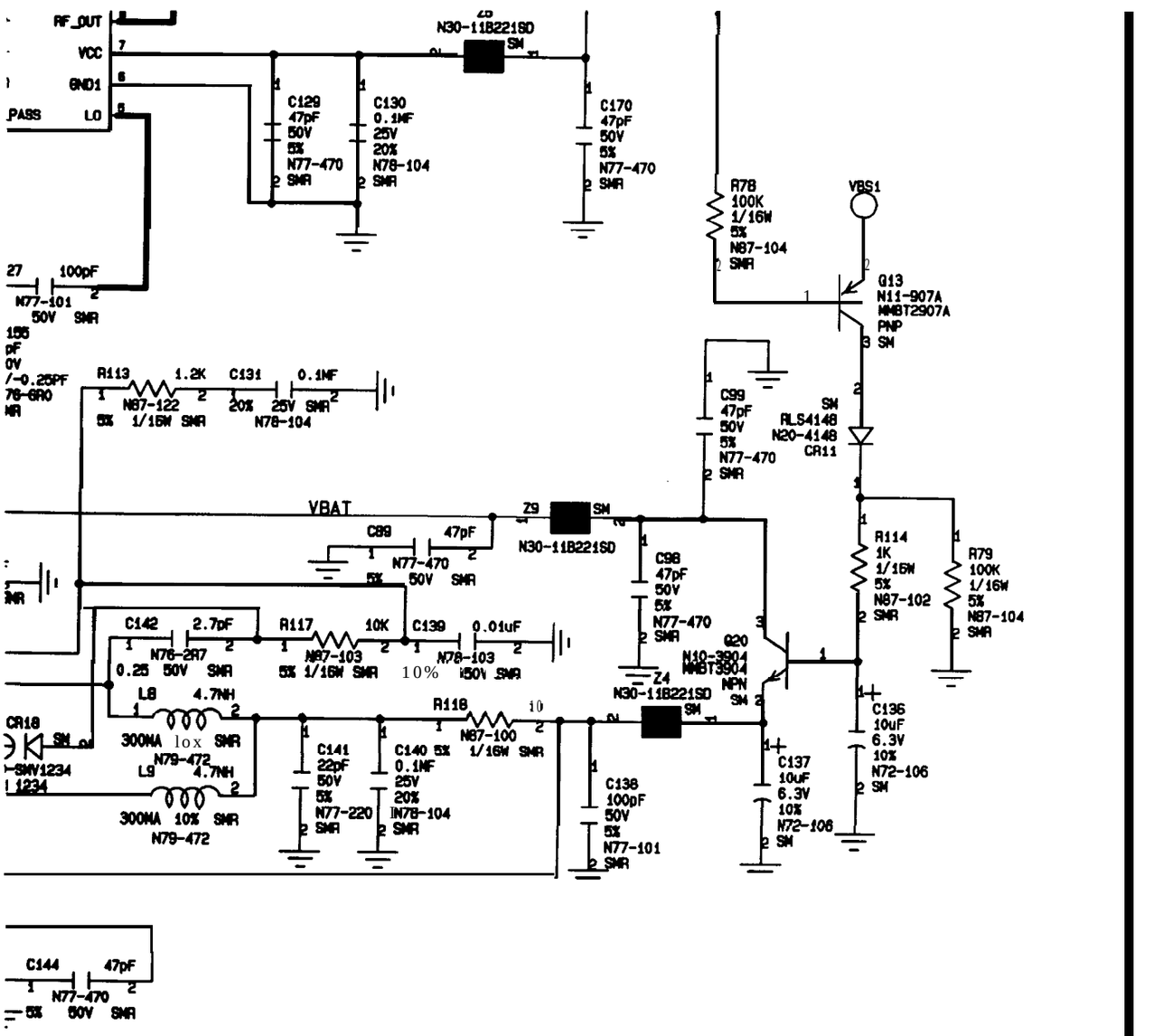
PCB (REF)

TITLE TRANE TRANSMITTER

DRAWING NUMBER

COMPUTER FILE NAME 7722TXBLOCK.SCH (ACCEL)

DATE: 11/4/99 | SHEET 1 OF 1



VALS	DATE
ZANO	2/96

ADEMCO 165 EILEEN WAY
SYOSSET, NEW YORK 11791

PCB (REF) N7440V3.PCB

TITLE TRANE, LOW-COST TRANSMITTER

DRAWING NUMBER SA7722TX

COMPUTER FILE NAME SA7722TX.SCH

DATE: 2/12/96 SHEET 1 OF 1

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EXHIBIT 3

Report of Measurements

Para. 2.1033 (b) (6)