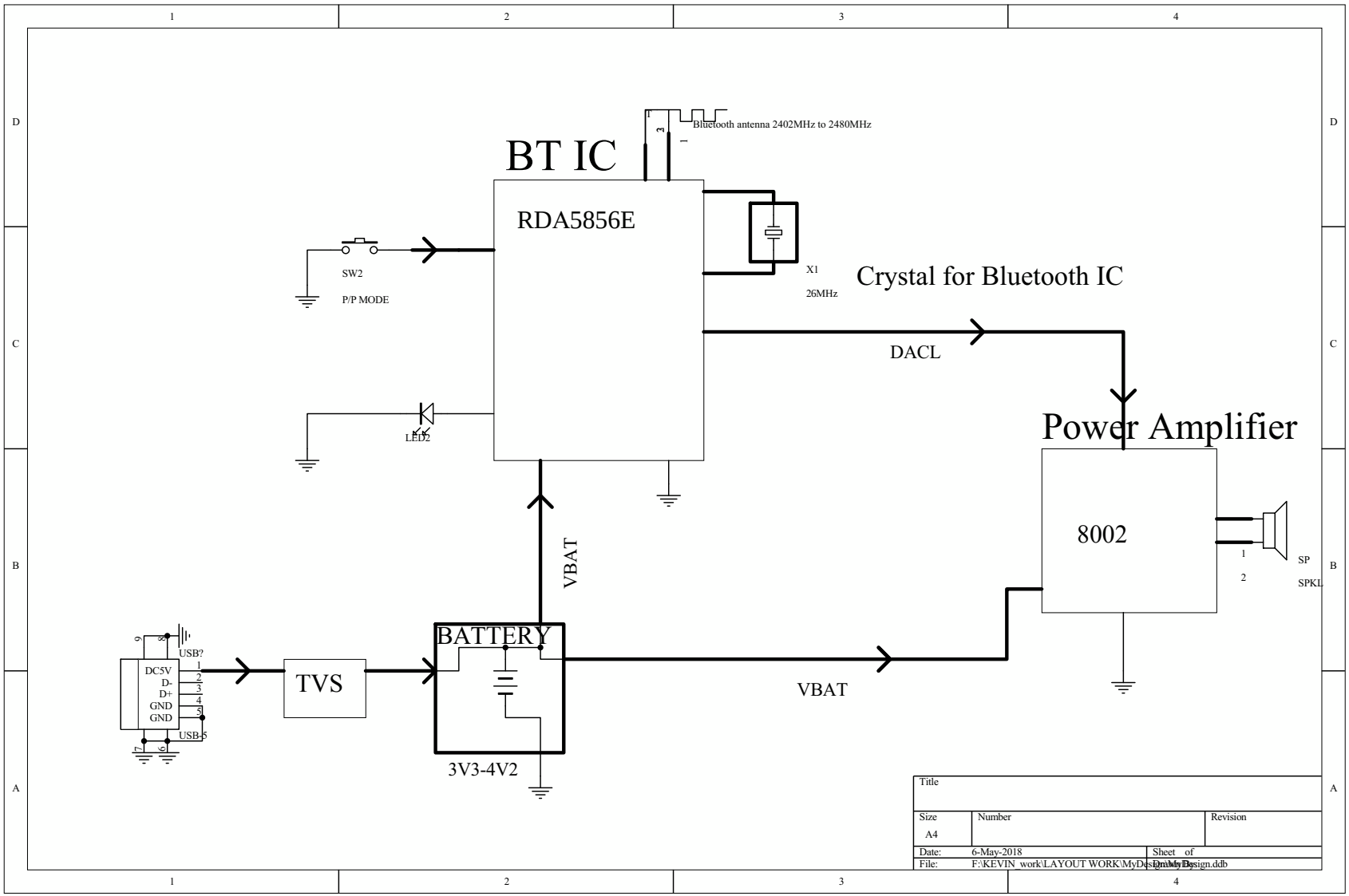
U12


BT IC
RDA5856E
Bluetooth antenna 2402MHz to 2480MHz
SW2
P/P MODE
LED2
X1
26MHz
Crystal for Bluetooth IC
DACL
Power Amplifier
8002
SP
SPKL
VBAT
BATTERY
3V3-4V2
TVS
USB?
DC5V
D-
D+
GND
GND
USB-5
VBAT
Title
Size
A4
Number
Revision
Date:
6-May-2018
Sheet of
File:
F:\KEVIN_work\LAYOUT WORK\MyDesign\MyDesign.ddb
Drawn By:

3. Function Block Diagram

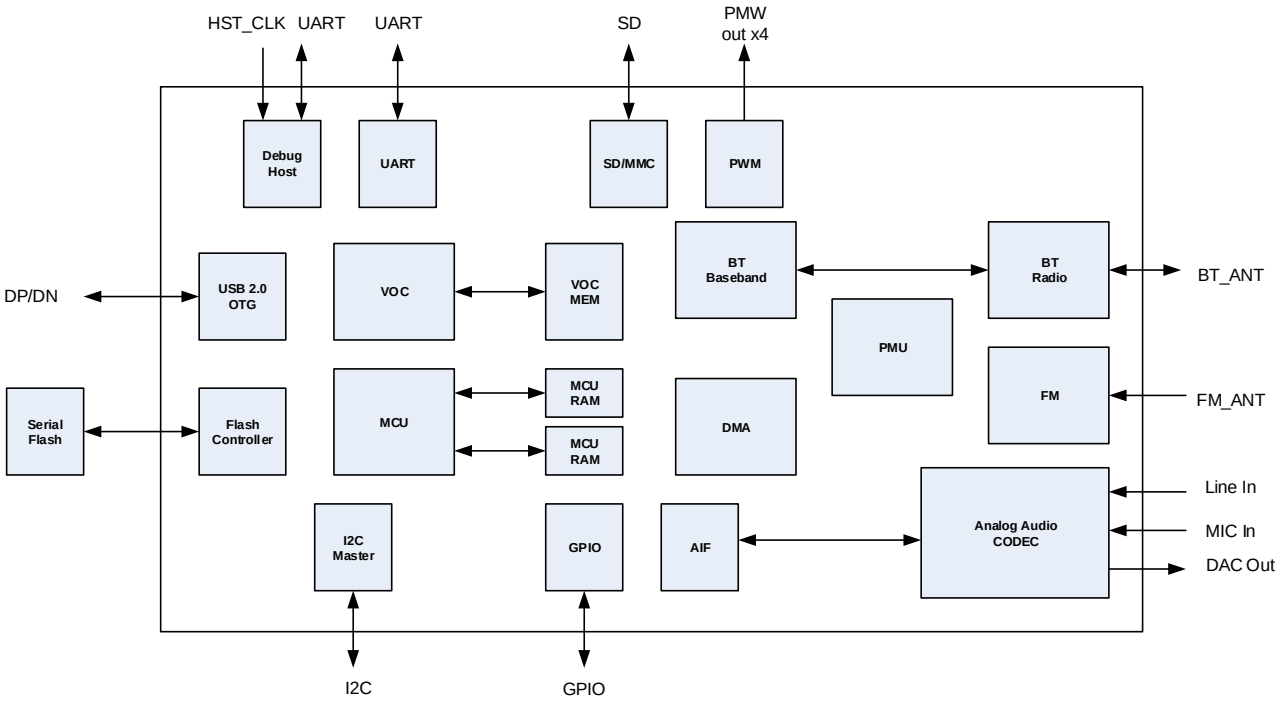


Figure 2 RDA5856TE Block Diagram

4. Clock and reset

RDA5856TE has a reference clock input from either a crystal or an external clock source. There are two internal PLL which use XTAL clock as reference. They are used for system and audio applications.

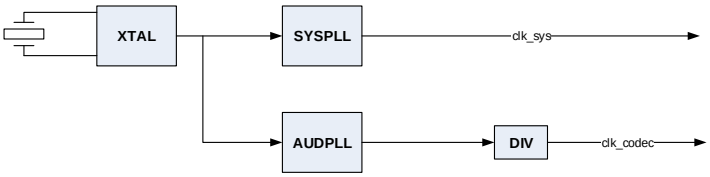


Figure 3 Clock Structure

RDA5856TE has several reset sources, as following:

- POR
  Entire SoC is reset after power supply ramping from 0v to VBAT.
- External Pin Reset
  Entire SoC is reset except PMU.
- Warm Reset
  - ✓ Global soft reset
    DBB can be reset by set soft reset register in system control register map.
  - ✓ Watch Dog Reset
    DBB will be reset when watch dog timer expired.

5. MCU

RDA RISC is a 16/32-bits processor which using a Reduced Instruction Set Architecture, an efficient 6-stage instruction pipeline, it provides high performance to the system.

- RDA RISC Core.
  - ✓ 32x32-bit Multiplier.