3.GPRS module part:

3.1 RF Receiver Operation

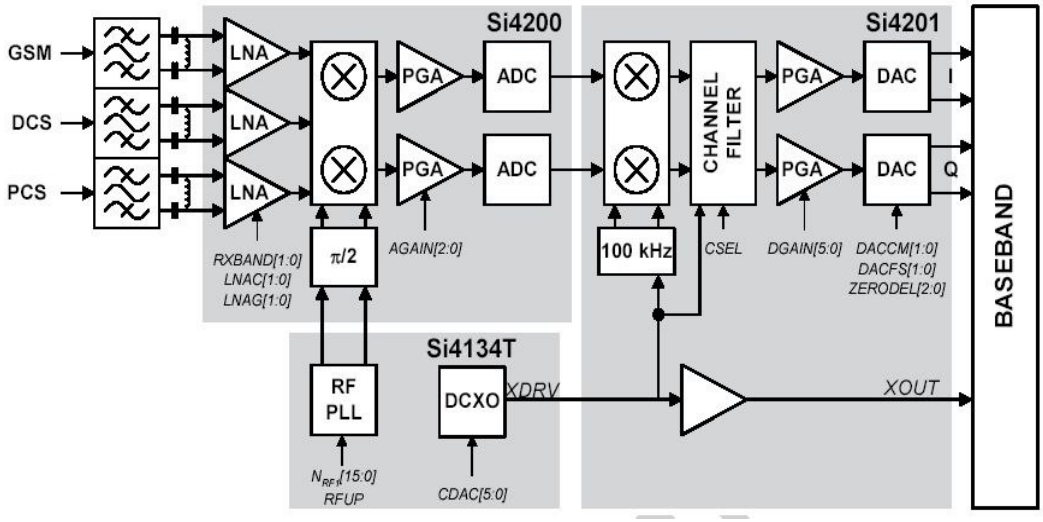

Fig 51

The Aero+ transceiver uses a low-IF receiver architecture that allows for the on-chip integration of the channel selection filters.

The Si4200 integrates three differential-input LNAs. The LNA amplifies the RF signal after selection by the T/R switch and RF saw filter before the signal enters the first mixer section. The LNA inputs are matched to the 200Ω balanced output SAW filters through external LC matching networks.

A mixer downconverts the RF signal to a 100 kHz intermediate frequency (IF) with the RFLO from the Si4134T frequency synthesizer. The RFLO frequency is between 1737.8 and 1989.9 MHz, and is divided by two in the Si4200 for EGSM 900 modes. The mixer output is amplified with an analog programmable gain amplifier (PGA), which dynamic range is 16 dB and gain step is 4 dB.

The quadrature IF signal is digitized with high resolution A/D converters (ADCs). The Si4201 downconverts the ADC output to baseband with a digital 100 kHz quadrature LO signal. The digital output is scaled with a digital PGA, which

dynamic range is 63 dB and gain step is 1 dB. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP and RXQN pins to interface to standard analog-input baseband ICs.

3.2 Transmitter Operation

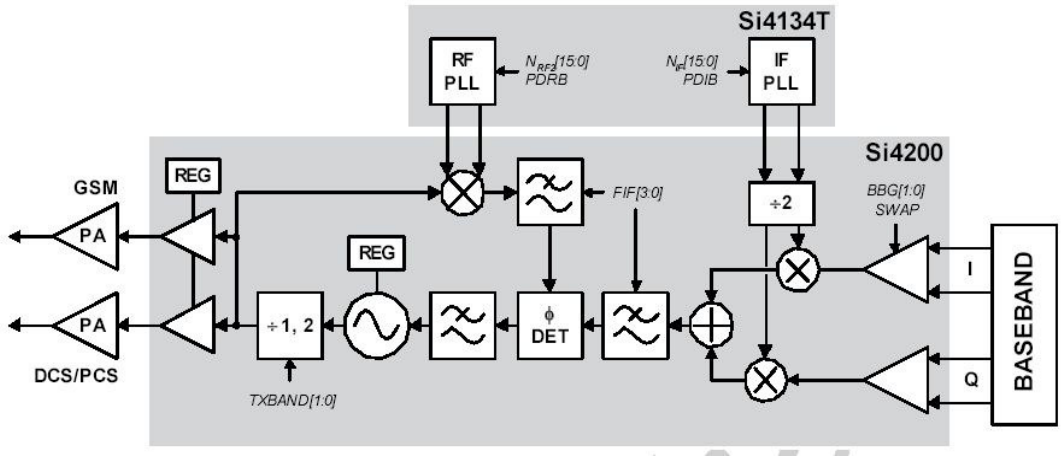

Fig 52

The transmitter chain converts differential IQ baseband signals to a suitable format for transmission by a power amplifier.

The transmit (TX) section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL) and two 50 Ω output buffers that can drive external power amplifiers (PA), one for the EGSM and one for the DCS 1800 band. A quadrature mixer upconverts the differential in-phase (TXIP, TXIN) and quadrature (TXQP, TXQN) signals with the IFLO to generate an IF signal which is filtered and used as the reference input to the OPLL. The Si4134T generates the IFLO frequency between 766 and 896 MHz. The IFLO is divided by two to generate the quadrature LO signals for the quadrature modulator, resulting in an IF between 383 and 448 MHz.

The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. The TXVCO is centered at DCS 1800 bands, and its output is divided by two for the E-GSM 900 band. The Si4134T generates the RFLO frequency between 1272 and 1483 MHz. To allow a single VCO to be used for the RFLO, high-side injection is used for the E-GSM 900 bands, and low-side injection is used for the DCS 1800 band.

The RF signal is then amplified by PA and power control loop to the assigned power level within the burst.

3.3 Circuit Operation Theory (BaseBand)

3.3.1 Introduction:

P50 utilizes TI's chipsets (CALYPSO and IOTA) as base-band solution. Base-band is composed with two potions: Logic and Analog/Codec. CALYPSO is a GSM/GPRS digital base-band logic solution included microprocessor, DSP, and peripherals. IOTA is a combination of analog/codec solution and power management which contain base-band codec, voice-band codec, several voltage regulators and SIM level shifter etc. In addition, 56F05 integrates with other features such as LED backlight, color LCD display , CLI, vibration, buzzer and charging etc. The following sections will present the operation theory with circuitry and descriptions respectively.

3.3.2 Block Diagram

3.3.2.1 CALYPSO (HERCROM40)

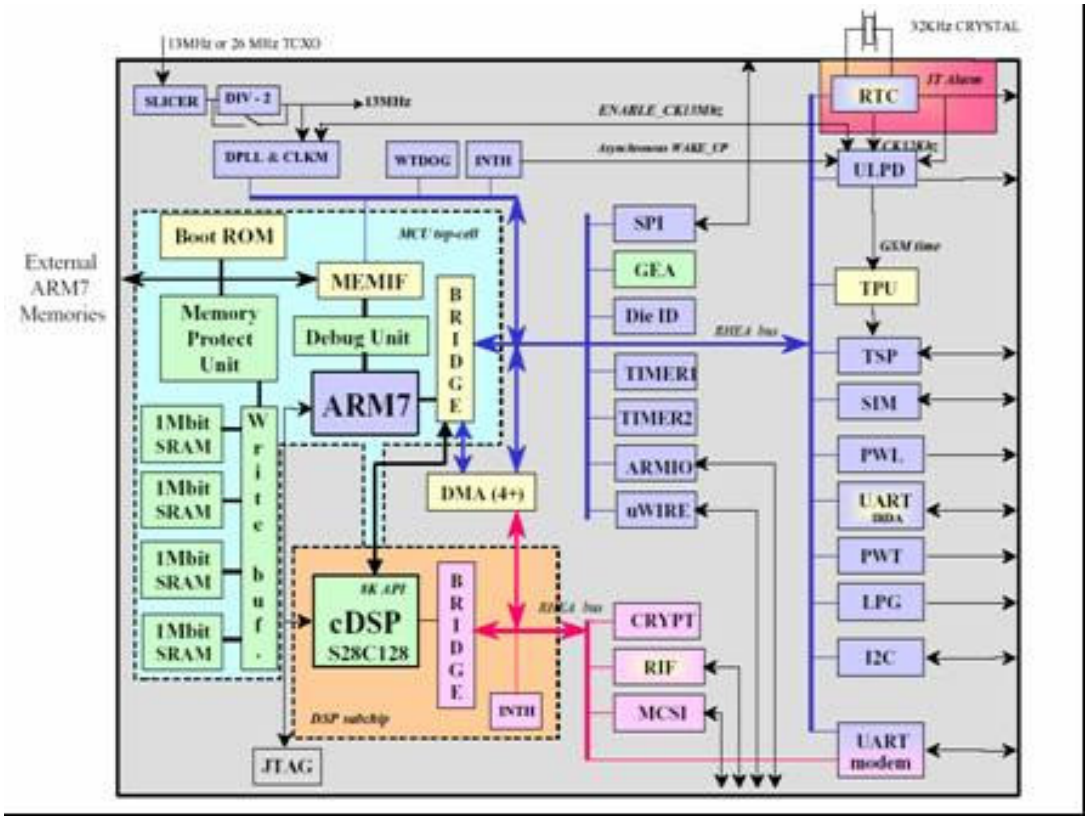

Fig 53

3.3.2.2 IOTA

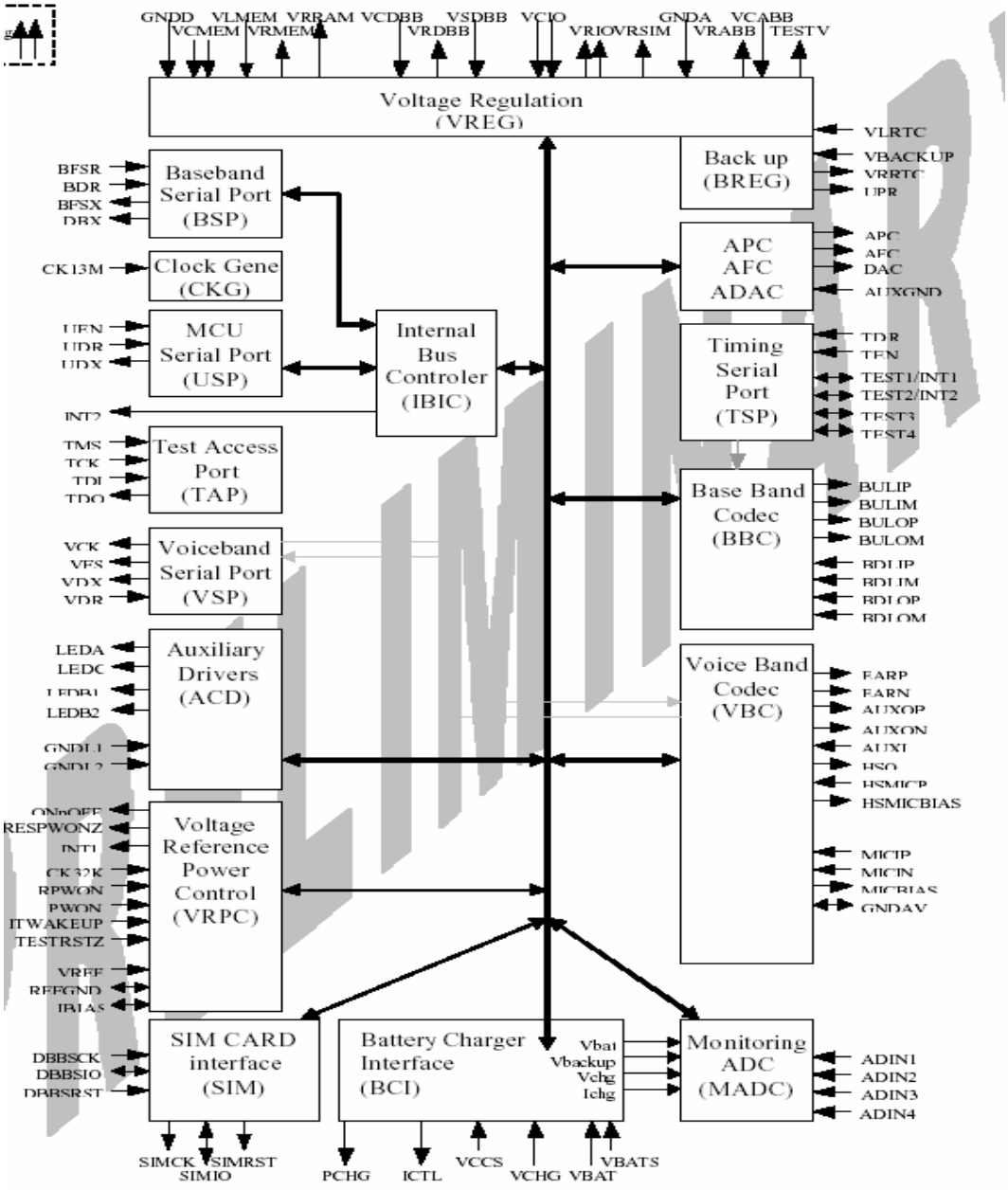

Fig 54

3.3.3 Operation theory

3.3.3.1 Calypso

CALYPSO (HERCROM400) is a chip implementing the digital base-band processor of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro-Controller core with emulation facilities (ARM7TDMIE) and an internal 4M-bit RAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates.

Major functions of this chip are as follows:

3.3.3.1.1 Real Time Clock (RTC)

The RTC block is an embedded RTC module fed with an external 32.768KHz Crystal. Its basic functions are:

1. Time information (seconds/minutes/hours)
2. Calendar information (Day/Month/Year/ Day of the week) up to year 2099
3. Alarm function with interrupts (RTCINT is generated to wake up ABB)
4. 32KHz oscillator frequency gauging

3.3.3.1.2 Pulse Width Light (PWL)

This module allows the control of the backlight of LCD and keypad by employing a 4096 bit random sequence.

3.3.3.1.3 MODEM-UART

This UART interface is compatible with the NS 16C750 device which is devoted to the connection to a MODEM through a standard wired interface. The module integrates two 64 words (9 and 11 bits) receive and transmit FIFOs which trigger levels are programmable. All modem operations are controllable either via a software interface or using hardware flow control signals. In 56F05, we

implement software flow control by only two signals: TXD0 and RXD0.

3.3.3.1.4 I2C master serial interface (I2C)

The I2C (Philips standard) is a half-duplex serial port using 2 lines (data and clock) for data transmission with software addressable external devices. In 56F05, we employ I2C bus to control CLI in LCD module.

The I2C signals are defined as follows:

I2C_SCL: programmed to the fast transmission mode (400KHz)

I2C_SDA: the serial bi-directional data of the LCM controller

3.3.3.1.5 General Purposes I/O (GPIO)

Calypso provides 16 GPIOs configurable in read or write mode by internal registers. In 56F05, we utilize 13 of them as follows:

IO0: N/A

IO1: Control audio amplifier; 'H'：enable, 'L'：disable

IO2: Interrupt from Melody IC

IO3: Over-discharge indicator control

Indicator for Low / High battery voltage while charging;

'H'：High battery voltage(>3.2V) , LEDs ON/OFF by Calypso ;

'L'： Low battery voltage(<3.2V), LEDs always ON

IO4: SW confirm handfree plugged-in and enable send/end detection

'H'：No send/end key detection allowed;

'L'： Enable send/end key function of handfree

IO5: SIM power control

IO6: Detection of earphone or download cable plugged-in

'H'：no accessory plugged-in

'L'： accessory plugged-in

IO7: Reset of external device: For 56F05, melody IC and CSTN

IO8: N/A

IO9: Backlight of CSTN :'H'：ON ,'L'：OFF

IO10: N/A

IO11: Switch of data service and audio path of earphone

IO12: Selection of melody via headset or speaker; 'H'：speaker, 'L':handfree

IO13: N/A

IO14: SRAM high-byte enable

IO15: SRAM low-byte enable

3.3.3.1.6 Serial Port Interface (SPI)

The SPI is a full-duplex serial port configurable from 1 to 32 bits and provides 3 enable signals programmable either as positive or negative edge or level sensitive. This interface is working on 13MHz and is used for the GSM/GPRS baseband and voice A/D, D/A with IOTA

3.3.3.1.7 Memory Interface and internal Static RAM

For external memory device (Flash and SRAM), this interface performs read and write access with adaptation to the memory width. It also provides 6 chip-select signals corresponding each to an address range of 8 mega bytes. One of these chip-select is dedicated to the selection of an internal memory. In 56F05, we employ NCS0 (NROMCS0) for external Flash and NCS2 (NRAMCS) for external SRAM.

A 4Mbit SRAM is embedded on the die and memory mapped on the chip-select nCS6 of the memory interface. The access cycle is guaranteed with 0 wait-state for any cycle frequency up to 39MHz.

3.3.3.1.8 SIM Interface

The Subscriber Identity Module interface will be fully compliant with the GSM 11.11 and ISO/IEC 7816-3 standards. Its external interface is 3 Volts only. 5 Volts adaptation will be based on external level shifters.

3.3.3.1.9 JTAG

In 56F05, JTAG is used for software debugging.

3.3.3.1.10 Time Serial Port (TSP)

The TPU is a real-time sequencer dedicated to the monitoring of GSM/GPRS baseband processing. The TSP is a peripheral of the TPU which includes both a serial port (32 bits) and a parallel interface. The serial port can be programmed by the TPU with a time accuracy of the quarter of GSM bit. The serial port is uni-directional (transmit only) when used with IOTA. The serial port provides 4 enable signals programmable either as positive or negative edge or level sensitive. This serial port is derived from 6.5MHz and used to control the real time GSM windows for the baseband codec and the windows for ADC conversion.

3.3.3.1.11 TSP Parallel interface (ACT)

The parallel interface allows control 13 external individual outputs and 1 internal signal with a time accuracy of the quarter of GSM bit. These parallel signals are mainly used to control the RF activity. In 56F05, we employ 5 of them to control RF activity.

TSPACT1: Band selection 1 (BS1)

TSPACT2: Band selection 2 (BS2)

TSPACT6: PA enable

TSPACT9: Aero+ enable

TSPACT10: Aero+ programming enable

3.3.3.1.12 Radio Interface (RIF)

The RIF (Radio Interface) Module is a buffered serial port derived from the BSP peripheral module of the defined for TMS320C5X. The external serial data transmission is supported by a full-duplex double-buffered serial port interface. The interface is used for transfer of baseband transmit and receive data and also to access all internal programmation registers of the device.

3.3.3.1.13 Miscellaneous:

Some important Baseband /RF interface signals are defined as follows:

CLKTCXO: 13MHz VTCXO Clock from RF circuit

TCXOEN: 13MHz VTCXO Clock Enable signal

3.3.3.2 IOTA

Together with a digital base-band device (Calypso), IOTA is part of a TI DSP solution intended for digital cellular telephone applications including GSM 900, DCS 1800 and PCS 1900 standards (dual band capability).

It includes a complete set of base-band functions to perform the interface and processing of voice signals, base-band in-phase (I) and quadrature (Q) signals which support single-slot and multi-slot mode, associated auxiliary RF control features, supply voltage regulation, battery charging control and switch ON/OFF system analysis. IOTA interfaces with the digital base-band device through a set of digital interfaces dedicated to the main functions of CALYPSO, a base-band serial port (BSP) and a voice-band serial port (VSP) to communicate with the DSP core (LEAD), a micro-controller serial port to communicate with the micro-controller core and a time serial port (TSP) to communicate with the time processing unit (TPU) for real time control.

IOTA includes also on chip voltage reference, under voltage detection and power-on reset circuits.

Major functions of this chip are as follows:

3.3.3.2.1 Baseband Codec (BBC)

The baseband codec includes a two-channel uplink path and a two-channel downlink path.

The baseband uplink path (BUL) modulates the bursts of data coming from

the DSP via the baseband serial port (BSP) and to be transmitted at the antenna. Modulation is performed by a GMSK modulator. The GMSK modulator implemented in digital technique generates In-phase (I) and Quadrature (Q) components, which are converted into analog base-band by two 10 bits DACs filters. It also includes secondary functions such as DC offset calibration and I/Q gain unbalance.

The baseband downlink path (BDL) converts the baseband analog I & Q components coming from the RF receiver into digital samples and filters these resulting signals through a digital FIR to isolate the desired data from the adjacent channels. During reception of burst I & Q digital data are sent to the DSP via the baseband serial port (BSP) at a rate of 270 KHz.

3.3.3.2.2 Automatic Frequency control (AFC)

The automatic frequency control function consists of a digital to analog converter optimized for high resolution DC conversion. Its purpose is to control the frequency of the GSM 13MHz oscillator to maintain mobile synchronization on the base station and allow proper transmission and demodulation.

3.3.3.2.3 Automatic Power Control (APC)

Purpose of the Automatic Power Control (APC) is to generate an envelope signal to control the power ramping up, ramping down and power level of the radio burst.

The APC structure is intended to support single slot and multi-slots transmission with smooth power transition when consecutive bursts are transmitted at different power level. It includes a DAC and a RAM in which the shape of the edges (ramp-up and ramp-down) of the envelope signals are stored digitally. This envelope signal is converted to analog by a 10 bits digital to analog converter. Timing of the APC is generated internally and depends of the real time signals coming from the TSP and the content of two registers which control the relative position of the envelope signal versus the modulated I & Q.

3.3.3.2.4 Time serial port (TSP)

Purpose of the time serial port is to control in real time the radio activation windows of IOTA which are BUL power-on, BUL calibration, BUL transmit, BDL power-on, BDL calibration and BDL receive and the ADC conversion start.

These real time control signals are processed by the TPU of DBB and transmitted serially to ABB via the TSP, which consists in a very simple two pins serial port. One pin is an enable (TEN) the other one the data receive (TDR). The master clock CK13M divided by 2 (6.5MHz) is used as clock for this serial port.

3.3.3.2.5 Voice band Codec (VBC)

The VBC processes analog audio components in the uplink path and transmits this signal to DSP speech coder through the voice serial port (VSP). In the downlink path the VBC converts the digital samples of speech data received from the DSP via the voice serial port into analog audio signal. Additional functions such as programmable gain, volume control and side-tone are performed into the voice band codec.

3.3.3.2.6 Micro-controller serial port (USP)

The micro-controller serial port is a standard synchronous serial port. It consists in three terminals, data transmit (UDX), data receive (UDR) and port enable (UEN). The clock signal is 13MHz clock. The USP receives and sends data in serial mode from and to the external micro-controller and in parallel mode from and to the internal GSM Baseband a Voice A/D D/A modules. The micro-controller serial port allow read and write access of all internal registers under the arbitration of the internal bus controller.

3.3.3.2.7 SIM card shifters (SIMS)

The SIM card digital interface in ABB insures the translation of logic levels between DBB and SIM card, for transmission of 3 different signals; a clock

derived from a clock elaborated in DBB, to the SIM card (DBBSCK➔SIMCLK). a reset signal from DBB to the SIM card (DBBSRST➔SIMRST), and serial data from DBB to SIM card (DBBSIO➔SIMIO) and vice-vera.

The SIM card interface can be programmed to drive a 1.8V and 3 V SIM card

3.3.3.2.8 Voltage Regulation (VREG)

Linear regulation is performed by several low dropout (LDO) regulators to supply analog and digital baseband circuits.

(1) LDO VRDBB generates the supply voltage (1.8V, 1.4V,and 1.2V) for the digital core of DBB. In 56F05, it is programmed to 1.8V. This regulator takes power from the battery voltage

(2) LDO VRABB generates the supply voltage 2.8V for the analog function of ABB. It is supplied by the battery.

(3) LDO VRIO generates the supply voltage 2.8V for the digital core of ABB and digital I/O's of DBB and ABB. It is supplied from battery voltage.

(4) LDO VRMEM generates the supply voltages 2.8V for DBB memory interfaces I/O's.

(5) LDO VRRAM generates the supply voltages 2.8V for DBB memory interfaces I/O's

(6) LDO VRRTC generates the supply voltages (1.8,1.4, or 1.2V) and supply voltage 1.4V for the following block of DBB (real time clock and 32K oscillator). It's supplied by UPR

(7) LDO VRSIM generates the supply voltages (1.8V, 2.9V) for SIM card interface I/O's

3.3.3.2.9 Baseband Serial Port (BSP)

The BSP serial interface is used for both configuration of the GSM baseband and voice A/D D/A (read and write operation in the internal registers), and transmission of the radio data to the DSP during reception of a burst by the downlink part of the GSM baseband & voice A/D D/A. Four pins are used by

the serial port: BFSR and BDR for receive, BFSX and BDX for transmit. BDX is the transmitted serial data output. BFSX is the transmit frame synchronization and is used to initiate the transfer of the transmit data. BDR is the received serial input. BFSR is the receive frame synchronization and is used to initiate the reception data.

3.3.3.2.10 Battery charger Interface (BCI)

The main function of the ABB charger interface is the charging control of either a 1-cell Li-ion Battery or 3-serie Ni-MH cell batteries with the support of the micro-controller. The battery monitoring uses the 10 bit ADC converter from the MADC to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage. The magnitude of the charging current is set by the 10 bits of a programming register converted by an 10 bit Digital to Analog Converter, whose output sets the reference input of the charging current control loop. The battery charger interface performs also some auxiliary functions. They are battery pre-charge, battery trickle charge and back-up battery charge if it is rechargeable.

3.3.3.2.11 Monitoring ADC (MADC)

The MADC consists in a 10-bit analog to digital converter combined with a nine inputs analog multiplexer. Out of the nine inputs five are available externally, the four remaining being dedicated to main battery voltage, back up battery voltage, charger voltage and charger current monitoring. On the five available externally three are standard inputs intended for battery temperature, battery type measurements.

3.3.3.2.12 Reference Voltage / Power on Control (VRPC)

An integrated band-gap generates a reference voltage. This reference is available on an external pin for external filtering purpose only. This filtered reference is internally used for analog functions. The external resistor connected between pin

IBIAS and GNDREF sets, from the band-gap voltage, the value of the bias currents of the analog functions. The VRPC block is in charge to control the Power ON, Power OFF, Switch On, and Switch OFF sequences. Even in Switch OFF state some blocks functions are performed. These “permanent” functions are functions, which insure the wake-up of the mobile such as ON/OFF button detection or charger detection. Interrupts are generated at power-down detection of the PWON button and when abnormal voltage conditions are detected.

3.3.3.2.13 Internal bus and interrupt controller (IBIC)

Read and write access to all internal registers being possible via both the BSP and USP, purpose of the internal bus controller is to arbitrate the access on the internal bus and to direct the read data to the proper serial port. During reception of a burst the internal bus controller assign the transmit part of the BSP to the base-band downlink to transfer the I & Q samples to the DSP.

This block also handles the internal interrupts generated by the MADC, BCI and VRPC blocks and generates the micro-controller interrupt signal INT2.