FSC-BW226

Single-Chip 802.11b/g/n 1T1R WLAN with 4.2 Dual Mode Bluetooth Module Datasheet

Version 1.4

Revision History

Version	Data	Notes	
1.0	2017/05/27	Initial Version	Devin Wan
1.1	2017/06/26	Revised some mistakes	Devin Wan
1.2	2018/05/12	1.Modify Bluetooth Version: Upgrade from BT4.0 to BT4.2 2.Modify Pin Definitions and Application Circuit Diagrams	Devin Wan
1.3	2019/03/11	Modify the definition of pins 1, 2, 3, 4: it can be either a serial communication or SPI communication	Fish
1.4	2019/05/24	Add Module accessories（WiFi Antenna）	Devin Wan

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1. INTRODUCTION

Overview

The FSC-BW226 is a highly integrated WiFi + BT Combo module, it features a 2.4GHz ISM RF transceiver, Bluetooth V4.2 baseband controller, single-Chip low power 802.11n WLAN network controller(combines an ARM-cortex M3);With on board antenna for BT(External Antenna is optional); Need external antenna for WIFI or Equipped with the RF Connector, connect to the external antenna.

With Feasycom's Bluetooth stack running on a host, designers can easily customize their applications to support different Bluetooth profiles.

The FSC-BW226 is an appropriate product for designers who want to add wireless capability to their products.

Features

- Bluetooth v4.2, Class 1.5
- COMS MAC,Baseband PHY,and RF in a single-Chip for 802.11 b/g/n compatible WLAN
- UART programming and data interface (baudrate can up to 921600bps)
- PCM/I2S audio interface(BT only)
- I2C/AIO/PIO/PWM/SPI control interfaces
- Postage stamp sized form factor
- Embedded Bluetooth stack profiles support: SPP/iAP,HID,GATT,ANCS etc
- WiFi Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- WiFi : Light Weight TCP/IP protocol
- Support External Antenna
- RoHS compliant

Application

- Wireless POS
- Measurement and monitoring systems
- Industrial sensors and controls
- Analogue and USB Multimedia Dongles
- Asset Tracking

Module picture as below showing

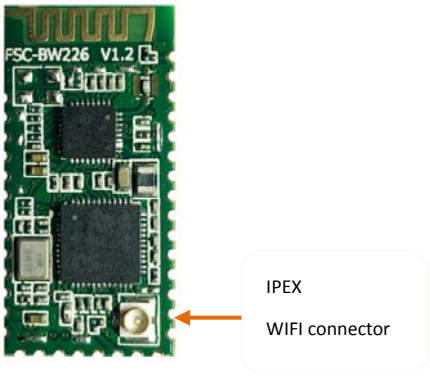


Figure 1: FSC-BW226 Picture

Module accessories

Figure 2: FSC-BW226 WiFi antenna Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth	Version : V4.2 Dual Mode
		Frequency : 2.402 - 2.480 GHz
		Transmit Power: +5.5 dBm (Maximum)
		Raw Data Rates (Air): 3 Mbps(Classic BT - BR/EDR)
	WiFi	IEEE 802.11 b/g/n compatible WLAN
		Frequency : 2.400～2.4835GHz
		Transmit Power: 17.5dBm(11 b), 15.5dBm(11 g), 13.5dBm(11 n)
		802.11e Qos Enhancement
		WiFi WPS & Direct support
		Light Weight TCP/IP protocol
		Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
		Default antenna interface: IPEX
Host Interface and Peripherals	UART Interface	TX, RX (Auto Flow Control)
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		5, 6, 7, 8 data bit character
	GPIO	11 (maximum – configurable) lines
		O/P drive strength (4 mA)
		Pull-up resistor (33 KΩ) control
		Read pin-level
	I2C Interface	1 (configurable from GPIO total). Up to 400 kbps
	SPI Interface	Support Master/Slave mode
	PWM	16-bit resolution
		8-bit prescaler and clock divider
		Supports PWM interrupts
		supports input capture function
Profiles	Classic Bluetooth	SPP (Serial Port Profile) - Up to 600 Kbps
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
	WiFi	WiFi-AP(access point), WiFi-Station
Maximum Connections	Classic Bluetooth	7 Clients(MAX)
	Bluetooth Low Energy	5 Clients(MAX)
FW upgrade		Via UART(TBD)
		J-link
Supply Voltage	Supply	3.0-3.6V
Power Consumption	Bluetooth	Max Peak Current(TX Power @ +5.5dBm TX): 84mA
		Standby Doze (Wait event) - 19mA (TBD)
		Deep Sleep - No Supports
	WiFi	3.3V Rating Current(with internal regulator and integrated COMS

		PA): 450mA (MAX)
		IO Rating Current(including VDD_IO): 200mA
Physical	Dimensions	13mm X 26.9mm X 2.0mm; Pad Pitch 1.5mm
Environmental	Operating	-20°C to +70°C
	Storage	-40°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class-2 Machine Model: Class-B

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

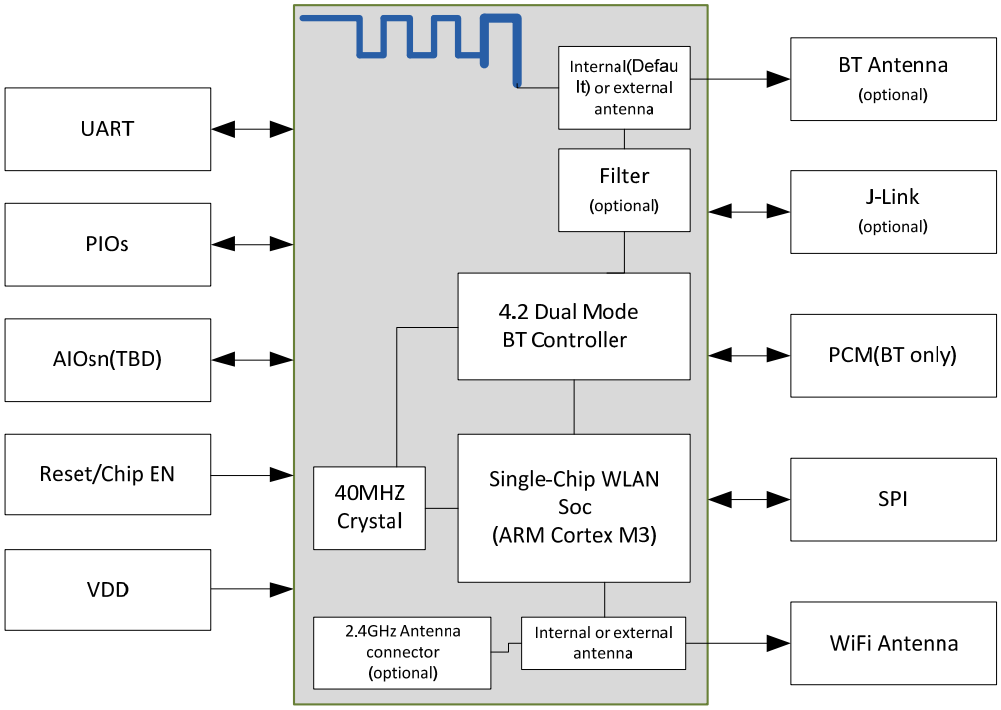


Figure 2: Block Diagram

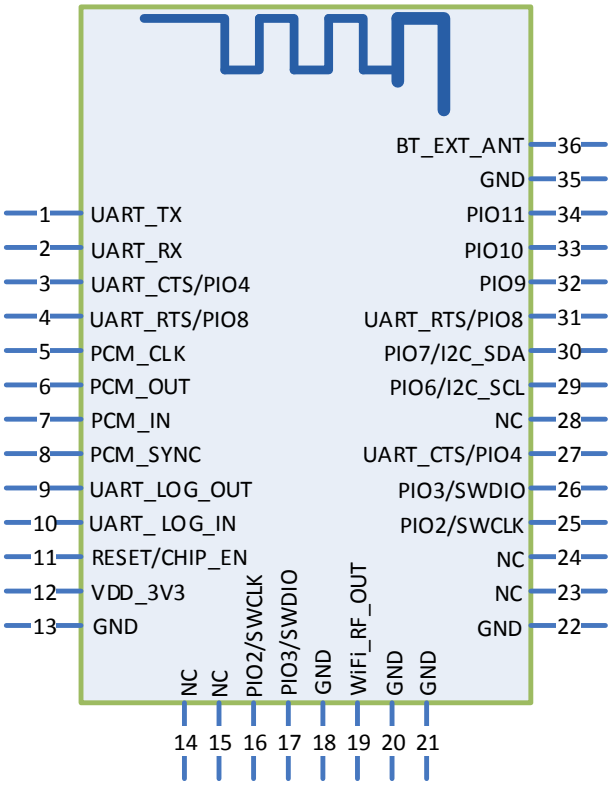


Figure 3: FSC-BW226 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX	O	UART Data output Alternative Function: SPI_MISO	Note 1
2	UART_RX	I	UART Data input Alternative Function: SPI_CS	Note 1
3	UART_CTS/PIO4	I/O	UART Clear to Send (active low) Alternative Function 1: Programmable input/output line Alternative Function 2: PWM Alternative Function 3: SPI_CLK	Note 1
4	UART_RTS/PIO8	I/O	UART Request to Send (active low) Alternative Function 1: Programmable input/output line Alternative Function 2: SPI_MOSI	Note 1
5	PCM_CLK	I/O	PCM bit clock pin(BT only)	
6	PCM_OUT	O	PCM data out(BT only)	
7	PCM_IN	I	PCM data input(BT only)	
8	PCM_SYNC	I/O	PCM left right channel clock(BT only)	
9	UART_LOG_OUT	O	Debug Interface (Data OUT)	
10	UART_ LOG_IN	I	Debug Interface (Data IN)	
11	RESET/CHIP_EN	I	External reset input: Active LOW, with an inter an internal pull-up. Set this pin low reset to initial state.	
12	VDD_3V3	Vdd	Power supply voltage 3.3V	

13	GND	Vss	Power Ground	
14	NC		NC	
15	NC		NC	
16	PIO2/SWCLK	I/O	Debugging through the clk line(Default) Alternative Function: Programmable input/output line	
17	PIO3/SWDIO	I/O	Debugging through the data line(Default) Alternative Function 1: Programmable input/output line Alternative Function 2: PWM	
18	GND	Vss	Power Ground	
19	WiFi_RF_OUT	O	WiFi RF signal output .	Note5
20	GND	Vss	Power Ground	
21	GND	Vss	Power Ground	
22	GND	Vss	Power Ground	
23	NC		NC	
24	NC		NC	
25	PIO2/SWCLK	I/O	Debugging through the clk line(Default) Alternative Function: Programmable input/output line	
26	PIO3/SWDIO	I/O	Debugging through the data line(Default) Alternative Function 1: Programmable input/output line Alternative Function 2: PWM	
27	UART_CTS/PIO4	I/O	UART Clear to Send (active low) Alternative Function 1: Programmable input/output line Alternative Function 2: PWM	Note 1
28	NC		NC	
29	PIO6/I2C_SCL	I/O	Programmable input/output line	Note 2
30	PIO7/I2C_SDA	I/O	Programmable input/output line	Note2
31	UART_RTS/PIO8	I/O	UART Request to Send (active low) Alternative Function 1: Programmable input/output line Alternative Function 2: SPI_MOSI	Note 1
32	PIO9	I/O	LED(Default) or Programmable input/output line Alternative Function: PWM	Note 3
33	PIO10	I/O	BT Status(Default) or Programmable input/output line Alternative Function: PWM	Note4
34	PIO11	I/O	Programmable input/output line	
35	GND	Vss	RF Ground	
36	BT_EXT_ANT	O	BT RF signal output .	Note5

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 3	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 4	BT Status(Default)-- Disconnected: Low Level; Connected: High Level.
Note 5	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth

signal coverage.

If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Audio Interfaces

4.2.1 PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (**Figure 4**), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (**Figure 5**)

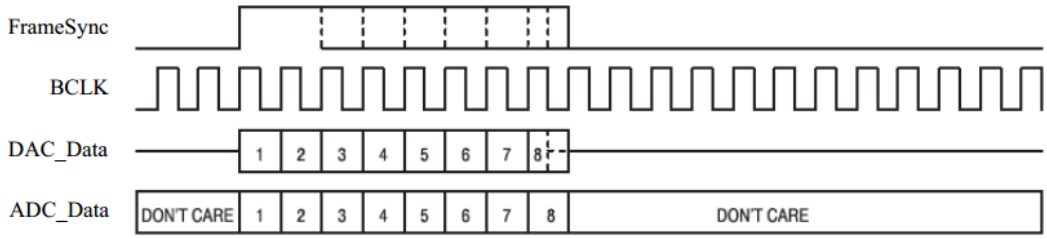


Figure 4: FSC-BW226 Long FrameSync (BT only)

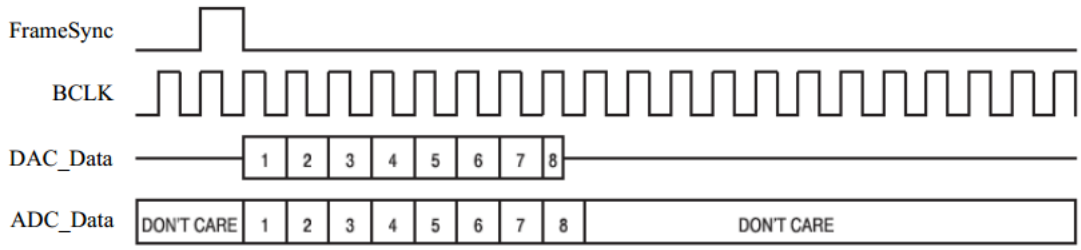


Figure 5: FSC-BW226 Short FrameSync (BT only)

4.3 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR) or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

4.4 General Purpose Digital IO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

4.5 RF Interface

For This Module, the default mode for antenna is internal ,it also has the interface for external antenna(BT). If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

Need external antenna for WIFI or Equipped with the RF Connector, connect to the external antenna.(Before you purchasing the samples, please confirm with our salesman for the antenna issues.)

The user can connect a 50 ohm antenna directly to the RF port.

Bluetooth basic parameter：

- 2402–2480 MHz Bluetooth 4.2 Dual Mode (BT and BLE); 1 Mbps to 3 Mbps over the air data rate.
- TX output power of +5.5dBm.
- Receiver to achieve maximum sensitivity -85dBm @ 1 Mbps BLE or Classic BT, 2 Mbps, 3 Mbps).

WiFi basic parameter：

- 2402–2483.5 MHz IEEE 802.11 b/g/n compatible WLAN
- Transmit Power: 17.5dBm(11 b), 15.5dBm(11 g), 13.5dBm(11 n).
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Receiver to achieve maximum sensitivity： -76dBm(11 b), -77dBm(11 g), -74dBm(11 n).

4.6 Serial Interfaces

4.6.1 UART

- Support 1 HS-UART
- UART(RS232 Standard) Serial Data Format
- Transmit and Receive data FIFO
- Programmable asynchronous clock support
- Auto flow control
- Programmable Receive data FIFO trigger level
- UART signal level ranges 3.3V

Table 3: Possible UART Settings

Parameter		Possible Values
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	921600bps(≤1%Error)
Flow control		RTS/CTS, or None(TBD)
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

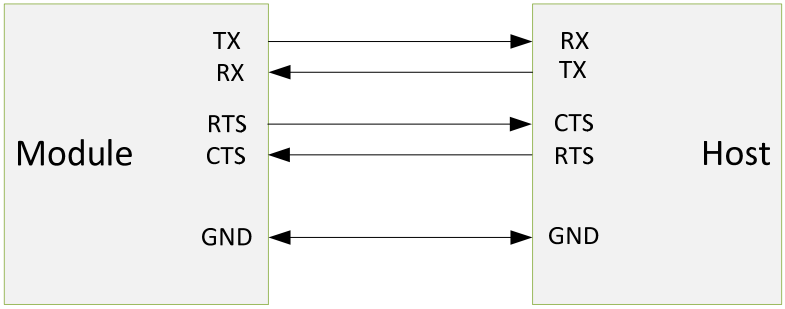


Figure 6: UART Connection

4.6.2 I2C Interface

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I2C Bus Timing.

- Three speeds: Standard mode(0 to 100Kb/S); Fast mode(<400 Kb/S); High-speed mode(<3.4Mb/S)
- Master or slave I2C operation
- 7- or 10-bit addressing
- Transmit and receive buffers

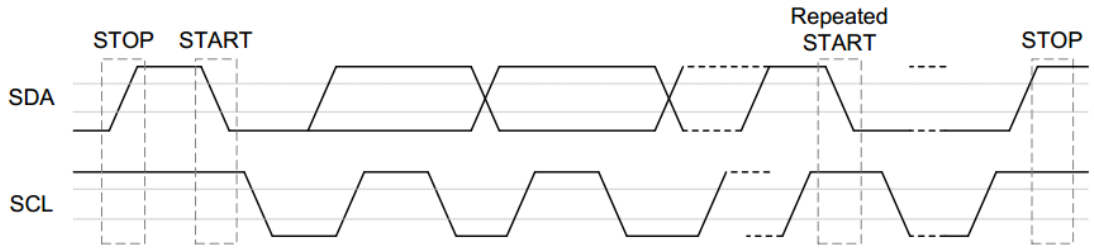


Figure 7: I2C Bus Timing

The device on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. The I2C H/W interfaces to the I2C bus via two pins: SDA and SCL. Pull up resistor is needed for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins function to I2C in advance.

4.7 PWM Generator and Capture Timer (PWM)

FSC-BW226 has **4** PWM generator. The PWM generator has a 16-bit PWM counter and comparator, and the PWM generator supports two standard PWM output modes: Independent output mode and Complementary output mode with 8-bit Dead-time generator. Each mode can be used as a timer and issues interrupt independently. In addition, It also has an 8-bit prescaler and clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16) to support wide range clock frequency of PWM counter. For PWM output control unit, it supports polarity output function.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

4.7.1 PWM function features

- Supports 4 PWM output channels with 16-bit resolution(optional)
- Supports 8-bit prescaler and clock divider
- Supports 4 PWM interrupts(optional)
- Supports One-shot or Auto-reload PWM counter operation mode
- Supports 8-bit Dead-time

4.7.2 Capture function features

- Supports 4 capture input channels with 16-bit resolution(optional)
- Supports rising or falling capture condition
- Supports 4 Capture interrupts(optional)

4.8 Security Engine（WiFi only）

4.8.1 Features

- Provide low SW computing and high performance encryption
- Supported authentication algorichms:
  1,MD5
  2,SHA-1
  3,SHA-2(SHA-224/SHA-256)
  4,HMAC-MD5
  5,HMAC-SHA1
  6,HMAC-SHA2
- Supports Encryption/Decryption mechanisms:
  1,DES(CBC/ECB)
  2,3DES(CBC/ECB)
  3,AES-128(CBC/ECB/CTR)
  4, AES-192(CBC/ECB/CTR)
  5, AES-256(CBC/ECB/CTR)

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.
The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	-0.3	+3.6	V
V_{IN} - Input Voltage	Vss-0.3	Vdd+0.3	V
T_A - Operating Temperature	-20	+70	°C
T_{ST} - Storage Temperature	-40	+85	°C
I_{IO} - Maximum Current sunk by a I/O pin		4	mA
I_{IO} - Maximum Current sourced by a I/O pin		4	mA

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	3	3.3	3.6	V
V_{IN} - Input Voltage	Vss-0.3	3.3	Vdd+0.3	V
T_A - Operating Temperature	-20	25	+70	°C

T_{ST} - Storage Temperature	-40	25	+85	°C
I_{IO} - Maximum Current sunk by a I/O pin	2	3	4	mA
I_{IO} - Maximum Current sourced by a I/O pin	2	3	4	mA
IDD- 3.3V Rating Current (With internal regulator and integrated COMS PA) (Wifi only)	-	-	450	mA

5.3 Input/output Terminal Characteristics

Table 6: DC Characteristics (V_{DD} - V_{SS} = 3 ~ 3.6 V, T_A = 25°C)

Parameter	Min	Type	Max	Unit
V_{DD} - Operation Voltage	3	3.3	3.6	V
V_{SS} - Power Ground	-0.3	-	-	V
V_{DD12} - Core Logic and I/O Buffer Pre-Driver Voltage	1.08	1.2	1.32	V
V_{OH} - High Level Output Voltage	2.4	-	-	V
V_{OL} - Low Level Output Voltage	-	-	0.4	V
V_{IH} - Input High Voltage	2.0	-	-	V
V_{IL} - Input Low Voltage	-	-	0.8	V
V_{TH} - Switch Threshold(Schmitt-falling-trigger)	1.36	1.45	1.56	V
V_{TH} - Switch Threshold(Schmitt-rising-trigger)	1.78	1.87	1.97	V
R_{PU} - Input Pull-up Resist(V_{IN}=V_{SS})	32	53	120	KΩ
R_{PD} - Input Pull-down Resist(V_{IN}=V_{DD})	37	49	120	KΩ
I_L - Input Leakage Current	-10	-	10	uA
I_{OZ} - Tri-State Output Leakage Current	-10	-	10	uA
I_{OL} - Low level sink current(V_{OL}=0.4V)	4	-	-	mA
I_{OH} - High level source current (V_{OH}=2.4V)	4	-	-	mA

5.4 Temperature Characteristics

Table 7: Temperature Characteristics

Power(W)	PCB(layer)	Theta ja(C/W)	Theta jc(C/W)	Psi jt(C/W)
1	4	28.1	11.1	0.24

5.5 Specification of Low Voltage Reset

Table 8: Specifications of Low Voltage Reset

Parameter	Min	Type	Max	Unit
V_{DD} - Supply Voltage	0	-	3.6	V
T_A - Temperature	-20	25	+70	°C
I_{LVR}- Quiescent Current	-	25	40	uA
V_{LVR} - Threshold Voltage	2.16	2.4	2.64	V

5.6 Specifications of Power-on Reset

Table 9: Specifications of Power-on Reset

Parameter	Min	Type	Max	Unit
T_A - Temperature	-20	25	+70	°C
I_{POR}- Quiescent Current(V_{DD}>Reset Voltage)	-	33	50	uA
V_{POR} - Reset Voltage(TA=-20~+70°C)	1.6	2	2.4	V
V_{POR} - VDD Start Voltage to Ensure Power on Reset	-	-	100	mV
PRV_{DD}- VDD Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms
t_{POR}- Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power on Reset	0.5	-	-	ms

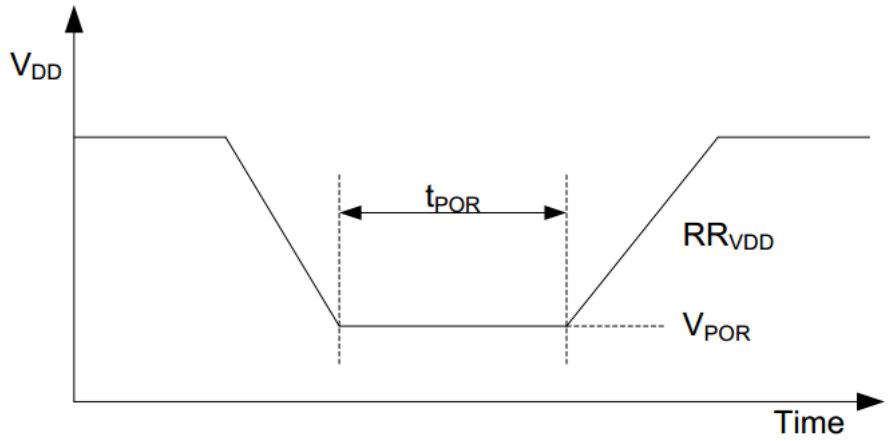


Figure 8: Power-up Ramp Condition

5.7 I2C Dynamic Characteristics

Table 10: I2C Dynamic Characteristics

Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
	Min	Max	Min	Max	
t_{LOW} - SCL low period	4.7	-	1.2	-	uS
T_{HIGH} - SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$ - Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$ - START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$ - STOP condition setup time	4	-	0.6	-	uS
t_{BUF} - Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$ - Data setup time	250	-	100	-	uS
$t_{HD;DAT}$ - Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r - SCL/SDA rise time	-	1000	20+0.1CB	300	uS
t_f- SCL/SDA fall time	-	300	-	300	uS
C_b - Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

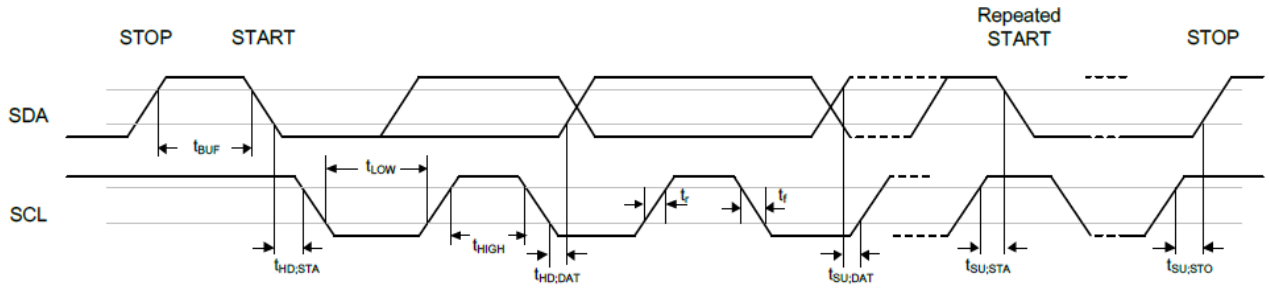


Figure 9: I2C Timing Diagram

5.8 Power consumptions

Table 11: Power consumptions

Parameter	Test Conditions	Type	Unit
Bluetooth			
Search		~35	mA
Unconnected (Deep Sleep Idle Mode)	No support	-	mA
Connected Idle		~19	mA
Shutdown		＜50	uA
WLAN			
3.3V Rating Current (With internal regulator and integrated COMS PA)		450	mA
Shutdown		＜50	uA

6. MSL & ESD

Table 12: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade:	Human Body Model: Class-2 Machine Model: Class-B

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 18** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 13**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 13: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

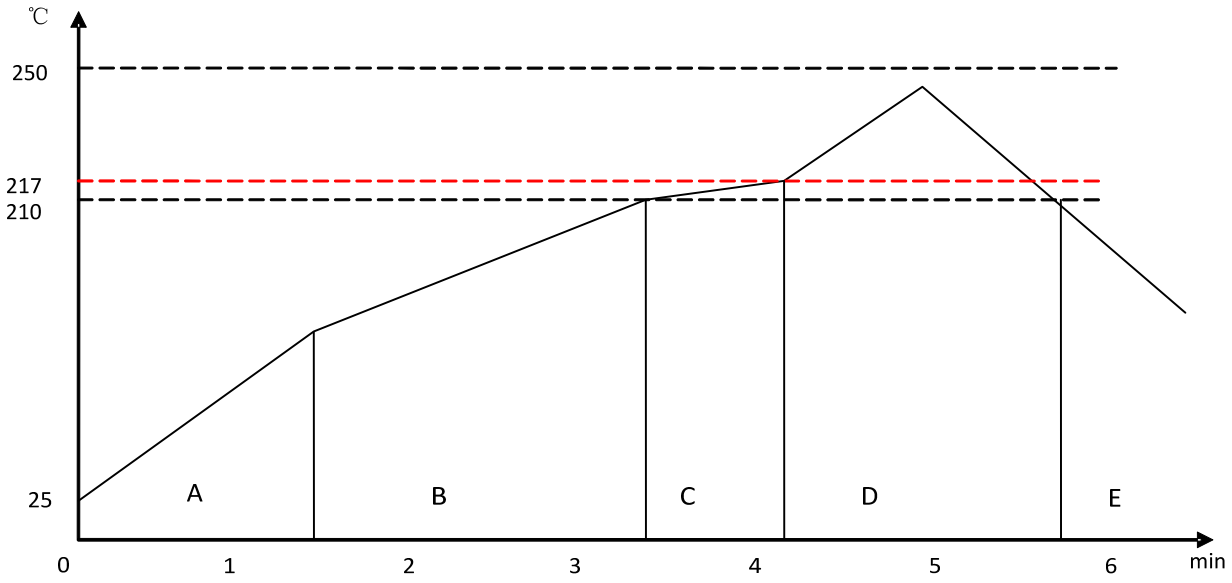


Figure 10: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

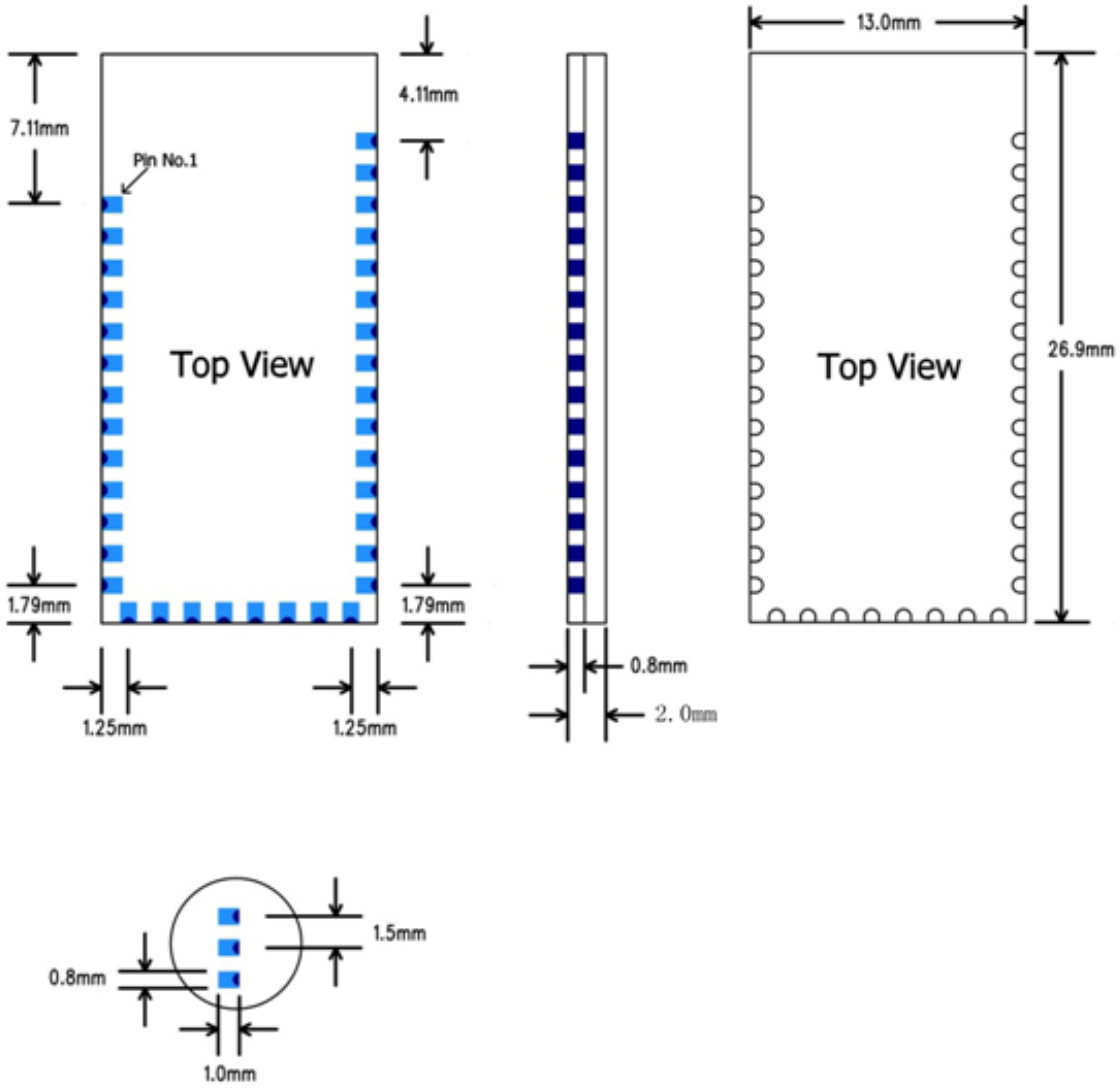


Figure 11: FSC-BW226 footprint

8.2 Host PCB Land Pattern and Antenna Keep-out for FSC-BW226

Please check the **Figure 12** for Pad Structure and Keep Out Area:

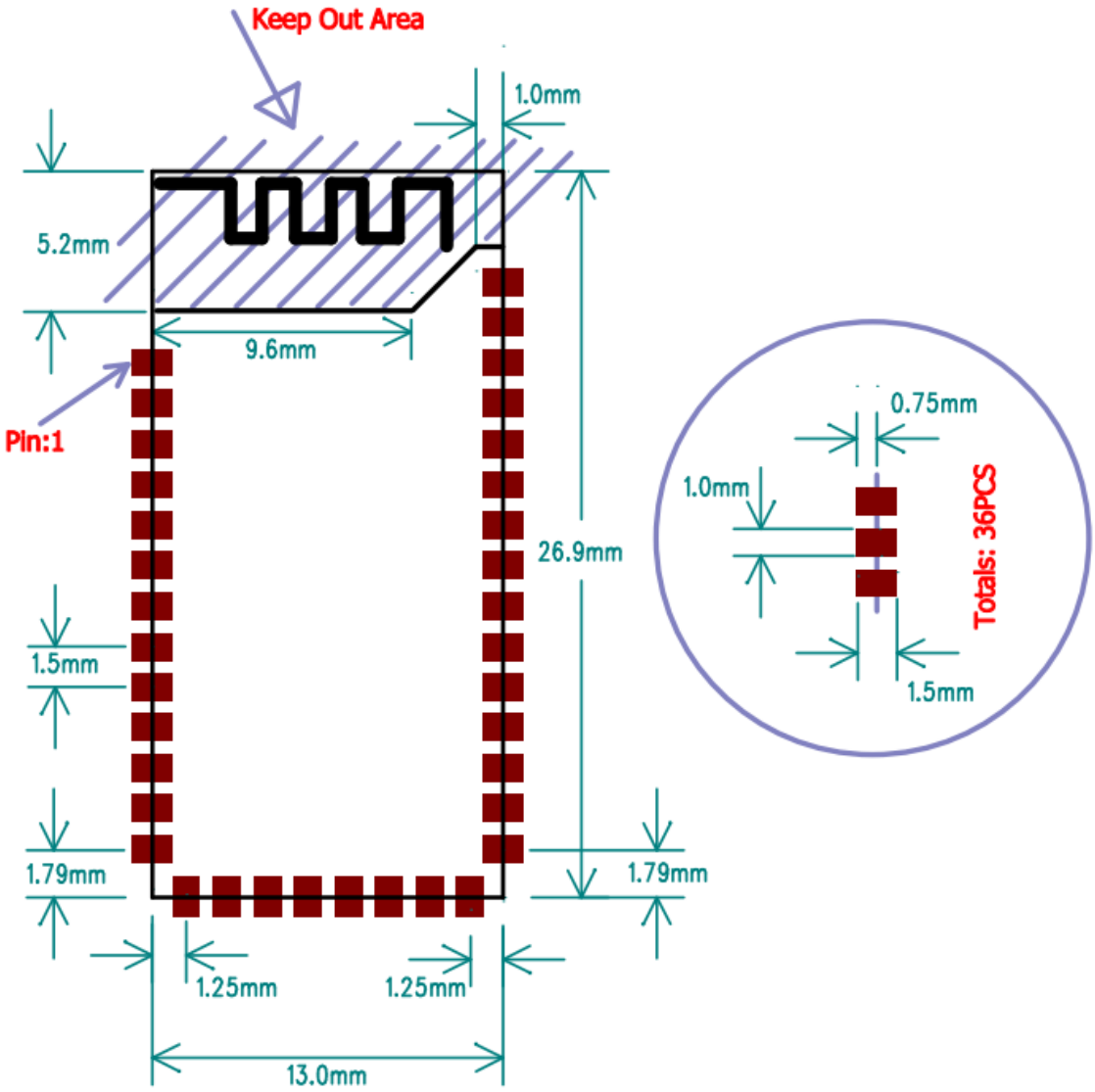


Figure 12: Host PCB-Top View

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT906 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

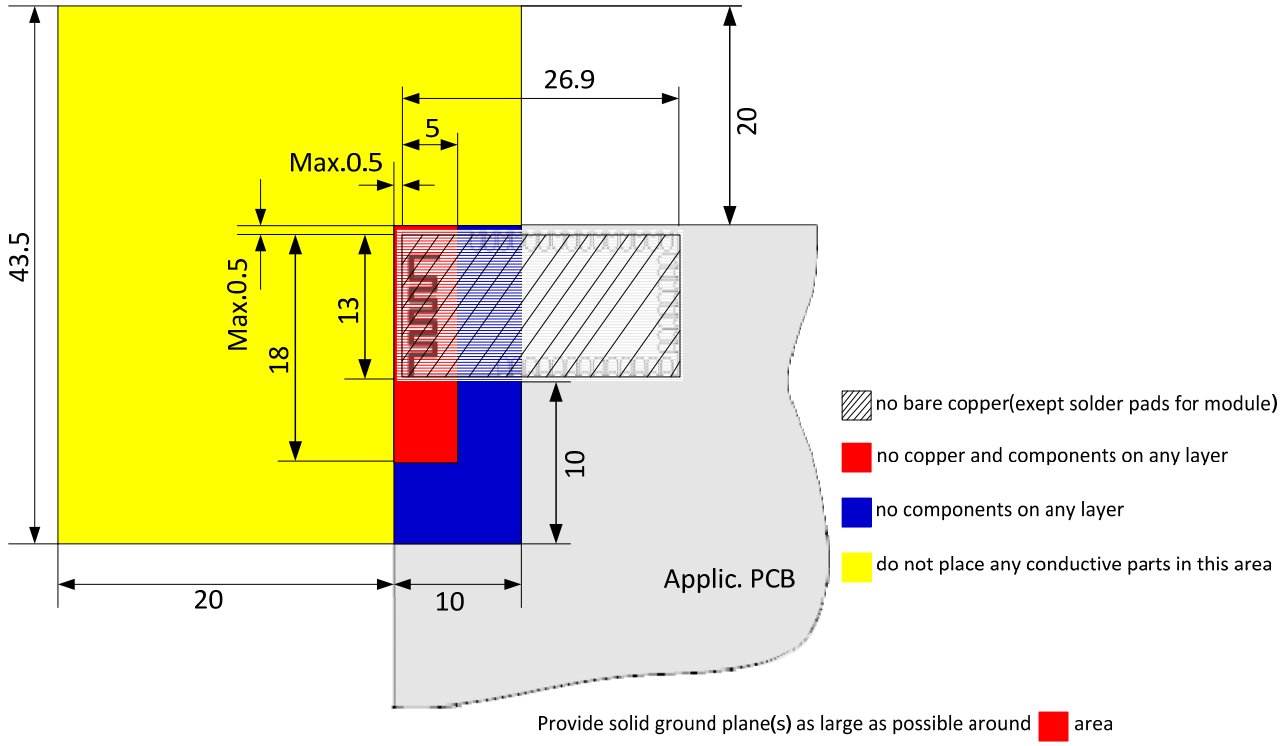


Figure 13: FSC-BW226 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

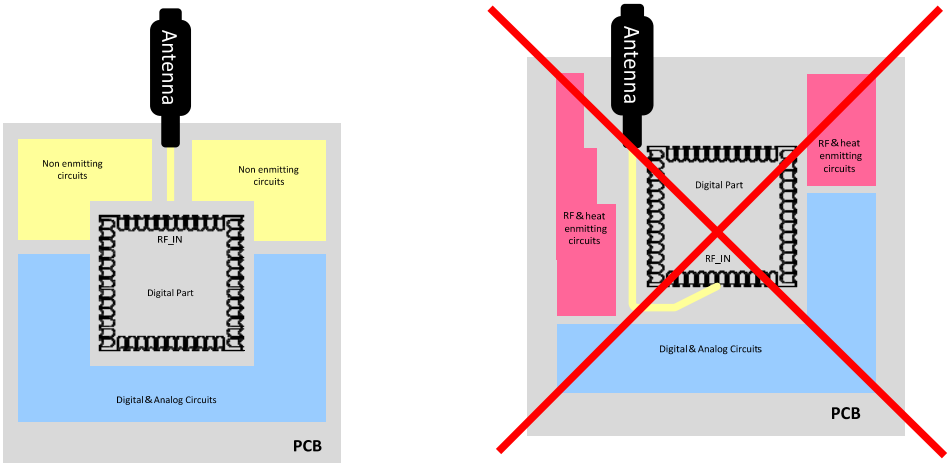


Figure 14: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

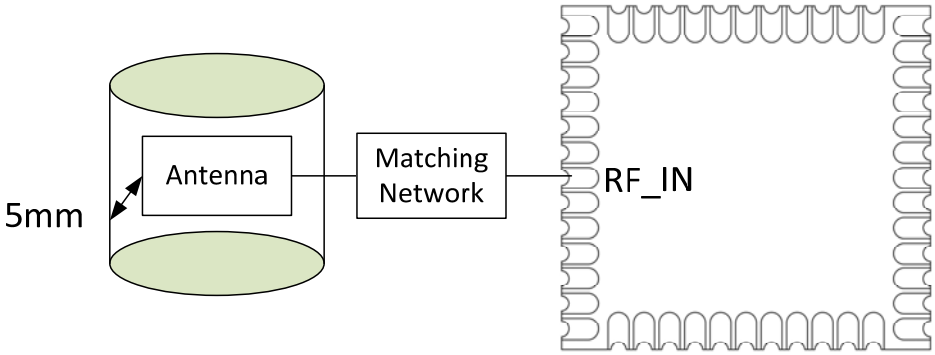


Figure 15: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

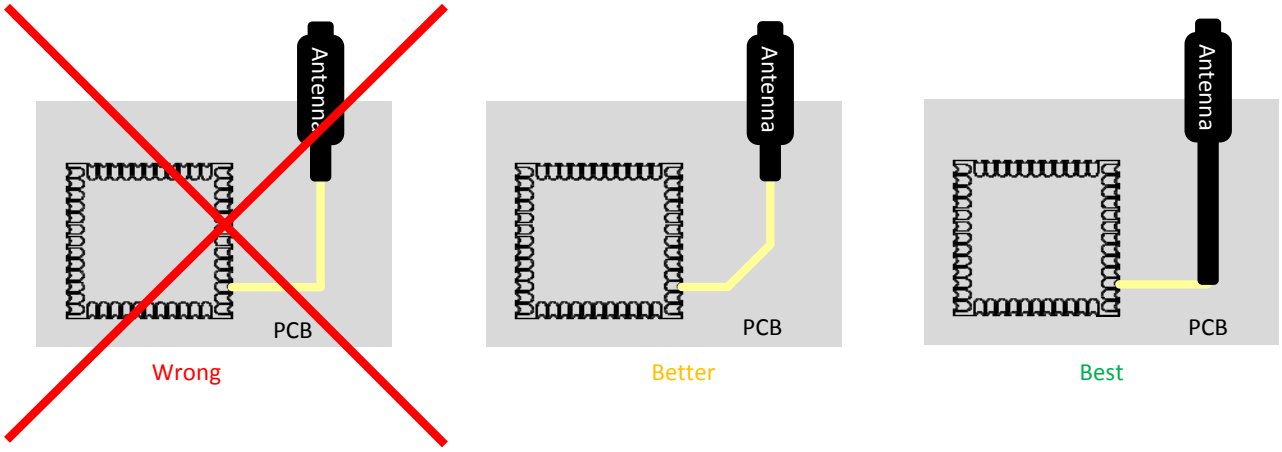


Figure 16: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

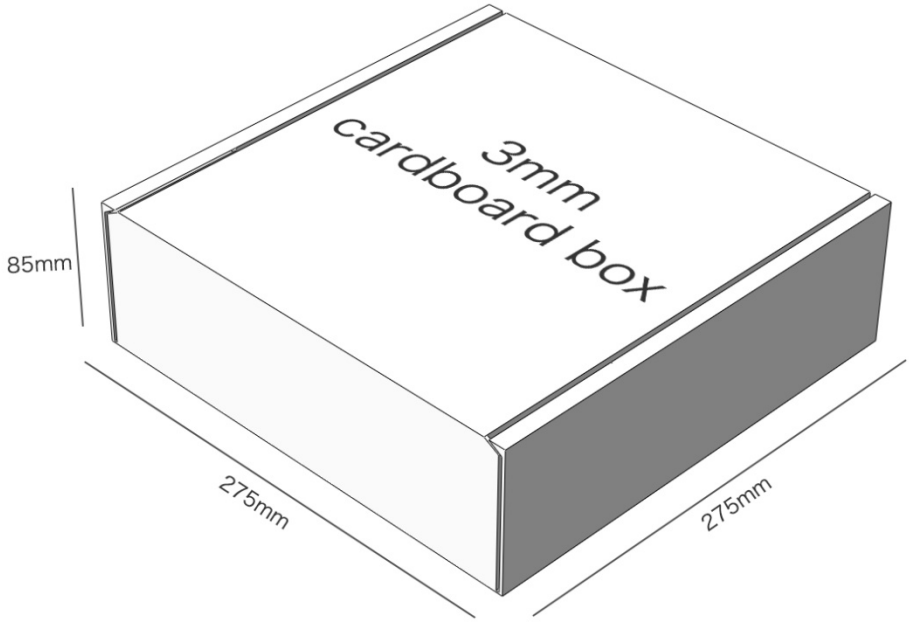
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 17: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 18: Packing Box

11. APPLICATION SCHEMATIC

FCC Statement

15.19

1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference.
(2) This device must accept any interference received, including interference that may cause undesired operation.

15.21

Note: The grantee is not responsible for any changes or modifications not expressly approved by the party responsible for compliance. Such modifications could void the user's authority to operate the equipment.

15.105(b)

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.
This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help

RF Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance of 20 cm between the radiator and your body.

Instructions to the OEM/Integrator:

This module has been granted modular approval for mobile applications. OEM integrators for host products may use the module in their final products without additional FCC/ISED (Innovation, Science and Economic Development Canada) certification if they meet the following conditions. Otherwise, Additional FCC/IC approvals must be obtained.

● The OEM must comply with the FCC labeling requirements. If the module's label is not visible when installed, then an additional permanent label must be applied on the outside of the finished product which states: "Contains transmitter module FCC ID: 2AMWOFSC-BW226".

Additionally, the following statement should be included on the label and in the final product's user manual:
"This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interferences, and (2) this device must accept any interference received, including interference that may cause undesired operation."

● The user's manual for the host product must clearly indicate the operating requirements and conditions that must be

observed to ensure compliance with current FCC / IC RF exposure guidelines.

- The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
- This Module is full modular approval, it is limited to OEM installation ONLY.
- The module is limited to installation in mobile application.
- A separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and difference antenna configurations.
- The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.
- The Grantee will provide guidance to the Host Manufacturer for compliance with the Part 15B requirements if requested.