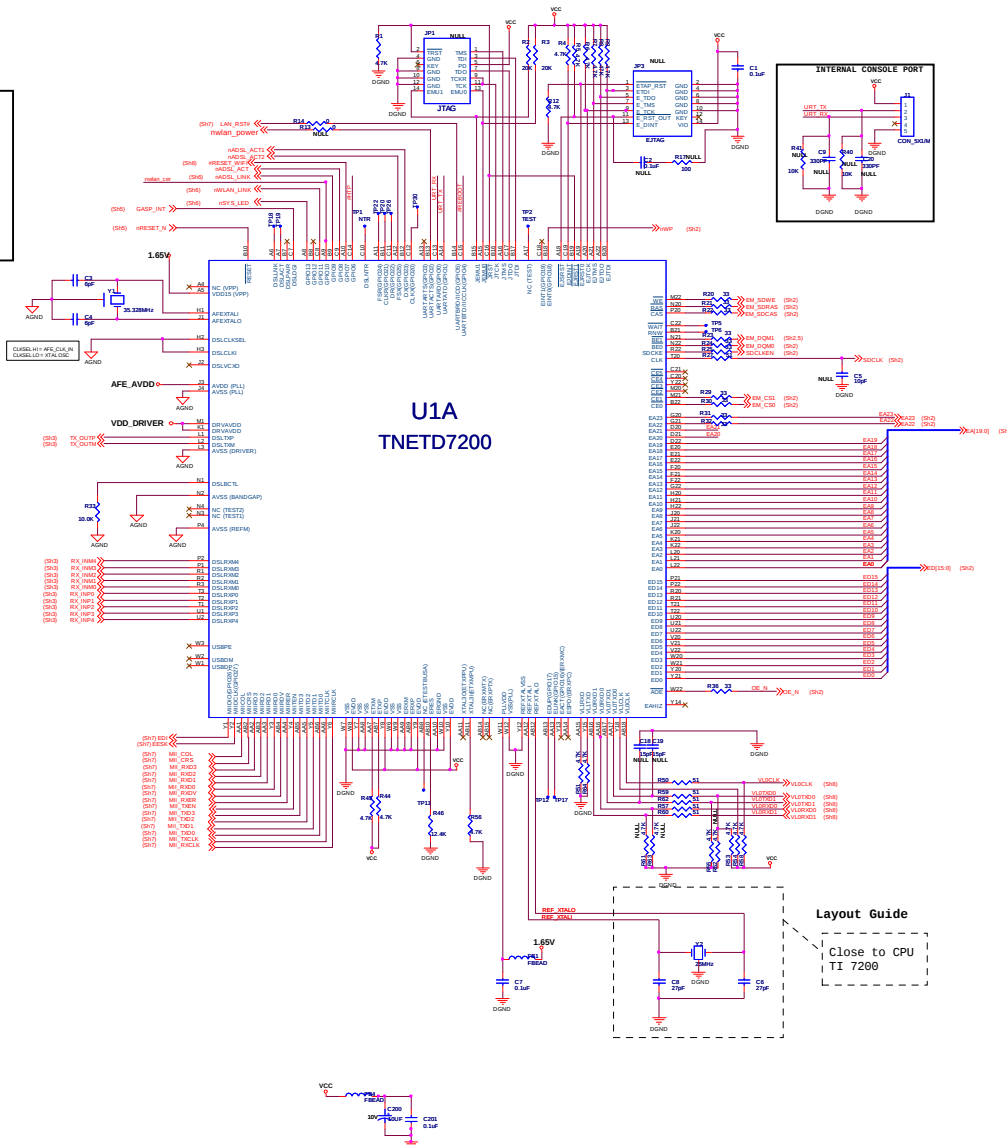
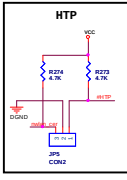
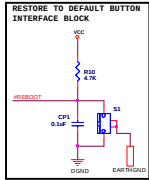
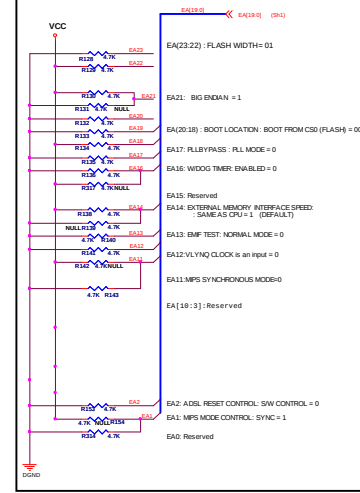




TNETD7200 BOOT CONFIGURATION

ALL BOOT CONFIG RESISTORS SIZE 0803



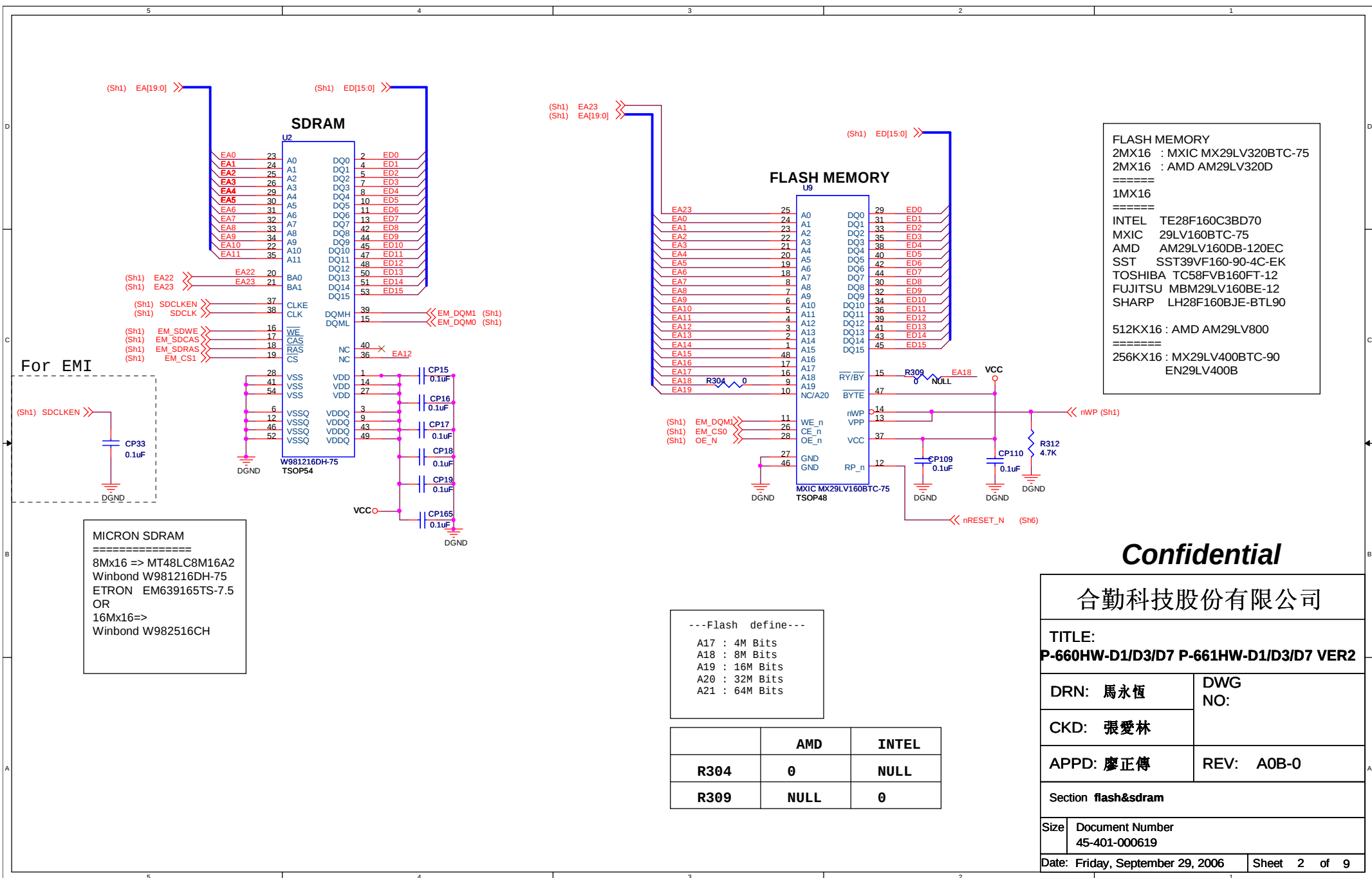
- EA(23:22) : FLASH WIDTH:
00 8-BIT FLASH
01 16-BIT FLASH(Default)
EA(21) : Endian:
0 -- Little Endian
1 -- Big Endian(Default)
EA(20:18) : Boot Location:
000 -- Reserved
001 -- Boot from CS0(Flash)(Default)
010 -- Boot from CS1(SDRAM)
011 -- Boot from CS2(8-bit Asynchronous Memory)
100 -- Boot from CS3(16-bit Asynchronous Memory)
101 -- Boot from small EEPROM
110 -- Boot from large EEPROM
111 -- Boot from VLYNQ
EA(17) : PLL Mode:
0 -- PLL mode(Default)
1 -- All PLLs are bypassed
EA(16) : Watchdog:
0 -- Watchdog timer enabled after reset(Default)
1 -- Watchdog timer disabled after reset
EA(15) : Reserved
EA(14) : EMF Rate:
0 -- half the speed of the system bus.
1 -- the same speed as the system bus (Default)
EA(13) : EMF Test:
0 -- External memory controller is in normal operating mode (Default)
1 -- External memory controller is in test mode.
EA(12) : VLYNQ_CLOCK_DEFAULT_DIRECTION:
0 -- VLYNQ CLOCK is an input(Default)
1 -- VLYNQ CLOCK is an output
EA(11) : MPS asynchronous mode control:
0 -- The internal system bus frequency of operation is equal to frequency of the MPS processor or clock
1 -- The internal system bus frequency of operation is equal to half the frequency of the MPS processor or clock (Default)
EA(10:3) : Reserved
EA(2) : ADSL Reset Control:
0 -- ADSLSS reset controlled by software(Default)
1 -- ADSLSS reset is de-asserted
EA(1) : MPS Clock Mode:
0 -- MPS processor clock is synchronous to the system clock
1 -- MPS processor clock is asynchronous(Default)
EA(0) : Reserved

Amendment History

Date	Release	Description
2006/4/13	A0B-0	C2 Sample Run
2006/6/26	A0B-0	C3 Sample Run
2006/9/29	A0B-0	FCS Sample Run

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TITLE: P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2	
DRN: 馬永健	DIWG: NO.
CKD: 張豐林	
APPD: 廖正傳	REV: A0B-0
Section TI 7200	
Size: 45-001-000619	Document Number
Date: Friday, September 29, 2006	Sheet 1 of 9



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TITLE:
P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2

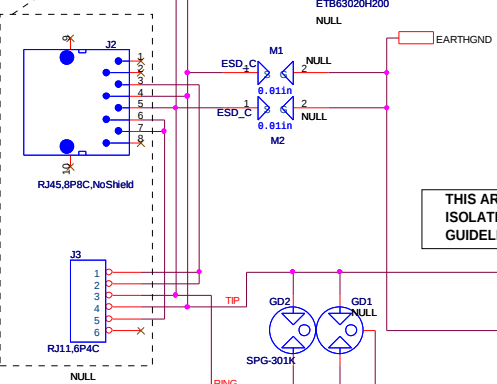
DRN: 馬永恆	DWG NO:
CKD: 張愛林	
APPD: 廖正傳	REV: A0B-0

Section **flash&sdr**

Size	Document Number 45-401-000619
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Date: Friday, September 29, 2006	Sheet 2 of 9
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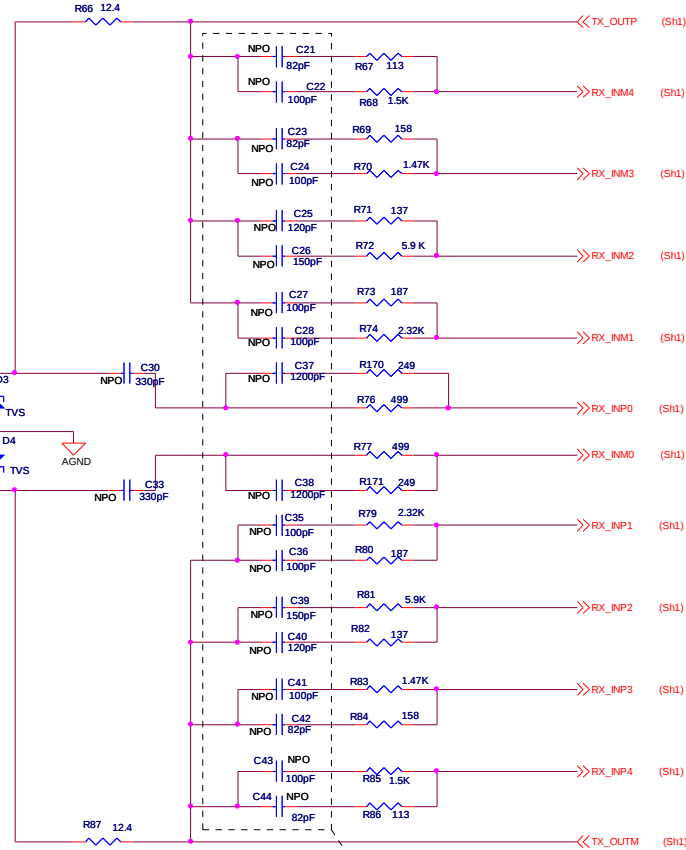
LAYOUT GUIDE:
DUAL LAYOUT



T1
ISOLATION
TRANSFORMER
POTS: LSE CE1069
SUMIDA S3001T(T10120)
ISDN: LSE CE1085
SUMIDA S3002T(T10121)

LAYOUT GUIDE:
DUAL LAYOUT

THIS AREA: USE HIGH VOLTAGE
ISOLATION LAYOUT
GUIDELINES



For P-660HW-D1 & P-660HW-D3 populate values as follows:

Components P-660HW-D1(Annex_A) P-660HW-D3(Annex_B)

R74, R79	232 ohm	1.18K ohm
C28, C35	180pF	220pF
R73, R80	3.32K ohm	196K ohm
C27, C36	270pF	56pF
R72, R81	158ohm	1.1K
C26, C39	180pF	220PF
R71, R82	6.49K ohm	NULL
C25, C40	330pF	NULL
R70, R83	499 ohm	NULL
C24, C41	220pF	Null
R69, R84	4.99K ohm	Null
C23, C42	270pF	Null
R68, R85	158 ohm	Null
C22, C43	180pF	Null
R67, R86	4.02K	Null
C21, C44	470pF	Null
R171, R170	249 ohm	Null
C37, C38	390pF	Null
C31	0.033uF	0.022uF
C30, C33	680pF	330pF
T1	CE1069	CE1085
C32	1uF	0.033uF

Note : NPO Material

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TITLE:
P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2

DRN: 馬永恆

DWG
NO:

CKD:張愛林

APPD: 廖正傳

REV: A0B-0

Section ADSL HYBRID

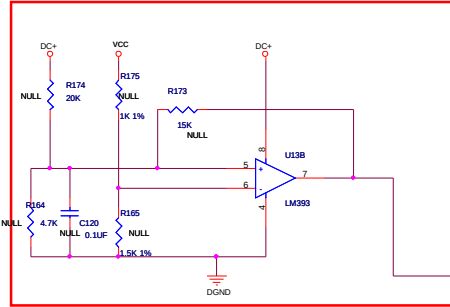
Size Document Number
45-401-000619

Date: Friday, September 29, 2006

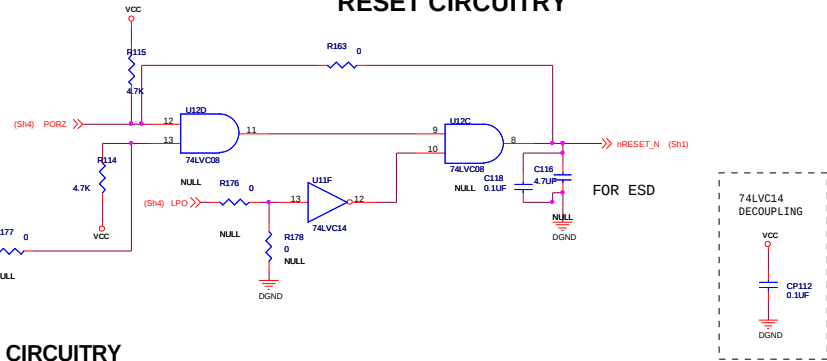
Sheet 3 of 9

合勤科技股份有限公司			
TITLE: -660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER:			
DRN: 周永復		DWG NO:	
CKD: 張愛林			
APPD: 廖正傳		REV: A0B-0	
Section POWER			
Size	Document Number		
	45-401-000619		
	Date: Friday, September 29, 2006		Sheet 4 of 5

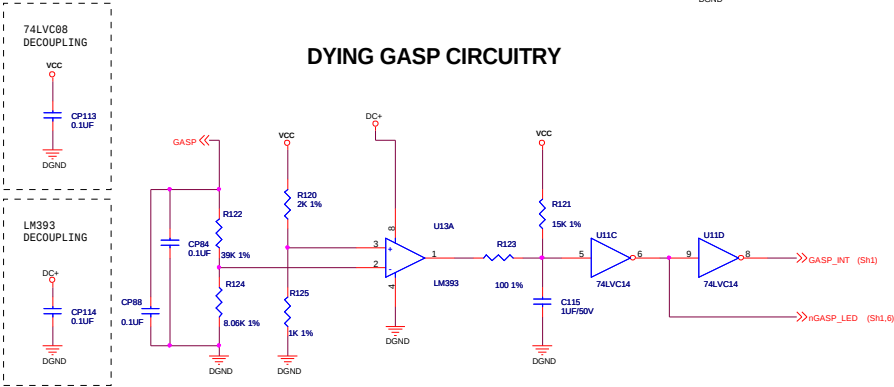
REGENERATIVE COMPARATOR CIRCUITRY



RESET CIRCUITRY



DYING GASP CIRCUITRY

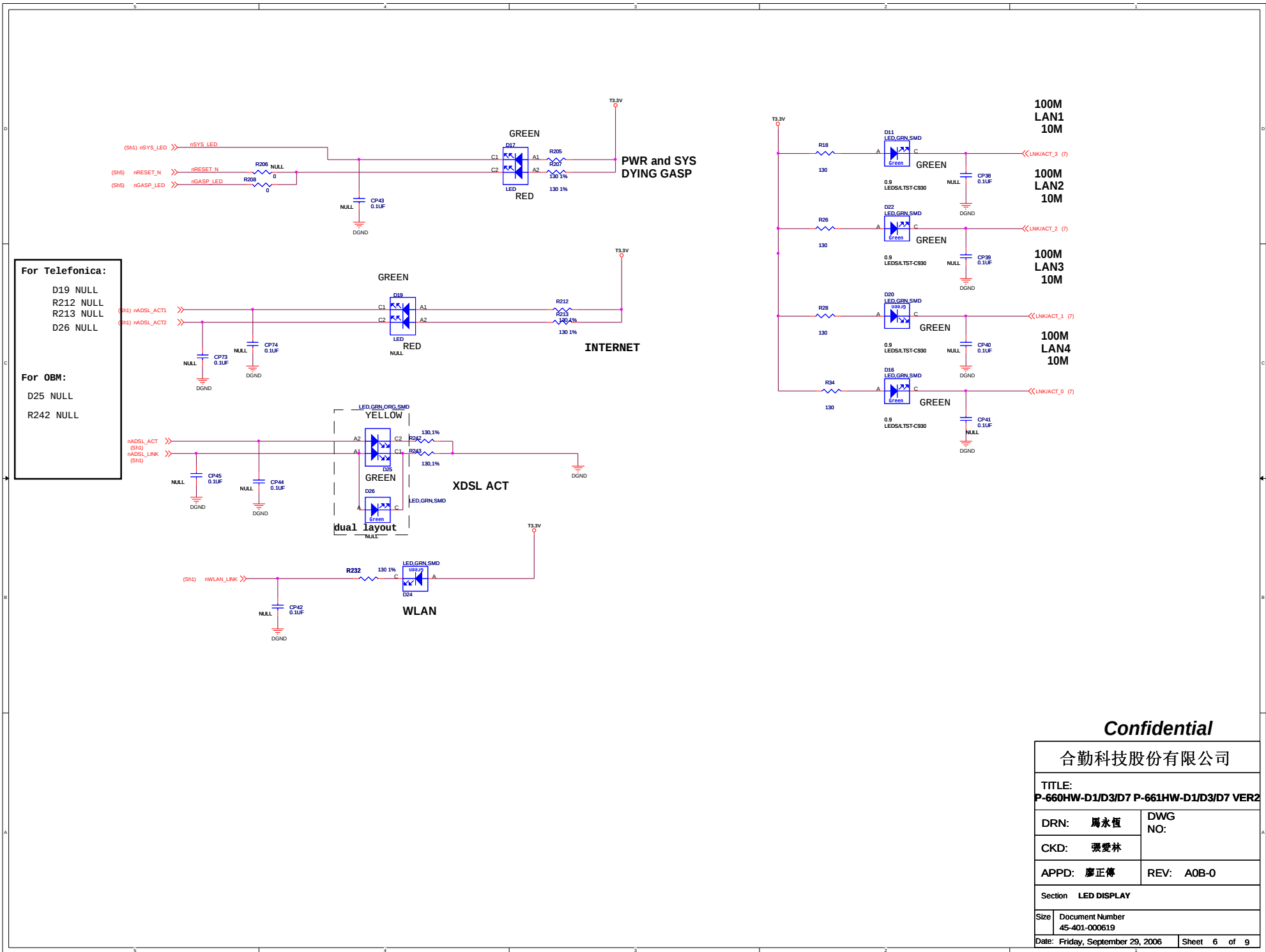


	for telefonica	not for telefonica
R174	20K 1%	NULL
R175	1K 1%	NULL
R165	1.5K 1%	NULL
R164	4.7K1%	NULL
R173	15K 1%	NULL
C120	NULL	NULL
R163	NULL	0
R176	0	NULL
C116	4.7UF	NULL
C118	NULL	0.1UF
R177	0	NULL
R122	39K	56K
U12	74LVC08	NULL

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TITLE: P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2	
DRN: 馬永恆	DWG NO:
CKD: 張愛林	
APPD: 廖正傳	REV: A0B-0
Section RESET & DYING GASP	
Size	Document Number 45-401-000619
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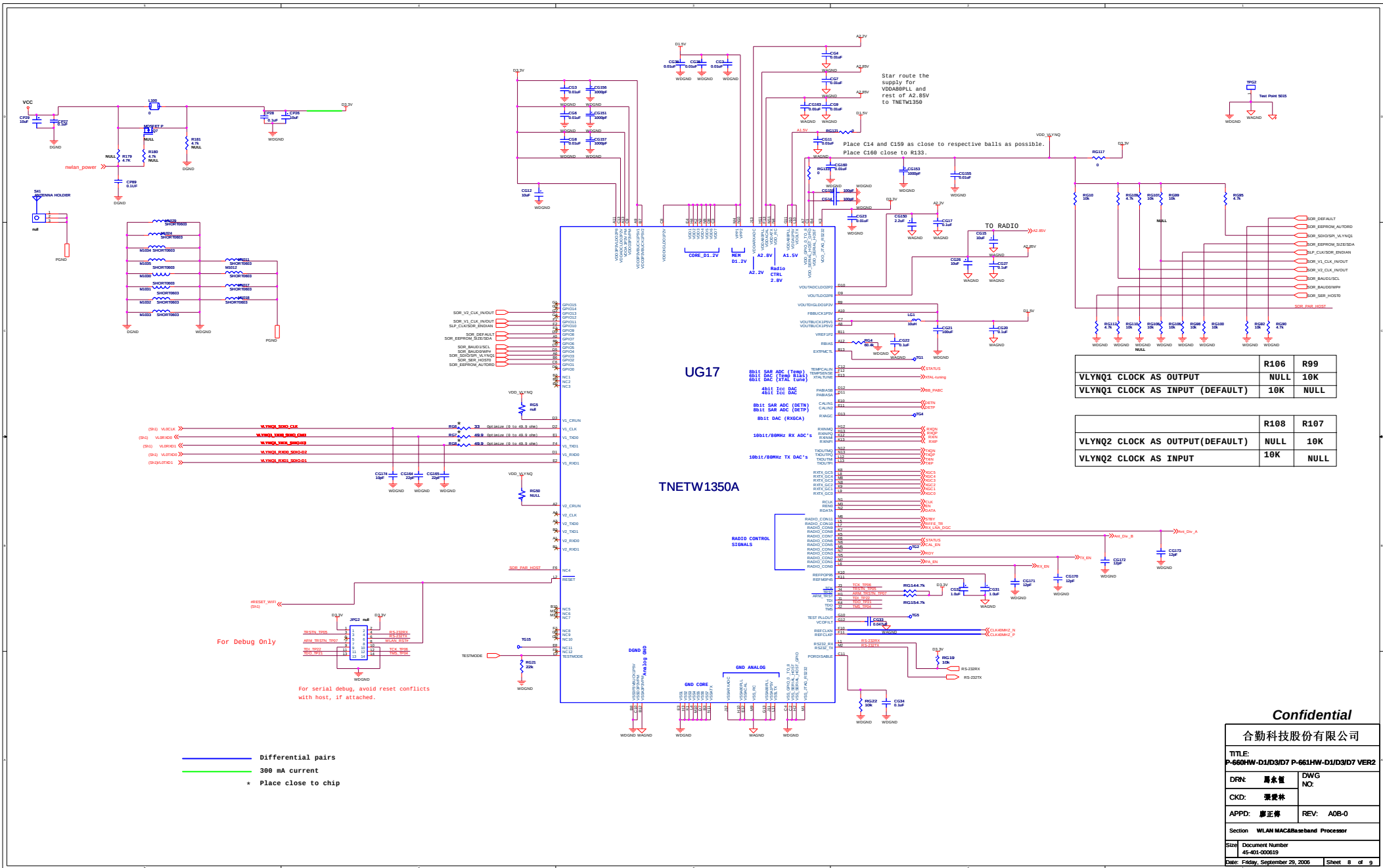
TITLE:
P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2

DRN: 馬永恆	DWG NO:
CKD: 張愛林	
APPD: 廖正傳	REV: A0B-0

Section LED DISPLAY

Size	Document Number 45-401-000619
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3. Pins 12,13 and 14 of U7 draw high current. Insure that the trace width between above pins is wide enough to minimize the voltage drop due to trace losses.

	VD_PA=3.3V (default)	VD_PA=5V
1)C82=10UF	NULL	YES
2)C84=1UF	NULL	YES
3)C83=0.1UF	NULL	YES
4)R24=0 OHM	NULL	YES
5)R25=0 OHM	YES	NULL

	Single Antenna (default)	Two Antenna with Antenna Diversity
1)U6	null	YES
2)C81=15PF	null	YES
3)C127=15PF	YES	YES
4)U14	YES	YES
5)C69=22PF	YES	YES
6)C68=22PF	YES	YES
7)R36=1K OHM	YES	YES
8)R37=1K OHM	YES	YES
9)C92=15PF	YES	YES
10)J5	YES	YES
11)J3	null	YES
12)R63, R64=1K OHM	null	YES
13)C67=15PF	YES	null
14)C124=22PF	null	YES
15)C125=22PF	null	YES
16)C62, C64, C94=15PF	null	YES
17)C91, C93	null	null

Section G-663 R02.11n WLAN Module Radio

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