HWM-WC1000 TABLE OF CONTENTS

INTRODUCTION

System Overview

The products have been developed for quick & stable service to customers in restaurants.

HWM-WC1000 consists of RX Module, Main Digital Board, and TX Module.

Functionally RX Module receives data from Table Unit, Main Digital Board process the data, and TX Module pages to each Pager by Pocsag protocol

Components

The basic System component are :

- HWM-WC1000

- Antenna
- Power Adapter

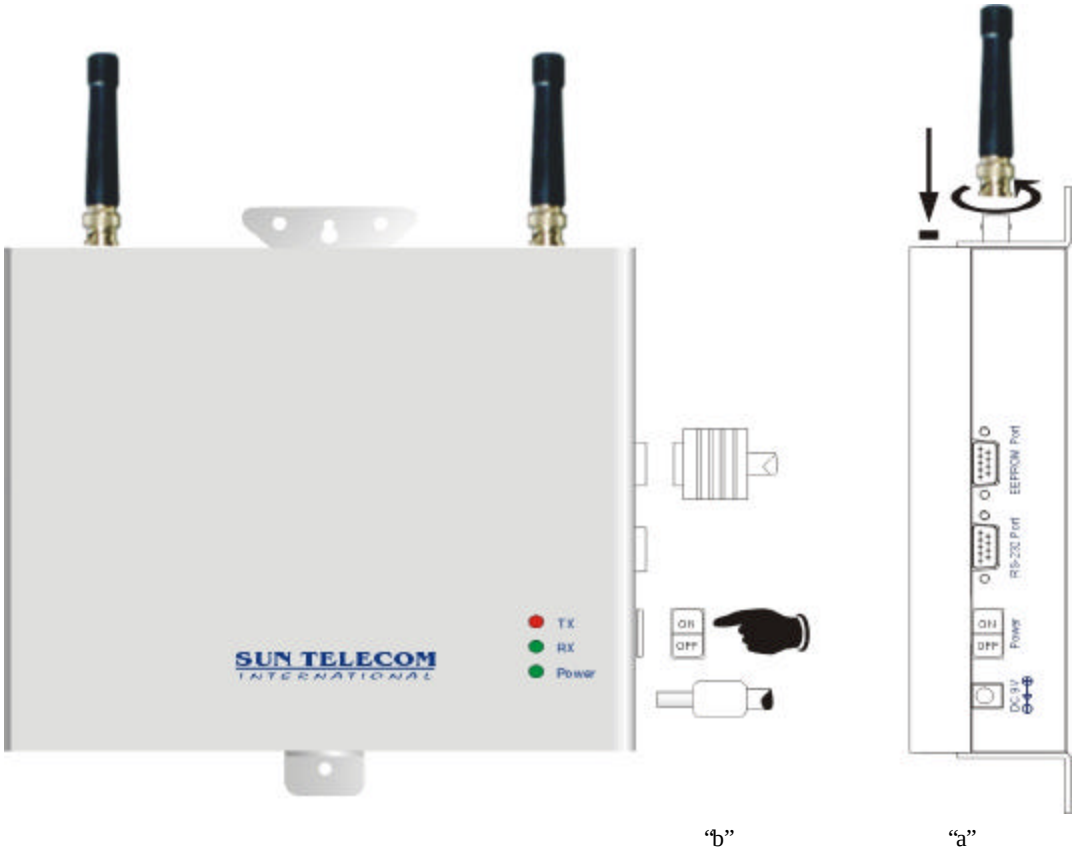
Main Unit Installation

Using an enhanced screw above 3M heights, Fix HWM -WC1000

Also HWM -WC1000 needs power cable within 3M for power supply.

.

1. Assemble the antenna like “a” in picture 2-1.



“b” “a”

PICTURE 2-1

2. Connecting the power adapter to power cable, Insert D/C output to D/C port like ‘b’ in picture 2-1.
3. Turn Main Unit power switch on.

When power is supplied, power lamp turns on.

When Main Unit receives data from Table Unit (HWM -TT1000), RX Lamp turns on.

When Main Unit transfers data to Pager, TX Lamp turns on.

Technical Circuit Description (HWM-WC1000)

1 Main Logic Board

UD1 (80C32)

80C32 is compatible with 80c51 in pin composition (8bit Micro controller), but 80c32 uses external ROM instead of internal ROM..

It processes data received from 89LV52 of Table Unit & Server Call Unit.

All the data is processed by Pocsag Encoding, transferred to Pager Unit by wireless, and transferred to Host Unit by RS -232C.

80C32 use port 0, & port 2 for address bus, and port 0 for data bus.

So, port 0 (pin 32~39) is used for being placed above 8bit(A0~A7) of address, and for data bus (D0~D7).

Port 2(pin21~280) is used for being placed below 8bit(A8~a15) of address.

Also, using 74HC373(Octal 3-state latches) from external, divide data bus and address bus.

As clock signal, used for ALE(Address Latch Enable, pin 30) to active high,

When interfaced with external memory component, it is used for being placed below address to latch.

U1 (89LV52)

Possesses the same characteristics as 80C32, the system, used 2 of RX Main Unit.

The transferred data From Table Unit & SCU, divide channel and receive independently.

Received data from each channel through error check, and pass DS1609(Dual Port RAM) to transfer to TX 80C32 of HWM -WC1000

UD3 (M27C512)

Eprom(Erasable Electrically Programmable Read Only Memory) 27C512 supports UV (Ultra Violet erase) & OTP(One Time Programmable). This is supported 45ns access

Time, and had 8 of in/output and 64Kbyte.

Main function of Eprom M27C512, input actual program of HWM -WC1000 and operate

as external program memory of 80C32.

As clock, to active low PSEN(Program Strobe Enable) and read data from external program memory

PSEN is printed 2 times in each Machine Cycle, port 0 is used for address in ALE Falling Edge.

Also, 8Kbyte internal Rom is inside 8052 but to connect EA(External Access Enable, pin 31) with ground for using 64Kbyte External Program Memory.

UD4 (62256)

External Data Memory 62256 has 8 of in/ouput and 32Kbyte as SRAM(Static Random Access Memory).

It is used for operating external RAM.

Until $A_0 \sim A_{13}$, has input address, and until , $I/O_7 \sim I/O_0$ has 8 data bus.

/OE(out Enable) is connected 8052 /RD, and operates when active low. Also, /WE (Write Enable) pin is connected 8052 /WD, and write when active low.

All of the work can operate when /CS(Chip Select) low.

UD6 (8255)

It calls PPI(Programmable Peripheral Interface), and common in/ output LSI for using with Intel Micro Processor. 8255 has 8bit of in/output port of 3 port(A,B,C), for lack of 80C32 port to easily control in outside.

Total 24bit port divide group A(port A, port $C_4 \sim C_7$) and group B(port B, port $C_0 \sim C_3$) to independently setup operating mode(mode0, mode1, mode2).

To decide & control print port to using A_0, A_1, CS(Chip Select)

UD11 (DS1609)

DS1609 is 256byte Dual Port RAM, receiving SCU & Table unit data from RX part 89LV52 of HWM-WC1000 are used when transferred to HWM -WC1000-TX part 80C32. Also it use a buffer.

It has 2 asynchronous address/data bus. Each port is controlled by /OE(Output Enable, /WE(Write Enable), /CE(Port Enable).

$AD_0 \sim AD_7$ are Port address/data.

UD7 (93C66)

E^2PROM 93C66 has 255~word*16bit. This is for when power is off, saving information before power off and initial information.

Can read & write data anytime by electrical signal, CS means Chip Select Input,

SK means Serial Clock Input, DI means Serial Data Input, DO means Serial Data Output.

UD9 (MAX-232)

This component is for communicating with Host Unit & RS232C.

It can change 5V Digital Level to 12V RS 232C or reverse it.

UD5 (74HC138)

74HC138 is Memory Decoder/Demultiplexer CMOS, for expanding lack port of 80C32

to use 80C32 address and generating CE(Chip Enable) signal to control in/output data of 8255, 62256 or DS1609.

It controls active low Output($Y_0 \sim Y_7$) by $A_0 \sim A_2$ 3bit Input.

The condition is Chip Enable Pin CS_1 High, and CS_2 & CS_3 Low.

UD2 (74HC373)

When it interfaces External Memory, controlled signal of address bus is needed, data bus, /RD and /WR,

From 80C32, port0, port2 are used address bus, to need port 0 for data bus

But, 80C32 port 0 used together address bus & data bus so, to use 74HC373

(Octal 3-state Latch) from outside, and latch printing address before data.

Finally, can use dividing address & data. That time clock signal use ALE.

. $D_0 \sim D_7$ are Data Input, $Q_0 \sim Q_7$ are Non-Inverting Output

2 RX Unit

LNA

The frequency from antenna only pass range of saw filter F1(DF430) -430MHz +/-4MHz and amplify gain from LNA circuit Q7,Q8 L1,C3,R1,C4.

Local Circuit

(PLL Synthesizer , Data Modulation .Loop)

PLL is consists of 3 parts, from Main Board UD1, frequency data input to PLL IC 11,12 and 13 pin.

PLL IC is received frequency from reference crystal (X1) 12.8MHz and divided 12.5KHz by reference divider.

Fixed voltage come from PLL IC Pin 5, passed through loop filter B3,R64, C119,R62 and C82

And approve VCO (D1,C18,L11,VC4,C21,Q5,L7),

next, oscillate relevant voltage, next, the voltage are inputted to PLL IC through C87,
next, divided at programmable divider where is in PLL IC, next, compare phase in Phase comparator, finally, revise error and offer an output to Pin 5(charge pump).

- Frequency Multiplier & Power AMP

The frequency from VCO circuit is 2 multiple in Multiplier Q13,L9,C86,R66.
PLL Frequency Band (430 +/- 2MHz)

Mixer Circuit

Gain amplified receiving frequency & local frequency from LNA are inputted to
Mixer Circuit (Q1,L1,R2, C14,C9) then made 1st IF 21,4 MHz it passed crystal filter F3
after, inputted to IF IC (IC1).

IF IC

Centered frequency 21.4MHz through IF Filter, to input to IF 20 pin(MIX IN),
2nd Local Crystal 20.945 MHz is mixed in 2nd Mixer of IF IC and made 2nd IF 455 KHz
and printed to Pin 3(MIX OUT) through ceramic filter (F7), to input to Pin 5(IF IN)
after gain amplified in limiting IF amplifier of internal IC,
through Quad detector in internal IC, to print real audio signal from Pin9(AF Out),
Pass again, low pass (R14,R16,R69,C121,C12,C45), to input to Pin 11(LPF IN)
and to print to Pin 12(LPF OUT). Also, filtering audio signal
is passed FSK comparator in internal IC, then changed to 2level quad type
and transferred receiving MPU of Main Board

3 TX Module

PLL Synthesizer , Data Modulation .Loop

PLL consists of 3 parts. (PLL Synthesizer, Data Modulation, Loop)

From Main Board UD1, PLL frequency data input to PLL IC(IC2) 11,12 and 13 pin.

PLL IC is received frequency from reference crystal (X1) 12.8MHz and divided 12.5KHz by the reference divider.

Fixed voltage come from PLL IC Pin 5, passes through loop filter C16,R18,R19, C17 and C18.

And approve VCO (D1,C19,LW1,VC2,C20,Q3,LW2),

next, oscillate relevant voltage, next, the voltage are inputted to PLL IC through C26,

next, divided at programmable divider where is in PLL IC, next, compare phase in Phase comparator, finally, revises errors and offer an output to Pin 5(charge pump).

Frequency Multiplier & Power AMP

The frequency from VCO circuit is 2 multiple in Multiplier Q4,L3,R24.

PLL Frequency Band (430 +/- 2MHz)

2 multiple carrier frequency is passes band pass filter, after, gain amplified in Amp1 Q5, Q6, passed saw filter and transferred to antenna.