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A Global Leading IoT Terminals And Wireless Data Solutions Provider

MA922 Hardware Design Manual

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EU Conformity Statement

CE Hereby, [MeiG Smart Technology Co.,Ltd] declares that the radio equipment type [MA922] is in compliance with Directive 2014/53/EU.

RF Exposure Information

This device has been tested and meets applicable limits for Radio Frequency (RF) exposure. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

FCC Statement:

Please take attention that changes or modification not expressly approved by the party res ponsible for compliance could void the user's authority to operate the equipment.
This device complies with Part 15 of the FCC Rules. Operation is subject to the following t wo conditions:
(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cau se undesired operation.
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

(1)Operational use conditions

Module has professional users use condition limitations, Host product manufacturer please ensure giving such warning like “Product is limited to professional users use” in your prod uct’s instruction.

（2）Antenna used

Antenna Type: External antenna
Max. Gain: 5.29dBi

（3）Labelling Instruction for Host Product Integrator

Please notice that if the FCC identification number is not visible when the module is install ed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. For FCC, this exterior label sho uld follow “Contains FCC ID: 2APJ4-MA922”. In accordance with FCC KDB guidance 78474 8 Labeling Guidelines.
§15.19 and RSS-Gen Labelling requirements shall be complied on end user device. Labell ing rules for special device, please refer to §2.925, § 15.19 (a)(5) and relevant KDB public ations. For E-label, please refer to §2.935.

（4）Installation Notice to Host Product Manufacturer

The OEM integrator is responsible for ensuring that the end-user has no manual instructio n to remove or install module.
The module is limited to installation in mobile application, a separate approval is required f or all other operating configurations, including portable configurations with respect to §2.10 93 and difference antenna configurations.

(5)Antenna Change Notice to Host manufacturer

If you desire to increase antenna gain and either change antenna type or use same antenn a type certified, a Class II permissive change application is required to be filed by us, or yo u (host manufacturer) can take responsibility through the change in FCC ID and IC ID (ne w application) procedure followed by a Class II permissive change application.

(6)FCC other Parts, Part 15B Compliance Requirements for Host prod uct manufacturer

This modular transmitter is only FCC authorized for the specific rule parts listed on our gra nt, host product manufacturer is responsible for compliance to any other FCC rules that ap ply to the host not covered by the modular transmitter grant of certification.

Host manufacturer in any case shall ensure host product which is installed and operating with the module is in compliant with Part 15B requirements.

Please note that For a Class B or Class A digital device or peripheral, the instructions furnished the user manual of the end-user product shall include statement set out in §15.105 Information to the user or such similar statement and place it in a prominent location in the text of host product manual. Original texts as following:

For Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

For Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Revision History

Serial Number	Revision	Date	Description
1	V1.00	2023-11	First edition
2	V1.01	2024-4	1. sheet74，3.14_SPI：correct SPI I/O type to DIO, add SPI Master and Slave mode Description 2. 3.3 pin Description: correct SPI I/O type to DIO 3. Sheet77，3.15_RGMII：correct RGMII layout line Tx bus and Rx bus traces at least 2 times trace width. 4. Sheet65，3.9_I2C\I2S: reflash I2C/I2SDescription ,add I2C1&I2S1 default for Audio codec 5. Sheet 56, 3.4.2 Reduce Voltage Drop:pitcure6,correct DC_IN to DC_3.8V
3	V1.02	2024-6	1. Reflash 2.2 main performance about PCI Express Base Specification Revision 2. Reflash 3.11 PCIE Interfaces Compliant with PCI Express Base Specification Revision 3. Reflash 3.11 PCIE Interfaces,about PCIE data rate 4. Reflash 3.11 PCIE Interfaces, about PCIE AC coupling capacitance change to 220nF. 5. Reflash 3.11 PCIE Interfaces, about PCIE Bus length change to 300mm. 6. Reflash 5.3 module power consumption,add power off leakage current data and Deep sleep mode minimum current data。 7. Reflash IMPORTANT NOTICE,add EU Conformity Statement and FCC Statement

Content

1. Introduction

This document introduces MA922 and the air interface and hardware interface between module and customer application.

This document can help customers quickly understand MA922 module interface specifications, electrical characteristics, mechanical specifications and related product information. With the help of this document, combined with our application manual and user guide, customers can quickly apply the MA922 module to wireless applications.

MA922 wireless module is a broadband wireless terminal product suitable for TDD-LTE/FDD-LTEG/5GNR multiple network standards and multiple frequency bands.

Except wireless data access, MA922 can provide functions such as voice and SMS, and can be widely used in M2M fields, such as OTT, CPE, routers, data cards, tablet computers, security and industrial-grade PDAs.

1.1 Safety Instruction

You can ensure personal safety and help protect your product and work environment from potential damage by following the following safety principles:

	Driving safety first! When you are driving, do not use a handheld mobile terminal unless it has a hands-free function. Please stop and call again!
	Please turn off your mobile terminal device before boarding. The wireless function of the mobile terminal is prohibited to be turned on on the aircraft to prevent interference with the aircraft communication system. Ignoring this reminder may lead to flight safety or even breaking the law.
	In hospitals or health care facilities, pay attention to whether there are restrictions on the use of mobile terminal devices. RF interference can cause medical equipment to malfunction, so mobile terminal equipment may need to be turned off.
	The mobile terminal device cannot be effectively connected under any circumstances, there is no call charge or the SIM is invalid in the mobile device. When you encounter the above situation in an emergency, please remember to make an emergency call, and make sure your device is turned on and in an area with sufficient signal strength.
	Your mobile terminal device receives and transmits radio frequency signals when it is turned on. Radio frequency interference may occur when near televisions, radios, computers or other electronic equipment.
	Keep mobile devices away from flammable gases. When you are near gas stations, oil depots, chemical plants or explosive workplaces, please turn off the mobile terminal equipment. Operating electronic equipment in any potentially explosive location is a safety hazard.

1.2 Document Purpose

This file elaborates the basic functions, main features, hardware interface and its use method, structural characteristics, power consumption index and electrical characteristics of MA922 wireless module in detail, and guides users to apply MA922 module to various application terminals.

1.3 Content

This article is divided into the following parts:

- Chapter 1 mainly introduces security instructions, document purpose, revision history, etc.;
- Chapter 2 describes the basic functions and main features of MA922 wireless module;
- Chapter 3 describes the functions, characteristics and usage of each hardware interface in detail;
- Chapter 4 related information and precautions of antenna interfaces ;
- Chapter 5 describes MA922 electrical characteristics in detail;
- Chapter 6 describes in detail the features and precautions of MA922 structure;
- Chapter 7 describes in detail MA922 precautions in storage and production ;
- Chapter 8 Appendix A Reference Documents and Term Abbreviations;

2. Product Overview

2.1 Basic Description

The MA922 is a 5GNR, Sub-6 GHz wireless communication module with 5GNR, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS network functions. It also has single/dual frequency, GNSS and voice capabilities for specific applications.

The MA922 module supports the following frequency bands.

FCC

- 5GNR: n2/n5/n12/n25/n41/n66/n71/n77/n78
- TDD-LTE: B41
- FDD-LTE: B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B30RX/B66/B71
- WCDMA: B2/B4/B5
- GNSS (optional)
- Single-frequency GNSS: L1 (GPS, GLONASS, BDS, Galileo, QZSS)
- Dual-frequency GNSS: L1 + L5 (GPS, GLONASS, BDS, Galileo, QZSS)

Module size: 54.5mm x 53.0mm x 3.45mm, which can basically cover all application scenarios of the car. The module is designed to meet the demanding requirements of automotive applications and other harsh conditions, providing premium solutions for safe and reliable connected car solutions and autonomous driving solutions. It is widely used in T-Boxes, TCU, ADAS, C-V2X (V2V, V21, V2P), OBU, RSU, and other automotive/traffic systems.

2.2 Main Performance

The following table shows the performance of MA922 module.

Table 1 List of main features of module

Parameter	Description
Power	VBAT_BB/VBAT_RF: □ Supply voltage range: 3.5 V～ 4.2 V □ Typical supply voltage: 3.8V VPH_5V_V2X □ Supply voltage range: 4.75 ～ 5.25 V □ Typical supply voltage: 5.0V
Transmit power	Class 2 (26 dBm +1/-2 dB) for 5G NR TDD HPUE n41/n77/n78/n79 bands Class 3 (23 dBm ±2 dB) for 5G NR FDD bands Class 3 (23 dBm ±2 dB) for LTE bands Class 3 (23 dBm ±2 dB) for WCDMA bands Class 4 (33 dBm ±2 dB) for EGSM900 Class 1 (30 dBm ±2 dB) for DCS1800 Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK
5G NR Features	Support 3GPP Rel-16 Support modulations: Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM Downlink: QPSK, 16QAM, 64QAM and 256QAM Support 4 × 4 MIMO for MHB bands in DL direction Support SCS 15 kHz (FDD) and 30 kHz (TDD) Support Option 3x, 3a and Option 2 Support SA and NSA Max. transmission data rates: NSA: 2.4 Gbps (DL)/550 Mbps (UL) SA: 2.0 Gbps (DL)/450 Mbps (UL)
LTE Features	Support up to 4CA Cat 16 Support 1.4/3/5/10/15/20 MHz RF bandwidth Support 4 × 4 MIMO in DL direction Support modulation mode: Uplink: QPSK, 16QAM, 64QAM, 256QAM* Downlink: QPSK, 16QAM, 64QAM, 256QAM LTE-FDD: Max. 1.2 Gbps (DL)/100 Mbps (UL) LTE-TDD: Max. 1.0 Gbps (DL)/60 Mbps (UL)
GSM Features	GPRS: Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS 1–4 Max. 107 kbps (DL)/85.6 kbps (UL) EDGE: Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: MCS 1–9 Uplink coding schemes: MCS 1–9 □ Max. 296 kbps (DL)/236.8 kbps (UL)

GNSS Features	Support GPS, GLONASS, BDS, Galileo, QZSS Support dual-frequency GNSS (L1 + L5) Agreement: NMEA 0183 Update rate: 1 Hz by default, max. up to 10 Hz
C-V2X Features	Support C-V2X TDD up to 30 Mbps (Tx)/30 Mbps (Rx) Support globally unified ITS @ 5.9 GHz
Network protocol characteristics	TCPIP/UDP/HTTP(S)/MQTT/FTP/SSL/OneNet
Short message (SMS)	Text and PDU mode Point-to-point MO and MT Cell broadcast
USIM Card interface	Support U/SIM1(2) card: 1.8V and 3V
I2S interface	Default for external codec configuration Supports the master-slave mode
I2C interface	Default for external Codec and IMUs Complies with I2C 3.0 bus specifications Multiple host modes are not supported
PCM interface	Can be used for audio use, requires an external Codec chip Default for Bluetooth audio data transmission Supports 16-bit data format Supports long frame synchronization and short frame synchronization Supports the master-slave mode
USB interface	Conforms to the USB 3.1 Gen 2 and USB 2.0 specifications, the maximum theoretical transfer rate of USB 3.1 can reach 10Gbps, and the maximum theoretical transfer rate of USB 2.0 can reach 480Mbps USB 2.0 and USB 3.1 are used for AT command communication, data transfer, software debugging, and GNSS NMEA statement output The firmware can be upgraded by USB 2.0 or USB3.1 When USB 2.0 and USB 3.1 are connected to the same host, the USB 3.1 port is used by default USB driver: Support Windows 7/8/8.1/10/11, Linux 2.6-5.18 and Android 4.x-12.x
Serial port	UART1: Used for AT command and data transmission For data transmission Baud rate up to 921600 bps, the default is 115200 bps Support RTS and CTS hardware flow control Bluetooth UART: For data transmission; The default value is Bluetooth Baud rate up to 921600 bps, the default is 115200 bps Support RTS and CTS hardware flow control Debug UART: For Linux console and log output The default baud rate is 115200bps

SDIO interface	□ Comply with SD3.0 protocol □ Supports eMMC and SD card or DSRC
SPI interface	□ Two SPI interfaces are supported by default □ Clock frequency Upper limit: 50MHz
RGMII interface	□ 2.5Gbps Ethernet connection is supported
USXGMI interface	□ USB interface
WLAN and Bluetooth interface	□ WLAN supports the PCIe (Gen 3) interface □ Supports Bluetooth UART and PCM interfaces
PCIe Interface	□ Supports two groups of PCIE ports □ Conforms to PCI Express Base Specification Revision 3.0 （PCIE1&2） and Revision 4.0 (PCIE1) □ Supports one set of 2-lane Pcles with a theoretical maximum speed of 8GT /s x 1-lane □ The WLAN function is used by default □ Supports one group of 1-lan PCIe with a theoretical maximum rate of 8GT /s
Audio function	□ GSM: HR/FR/EFR/AMR/AMR-WB □ WCDMA: AMR/AMR-WB □ LTE: AMR/AMR-WB □ Supports echo cancellation and noise suppression
AT command	□ Comply with 3GPP TS 27.007, 27.005, and add MeiG AT command
Antenna interface	□ Main antenna interface (ANT_MAIN) □ RX- Hierarchical Antenna Interface (ANT_DIV) □ Two MIMO antenna interfaces (ANT_MIMO3,ANT_MIMO4) □ Two C-V2X interfaces (ANT_CV2X_TRX0,ANT_CV2X_TRX1) □ One GNSS antenna interface (ANT_GNSS)
Physical characteristics	□ Dimensions: (54.5±0.2)×(53.0±0.2)×(3.45±0.2)mm □ Weight: TBD
Temperature range	□ Normal working temperature: -35℃ ~ +75℃ □ Extended temperature: -40℃ ~ +85℃ □ Storage temperature: -40℃ ~ +95℃
Software upgrade	□ USB 2.0/USB 3.1 □ DFOTA
RoHS	□ All devices are fully compliant with EU RoHS standards
Ambient humidity	□ 5%~95%
Interface	□ 524 LGA Pins
LGA function interface	□ Power interface □ USIM/SIM card interface (support 3V, 1.8V) □ I2S interface □ I2C interface □ PCM interface □ USB2.0 and USB3.1 interfaces □ UART interface □ SDIO interface

	▯ SPI interface ▯ RGMII&SGMII&USXGMII interface ▯ PCIe interface (can be used for external WLAN&BT modules) ▯ ADC interface ▯ Hardware boot and reset interface ▯ Dormancy indication interface ▯ GPIO port ▯ USB_BOOT Indicates the interface

2.3 Functional Block Diagram

The following is the block diagram of MA922, explaining its main function part.

- Power management unit
- Baseband unit
- Built-in memory
- RF part
- Peripheral interface

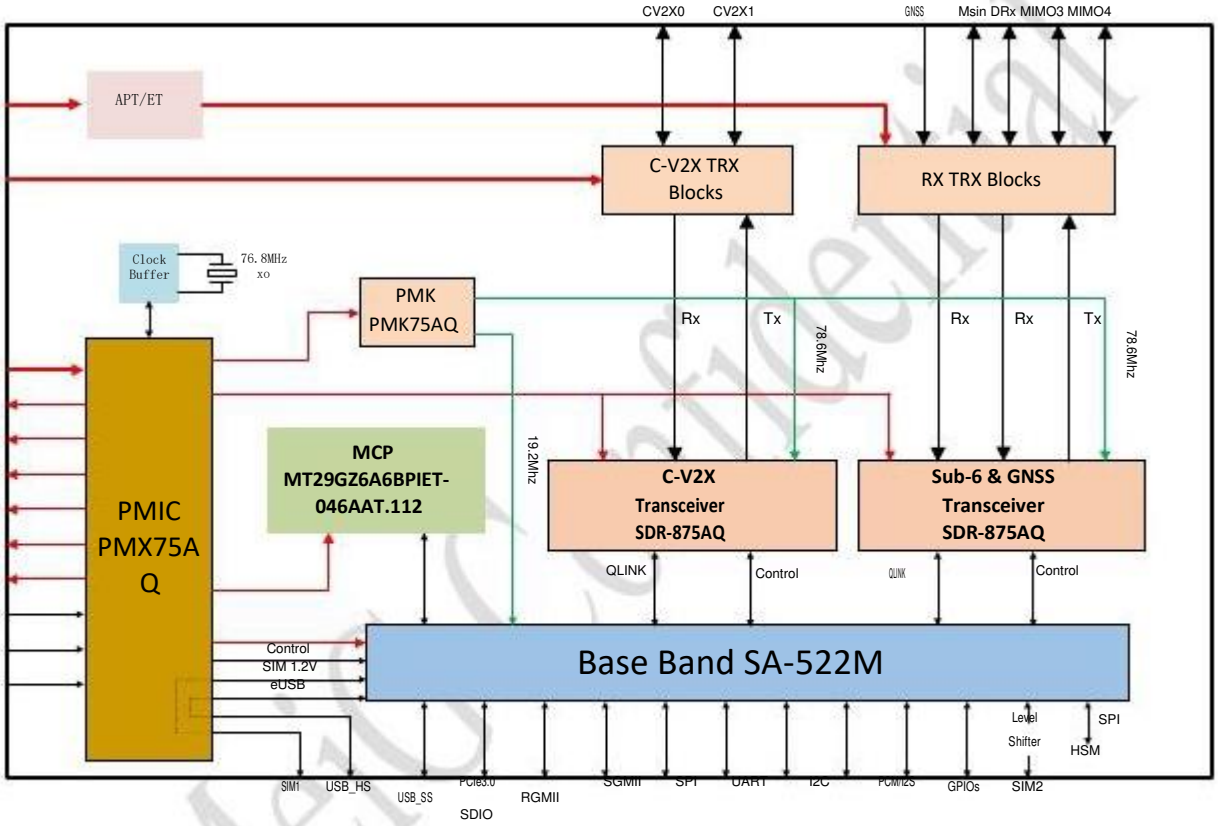


Figure 1 Functional block diagram

2.4 Evaluation Board

For testing and use of MA922, MeiG provides a set of evaluation boards, including USB cables, antennas, and other peripherals.

Please refer to the “MA922_USB_EVB User Manual” for the specific usage of the evaluation board.

3. Application Interface

3.1 Basic Description

MA922 adopts 80 pin LCC+64 pin LGA package, providing the following functional interfaces:

- Power interface
- USIM/SIM interface (support 3V, 1.8V) *2
- I2S port *2
- I2C interface *2
- PCM interface
- USB2.0 and USB3.1 interfaces
- UART interface *5
- SDIO Interface *2
- SPI interface *2
- RGMII&SGMII&USXGMII interface
- PCIe port *2 (can be used for external WLAN&BT modules)
- ADC interface *3
- Hardware boot and reset interface
- Dormancy indication interface
- GPIO port *15
- USB_BOOT Indicates the interface

3.2 LGA Interface Definition

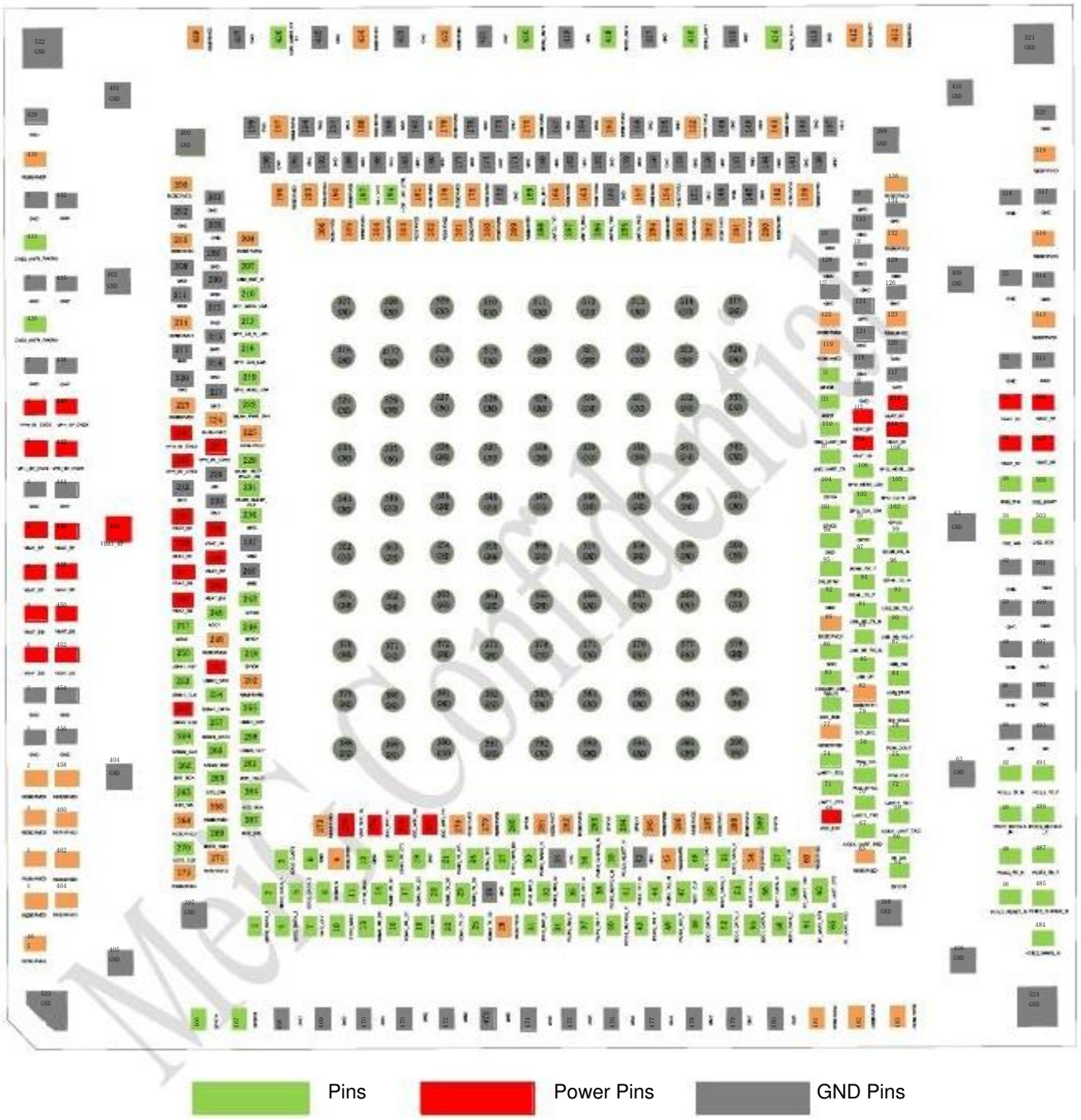


Figure 2 Module serial number pin diagram

Remark:

Module serial number pin diagram is the actual wiring name inside the module;

3.3 Pin Description

The following table shows the definition of each pin of MA922 module.

Table 2 IO parameter definition

No.	Name	I/O	Electrical Level	Description	Remark
1	SDC2_DATA_0	DIO	V_{IH}min = 1.27 V V_{IH}max = 2.0 V V_{IL}max = 0.58 V V_{OH}min = 1.4 V	SDIO2 data bit 0	1.8 V power domain
2	SDC2_DATA_1	DIO		SDIO2 data bit 1	
3	SDC2_CLKFB	DIO		SDIO2 data strobe	
4	SDC2_DATA_2	DIO		SDIO2 data bit 2	
5	SDC2_DATA_3	DIO		SDIO2 data bit 3	
6	GND	G		GND	

Table 3 Pin Description

Type	Description
IO	Input and output bidirectional signal.
DI	Digital input signal.
DO	Digital output signal.
OD	Open-drain output signal.
AI	Analog signal input
BOT	Bidirectional signal with open-drain output.
PI	power input.
PO	Power Output.
G	Ground

7	PWR_KEY	DI		Turn on/off the module	Valid low level
8	RESIN_N	DI		Reset the module	Valid low level
9	RESERVED				
10	ETH0_MDIO	DIO	V_{IH}min = 1.17 V V_{IL}max = 0.63 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Ethernet data	Close to external PHY plus pull-up resistor
11	ETH0_MDC	DO		Ethernet clock	
12	GND	G		GND	
13	RGMII_RX_D0	DI		RGMII receive data bit 0	
14	RGMII_RX_D1	DI		RGMII receive data bit 1	
15	RGMII_RX_CTL	DI		RGMII receive control	
16	RGMII_RX_D2	DI		RGMII receive data bit 2	
17	RGMII_RX_D3	DI		RGMII receive data bit 3	
18	GND	G		GND	

19	RGMII_RXC	DI		RGMII receive clock	
20	RGMII_TX_D0	DO		RGMII transmit data bit 0	
21	RGMII_TX_CTL	DO		RGMII transmit control	
22	RGMII_TX_D1	DO		RGMII transmit data bit 1	
23	RGMII_TX_D2	DO		RGMII transmit data bit 2	
24	RGMII_TXC	DO		RGMII transmit clock	
25	RGMII_TX_D3	DO		RGMII transmit data bit 3	
26	GND	G		GND	
27	ETH1_PWR_EN	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Enable external power supply to power Ethernet PHY	
28	RESERVED				Keep pin open
29	ETH0_INT_N	DI	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Ethernet PHY interrupt input	
30	PCIE0_WAKE_N	DIO		PCIe wake up	Input in RC mode, output in EP mode

31	ETH0_RST_N	DO		Reset output for Ethernet PHY	
32	PCIE0_RX0_M	AI		PCIE0_RX0_M	
33	GND	G		GND	
34	PCIE0_RX0_P	AI		PCIE0_RX0_P	
35	PCIE0_RX1_M	AI		PCIE0_RX1_M	
36	PCIE0_CLKREQ_N	DIO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	PCIe1 clock request	Input in RC mode, output in EP mode
37	PCIE0_RX1_P	AI			
38	PCIE0_REFCLK_M	AIO		PCIE0_REFCLK_M	Input in RC mode, output in EP mode
39	PCIE0_RESET_N	DIO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V		
40	PCIE0_REFCLK_P	AIO		PCIE0_REFCLK_P	
41	PCIE0_TX1_M	AO		PCIE0_TX1_M	
42	GND	G		GND	

43	PCIE0_TX1_P	AO		PCIE0_TX1_P	
44	PCIE0_TX0_M	AO		PCIE0_TX0_M	
45	RESERVED				Keep pin open
46	PCIE0_TX0_P	AO		PCIE0_TX0_P	
47	SDC1_CLK	DO	$V_{IH}min$ = 1.27 V $V_{IH}max$ = 2.0 V $V_{IL}max$ = 0.58 V $V_{OH}min$ = 1.4 V $V_{OL}max$ = 0.45 V	SDIO1 clock	1.8 V power domain.
48	SDC1_CMD	DIO		SDIO1 command	
49	SDC1_DATA_0	DIO		SDIO1 data bit	
50	SDC1_DATA_1	DIO		SDIO1 data bit	
51	SDC1_DATA_2	DIO		SDIO1 data bit	
52	SDC1_DATA_3	DIO		SDIO1 data bit	
53	SDC1_DATA_4	DIO		SDIO1 data bit	
54	RESERVED				Keep pin open

55	SDC1_DATA_5	DIO	V_{IH}min = 1.27 V V_{IH}max = 2.0 V V_{IL}max = 0.58 V V_{OH}min = 1.4 V V_{OL}max = 0.45 V	SDIO1 data bit	1.8 V power domain.
56	SDC1_DATA_6	DIO		SDIO1 data bit	
57	SDC1_DS	DIO		SDIO1 data strobe	
58	SDC1_DATA_7	DIO		SDIO1 data bit	
59	BT_UART_TXD	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Bluetooth UART transmit	1.8V power domain, suspended if not used
60	RESERVED				Keep pin open
61	BT_UART_RTS	DI	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Module Bluetooth receive data Receive slave device RTS	1.8V power domain, suspended if not used
62	BT_UART_CTS	DO		Module Bluetooth receive data Receive slave device CTS	
63	BT_UART_RXD	DI		Bluetooth UART receive	
64	GPIO13	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
65	RESERVED				Keep pin open
66	BT_EN	DO	VIHmin = 1.17 V VILmax = 0.63 V VOHmin = 1.44 V VOLmax = 0.36	Bluetooth enable control	

67	COEX_UART_RXD	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	LTE & WLAN & Bluetooth coexistence UART receive	
68	VDD_EXT	PO	VIHnom=1.8V I_{Omax} = 50 mA	Provide 1.8 V for external circuits	Power supply for external pull up circuits.
69	COEX_UART_TXD	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	LTE & WLAN & Bluetooth coexistence UART transmit	
70	UART1_TXD	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	UART1 transmit	1.8V power domain, suspended if not used
71	UART1_CTS	DO		DTE clear to send signal from DCE (Connects to DTE's CTS)	
72	UART1_RXD	DI		UART1 receive	
73	PCM_SYNC	DIO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	PCM data frame sync	1.8V power domain, master mode output, slave mode input
74	UART1_RTS	DI		DTE request to send signal to DCE (Connects to DTE's RTS)	1.8V power domain, suspended if not used
75	PCM_CLK	DIO		PCM clock	1.8V power domain, master mode output, slave mode input
76	PCM_DIN	DI		PCM data input	1.8 V power domain.
77	RESERVED				Keep pin open
78	PCM_DOUT	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	PCM data output	1.8 V power domain.

79	I2C1_SCL	OD	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	I2C1 serial clock	External pull-up resistors are required. 1.8V power domain, suspended if not used.
80	I2C1_SDA	OD		I2C1 serial data	
81	I2S_MCLK	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Clock output for codec	12.288 MHz clock output
82	RESERVED				Keep pin open
83	FORCED_USB_BOOT	DI	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Force download	High level active, recommended to reserve a test point.
84	USB_VBUS	AIO	Vnom=5.0V	USB connection detect	recommended to reserve a test point.
85	USB_DP	AIO		USB 2.0 DP	
86	GND	G		GND	
87	USB_DM	AIO		USB 2.0 DM	
88	USB_SS_RX_M	AI		USB 3.1 Receiving signal cable RX_M	
89	RESERVED				Keep pin open
90	USB_SS_RX_P	AI		USB 3.1 Receiving signal cable RX_P	

91	USB_SS_TX_M	AO		USB 3.1 Transmission signal cable TX_M	
92	GND	G		GND	
93	USB_SS_TX_P	AO		USB 3.1 Transmission signal cable TX_P	
94	SGMII_TX_P	AO		SGMII_TX_P	
95	DR_SYNC	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Dead reckoning sync	
96	SGMII_TX_M	AO		SGMII_TX_M	
97	SGMII_RX_P	AI		SGMII_RX_P	
98	GND	G		GND	
99	SGMII_RX_M	AI		SGMII_RX_M	
100	GPIO1	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
101	GPIO2	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
102	GPIO3	DIO	VILnom=0V VIHnom=1.8V	GPIO	Not support wake-up interrupt.

103	SPI2_CLK_LGA	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	SPI2 clock	Supports SPI Master and Slave mode .
104	GPIO4	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
105	SPI2_CS_N_LGA	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	SPI2 chip select	Supports SPI Master and Slave mode .
106	SPI2_MISO_LGA	DI		SPI2 master-in slave-out	Supports SPI Master and Slave mode .
107	DBG_UART_TX	DO		Debug UART transmit	1.8V power domain, suspended if not used.recommended to reserve a test point.
108	SPI2_MOSI_LGA	DO		SPI2 master-out slave-in	Supports SPI Master and Slave mode .
109	VBAT_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	
110	DBG_UART_RX	DI	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Debug UART receive	1.8V power domain, suspended if not used.recommended to reserve a test point.
111	VBAT_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	
112	VBAT_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	
113	ADC2	AI	Voltage range: 0–1.875 V	General-purpose ADC interface	

114	VBAT_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	
115	GND	G		GND	
116	GPIO5	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
117	GND	G		GND	
118	GND	G		GND	
119	RESERVED				Keep pin open
120	GND	G		GND	
121	GND	G		GND	
122	RESERVED				Keep pin open
123	RESERVED				Keep pin open
124	GND	G		GND	
125	GND	G		GND	

126	GND	G		GND	
127	GND	G		GND	
128	GND	G		GND	
129	GND	G		GND	
130	GND	G		GND	
131	GND	G		GND	
132	RESERVED				Keep pin open
133	GND	G		GND	
134	GND	G		GND	
135	GND	G		GND	
136	RESERVED				Keep pin open
137	GND	G		GND	

138	GND	G		GND	
139	RESERVED				Keep pin open
140*	GND	G		GND	
141	GND	G		GND	
142	RESERVED				Keep pin open
143	RESERVED				Keep pin open
144-151	GND	G		GND	
152	RESERVED				Keep pin open
153	GND	G		GND	
154	RESERVED				Keep pin open
155	GND	G		GND	
156	GND	G		GND	

157	RESERVED				Keep pin open
158	GND	G		GND	
159	GND	G		GND	
160	GND	G		GND	
161	RESERVED				Keep pin open
162	GND	G		GND	
163	RESERVED				Keep pin open
164	GND	G		GND	
165	GND	G		GND	
166	RESERVED				Keep pin open
167	GND	G		GND	
168	GND	G		GND	

169	IMU_INT1	DI	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	IMU interrupt 1	
170	RESERVED				Keep pin open
171	GND	G		GND	
172	GND	G		GND	
173	GND	G		GND	
174	GND	G		GND	
175	RESERVED				Keep pin open
176	GND	G		GND	
177	GND	G		GND	
178	RESERVED				Keep pin open
179	RESERVED				Keep pin open
180	GND	G		GND	

181	RESERVED				Keep pin open
182	GND	G		GND	
183	GND	G		GND	
184	HOST_SW_CTRL	DI	VIHmin = 1.17 V VILmax = 0.63 V VOHmin = 1.44 V VOLmax = 0.36	Switch control	
185	GND	G		GND	
186	GND	G		GND	
187	IMU_INT2	DI	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	IMU interrupt 2	
188	RESERVED				Keep pin open
189	GND	G		GND	
190	RESERVED				Keep pin open
191	GND	G		GND	
192	GND	G		GND	

193	RESERVED				Keep pin open
194	GND	G		GND	
195	GND	G		GND	
196	RESERVED				Keep pin open
197	RESERVED				Keep pin open
198	GND	G		GND	
199	GND	G		GND	
200	RESERVED				Keep pin open
201	GND	G		GND	
202	GND	G		GND	
203	GND	G		GND	
204	RESERVED				Keep pin open

205	RESERVED				Keep pin open
206	GND	G		GND	
207	HSM_RST_N	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Reset output to external HSM	
208	GND	G		GND	
209	GND	G		GND	
210	SPI1_MOSI_LGA	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	SPI1 master-out slave-in	Supports SPI Master and Slave mode .
211	GND	G		GND	
212	GND	G		GND	
213	SPI1_CS_N_LGA	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	SPI1 chip select	Supports SPI Master and Slave mode .
214	RESERVED				Keep pin open
215	GND	G		GND	
216	SPI1_CLK_LGA	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	SPI1 clock	Supports SPI Master and Slave mode .

217	GND	G		GND	
218	GND	G		GND	
219	SPI1_MISO_LGA	DI	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	SPI1 master-in slave-out	Supports SPI Master and Slave mode .
220	GND	G		GND	
221	GND	G		GND	
222	WLAN_PWR_EN1	DO	VIHmin = 1.17 V VILmax = 0.63 V VOHmin = 1.44 V VOLmax = 0.36	WLAN power supply enable control 1	Used for Quectel AF50T VDD_RF power control.
223	RESERVED				Keep pin open
224	RESERVED				
225	RESERVED				Keep pin open
226	VPH_5V_CV2X	PI	Vmax = 5.25 V Vmin = 4.75 V Vnom = 5.0 V	Power supply for the module's C-V2X part	
227	VPH_5V_CV2X	PI	Vmax = 5.25 V Vmin = 4.75 V Vnom = 5.0 V	Power supply for the module's C-V2X part	
228	WLAN_HSTP_WLAN _EN	DO		WLAN function enable control	

229	VPH_5V_CV2X	PI	Vmax = 5.25 V Vmin = 4.75 V Vnom = 5.0 V	Power supply for the module's C-V2X part	
230	GND	G		GND	
231	WLAN_SLEEP_CLK	DO		WLAN 32 kHz sleep clock	
232	GND	G		GND	
233	GND	G		GND	
234	GND	G		GND	
235	VPH_PWR1_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	
236	VPH_PWR1_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V		
237	GND	G		GND	
238	VPH_PWR1_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	
239	VPH_PWR1_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V		
240	GND	G		GND	

241	VBAT_BB	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's baseband part	
242	VBAT_BB	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V		
243	GPIO6	DIO	VILnom=0V VIHnom=1.8V	GPIO	Not support interrupt wake-up
244	VBAT_BB	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's baseband part	
245	ADC1	AI	Voltage range: 0–1.875 V	General-purpose ADC interface	
246	GPIO7	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
247	ADC0	AI	Voltage range: 0–1.875 V	General-purpose ADC interface	
248	RESERVED				Keep pin open
249	GPIO8	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
250	USIM1_RST	DO	**For 1.8 V** VIHmin = 1.26 V VILmax = 0.36 V VOHmin = 1.44 V VOLmax = 0.4 V **For 3.0 V (U)SIM:** VIHmin = 2.1 V VILmax = 0.6 V VOHmin = 2.4 V VOLmax = 0.4 V	(U)SIM1 reset signal	
251	USIM1_VDD	PO	**For 1.8 V (U)SIM:** VOmax = 1.95 V VOmin = 1.65 V VOnom = 1.8 V **For 3.0 V (U)SIM:** VOmax = 3.05 V VOmin = 2.7 V	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.

			VOnom = 2.95 V		
252	RESERVED				Keep pin open
253	USIM1_CLK	DO	**For 1.8 V** VIHmin = 1.26 V VILmax = 0.36 V VOHmin = 1.44 V VOLmax = 0.4 V **For 3.0 V (U)SIM:** VIHmin = 2.1 V VILmax = 0.6 V VOHmin = 2.4 V VOLmax = 0.4 V	(U)SIM1 clock data	
254	USIM1_DATA	DIO	**For 1.8 V** VIHmin = 1.26 V VILmax = 0.36 V VOHmin = 1.44 V VOLmax = 0.4 V **For 3.0 V (U)SIM:** VIHmin = 2.1 V VILmax = 0.6 V VOHmin = 2.4 V VOLmax = 0.4 V	(U)SIM1 card data	
255	USIM1_DET	DI	VIHmax = 2.1 V VIHmin = 1.26 V VILmax = 0.54 V	(U)SIM1 card hotplug detect	1.8 V power domain.If unused, keep them open
256	USIM2_VDD	PO	**For 1.8 V (U)SIM:** VOmax = 1.95 V VOmin = 1.65 V VOnom = 1.8 V **For 3.0 V (U)SIM:** VOmax = 3.05 V VOmin = 2.7 V VOnom = 2.95 V	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
257	USIM2_DATA	DIO	**For 1.8 V** VIHmin = 1.26 V VILmax = 0.36 V VOHmin = 1.44 V VOLmax = 0.4 V **For 3.0 V (U)SIM:** VIHmin = 2.1 V VILmax = 0.6 V VOHmin = 2.4 V VOLmax = 0.4 V	(U)SIM2 data signal	
258	USIM2_DET	DI	VIHmax = 2.1 V VIHmin = 1.26 V VILmax = 0.54 V	(U)SIM2 card hotplug detect	1.8 V power domain.If unused, keep them open

259	USIM2_CLK	DO	**For 1.8 V** VIHmin = 1.26 V VILmax = 0.36 V VOHmin = 1.44 V VOLmax = 0.4 V **For 3.0 V (U)SIM**: VIHmin = 2.1 V VILmax = 0.6 V VOHmin = 2.4 V VOLmax = 0.4 V	(U)SIM2 clock signal	
260	USIM2_RST	DO	**For 1.8 V** VIHmin = 1.26 V VILmax = 0.36 V VOHmin = 1.44 V VOLmax = 0.4 V **For 3.0 V (U)SIM:** VIHmin = 2.1 V VILmax = 0.6 V VOHmin = 2.4 V VOLmax = 0.4 V	(U)SIM2 reset signal	
261	I2S1_DOUT	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	I2S data out	1.8 V power domain.
262	I2S1_SCK	DIO		I2S1 clock	1.8 V power domain.Serve as output signals in master mode. Serve as input signals in slave mode.
263	I2S1_DIN	DI		I2S data in	1.8 V power domain.
264	I2C2_SDA	OD	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	I2C2 serial data	External pull-up resistors are required. 1.8 V power domain.If unused, keep them open.
265	I2S1_WS	DIO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	I2S1 word select	1.8 V power domain.Serve as output signals in master mode. Serve as input signals in slave mode.
266	RESERVED				

267	I2C2_SCL	OD	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	I2C2 serial clock	External pull-up resistors are required. 1.8 V power domain.If unused, keep them open.
268	RESERVED				
269	SDC2_CMD	DO	V_{IH}min = 1.27 V V_{IH}max = 2.0 V V_{IL}max = 0.58 V V_{OH}min = 1.4 V V_{OL}max = 0.45 V	SDIO2 command	1.8 V power domain
270	SDC2_CLK	DO		SDIO2 clock	
271	RESERVED				Keep pin open
272	RESERVED				Keep pin open
273	RESERVED				Keep pin open
274	VDD_WIFI_VL	PO	Iomax = 1.7 A	Low-voltage power supply for Wi-Fi & Bluetooth modules	
275	VDD_WIFI_VL	PO	Iomax = 1.7 A	Low-voltage power supply for Wi-Fi & Bluetooth modules	
276	VDD_WIFI_VM	PO	Iomax = 450mA	Medium-voltage power supply for Wi-Fi & Bluetooth Modules	
277	VDD_WIFI_VH	PO	Iomax = 450mA	High-voltage power supply for Wi-Fi & Bluetooth Modules	

278	RESERVED				Keep pin open
279	RESERVED				Keep pin open
280	GPIO9	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
281	RESERVED				Keep pin open
282	RESERVED				Keep pin open
283	GPIO10	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
284	GPIO11	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
285	RESERVED				Keep pin open
286	RESERVED				Keep pin open
287	RESERVED				Keep pin open
288	RESERVED				Keep pin open
289	GPIO12	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.

290	RESERVED				Keep pin open
291	RESERVED				Keep pin open
292	RESERVED				Keep pin open
293	RESERVED				Keep pin open
294	RESERVED				Keep pin open
295	UART4_RXD	DI	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Receive signal	1.8 V power domain. If unused, keep these pins open.
296	UART4_TXD	DO		Transmit signal	
297	UART3_RXD	DI		Receive signal	
298	UART3_TXD	DO		Transmit signal	
299-306	RESERVED				Keep pin open
307-402	GND	G		GND	
403	VBAT_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	

404	GND	G		GND	
405	GND	G		GND	
406	GND	G		GND	
407	GND	G		GND	
408	GND	G		GND	
409	GND	G		GND	
410	GND	G		GND	
411	RESERVED				Keep pin open
412	RESERVED				Keep pin open
413	GND	G		GND	
414	SDR0_ANT0	AIO		Main antenna interface	50 Ω impedance
415	GND	G		GND	

416	SDR0_ANT1	AIO		Main antenna interface	50 Ω impedance
417	GND	G		GND	
418	SDR0_ANT2	AI		MIMO2 antenna interface	
419	GND	G		GND	
420	SDR0_ANT3	AI		MIMO3 antenna interface	
421	GND	G		GND	
422	RESERVED				Keep pin open
423	GND	G		GND	
424	RESERVED				Keep pin open
425	GND	G		GND	
426	SDR_GNSS_ANT4	AI		GPS antenna interface	
427	GND	G		GND	

428	RESERVED				Keep pin open
429	GND	G		GND	
430	RESERVED				Keep pin open
431	GND	G		GND	
432	GND	G		GND	
433	CV2X_ANT5_FAKRA	AIO		CV2X_ANT5 antenna interface	
434	GND	G		GND	
435	GND	G		GND	
436	CV2X_ANT6_FAKRA	AIO		CV2X_ANT6 antenna interface	
437	GND	G		GND	
438	GND	G		GND	
439	VPH_5V_CV2X	PI	Vmax = 5.25 V Vmin = 4.75 V Vnom = 5.0 V	Power supply for the module's C-V2X part	

440	VPH_5V_CV2X	PI			
441	VPH_5V_CV2X	PI			
442	VPH_5V_CV2X	PI			
443	GND	G		GND	
444	GND	G		GND	
445	VBAT_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	
446	VBAT_RF	PI			
447	VBAT_RF	PI			
448	VBAT_RF	PI			
449	VBAT_BB	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's baseband part	
450	VBAT_BB	PI			
451	VBAT_BB	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's baseband part	

452	VBAT_BB	PI			
453	GND	G		GND	
454	GND	G		GND	
455	GND	G		GND	
456	GND	G		GND	
457	RESERVED				Keep pin open
458	RESERVED				Keep pin open
459	RESERVED				Keep pin open
460	RESERVED				Keep pin open
461	RESERVED				Keep pin open
462	RESERVED				Keep pin open
463	RESERVED				Keep pin open

464	RESERVED				Keep pin open
465	RESERVED				Keep pin open
466	GPIO14	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
467	GPIO15	DIO	VILnom=0V VIHnom=1.8V	GPIO	Support wake-up interrupt.
468	GND	G		GND	
469	GND	G		GND	
470	GND	G		GND	
471	GND	G		GND	
472	GND	G		GND	
473	GND	G		GND	
474	GND	G		GND	
475	GND	G		GND	

476	GND	G		GND	
477	GND	G		GND	
478	GND	G		GND	
479	GND	G		GND	
480	GND	G		GND	
481	RESERVED				Keep pin open
482	RESERVED				Keep pin open
483	RESERVED				Keep pin open
484	PCIE2_WAKE_N	DIO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	PCIe wakeup	Only used in RC mode and serve as input signals in RC mode.
485	PCIE2_CLKREQ_N	DIO		PCIe clock request	
486	PCIE2_RESET_N	DIO		PCIe reset	Only used in RC mode and serve as Output signals in RC mode.
487	PCIE2_RX_P	AI		PCIE2_RX_P	

488	PCIE2_RX_M	AI		PCIE2_RX_M	
489	PCIE2_REFCLK_P	AO		PCIE2_REFCLK_P	Only used in RC mode and serve as Output signals in RC mode.
490	PCIE2_REFCLK_M	AO		PCIE2_REFCLK_M	
491	PCIE2_TX_P	AO		PCIE2_TX_P	
492	PCIE2_TX_M	AO		PCIE2_TX_M	
493	GND	G		GND	
494	GND	G		GND	
495	GND	G		GND	
496	GND	G		GND	
497	GND	G		GND	
498	GND	G		GND	
499	GND	G		GND	

500	GND	G		GND	
501	GND	G		GND	
502	GND	G		GND	
503	I2S2_SCK	DO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	I2S1 clock signal	1.8 V power domain.Serve as output signals in master mode. Serve as input signals in slave mode.
504	I2S2_WS	IO		I2S1 select signal	
505	I2S2_DOUT	DO		I2S data out	1.8 V power domain.
506	I2S2_DIN	DI		I2S data in	
507	VBAT_RF	PI	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Power supply for the module's RF part	
508	VBAT_RF	PI			
509	VBAT_RF	PI			
510	VBAT_RF	PI			
511	GND	G		GND	

512	GND	G		GND	
513	RESERVED				Keep pin open
514	GND	G		GND	
515	GND	G		GND	
516	RESERVED				Keep pin open
517	GND	G		GND	
518	GND	G		GND	
519	RESERVED				Keep pin open
520-524	GND	G		GND	

Remark:

1. * means that the function is under development;

2. The above interface functions are not supported at the same time, some pins are multiplexed functions, please pay attention when choosing!

3. MA922 pin multiplexing see “MA922 _GPIO function multiplexing”

3.4 Power

Table 4 MA922 module power interface description

Pin Name	I/O	Pin	Description
VBAT_RF	PI	109, 111, 112, 114, 235, 236, 238, 239, 445, 446, 447, 448, 507, 508, 509, 510 403	Module power supply,3.3~4.3V, nominal value 3.8V
VBAT_BB	PI	241, 242, 244, 449, 450, 451, 452	Module power supply, 3.3~4.3V, nominal value 3.8V
VBAT_CV2X	PI	226, 227, 229, 439, 440, 441, 442	Module C-V2X power supply, 4.75~5.25V, nominal value 5.0V
VDD_EXT	PO		Voltage output, 1.8V
GND	G	6,12,18,26,33,42,86,92,98,115,117,118,120,121, 124,125,126,127,128,129,130,131,133,134,135,137,138,140, 141,144,145,146,147,148, 149, 150,151,153,155,156,158, 159,160,162,164,165, 167, 168, 171, 172, 173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206,208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308,309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325,326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342,343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359,360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376,377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393,394, 395, 396, 397, 398, 399, 400, 401, 402, 404, 405, 406, 407, 408, 409, 410, 413,415, 417, 419, 421, 423, 425, 427, 429, 431, 432, 434, 435, 437, 438, 443, 444, 453,454, 455, 456, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 493,494, 495, 496, 497, 498, 499, 500, 501, 502, 511, 512, 514, 515, 517, 518, 520, 521,522, 523, 524	

3.4.1 Power Supply

The following figure 3 shows a reference design for +12/+24 V input power source when applying the module to 5G + C-V2X solution. The designed outputs are 5.0 V and 3.8 V, and the maximum rated current is 5 A.

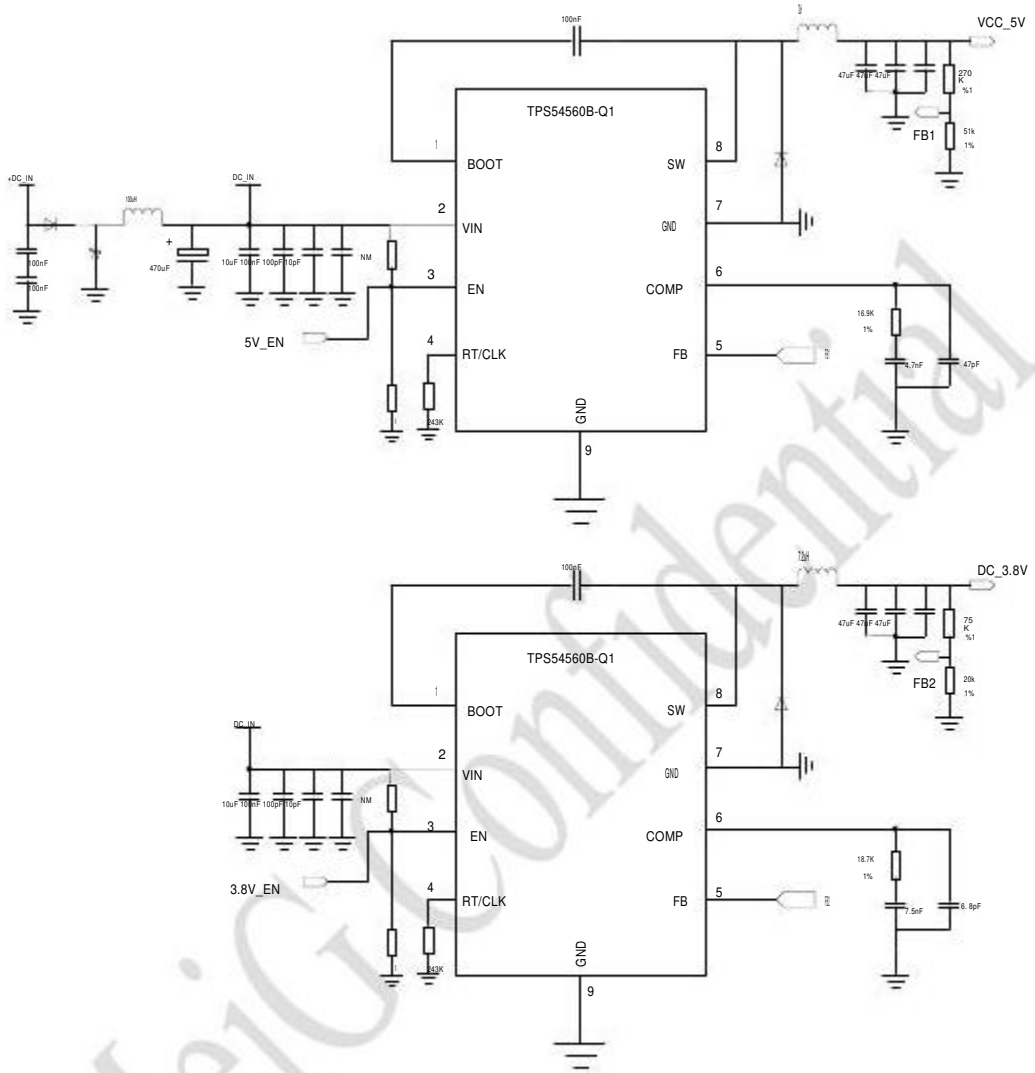


Figure 3 Module power supply circuit

The following figure shows another reference design for +12/+24 V input power source when applying the module to 5G + C-V2X solution. The designed outputs are 5.0 V (with maximum rated current of 5 A) and 3.8 V (with maximum rated current of 3 A).

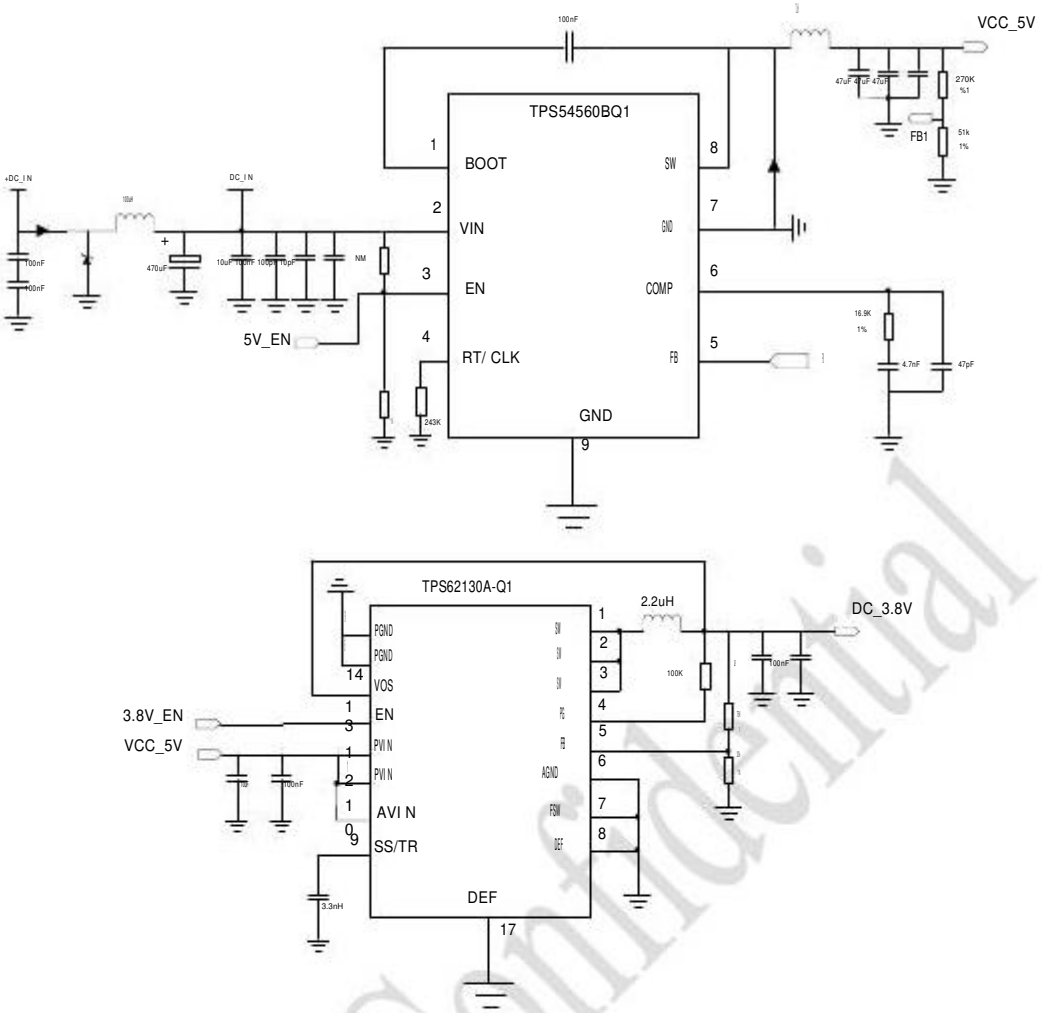


Figure 4 Module power supply circuit

3.4.2 Reduce Voltage Drop

The power supply range of VBAT_BB and VBAT_RF is 3.3–4.3 V. The power supply range of VBAT_CV2X is 4.75–5.25 V. Ensure that the input voltage of VBAT_BB and VBAT_RF never drops below 3.3 V, and the input voltage of VBAT_CV2X never drops below 4.75 V. The following figure shows the voltage drop during burst transmission in GSM and 5G (NSA) networks. The voltage drop will be less in 3G, 4G and 5G (SA) networks.

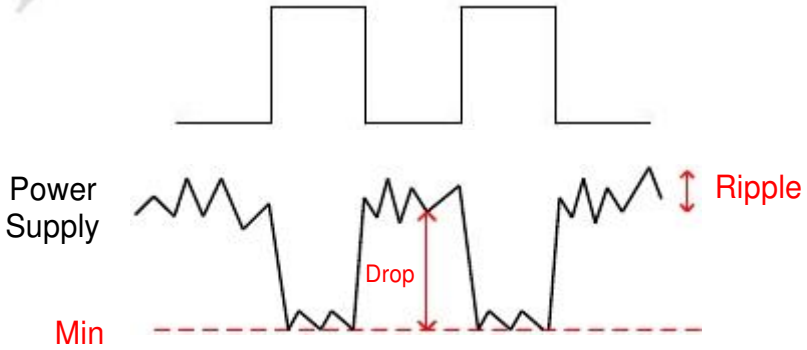


Figure 5 Burst transfer power requirements

To reduce voltage drop, VBAT_RF and VPH_5V_V2X use bypass capacitors with at least 100uF and low ESR, and VBAT_BB uses bypass capacitors with at least 220uF and retains multi-layer ceramic chip capacitor (MLCC) arrays due to their low ESR. It is recommended that at least three ceramic capacitors (100nf, 33pf, 10pf) be used to form the MLCC array and that these capacitors be placed close to the VBAT pins. When the module is connected to an external 3.8V power supply, the VBAT_BB and VBAT_RF cables are in a star structure. VBAT_BB cable width should not be less than 1.5 mm. The VBAT_RF cable width of the main power cable is not less than 3mm, and the branch cable width is not less than 2mm. VPH_5V_V2X Cable width should not be less than 1.6 mm. In principle, the longer the VBAT line, the wider the line width.

In addition, in order to make the power supply stable, it is recommended to use a TVS diode to prevent EOS and place it as close to the VBAT pin as possible. The recommended circuit diagram is as follows:

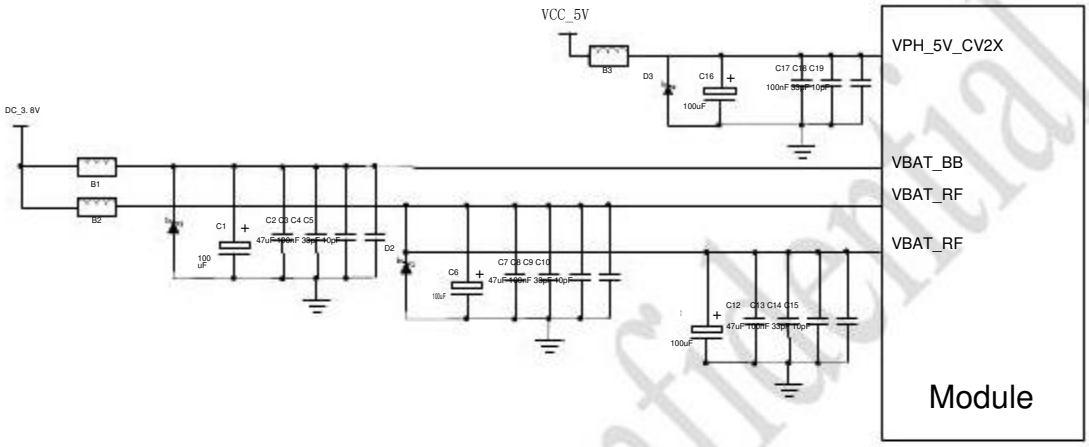


Figure 6 Power supply design

3.4.3 VDD_EXT Voltage Output

When the MA922 module is powered on normally, Pin68 output voltage is 1.8V and current load is 50mA. This output voltage can be used as an external pull-up source, such as level reference.

3. 5 Power on/off

3.5.1 PWRKEY Pin Power on

When the module is in power down mode, it can be turned on by driving the PWRKEY pin low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

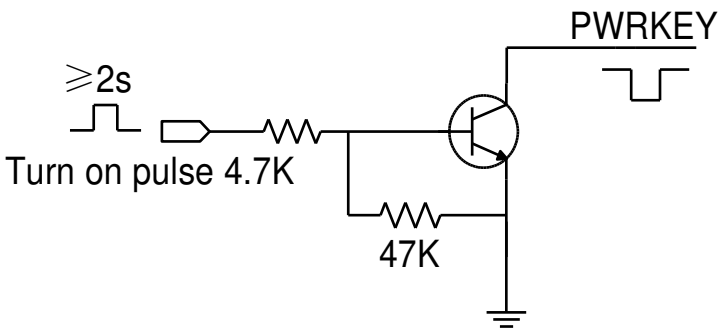


Figure 7 Open collector driver reference boot circuit

Another way to control the PWRKEY pin is to directly use a button switch. A TVS should be placed near the button for ESD protection. The reference circuit is as follows:

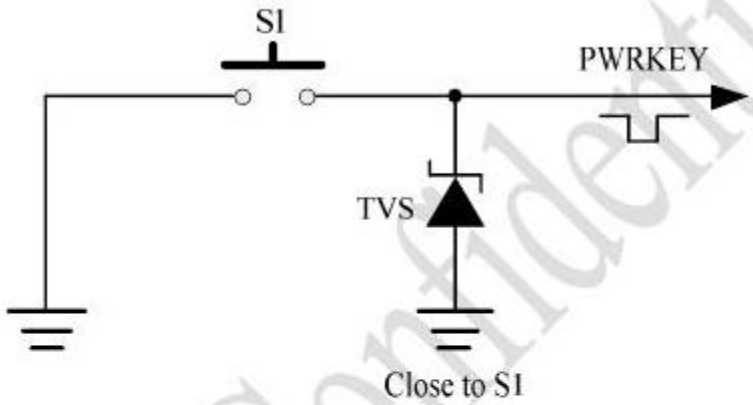


Figure 8 Button boot reference circuit

The boot timing (to be tested) is shown in the following figure:

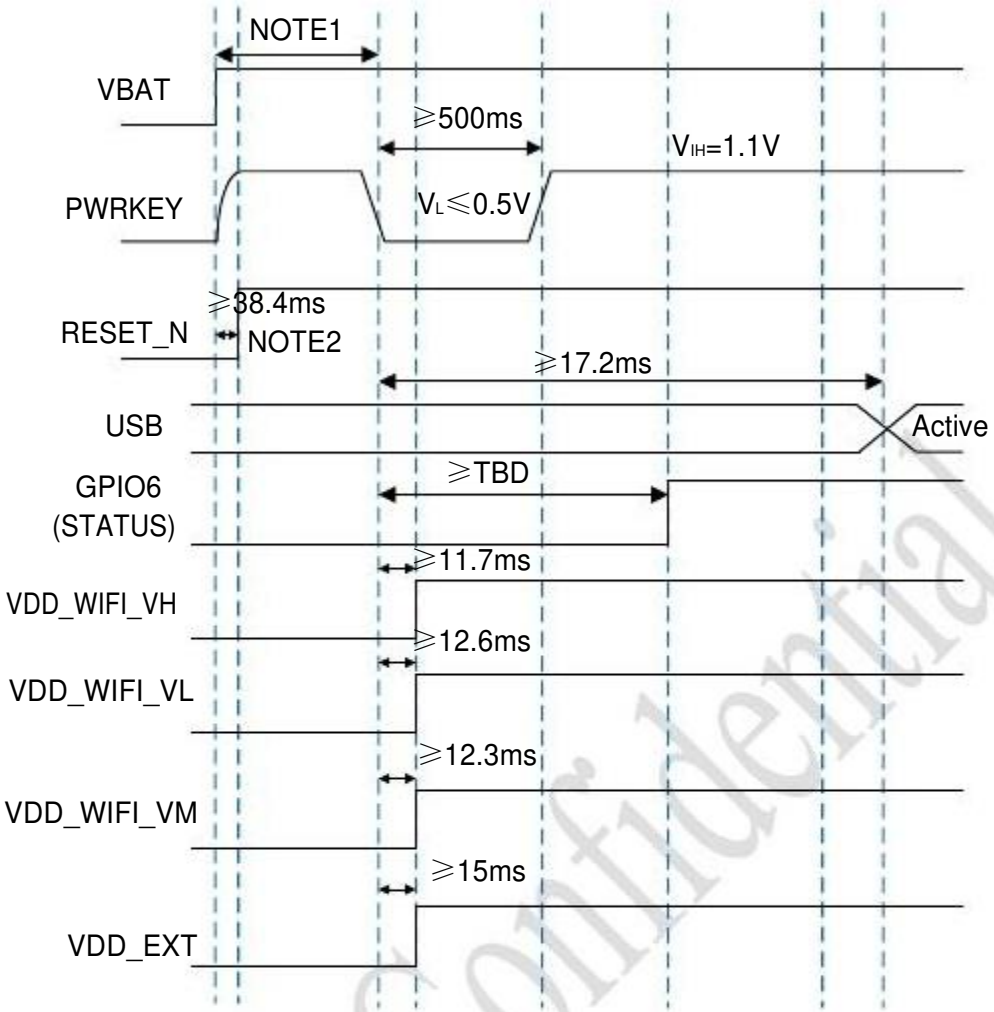


Figure 9 Boot sequence diagram

Note:
Before pulling down the PWRKEY pin, make sure that the VBAT voltage is stable. It is recommended that the time interval between powering up VBAT and pulling the PWRKEY pin low is no less than 30ms. If the module needs to be powered on automatically, the PWRKEY pin can be directly connected to the ground. The maximum resistance to ground cannot exceed 1k, and 0R is recommended. In this way, shutdown can only be done by direct powered off.

3.5.2 Shutdown

Table 5 Three shutdown modes:

Shutdown method	Step	Applicable scene
Low voltage shutdown	When VBAT voltage is too low or power down, the module will shutdown	At this time, the module does not perform the normal shutdown process, and does not go through the process of logging out from the base station.

Hardware shutdown	Pull down PWRKEY (greater than 3s), then release	Normal shutdown
AT shutdown	AT+CPOF	Software shutdown

Driving PWRKEY low for at least 2 s and then releasing it will enable the module to execute power-off procedure. The power-down scenario is illustrated in the following figure.

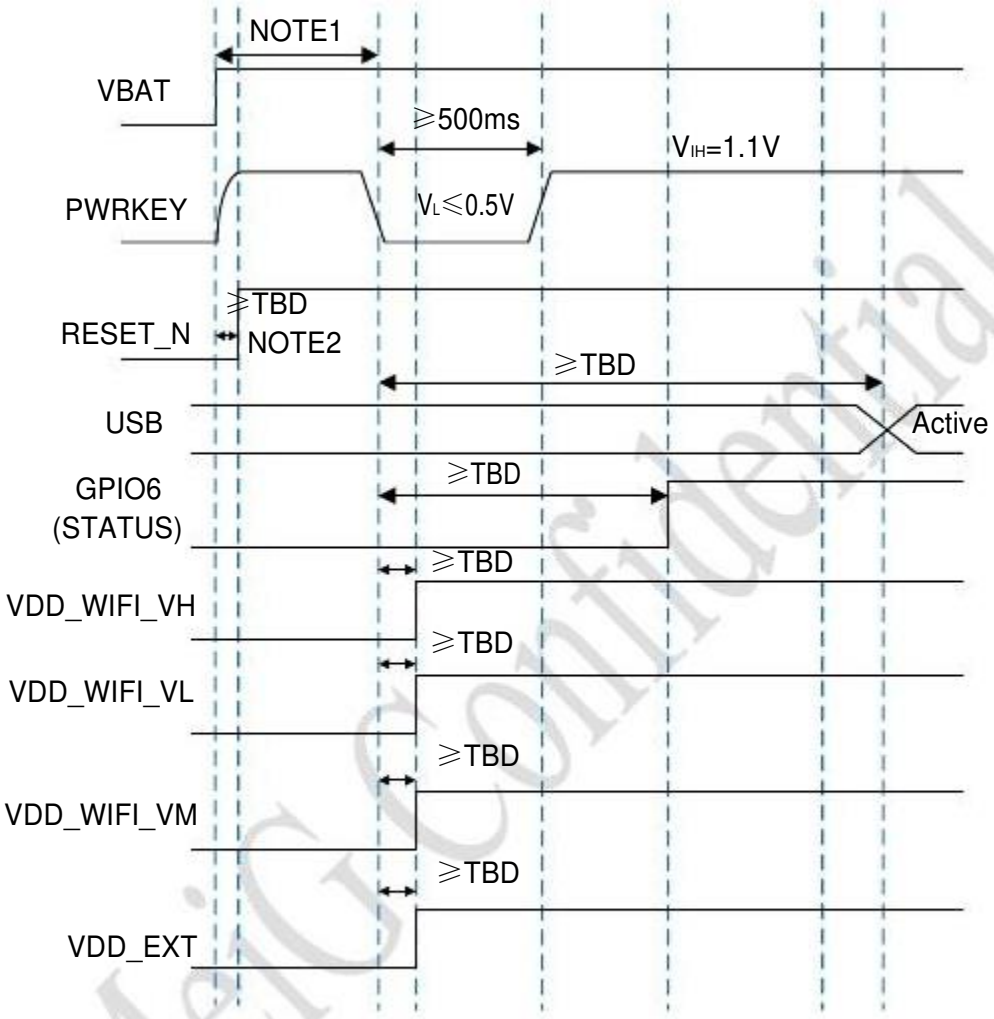


Figure 10 Power-down Timing

Remark:

1. When the module is working normally, do not cut off the power of the module immediately to avoid damaging the Flash data inside the module. It is strongly recommended to turn off the module through the AT command before disconnecting the power.

2. When using the AT command to shut down, make sure that PWRKEY is always in a high level state after the shutdown command is executed, otherwise the module will automatically restart after shutting down.

3. 6 Reset Function

There are two reset methods for MA922: hardware reset and AT command reset.

3.6.1 Hardware Reset

When the module is working, pull down the RESET_N pin for at least 250-550ms to reset the module. The RESET_N signal is sensitive to interference, so it is recommended that the traces on the module interface board should be as short as possible, and should be handled with the ground.

The reference circuit is similar to the PWRKEY control circuit, and customers can use an open-collector drive circuit or a button to control the RESET_N pin.

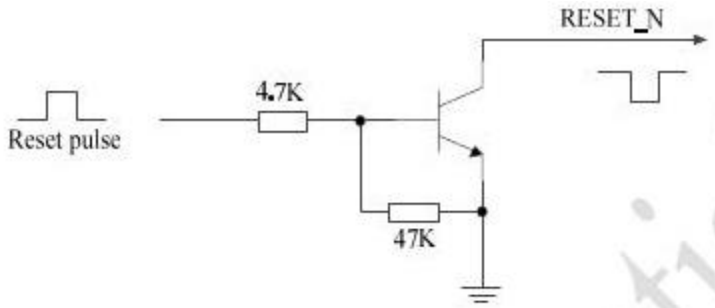


Figure 11 RESET_N reset open collector reference circuit

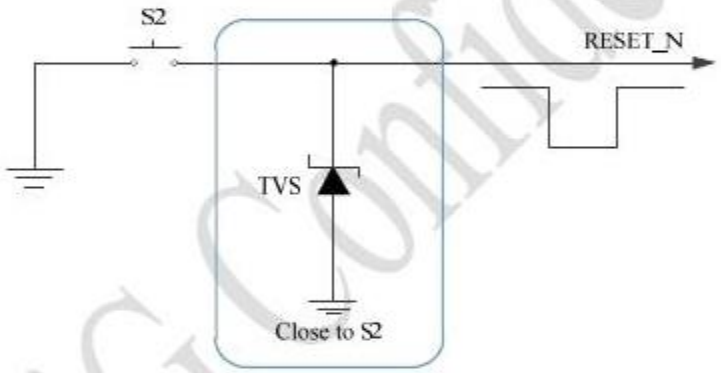


Figure 12 RESET_N reset button reference circuit

The reset timing diagram is as follows:

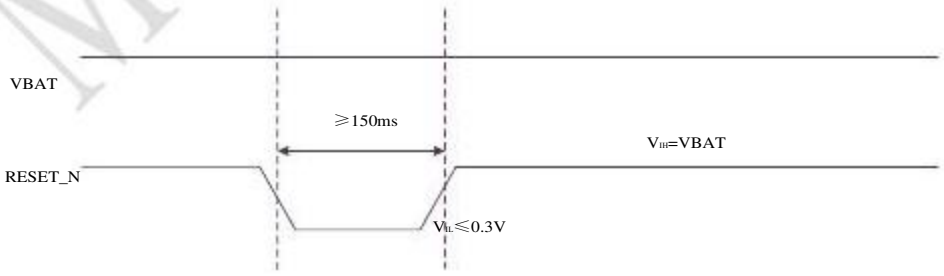


Figure 13 RESET_N reset timing diagram

3.6.2 AT Command Reset

Input AT+TRB command through MA922 UART or USB AT port to reset and restart MA922.

3. 7 USIM/SIM Interface

MA922 supports 1.8V and 3.0V SIM cards.

Table 6 USIM/SIM interface description

Pin name	I/O	Pin	Pin description
USIM1_VDD	PO	251	USIM1/SIM card power supply
USIM1_CLK	DO	253	USIM1/SIM card clock
USIM1_RESET	DO	250	USIM1/SIM card reset
USIM1_DATA	DIO	254	USIM1/SIM card data
USIM1_PRESENCE	DI	255	USIM1/SIM card hot-plug detect
USIM2_VDD	PO	256	USIM2/SIM card power supply
USIM2_CLK	DO	259	USIM2/SIM card clock
USIM2_RESET	DO	260	USIM2/SIM card reset
USIM2_DATA	DIO	257	USIM2/SIM card data
USIM2_PRESENCE	DI	258	USIM2/SIM card hot-plug detect

MA922 module supports (U)SIM card hot-plug via USIM_DET pins, and either low-level or high-level detection is supported. The function is disabled by default, and can be enabled by related software command.

The SIM card hot-plug function can be configured through the “AT+SIMHOTSWAP” command. The AT command description is shown in the following table:

Table 7 SIM card hot swap function setting description

AT command	SIM card hot-plug detection	Function Description
AT+PENDING=1	open	By default, the SIM card hot swap detection function is enabled, and the module detects whether the SIM card is inserted through the USIM_PRESENCE pin status
AT+PENDING= 0	close	The SIM card hot swap detection function is disabled, the module reads the SIM card when powering on, and does not detect the USIM_PRESENCE state

The circuit design of the SIM card with hot swap function is as shown in the figure below.

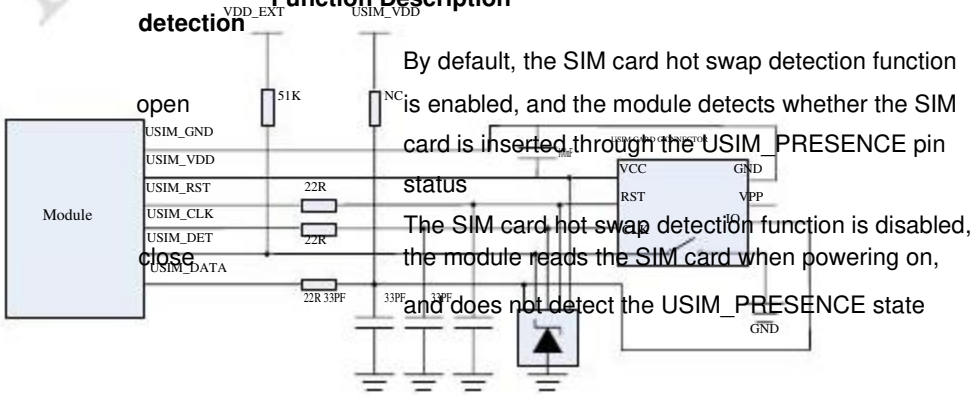


Figure 14 Reference design of card holder with hot-swap function

If you do not need to use the USIM card hot swap detection function, please keep the USIM_DET pin floating. The reference circuit is as follows:

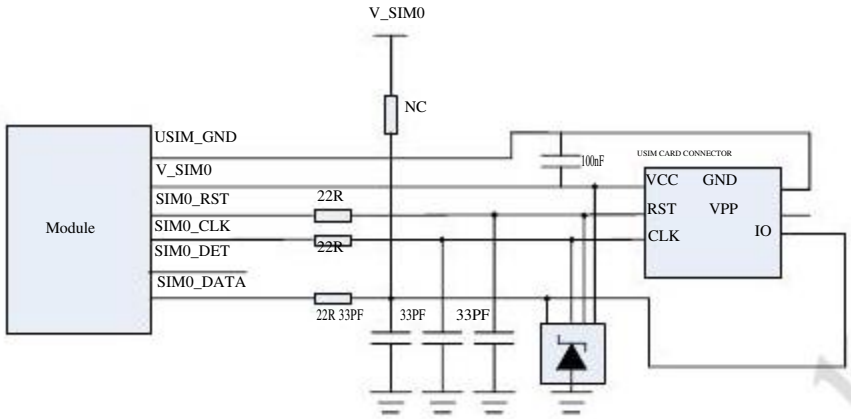


Figure 15 Reference design of card holder without hot-swap function

In the circuit design of the USIM card interface, in order to ensure the good performance and reliability of the USIM card, it is recommended to follow the following design principles in the circuit design:

- A 22Ω resistor is connected in series on the USIM_DATA, USIM_CLK and USIM_RST lines to suppress stray EMI, enhance ESD protection, and facilitate debugging;
- In order to improve the anti-static ability, add TVS tubes to the USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST lines, and the parasitic capacitance is not more than 30Pf ESD protection device;
- Connect 33pF capacitors in parallel on the USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST lines to filter out GSM900 interference; the peripheral devices of the USIM card should be placed as close as possible to the USIM card holder;
- The USIM card holder is placed close to the module, try to ensure that the wiring length of the USIM card signal line does not exceed 100mm ;
- The wiring of the USIM card signal line is far away from the RF line and the VBAT power line;
- In order to prevent crosstalk between USIM_CLK signal and USIM_DATA, the wiring of the two should not be too close, and a ground shield should be added between the two traces;

3. 8 USB Interface

The MA922 provides a USB interface. This interface is used for AT command interaction, data transfer, software debugging and version upgrading. Provides a USB interface, USB interface follows USB 3.1 Gen 2 and USB2.0 standards, USB 3.1 theoretically supports 10Gbps ultra-high speed, USB2.0 theoretically supports high-speed 480Mbps and full speed 12Mbps.

USB 2.0 and USB 3.1 share a hardware controller, so USB 2.0 and USB 3.1 cannot be used simultaneously. When USB 2.0 and USB 3.1 are connected to the same host, the default USB 3.1 interface is used.

3.8.1 USB Pin Description

Table 8 USB interface description

Pin name	I/O	Pin	Description
USB_VBUS	DI	84	USB insertion detection, Maximum current: 0.1 mATypical 5.0 V.Test points must be reserved.
USB_DP	AIO	85	USB 2.0 Differential Data+,90Ω impedance
USB_DM	AIO	87	USB 2.0 Differential Data -,90Ω impedance
USB_SS_TX_P	AO	93	USB 3.1_TX_P, USB3.1 differential 70-100Ω impedance, 85Ω recommended
USB_SS_TX_M	AO	91	USB 3.1_TX_M
USB_SS_RX_P	AI	90	USB 3.1_RX_P
USB_SS_RX_M	AI	88	USB 3.1_RX_M

3.8.2 USB Reference Circuit

It is recommended to use USB 2.0 for firmware upgrading in application designs, and test points must be reserved for debugging purposes. USB 2.0 interface reference circuit is presented below.

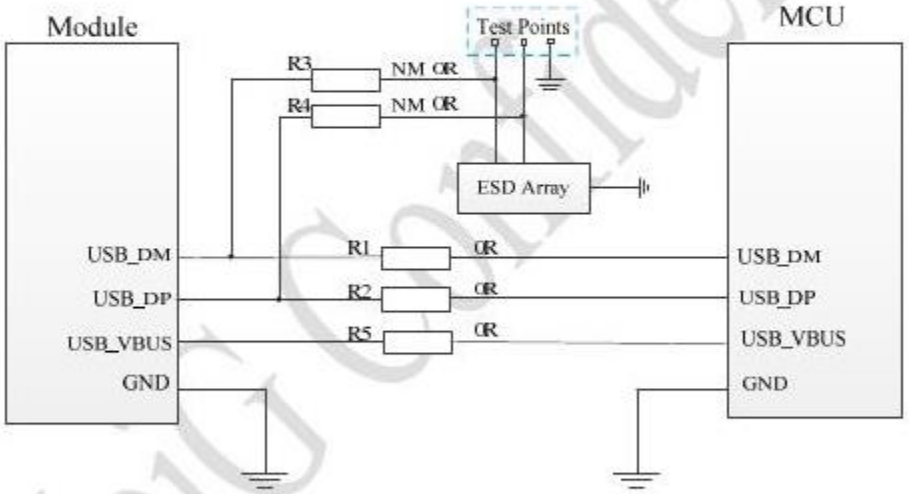


Figure 16 USB2.0 interface reference design diagram

In order to meet the signal integrity requirements of the USB 2.0 data cable, resistors R1/R2/R3/R4 must be placed close to the module, and the resistors need to be placed close to each other. The branch of the connection test point must be as short as possible.

The USB 3.1 interface reference circuit is shown in the following figure.

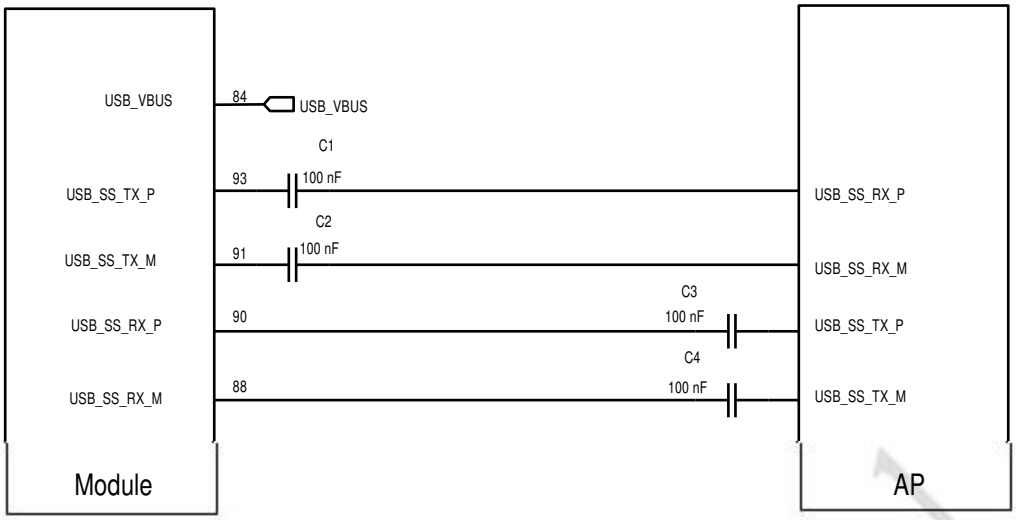


Figure 17 Reference design of USB 3.1 Application

In USB 3.1 applications, place C1 and C2 near the module, and place C3 and C4 near the AP. The extra stubs of trace must be as short as possible.

In the design of the USB interface circuit, in order to ensure the USB performance, it is recommended to follow the following principles in the circuit design:

- The module USB_VBUS is not used to supply power to the module, but is used to detect the insertion and removal of USB;
- In order to reduce the signal interference during USB high-speed data transmission, connecting R1 and R2 in series on the USB_DM and USB_DP interface circuits can improve the accuracy of data transmission. It is recommended to use 0Ω for both R1 and R2;
- USB 2.0 and 3.1 signal differential routing packet ground processing. USB 2.0 recommends a differential impedance of 90Ω, and USB 3.1 recommends a differential impedance of 85Ω.
- The USB 2.0 wiring error should be less than 2.0mm, and the USB 3.1 wiring error should be less than 0.7mm.
- Do not line the crystal, oscillator, magnetic device, PCIE and RF signal. Differential wiring in the inner layer of the PCB, and three-dimensional package processing. The RF signal operates at 2.4 GHz with maximum isolation from the USB_SS_TX/RX trace.
- In order to improve the anti-static performance of the USB interface, it is recommended to add ESD protection devices to the USB_DP and USB_DM interface circuits, and it is recommended to use ESD devices with a junction capacitance of less than 1pF; the USB ESD protection devices should be placed as close to the USB interface as possible;
- In order to improve the anti-static performance of the USB interface, it is recommended to add ESD protection devices on the USB_DP and USB_DM interface circuits. USB 2.0 is recommended to use ESD devices with junction capacitance less than 1pF, and USB 3.1 is recommended to use parasitic capacitance less than 0.3pF. The USB ESD protection device should be placed as close as possible to the USB interface.
- Do not route USB cables under crystal oscillators, oscillators, magnetic devices, and RF signals. It is recommended to route the inner layer differential cables and wrap the ground on the top, bottom, left, and right sides.

Remark

1. The module supports master mode, but works in slave mode by default.
2. The high-speed PHY and SuperSpeed PHY share the same USB 3.1 Gen 2 controller inside baseband chipset, so USB 2.0 and USB 3.1 cannot be used simultaneously.
3. As for the AC coupling capacitors C1–C4, the recommended value is 220 nF for USB 3.1 Gen 2 and 100 nF for USB 3.1 Gen 1.

3.9 I2S and I2C Interfaces

The module provides one I2S interface and one I2C interface for external audio codec design. The module can provide a second I2C interface through pin multiplexing. （ I2C1&I2S1 default for Audio codec）

The following table shows the pin definition of I2S and I2C interfaces.

Table 9: Pin Definition of I2S Interface

Pin name	I/O	Pin	Describe
I2S_MCLK	DO	81	Clock output for codec, 12.288MHz
I2S1_WS	DIO	265	I2S1 word select, Serve as output signals in master mode.Serve as input signals in slave mode.
I2S1_SCK	DIO	262	I2S1 clock, Serve as output signals in master mode.Serve as input signals in slave mode.
I2S1_DIN	DI	263	I2S1data in
I2S1_DOUT	DO	261	I2S1data out
I2S2_WS	DIO	504	I2S2 word select, Serve as output signals in master mode.Serve as input signals in slave mode.
I2S2_SCK	DIO	503	I2S2 clock, Serve as output signals in master mode.Serve as input signals in slave mode.
I2S2_DIN	DI	506	I2S2 data in
I2S2_DOUT	DO	505	I2S2 data out

Table 10: Pin Definition of I2C Interface

Pin name	I/O	Pin	Describe
I2C1_SDA	OD	80	I2C1 serial data, Require external pull-up to 1.8 V.If unused, keep them open.
I2C1_SCL	OD	79	I2C1 serial clock, Require external pull-up to 1.8 V.If unused,Clock output open.
I2C2_SDA	OD	264	I2C2 serial data, Require external pull-up to 1.8 V.If unused, keep them open.
I2C2_SCL	OD	267	I2C2 serial clock, Require external pull-up to 1.8 V.If unused, keep them open.

The following figure shows a reference design of I2S and I2C interfaces with an external codec IC.

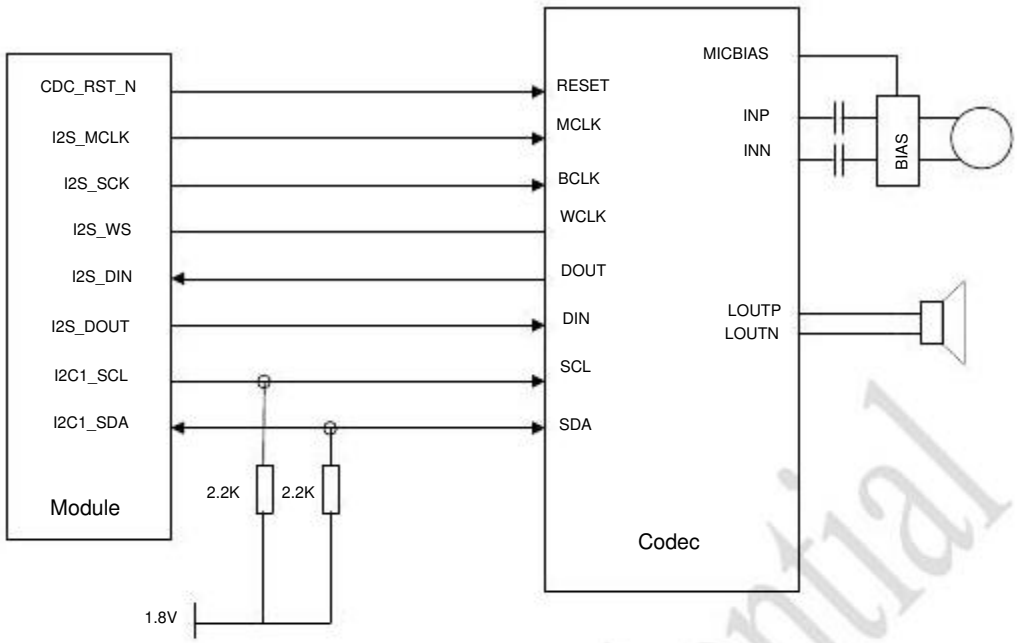


Figure 18 Reference design of I2C and I2S Interfaces with External Audio Codec

Remark:

1. It is recommended to reserve an RC circuit on the I2S signal traces, especially for I2S_SCK and I2S_MCLK.
2. The module works as a master device in I2C applications.

3.10 PCM Interfaces

The module provides one PCM interface for Bluetooth audio transmission by default. See ***Chapter 4.7*** for details. The PCM interface supports primary (short frame sync) and auxiliary (long frame sync) modes.

Table 11: Pin Definition of PCM Interface

Pin name	I/O	Pin	Description
PCM_SYNC	DIO	73	PCM data frame sync, Serve as output signals in master mode.Serve as input signals in slave mode.
PCM_CLK	DIO	75	PCM clock, Serve as output signals in master mode.Serve as input signals in slave mode.
PCM_DIN	DI	76	PCM data input
PCM_DOUT	DO	78	PCM data output

The module supports 16-bit linear data format. Clock and mode can be configured, and the default configuration is primary mode using short frame sync format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. For more details, see document [6].

Remark:

1. When using Bluetooth, PCM_SYNC and PCM_CLK can only be used as output signals.

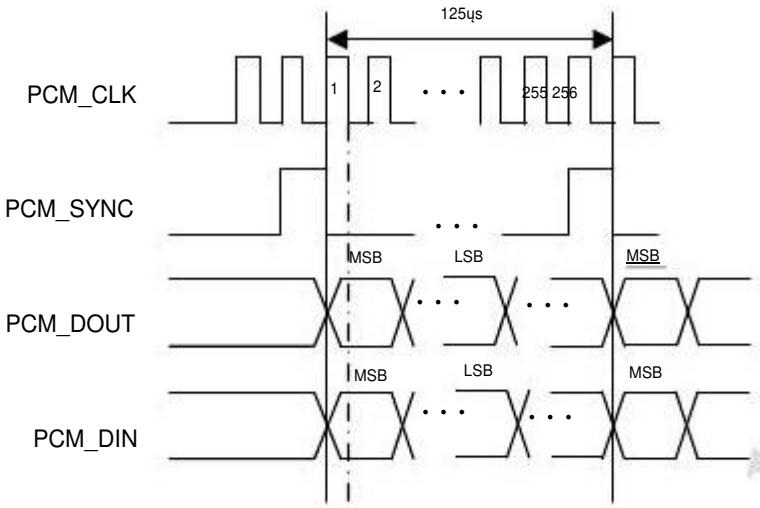


Figure 19 PCM timing diagram (Short frame synchronization)

3.11 PCIE Interfaces

The module provides two PCIe interface.

- The PCIe 1 interface supports RC and EP modes, works in RC mode by default
- The PCIe 2 interface only supports RC mode，default for WLAN&BT module.
- The PCIe 1 Compliant with PCI Express Base Specification Revision 3.0（2-lines）and Revision 4.0（1-line）
- The PCIe 2 Compliant with PCI Express Base Specification Revision 3.0
- Maximum rate: 8 Gbps for PCIE gen3.0 and 16 Gbps for PCIE gen4.0
- Backward compatible
- Can be used to connect to an external WLAN chip or application processor

Table 12: Pin Definition of PCIe Interface

Pin name	I/O	Pin	Description	Remark
PCIE1_REFCLK_P	AIO	40	PCIe1reference clock (+), Serve as output signals in RC mode. Serve as input signals in EP mode.	If PCIE_TX1 and PCIE_RX1 are unused, keep these pins unconnected. Require differential impedance of 70–110 Ω, and 85 Ω is recommended
PCIE1_REFCLK_M	DIO	38	PCIe1reference clock (-), Serve as output signals in RC mode. Serve as input signals in EP mode.	
PCIE1_TX0_M	AO	44	PCIe1 transmit 0 (-)	
PCIE1_TX0_P	AO	46	PCIe1 transmit 0 (+)	
PCIE1_TX1_M	AO	41	PCIe1 transmit 0 (-)	
PCIE1_TX1_P	AO	43	PCIe1 transmit 0 (+)	
PCIE1_RX0_M	AI	32	PCIe1 receive 0 (-)	
PCIE1_RX0_P	AI	34	PCIe1 receive 0 (+)	
PCIE1_RX1_M	AI	35	PCIe1 receive 0 (-)	

PCIE1_RX1_P	AI	37	PCIe1 receive 0 (+)	
PCIE1_CLKREQ_N	DIO	36	PCIe1 clock request	Serve as input signals in RC mode. Serve as output signals in EP mode. Require a 100 kΩ pull-up to VDD_EXT. 1.8 V power domain.
PCIE1_WAKE_N	DIO	30	PCIe1 wake up	
PCIE1_RST_N	DO	39	PCIe1 reset	Serves as an output signal in RC mode. Serves as an input signal in EP mode.
PCIE2_REFCLK_P	AO	489	PCIe2 reference clock (+),	Only used in RC mode and serve as an output signal in RC mode. Require differential impedance of 72.5–97.5 Ω, and 85 Ω is recommended
PCIE2_REFCLK_M	AO	490	PCIe2 reference clock (-),	
PCIE2_TX_P	AO	491	PCIe2 transmit 0 (+)	Require differential impedance of 72.5–97.5 Ω and 85 Ω is recommended
PCIE2_TX_M	AO	492	PCIe2 transmit 0 (-)	
PCIE2_RX_P	AI	487	PCIe2 receive 0 (+)	
PCIE2_RX_M	AI	488	PCIe2 receive 0 (-)	
PCIE2_CLKREQ_N	DI/DO	485	PCIe2 clock request	Only used in RC mode and serve as input signals in RC mode.
PCIE2__WAKE_N	DI/DO	484	PCIe2 wake up	
PCIE2_RST_N	DI/DO	486	PCIe2 Reset	

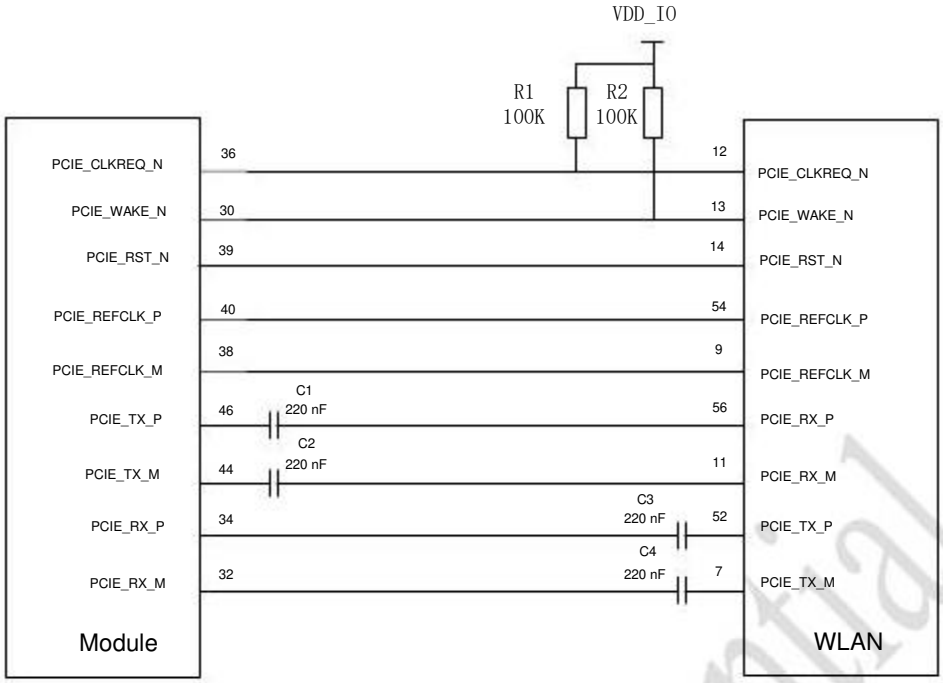


Figure 20 PCIe interface reference design

To meet PCIe specifications and enhance the reliability of applications, follow the criteria below in the PCIe interface circuit design:

- It is important to route the PCIe signal traces as differential pairs with ground surrounded. The differential impedance is 70–110 Ω and 85 Ω is recommended for PCIe Tx/Rx/REFCLK traces.
- PCIe signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- For each differential pair, the intra-lane length match should be less than 0.7 mm, while the inter-lane
- length match, that is, the trace length matching between the Tx, Rx and reference clock pairs is not required. Do not stagger the capacitors, as this can affect the differential integrity of the design and can create EMI.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions for the main route on the PCB (that is, apply layer transitions only at break in and break out regions). When the differential signal traces changes layers, create ground vias near signal vias, and create at least 1–3 ground vias for each differential pair.
- Avoid bending of the traces to avoid common mode noise to the system. When bending is required, maintain a bend angle greater than 135°as shown in the figure below, and the shortest trace caused by bending should be at least 1.5 times the trace width (1.5W). The spacing between Tx and Rx pairs, and the spacing between PCIe lanes and all other signals, should exceed 4 times the trace width (4W).

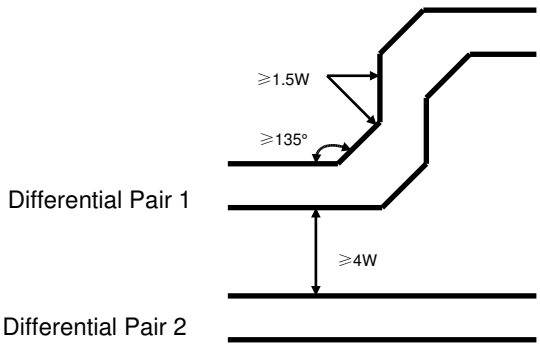


Figure 21 Schematic diagram of differential routing

- PCIe Tx AC coupling capacitors can be anywhere along the line, but better to be placed close to the source or the receiver side to keep good signal integrity of main route on PCB. Use a serpentine to keep the difference pairs equal in the break out region as much as possible, to ensure that the traces stay differential thereafter. The length of each serpentine section should be at least 3 times the trace width (≥ 3W), and the maximum spacing between the serpentine section and the other differential trace should be less than twice of the normal differential trace spacing (S1 < 2S).

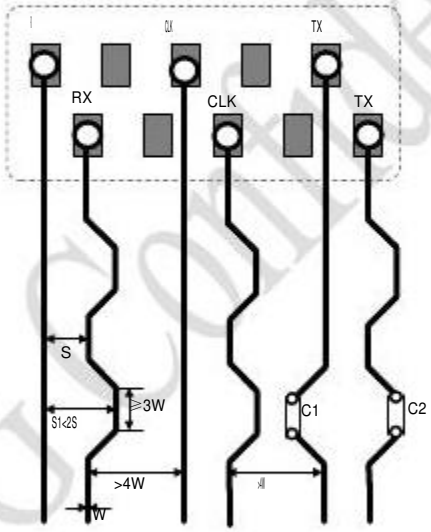


Figure 22 Schematic diagram of PCIe cabling requirements

- PCIe Tx AC coupling capacitors should be 220 nF.
- The maximum trace length of each differential pair for PCIe should be less than 300 mm.

3.12 WLAN and Bluetooth Application

The module provides one PCIe interface for WLAN function (see Chapter 4.6 for more details), and Bluetooth UART and PCM interfaces for Bluetooth function (see Chapter 4.3 and Chapter 4.5 for more details).

The following table shows the pin definition of WLAN and Bluetooth application interfaces.

Table 13: Pin Definition of WLAN and Bluetooth Application Interfaces

Pin name	I/O	Pin	Description
VDD_EXT	PO	68	Provide 1.8 V for external circuits.This pin can be used to connect with VDD_IO of Quectel WLAN module, it also can be used as power supply for external pull up circuits.
VDD_WIFI_VL	PO	274,275	0.95 V low-voltage power supply for Wi-Fi & Bluetooth modules
VDD_WIFI_VM	PO	276	1.35 V medium-voltage power supply for Wi-Fi & Bluetooth modules
VDD_WIFI_VH	PO	277	1.95 V high-voltage power supply for Wi-Fi & Bluetooth modules
Coexistence Control Interface			
COEX_UART_TXD	DO	69	LTE & WLAN & Bluetooth UART coexistence transmit
COEX_UART_RXD	DI	67	LTE & WLAN & Bluetooth UART coexistence receive
Others Interfaces			
WLAN_PWR_EN1	DO	222	WLAN power supply enable control 1.Used for Quectel AF50T VDD_RF power control.
WLAN_EN	DO	228	WLAN function enable control
BT_EN	DO	66	Bluetooth enable control
HOST_SW_CTRL	DI	184	Switch control
WLAN_SLP_CLK	DO	231	WLAN 32 kHz sleep clock.If unused, keep it open.

Remark:

When WLAN or Bluetooth function is intended to be used, the coexistence UART interface must be used simultaneously. The coexistence UART interface cannot be used as general-purpose UART interface.

The following figure shows a reference design of WLAN and Bluetooth application interfaces. For more details, see document [7].

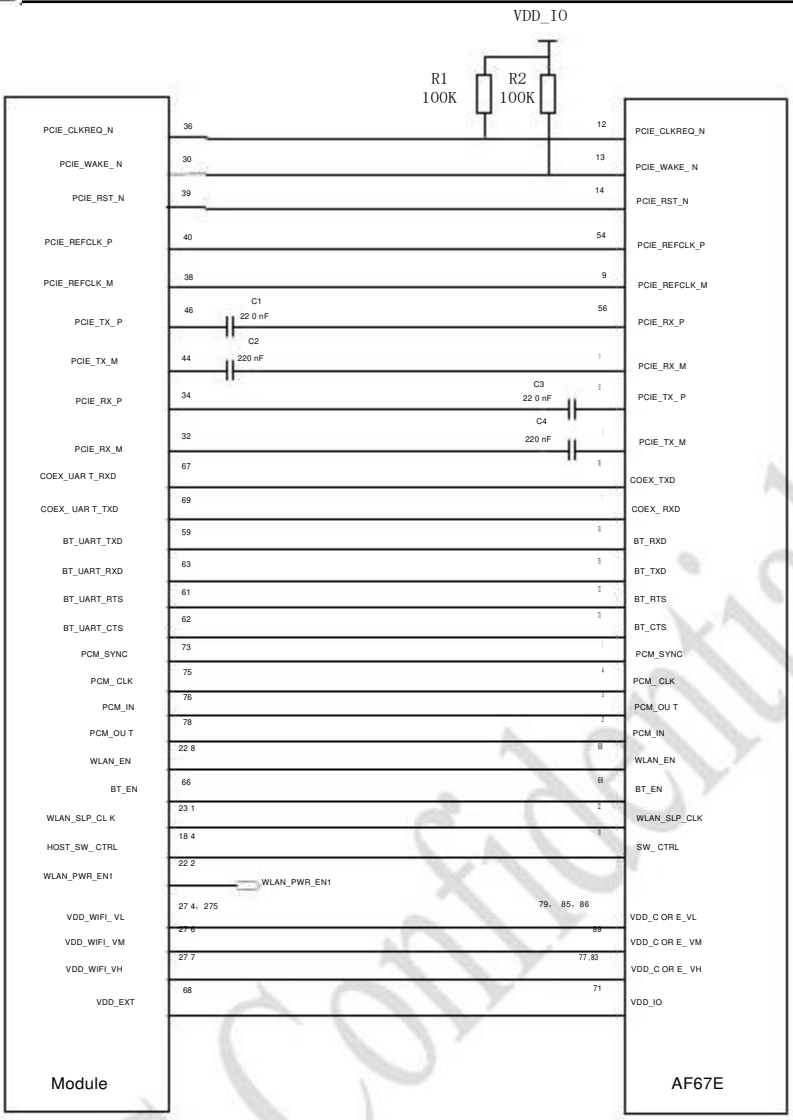


Figure 23 WLAN and Bluetooth Application interface Reference design (AF67E)

3.13 SDIO Interfaces

The module provides two SDIO interfaces: SDIO1 can be used for eMMC functions; SDIO2 can be used to connect external SD cards or DSRC modules.

The following table shows the pin definitions for the SDIO interface.

Table 14: Pin Definition of SDIO Interface

Pin name	I/O	Pin	Description
SDIO1_DATA_0	DIO	49	SDIO1data bit 0
SDIO1_DATA_1	DIO	50	SDIO1data bit 1
SDIO1_DATA_2	DIO	51	SDIO1data bit 2
SDIO1_DATA_3	DIO	52	SDIO1data bit 3
SDIO1_CMD	DIO	48	SDIO1 command

SDIO1_CLK	DO	47	SDIO1 clock
SDIO1_DS	DIO	57	SDIO1_DS
SDIO1_DATA_4	DIO	53	SDIO1data bit 4
SDIO1_DATA_5	DIO	55	SDIO1data bit 5
SDIO1_DATA_6	DIO	56	SDIO1data bit 6
SDIO1_DATA_7	DIO	58	SDIO1data bit 7
SDIO2_DATA_0	DIO	1	SDIO2 data bit 0
SDIO2_DATA_1	DIO	2	SDIO2 data bit 1
SDIO2_DATA_2	DIO	4	SDIO2 data bit 2
SDIO2_DATA_3	DIO	5	SDIO2 data bit 3
SDIO2_CMD	AO	269	SDIO2 command
SDIO2_CLK	AO	270	SDIO2 clock
SDIO2_DS	DIO	3	SDIO2_DS

3.13.1 Reference Design for eMMC Application

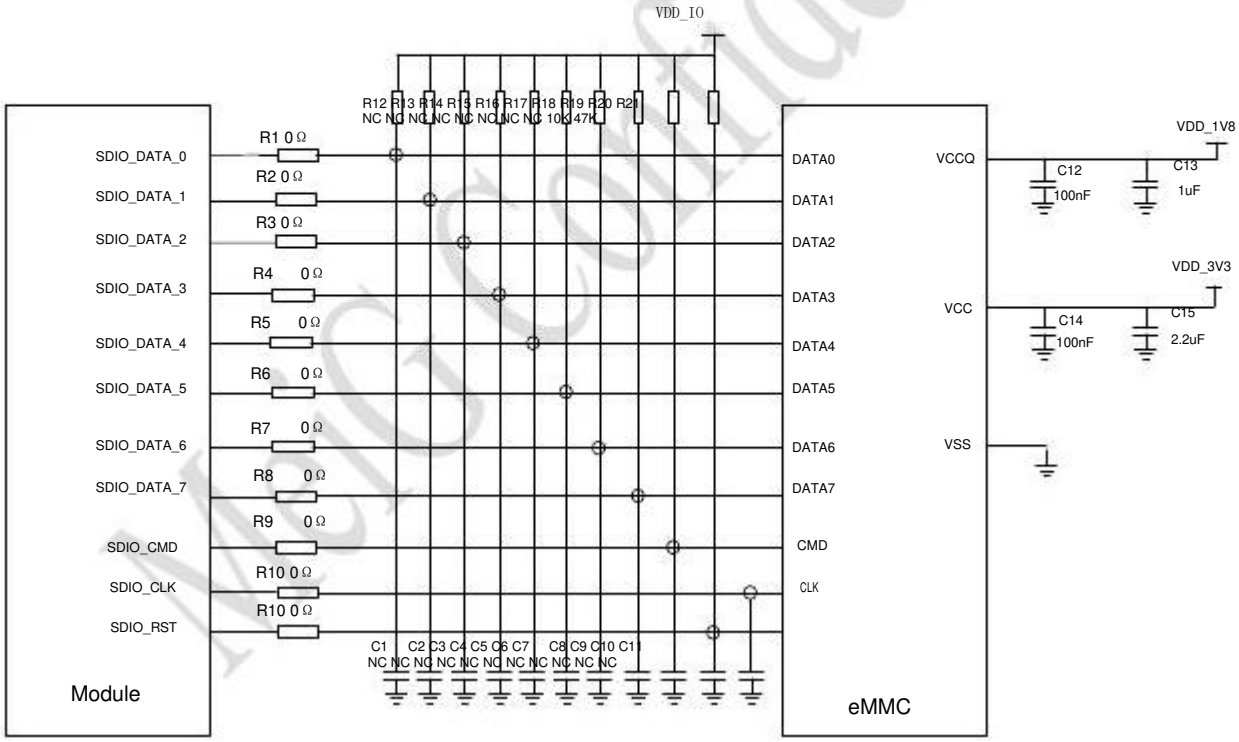


Figure 24 Reference design for eMMC application

Follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve R12–R19 (10–100 kΩ) to pull up SDIO signals to an external 1.8 V VDD. The resistors are not mounted by default, and the recommended value is 100 kΩ.

- To improve signal quality, it is recommended to add resistors R1–R10 in series between the module and eMMC. Resistor R10 should be 20–30 Ω and the other resistors are 0 Ω by default. The bypass capacitors C1–11 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between SDIO_CLK and SDIO_DATA[0:7]/SDIO_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 17 mm, so the exterior total trace length should be less than 33 mm.
- Keep the spacing between SDIO and other signal traces at least twice the trace width and the load capacitance of SDIO bus less than 30 pF.

3.14 SPI Interfaces

The module provides two SPI interfaces by default. The maximum clock frequency is up to 50 MHz.The following tables show the pin definition of SPI interfaces.The two SPI interfaces are in the 1.8V power domain and supports SPI Master and Slave mode .

Table 15: Pin Definition of SPI Interfaces.

Pin name	I/O	Pin	Description
SPI1_CLK	DIO	216	SPI1clock
SPI1_CS	DIO	213	SPI1 chip select
SPI1_MISO	DIO	219	SPI1 master-in slave-out
SPI1_MOSI	DIO	210	SPI1 master-out slave-in
SPI2_CLK	DIO	103	SPI2 clock
SPI2_CS	DIO	105	SPI2 chip select
SPI2_MISO	DIO	106	SPI2 master-in slave-out
SPI2_MOSI	DIO	108	SPI2 master-out slave-in

The following figure shows the timing relationship of SPI interface.

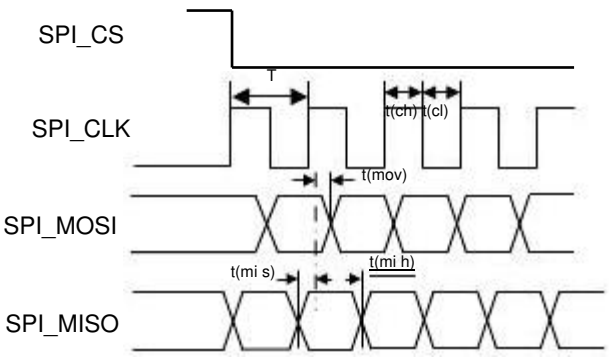


Figure 25 SPI Timing

The related parameters of SPI timing are shown in the table below.

Table 16: Parameters of SPI Interface Timing

Pin name	I/O	Pin	Description	Remark
ETH_MDIO	DIO	10	Ethernet management data	It generally requires a pull-up resistor close to the external PHY end.
ETH_MDC	DO	11	Ethernet management clock	Do not add any pull-up resistor to this pin, or it may cause higher current consumption during sleep mode.
ETH_PWR_EN	D0	27	Enable external power	

NOTE:

The module provides 1.8 V SPI interfaces. A voltage-level translator should be used between the module and the host if the application is equipped with a 3.3 V processor or device interface.

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period		-	-	ns
t(ch)	SPI clock high-level time		-	-	ns
t(cl)	SPI clock low-level time		-	-	ns
t(mov)	SPI master output valid time		-	-	ns
t(mis)	SPI master input setup time		-	-	ns
t(mih)	SPI master data input hold time		-	-	ns

3.15 RGMII Interfaces

The module includes an integrated Ethernet MAC with a RGMII interface which also supports EAVB. Key features of the RGMII interface are shown below:

- IEEE 802.3 compliant
- Supports 10/100/1000 Mbps operation
- Supports protocols such as IEEE 1722.A (AVTP), 802.1Qav (FQTSS), 802.1Qat (SRP), 802.1AS (gPTP)
- Support connecting to an external Ethernet PHY or switch
- Support 1.8 I/O standards

The following table shows the pin definition of RGMII interface.

Table 17: Pin Definition of RGMII Interface

Pin name	I/O	Pin	Description	Remark
ETH_MDIO	DIO	10	Ethernet management data	It generally requires a pull-up resistor close to the external PHY end.
ETH_MDC	DO	11	Ethernet management clock	Do not add any pull-up resistor to this pin, or it may cause higher current consumption during sleep mode.
ETH_PWR_EN	D0	27	Enable external power	

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period		-	-	ns
t(ch)	SPI clock high-level time		-	-	ns

			supply to power Ethernet PHY	
ETH_INT	DI	29	Ethernet PHY interrupt input	
ETH_RST	DO	31	Reset output for Ethernet PHY	
RGMII_CK_RX	DI	19	RGMII receive clock	The single-ended impedance requires 50 Ω.
RGMII_CTL_RX	DI	15	RGMII receive control	
RGMII_RX_0	DI	13	RGMII receive data bit 0	
RGMII_RX_1	DI	14	RGMII receive data bit 1	
RGMII_RX_2	DI	16	RGMII receive data bit 2	
RGMII_RX_3	DI	17	RGMII receive data bit 3	
RGMII_CK_TX	DO	24	RGMII transmit clock	
RGMII_CTL_TX	DO	21	RGMII transmit control	
RGMII_TX_0	DO	20	RGMII transmit data bit 0	
RGMII_TX_1	DO	22	RGMII transmit data bit 1	
RGMII_TX_2	DO	23	RGMII transmit data bit 2	
RGMII_TX_3	DO	25	RGMII transmit data bit 3	

The following figure shows the simplified block diagram for Ethernet application.

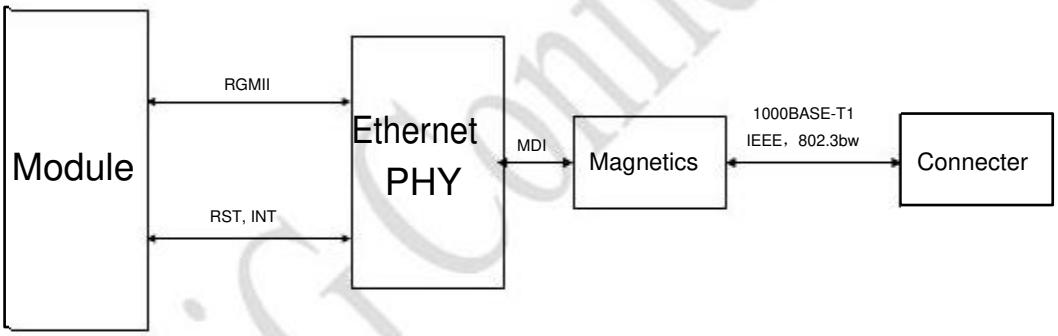


Figure 26Simplified block diagram of automotive Ethernet application

The following is the RGMII interface reference design for the PHY application.

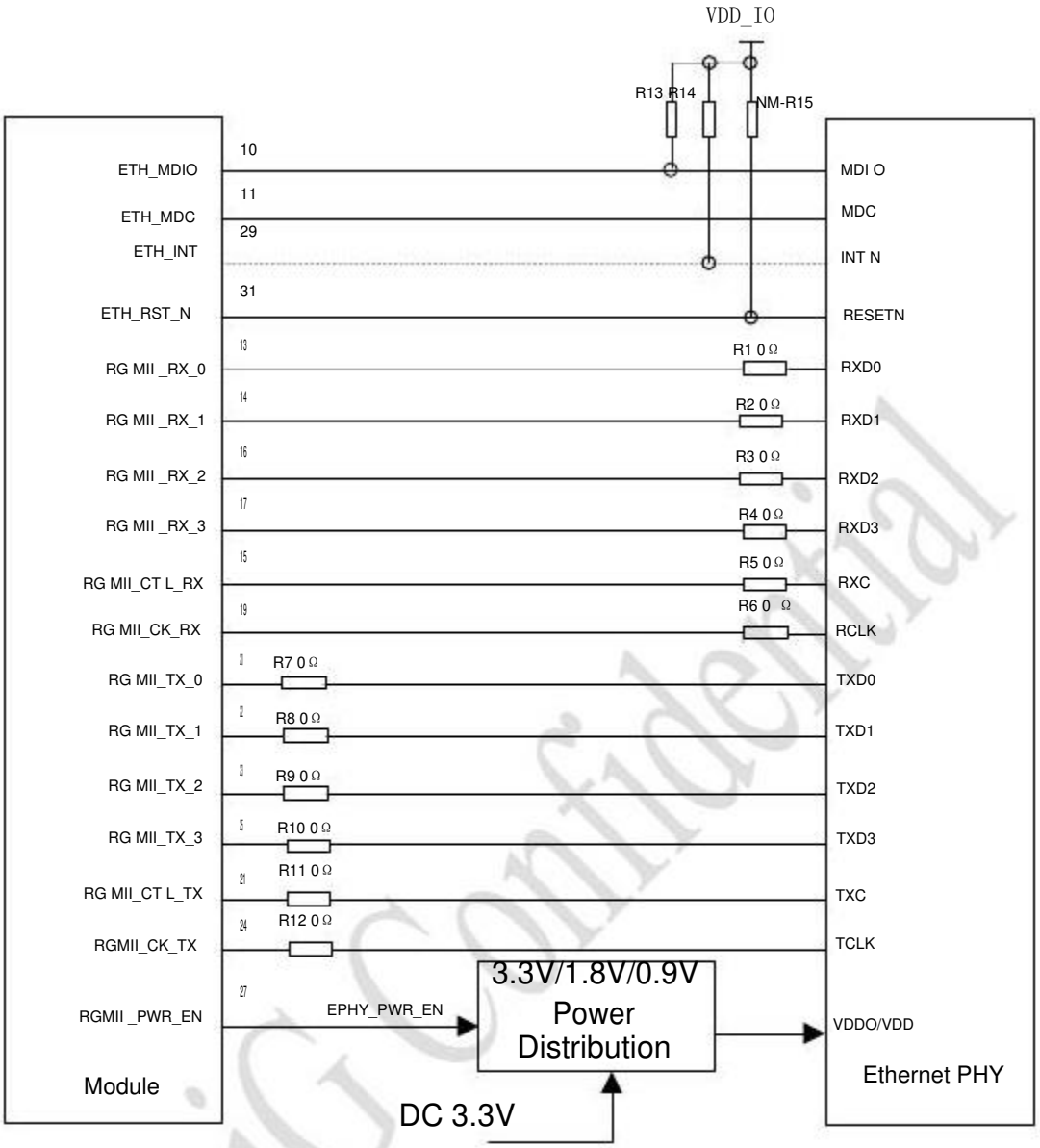


Figure 27 RGMII interface and PHY application reference circuit

To enhance the reliability and availability of application designs, follow the criteria below in the Ethernet

PHY circuit design:

- Keep RGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- The single-ended impedance of RGMII data traces is 50 Ω ±20 %.
- The length matching between Tx signals (RGMII_CK_TX, RGMII_CTL_TX and RGMII_TX_[0:3]) or Rx signals (RGMII_CK_RX, RGMII_CTL_RX and RGMII_RX_[0:3]) is less than 2 mm.
- Keep the spacing between Tx bus traces (RGMII_CK_TX to RGMII_TX_[0:3]/RGMII_CTL_TX) or that between Rx bus traces (RGMII_CK_RX to RGMII_RX_[0:3]/RGMII_CTL_RX) at least 2 times thetrace width.
- Keep the spacing between Tx bus and Rx bus traces at least 2 times trace width.
- Keep the spacing between RGMII and other signal traces at least 3 times trace width.

- Resistors R7–R12 should be placed near the module. Resistors R1–R6 should be placed near the Ethernet PHY. The value of R1–R15 varies with the selection of PHY.
- RGMII_INT and RGMII_RST_N are always 1.8 V power domain. A voltage-level translator should be used when the module I/O level does not match with PHY.

3.16 SGMI Interfaces

The module includes an integrated Ethernet MAC with a SGMII interface. Key features of the SGMII interface are shown below:

- Supports 1000/2500 Mbps operation
- RGMII and SGMII can not operate concurrently

Table 18: Pin Definition of SGMII Interface

Pin name	I/O	Pin	Description	Remark
ETH_MDIO	DIO	10	Ethernet management data	It generally requires a pull-up resistor close to the external PHY end.
ETH_MDC	DO	11	Ethernet management clock	Do not add any pull-up resistor to this pin, or it may cause higher current consumption during sleep mode.
ETH_PWR_EN	D0	27	Enable external power supply to power Ethernet PHY	
ETH_INT	DI	29	Ethernet PHY interrupt input	
ETH_RST	DO	31	Reset output for Ethernet PHY	
RGMII_TX_P	DO	94	RGMII transmit(+)	Require differential impedance of 70–100Ω, and 90Ωis recommended.
RGMII_TX_M	DO	96	RGMII transmit(-)	
RGMII_RX_P	DI	97	RGMII receive(+)	
RGMII_RX_M	DI	99	RGMII receive(-)	

The following figure shows the simplified block diagram for Ethernet application.

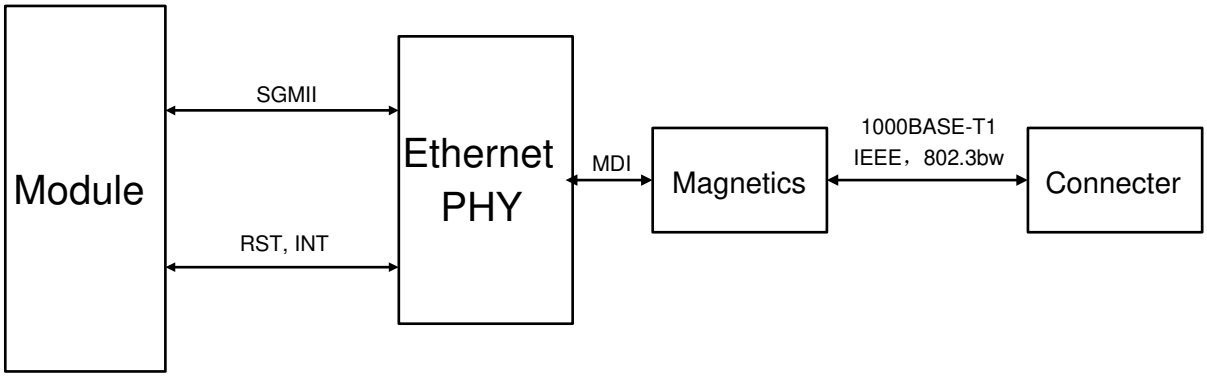


Figure 28 Simplified block diagram of automotive Ethernet application

The following figure shows a reference design of SGMII interface with PHY application. For more details, see document.

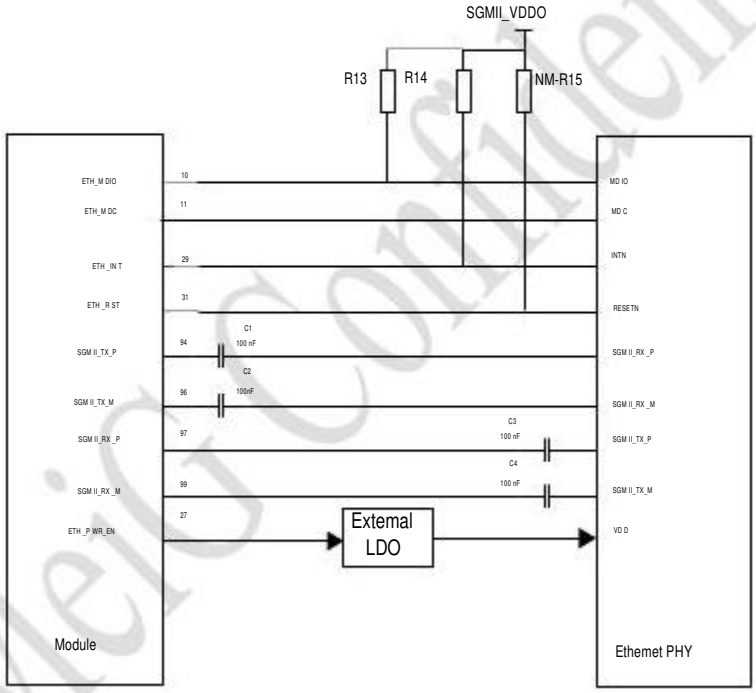


Figure 29 SGMII interface and PHY application reference circuit

To enhance the reliability and availability of application designs, follow the criteria below in the Ethernet PHY circuit design:

- It is important to route the SGMII signal traces as differential pairs with ground surrounded. The differential impedance is 70–100 Ω and 90 Ω is recommended for SGMII Tx/Rx traces.
- SGMII signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from SGMII traces.

- For each differential pair, the intra-lane length match should be less than 0.7 mm, while the inter-lane length match, that is, the trace length matching between the Tx, Rx and reference clock pairs is not required.
- The spacing between Tx and Rx pairs, and the spacing between SGMII lanes and all other signals, should exceed 4 times the trace width (4W).

3.17 RTC

The module has a real time clock within the PMIC, but has no dedicated RTC power supply pin. The RTC is powered by VBAT_BB. If VBAT_BB is removed, the RTC will not maintain. If RTC is needed, then VBAT_BB must be powered.

3.18 DR_SYNC

The module obtains time through GNSS positioning and outputs 1PPS signal for clock synchronization.The DR_SYNC pin usually connects to an external AP and a MCU to maintain the local time consistencybetween the three.

Table 19: Pin Definition of DR_SYNC Interface

Pin name	I/O	Pin	Description
DR_SYNC	DO	95	Dead reckoning sync

A reference design of DR_SYNC interface for clock synchronization application is shown as below:

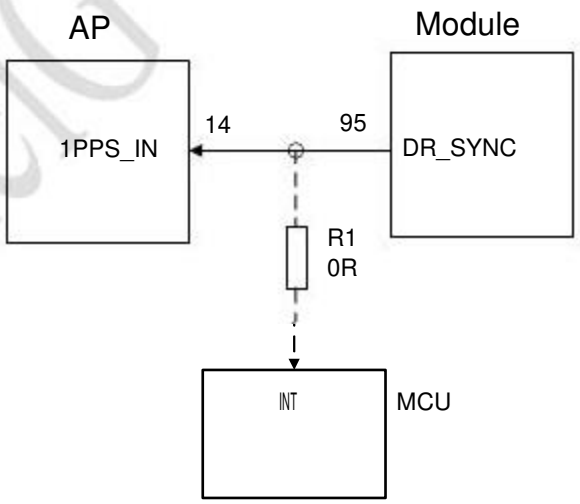


Figure 30 DR SYNC clock synchronization application reference design

Remark:

Pay attention to the level matching of the signal shown in dotted line between the module and the MCU.

3.19 IMU Interrupt Interfaces

The module realizes DR (dead-reckoning) function through an external IMU (inertial measurement unit).
For more details about QDR, see document [9].

Table 20: Pin Definition of IMU Interrupt Interface

				DTE clear to send signal from DCE
				(Connects to DTE's CTS)
UART1_RTS		DI	74	DTE request to send signal to DCE

Pin Name	I/O		Pin	Description
IMU_INT1	DI		169	
IMU_INT2	DI	Module	187	

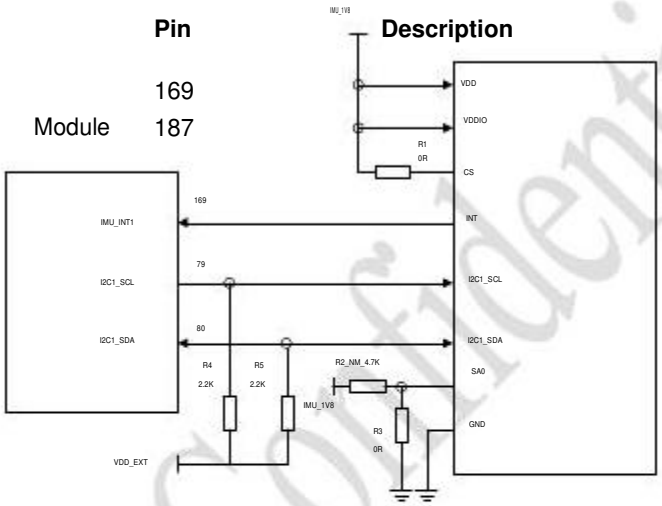


Figure 31 IMU reference design circuit

3.20 UART Interfaces

The MA922 module has 5 serial ports:UART1,UART2,UART3,UART4 and debug UART.

The main features of the main serial port and debug serial port are described below.

- The main serial port supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps baud rate, the default baud rate is 115200bps, used for data transmission and AT command transmission.
- The debugging serial port supports 115200bps baud rate for R&D debugging.

Table 21 Main serial port pin description

Pin name	I/O	Pin	Description
UART1_TXD	DO	70	Module sends data
UART1_RXD	DI	72	Module accepts data
UART1_CTS	DO	71	DTE clear to send signal from DCE (Connects to DTE's CTS)
UART1_RTS	DI	74	DTE request to send signal to DCE

Pin Name	I/O	Pin	Description
IMU_INT1	DI	169	IMU interrupt signal, suspended if not used.
IMU_INT2	DI	187	IMU interrupt signal, suspended if not used.

Pin name	I/O	Pin	Description
UART1_TXD	DO	70	Module sends data
UART1_RXD	DI	72	Module accepts data
UART1_CTS	DO	71	below: IAM-20680HT IMU interrupt signal, suspended if not used. IMU interrupt signal, suspended if not used.

			(Connects to DTE's RTS)
UART2_TXD	DO	59	Module sends data
UART2_RXD	DI	63	Module accepts data
UART2_CTS	DO	62	DTE clear to send signal from DCE (Connects to DTE's CTS)
UART2_RTS	DI	61	DTE request to send signal to DCE (Connects to DTE's RTS)
UART3_TXD	DO	298	Module sends data
UART3_RXD	DI	297	Module accepts data
UART4_TXD	DO	296	Module sends data
UART4_RXD	DI	295	Module accepts data
DBG_TXD	DO	107	Module sends data,It is recommended to reserve test points for debug UART
DBG_RXD	DI	110	Module accepts data.It is recommended to reserve test points for debug UART

Table 22 Serial port logic levels

Parameter	Minimum	Maximum value	Unit
VIL_	-0.3	0.6	V
V_{IH}	1.2		V
VOL_	0		V
VOH_	1.35		V

The module provides 1.8 V UART interfaces. Use a voltage-level translator if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design. It is recommended that the enable pin of the translator is controlled by VDD_EXT, then its built-in pull-ups will not influence the module normal operation.

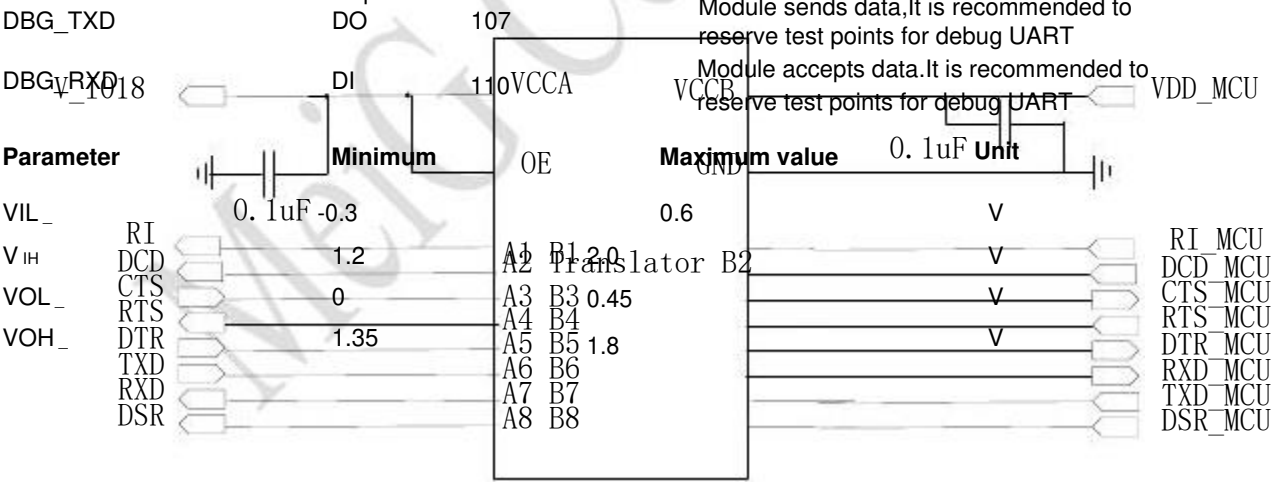


Figure 32 Level conversion chip reference circuit

Another level shifting circuit is shown in the figure below. The input and output circuit design of the dotted line part below can refer to the solid line part, but pay attention to the connection direction. At the same time, this level conversion circuit is not suitable for applications with baud rate exceeding 460Kbps.

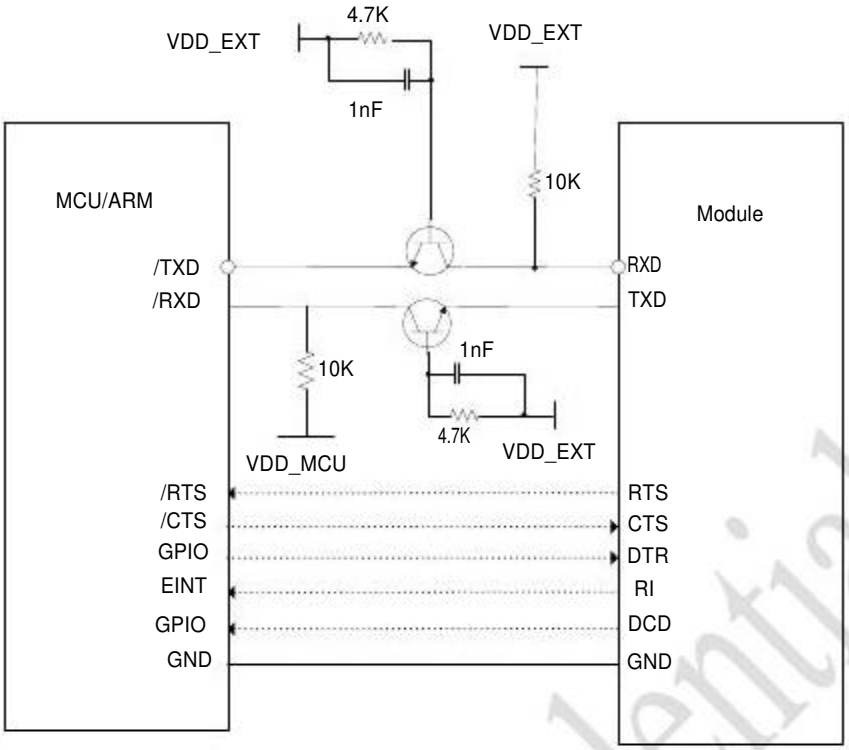


Figure 33 UART signal connection 2

Remark:

When designing, it is recommended to reserve 0R resistors and parallel capacitors on the main serial port and debug serial port lines, which can be added on the bottom plate to prevent RF interference.

3.21 Low Power Mode

3.21.1 Flight Mode

The MA922 module supports entry into airplane mode:

Table 23: Airplane mode Settings description

1	AT command control	AT+CFUN=4--Enter airplane mode AT+CFUN=1--Enter normal mode

3.21.2 Sleep Mode

The module can activate sleep mode in the following ways:

AT to be determined

3.21.3 Ultra-low Power ModeT

Use the following AT instructions to put the module into ultra-low power mode (can be used for power testing)

AT to be determined

3.22 ADC Function

The module provides two analog-to-digital converter (ADC) interfaces. To improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 24 ADC pin description

Pin name	I/O	Pin	Description
ADC0	I	247	Voltage range:0–1.875 V
ADC1	I	245	
ADC2	I	113	

Remark:

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.23 USB_BOOT Interface

MA922 supports USB_BOOT function . Customers can short- circuit USB_BOOT and VDD_EXT before

the module is turned on, and the module will enter the forced download mode when the module is turned on. In this mode, the module can be upgraded through the USB interface.

Table 25 USB_BOOT pin definition

Pin name	I/O	Pin	Description
USB_BOOT	DI	83	It is recommended to reserve test points.
VDD_EXT	PO	68	

4. Antenna Interfaces

The MA922 module is designed with three antenna interfaces, and the impedance of the antenna interface is 50Ω.

Table 26 Antenna interface pin definition

Pin name	Pin number	Description	I/O	Remark
ANT_MAIN	49	main antenna interface	IO	50Ω impedance
BT_ANT	35	WIFI/BT antenna interface	IO	50Ω impedance
ANT_GNSS	47	GPS antenna interface	IO	50Ω impedance

4.1 Introduction of Antenna Interface

MA922 provides three antenna pins: ANT_MAIN, BT-ANT, ANT_GNSS to improve the TDD-LTE/ FDD-LTE, WIFI/BT, GNSS transceiver performance of the product. It is recommended that users use an antenna with an impedance of 50Ω that matches the RF connector on the module end.

Remark:

To ensure communication capability in all frequency bands, please connect all antennas .

It is recommended that the RF adapter cable be carefully selected on the application side. It is necessary to choose an RF patch cord with as little loss as possible. It is recommended to use RF patch cables with the following RF loss requirements:

- GSM900 < 0.6 dB;
- DCS1800 < 1.0 dB;
- TDD- LTE< 1.2dB;
- FDD-LTE < 1.2dB ;
- WIFI/BT<1.2dB;
- GNSS<1.0dB.

The RF Connectors are recommended：

Product name		MHF ILK	MHF I	MHF I	MHF III
Appearance					
		MHF I with mechanical lock	Best Insertion Loss	Most Cable O.D. options	low profile 1.60mm
Plug part number		-	20767-001R	20279-112R-**	20609-002R
Receptacle part number		20279-001E-**(3 pads) 20441-001E-01(4 pads)			20369-001E-**
Maximun height (mm)		2.0	3.0	2.5	1.6
Outside dimension of receptacle(mm)		3.0×3.0			2.0×2.0
Coax O.D. (Center Conductor AWG)	2.00 mm(26)		●		
	1.80 mm(30)	●		●	
	1.37 mm(30)	●		●	
	1.32 mm(32)	●		●	
	1.13 mm(32)	●		●	
	0.95 mm(33)				
	0.81mm (33)				
	0.81 mm(36)	●		●	●
	0.64 mm(36)				●
	0.48 mm(38)				
Frequency		DC - 6GHz			DC - 6GHz
VSWR (L=100mm)	DC-3GHz	1.3 max.(PLUG)/1.3 max.(RECE)			1.3 max.
	3GHz-6GHz	1.5 max.(PLUG)/1.4 max.(RECE)			1.5 max.
	6GHz-9GHz	1.9 max.(PLUG)/1.9 max.(RECE)		1.6 max.(PLUG) 1.8 max.(RECE)	-
	9GHz-12GHz	-			
	12GHz-15GHz	-			
Service temp.(Celsius)		-40 degree - 90degree			
Characteristic impedance		50ohm			
Rated voltage		AC60V			
Contact resistance		20m ohm max.			
Withstand voltage		AC200V/min			
Insulation resistance		500M ohm min./DC100V			

Figure 34. The RF Connector

4.2 RF Reference Circuit

4.2.1 Antenna Connection Reference Design

The SDR0_ANT0, SDR0_ANT1, SDR0_ANT2, SDR0_ANT3, CV2X_ANT5, CV2X_ANT6, SDR_GNSS_ANT4 antenna connection reference design circuit is shown in the figure below. In order to obtain better RF performance, the following four points should be paid attention to in schematic design and PCB layout:

1. Schematic design, a π-type matching circuit is reserved near the RF port of the module, and the capacitor is not pasted by default;

2. Schematic design, redundant RF connectors between the module RF port and the antenna are used for certification testing, and the RF connectors may not be attached after mass production and delivery; (Reference: RF Connector-1P-H176);

3. Schematic design, a π-type matching circuit is reserved near the antenna end, and the capacitor is not pasted by default;

4. PCB layout, the wiring between the module RF port and the antenna is as short as possible, and the board factory needs to do 50Ω impedance control on the RF wiring.

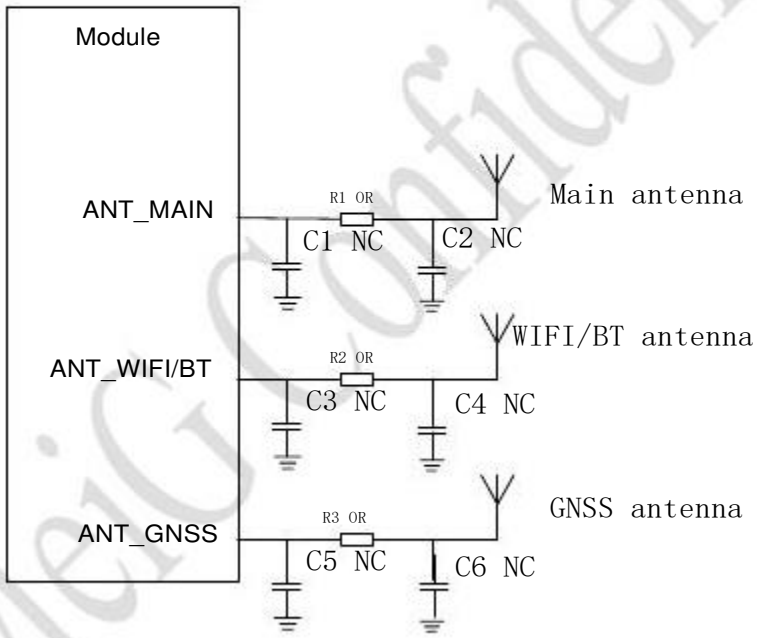


Figure 35 RF Reference Circuit

4.2.2 RF Signal Line Layout

For the user PCB, the characteristic impedance of all the RF signal lines shall be controlled at 50 Ω. Generally, the impedance of the RF signal line is determined by the dielectric constant of the material, the wiring width (W), the ground gap (S), and the height (H) of the reference ground plane. The control of PCB property impedance usually adopts microband line and coplanar waveguide. To reflect the design principles, the following pictures show the structural design of the microstrip line and the coplanar waveguide when the impedance line controls the 50Ωwaveguide.

W1: Maximum line width W2: minimum line width T1: copper thickness H1: plate medium thickness ERI: plate dielectric constant.

- Microband line complete structure

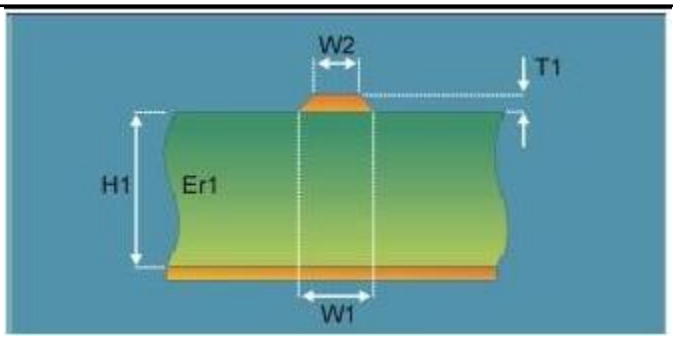


Figure 36 Microband line structure of two-layer PCB plates

- Complete structure of the coplanar waveguide

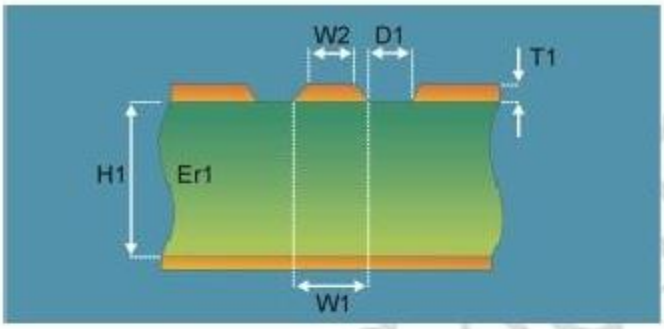


Figure 37 Co-planar waveguide structure of two-layer PCB plates

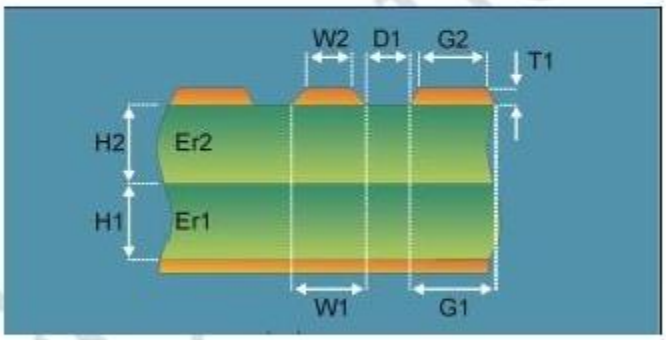


Figure 38 Multi-layer PCB board common-planar waveguide structure (reference for the third layer)

In the circuit design of RF antenna interface, the following design principles are recommended to ensure the good design and reliability of RF signal：

- Precise 50 Ω impedance control of the RF signal lines shall be performed using impedance simulation calculation tools.

- GND pins adjacent to RF pins do not make hot pads and make full contact with the ground.

- The distance between the RF pin and the RF connector should be as short as possible; also avoid a recommended alignment angle of 135.

- When the connection device package is established, the signal foot should keep a certain distance from the ground.

- The ground plane of the RF signal line reference shall be complete; adding a certain amount of ground holes around the signal line and the reference ground may help improve the RF

performance; the distance between the ground hole and the signal line shall be at least 2 times the line width (2 W).

 RF signal lines must be away from interference sources and avoid crossing or parallel to any signal lines in adjacent layers.

4.3 Antenna installation

4.3.1 Antenna Requirements

Antenna The requirements for the receiving antenna are shown in the table below:

Table 27 Antenna requirements

Type	Requirement
GSM/TDD-LTE/FDD-LTE/NR	VSWR: < 2
	Gain (dBi): 1
	Maximum input power (W): 2W
	Input Impedance (ohm): 50
	Polarization Type: Vertical
	Cable insertion loss: < 1.5dB (GSM 900 / 18 00 ; LTE B 1 /B 3 /B 5 /B 8 /B 34 / B39)
	Cable Insertion Loss: < 2dB (LTE B38/B40/B41)
C-V2X	Frequency range: 5855–5925 MHz
	Gain: Min. 4 dBi
	VSWR: ≤ 2
	efficiency: > 30 %
	Maximum output power: 10 W
	Recommended antenna pattern: ±10–15°(Azimuth Beamwidth: 360°
	Elevation beamwidth: ±10–15°)
	Input Impedance (ohm): 50 Ω
	Cable insertion loss: < 2 dB: C-V2X TDD B47
GNSS	VSWR: < 2
	Gain (dBi): 1
	Maximum input power (W): 0.1 W
	Input Impedance (ohm): 50
	Polarization Type: Vertical
	Cable insertion loss: < 1.5dB

4.3.2 RF Output Power

The RF output power of the MA922 is shown in the table below.

Table 28 MA922 RF transmit power

Frequency	Maximum value	Minimum
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
WCDMA	23 dBm ±2 dB (Class 3)	WCDMA
LTE	23dBm±2dB(Class 3)	LTE

Remark:

Information on other sub-models and frequency bands will be reflected in subsequent editions of the

4.3.3 RF Receive Sensitivity

Table 29 MA922 module RF receiving sensitivity

Frequency	Receiving Sensitivity (Typical BW) -10M			
	Main episode	Separation	Main episode + Diversity	3GPP (Main + Diversity)
EGSM900	-108dBm	NA	NA	-102.4dBm
DCS1800	-108dBm	NA	NA	-102.4dBm
LTE-FDD B1	-97dBm	NA	NA	-96.3dBm
LTE-FDD B3	-97dBm	NA	NA	-93.3dBm
LTE-FDD B5	-98dBm	NA	NA	-94.3dBm
LTE-FDD B8	-98dBm	NA	NA	-93.3dBm
LTE-FDD B28A	-98dBm	NA	NA	-93.3dBm
LTE-TDD B34	-97.5dBm	NA	NA	-96.3dBm
LTE-TDD B38	-97.5dBm	NA	NA	-96.3dBm
LTE-TDD B39	-97.5dBm	NA	NA	-96.3dBm
LTE-TDD B40	-97.5dBm	NA	NA	-96.3dBm
LTE-TDD B41	-97.5dBm	NA	NA	-94.3dBm
WCDMA B1	-106.7	NA	NA	-106.7
WCDMA B8	-106.7	NA	NA	-103.7
5G NR FDD n1	-95.8	NA	NA	-95.8
5G NR FDD n3	-92.8	NA	NA	-92.8
5G NR FDD n8	-92.8	NA	NA	-92.8
5G NR FDD n28A	-90.1	NA	NA	-90.1
5G NR FDD n41	-86.7	NA	NA	-86.7
5G NR FDD n78	-86.8	NA	NA	-86.8
5G NR FDD n79	-86.8	NA	NA	-86.8
5G NR FDD n77	-86.3	NA	NA	-86.3

document.

4.3.4 Operating Frequency

Table 30 MA922 operating frequency

3GPP frequency band	Send	Take over	Unit
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE-FDD B28A	703–733	758–788	MHz
LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz
C-V2X B47	5855–5925	5855–5925	MHZ
5G NR FDD n1	1920–1980	2110–2170	MHZ
5G NR FDD n3	1710~1785	1805~1880	MHZ
5G NR FDD n8	880~915	925~960	MHZ
5G NR FDD n28A	703–733	758–788	MHZ
5G NR FDD n41	2496–2690	2496–2690	MHZ
5G NR FDD n77	3300–4200	3300–4200	MHZ
5G NR FDD n78	3300–3800	3300–3800	MHZ
5G NR FDD n79	4400–5000	4400–5000	MHZ
GPS	/	L1:1575.42±1 L5: 1176.45±1	MHZ
BDS	/	1559~1563	MHZ
Glonass	/	1597~1606	MHZ

5. Electrical Characteristics

5.1 Limited Voltage Range

The limit voltage range refers to the module power supply voltage and the maximum voltage range that the digital and analog input/output interfaces can withstand. Working outside this range may result in damage to the product.

The limit voltage range of MA922 is shown in the table below.

Table 31 The limit working voltage range of the module

Parameter	Description	Minimum	Typical value	Maximum value	Unit
VBAT_BB, VBAT_RF	VBAT_BB and VBAT_RF	-0.3	3.8	6.0	V
USB_VBUS	USB connection detect	-0.3	5.0	5.5	V
VBAT_CV2X	Power supply for the module's C-V2X part	-0.5	5.0	5.3	V
Voltage at Digital Pins	Digital I/O supply voltage	-0.3		2.13	V
Voltage at ADC0		0		4.8	V
Voltage at ADC1		0		4.8	V

parameter	minimum	Typical value	maximum value	unit
Operating temperature	-35	+25	+75	℃
Extended Temperature Range	-40	-	+ 85	℃
Emergency Call	-40	-	+ 95	℃

5.2 Ambient Temperature Range

MA922 module is recommended to work in the environment of -30~+70 ℃。It is recommended that the application side consider temperature control measures under harsh environmental conditions. At the same time, the extended operating temperature range of the module is provided. When used under extended temperature, the function is normal, but some RF indicators may deteriorate. At the same time, it is recommended that the module application terminal be stored under certain temperature conditions. Modules beyond this range may not work properly or may be damaged.

Table 32 Module temperature range

Parameter	Description	Minimum	Typical value	Maximum value	Unit
VBAT_BB, VBAT_RF	VBAT_BB and VBAT_RF	-0.3	3.8	6.0	V
USB_VBUS	USB connection detect	-0.3	5.0	5.5	V
VBAT_CV2X	Power supply for the module's C-V2X part	-0.5	5.0	5.3	V
Voltage at	Digital I/O supply voltage	-0.3		2.13	V

Module state	Pilot projects	Test case	Result (mA)
Shutdown	Shutdown leakage current	Maintain normal voltage (3.8 V) power supply in case of power failure	TBD

5.3 Module Power Consumption Range

Table 33 Power consumption

Module state	Pilot projects	Test case	Result (mA)
Shutdown	Shutdown leakage current	Maintain normal voltage (3.8 V) power supply in case of power failure	TBD
	Real Bottom current network sleep	Power on, no sim card, no T card, test the minimum current value in flight mode.	TBD
Hibernate	Real network sleep	Insert the mobile card, wait for the actual network, use the AT command to query the registration on the network, and record the average current for 10 minutes.	TBD
		Insert the China Unicom card, wait for the actual network, use the AT command to query and register on the network, and record the average current for 10 minutes.	TBD
		Insert the telecommunication card, wait for the actual network, use the AT command to query and register on the network, and record the average current for 10 minutes.	TBD
Hibernate	GSM850 powered on, and the USB is in a suspended state	GSM850 CH190 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT commands (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
	GSM850 the module is powered on, and the USB is in a suspended state	GSM850 CH128 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT commands (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
Temperature	-40 - + 95 °C	GSM850 CH190 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT commands (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current	TBD
Storage			

Temperature Range
Storage temperature -40 - + 95 °C

			for 10 minutes.	
			GSM850 CH251 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT commands (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
	GSM900		GSM900 CH62 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			GSM900 CH1 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is in the suspended state) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			GSM900 CH124 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT commands (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD

	DCS		DCS CH698 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			DCS CH512 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			DCS CH885 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
	PCS		PCS CH661 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			PCS CH512 1) The module under test is powered on and successfully registered with the data network;	TBD

			2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	
			PCS CH810 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
	FDD	The module is powered on, registered in the network idle state, the DRX monitoring period is 1.28s , no data transmission, and the USB is in the suspended state	Band1 CH18300 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band1 CH18050 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band1 CH18550 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the	TBD

			state of no data transmission for 10 minutes, and records Average current for 10 minutes.	
			Band3 CH19575 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band3 CH19250 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band3 CH19900 1) The module under test is powered on and successfully registered to the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band5 CH20525 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD

			Band5 CH20450 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band5 CH20600 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band8 CH21625 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band8 CH21500 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band8 CH21750 1) The module under test is powered on and successfully registered with the data network;	TBD

			2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	
	TDD	The module is powered on, registered in the network idle state, the DRX monitoring period is 1.28s , no data transmission, and the USB is in the suspended state	Band34 CH36275 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band34 CH36250 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT commands (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band34 CH36300 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band38 CH38000 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the	TBD

			state of no data transmission for 10 minutes, and records Average current for 10 minutes.	
			Band38 CH38250 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band38 CH38300 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band39 CH38450 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band39 CH38300 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in the suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD

			Band39 CH38600 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state through AT command (USB is in suspended state); 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band40 CH39150 1) The module under test is powered on and successfully registered to the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band40 CH38700 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band40 CH39600 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band41 CH40620 1) The module under test is powered on and successfully registered with the data network;	TBD

			2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	
			Band41 CH40290 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
			Band41 CH41190 1) The module under test is powered on and successfully registered with the data network; 2) The module is set to sleep state (USB is suspended) through AT commands; 3) The module under test remains in the state of no data transmission for 10 minutes, and records Average current for 10 minutes.	TBD
	FDD	The module is powered on and registered in the network idle state. The DRX monitoring period is 1.28s , no data transmission, and the USB is active.	Band1 CH18300 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band1 CH18050 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band1 CH118550 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band3 CH19575 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is	TBD

			recorded.	
			Band3 CH19250 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band3 CH19900 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band5 CH20600 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band5 CH20450 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band5 CH20525 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band8 CH21750 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band8 CH21625 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			The Band8 CH21500 module under test remains in the state of no data transmission for 10 minutes, and the average current for 10 minutes is recorded.	TBD
	TDD	The module is powered on, registered in the network idle	Band34 CH436275 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is	TBD

		state, the DRX monitoring period is 1.28s , no data transmission, and the USB is in the suspended state	recorded.	
			Band34 CH36250 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band34 CH36300 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band38 CH38300 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band38 CH37800 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band38 CH38200 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band39 CH38450 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band39 CH38300 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band39 CH38600 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band40 CH39150 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is	TBD

			recorded.	
			Band40 CH38700 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band40 CH39600 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band41 CH40620 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band41 CH40209 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
			Band41 CH41190 module under test is kept for 10 minutes without data transmission, and the average current for 10 minutes is recorded.	TBD
	Real network data hibernation	Unicom/Mobile	Keep the data connection and send a 256-byte packet every 5 minutes. The server returns a 256-byte packet	TBD
	FDD	1) Indoor room temperature state; 2) Use DC power supply to supply the module, the voltage is set to 3.8V;	Band1 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band1 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band1 23dBm CH18300 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band1 23dBm CH18050	TBD

			module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	
			Band1 23dBm CH18550 module under test performs data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band3 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band3 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band3 23dBm CH19575 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band3 23dBm CH19250 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band3 23dBm CH19900 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band5 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band5 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band5 23dBm CH20525 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD

			Band5 23dBm CH20450 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band5 23dBm CH20600 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band8 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band8 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band8 23dBm CH21625 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band8 23dBm CH21500 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band8 23dBm CH21750 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band34 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band34 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
	TDD		Band34 23dBm CH36275 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD

			Band34 23dBm CH36250 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band34 23dBm CH36300 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band38 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band38 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band38 23dBm CH38000 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band38 23dBm CH37800 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band38 23dBm CH38200 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band39 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band39 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band39 23dBm CH38450 module under test performs data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD

			Band39 23dBm CH38300 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band39 23dBm CH38600 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band40 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band40 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band40 23dBm CH39150 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band40 23dBm CH38700 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band40 23dBm CH39600 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band41 0dBm module under test for data transmission and hold for 5 minutes, record the average current for 5 minutes	TBD
			Band41 10dBm module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band41 23dBm CH40620 module under test conducts data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD

			Band41 23dBm CH40290 module under test performs data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
			Band41 23dBm CH41190 module under test performs data transmission and keeps it for 5 minutes, and records the average current for 5 minutes	TBD
	5G SA		n41A CH509202 @ 23. 30 dBm n41A CH518598 @ 23.49 dBm n41A CH528000 @ 23.42 dBm n77A CH623334 @ 26.01 dBm n77A CH650000 @ 26.06 dBm n77A CH676666 @ 26.00 dBm n78A CH623334 @ 25.97 dBm n78A CH636666 @ 25.99 dBm n78A CH650000 @ 26.21 dBm n1A CH426000 @ 23.05 dBm n1A CH428000 @ 23.29 dBm n1A CH430000 @ 23.33 dBm n3A CH364000 @ 23.30 dBm n3A CH368500 @ 23.26 dBm n3A CH373000 @ 23.08 dBm n8A CH364000 @ 23.30 dBm n8A CH368500 @ 23.26 dBm n8A CH373000 @ 23.08 dBm n28A CH154600 @ 22.99 dBm The module under test transmits data and holds it for 5 minutes, recording the average current for 5 minutes	TBD
	5G NSA		1A_n78A CH623334 @ 22.85 dBm 1A_n78A CH636666 @ 22.85 dBm 1A_n78A CH650000 @ 22.78 dBm 3A_n78A CH623334 @ 25.71 dBm 3A_n78A CH636666 @ 25.67 dBm 3A_n78A CH650000 @ 25.60 dBm 5A_n78A CH623334 @ 22.98 dBm 5A_n78A CH636666 @ 22.56 dBm 5A_n78A CH650000 @ 22.95 dBm 7A_n78A CH623334 @ 23.07 dBm 7A_n78A CH636666 @ 22.94 dBm 7A_n78A CH650000 @ 23.09 dBm 8A_n78A CH623334 @ 22.92 dBm 8A_n78A CH636666 @ 22.51 dBm 8A_n78A CH650000 @ 22.91 dBm 38A_n78A CH623334 @ 23.17 dBm	TBD

			38A_n78A CH636666 @ 23.15 dBm 38A_n78A CH650000 @ 23.23 dBm 40A_n78A CH623334 @ 22.97 dBm 40A_n78A CH636666 @ 22.94 dBm 40A_n78A CH650000 @ 23.06 dBm 1A_n77A CH623334 @ 22.90 dBm 1A_n77A CH650000 @ 22.80 dBm 1A_n77A CH676666 @ 22.92 dBm 3A_n77A CH623334 @ 25.75 dBm 3A_n77A CH650000 @ 25.68 dBm 3A_n77A CH676666 @ 25.68 dBm 5A_n77A CH623334 @ 22.98 dBm 5A_n77A CH650000 @ 23.03 dBm 5A_n77A CH676666 @ 22.99 dBm 7A_n77A CH623334 @ 23.08 dBm 7A_n77A CH650000 @ 23.04 dBm 7A_n77A CH676666 @ 23.15 dBm 8A_n77A CH623334 @ 22.87 dBm 8A_n77A CH650000 @ 23.02 dBm 8A_n77A CH676666 @ 23.08 dBm The module under test transmits data and holds it for 5 minutes, recording the average current for 5 minutes	

5.4 ESD Characteristics

The module is not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling and operating modules.Refer to the table below for .

6. Mechanical Characteristics

This chapter describes the mechanical dimensions of the module, all dimensions are in millimeters, and all dimensions without tolerances are ±0.05mm.

6.1 Module Mechanical Dimensions

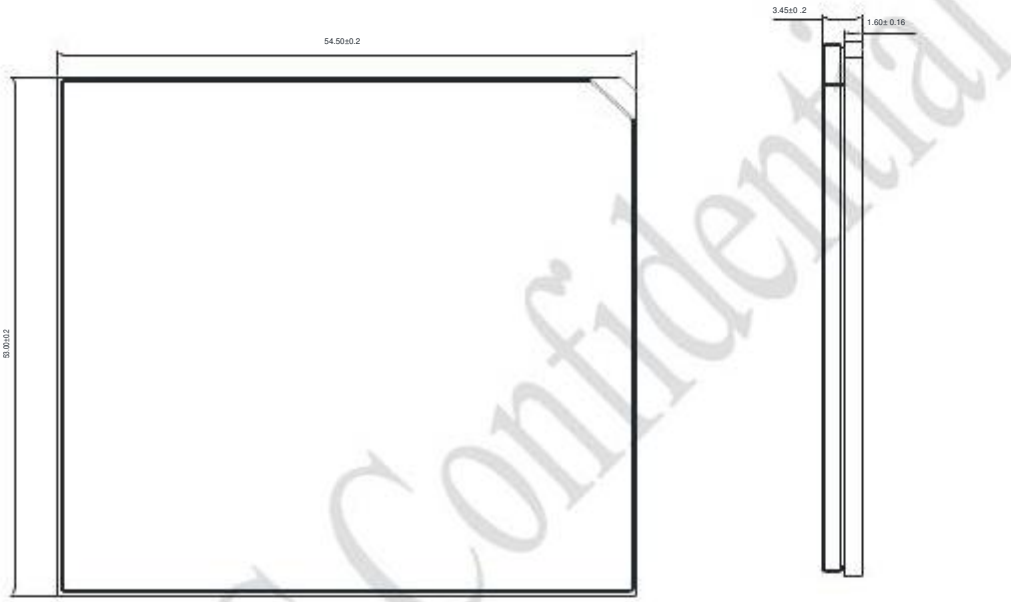


Figure 39 Top view and side view dimension drawing (unit: mm)

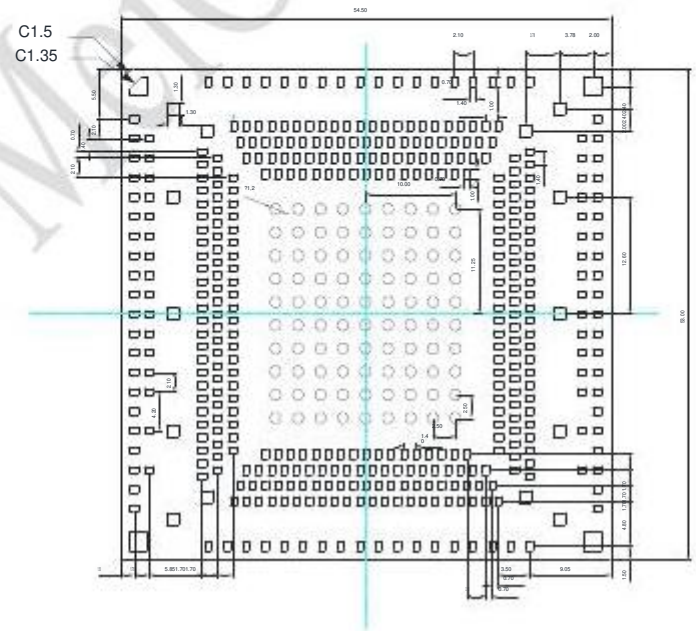
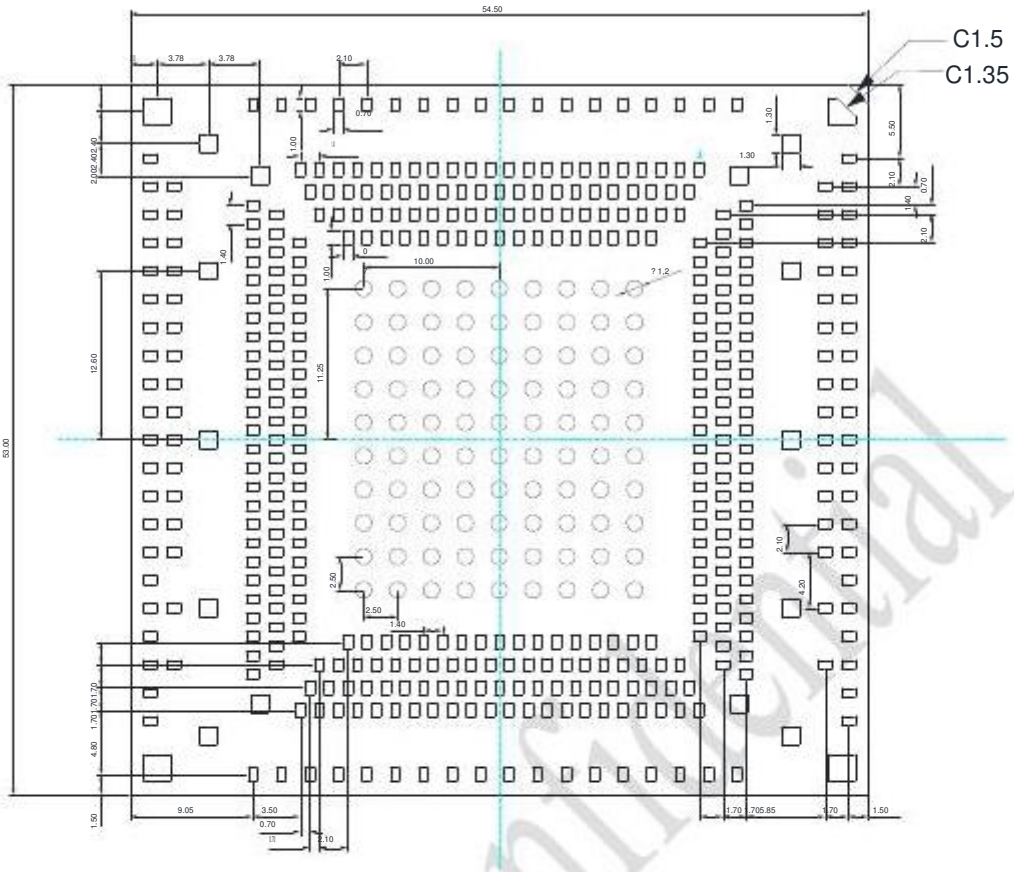
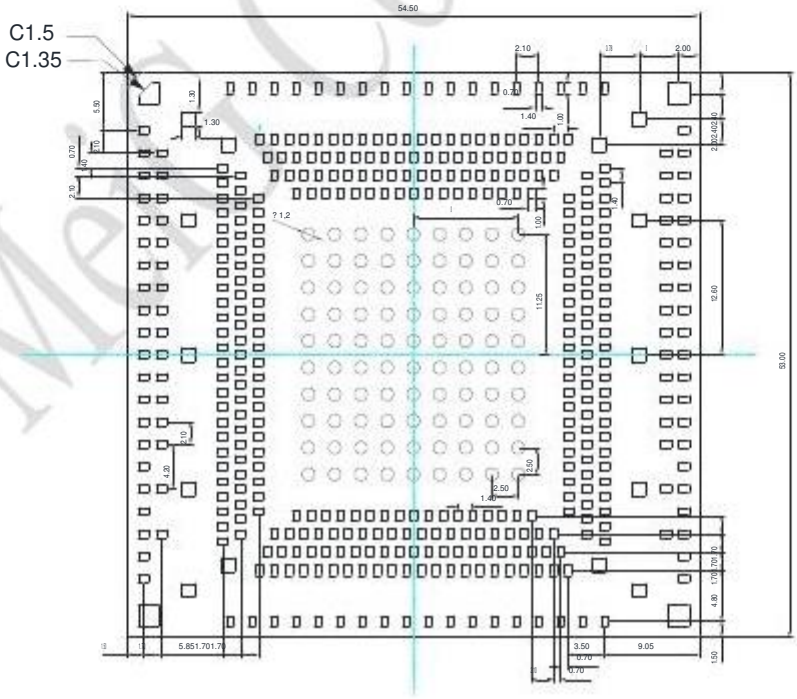


Figure 40 Bottom view dimension drawing (unit: mm)

6.2 Recommended Package



a. Recommended packaging



b. Recommended packaging

Figure 41 Recommended package (top view) (unit: mm)

6.3 Module Top View

Figure 42 Module top view

6.4 Module Bottom View

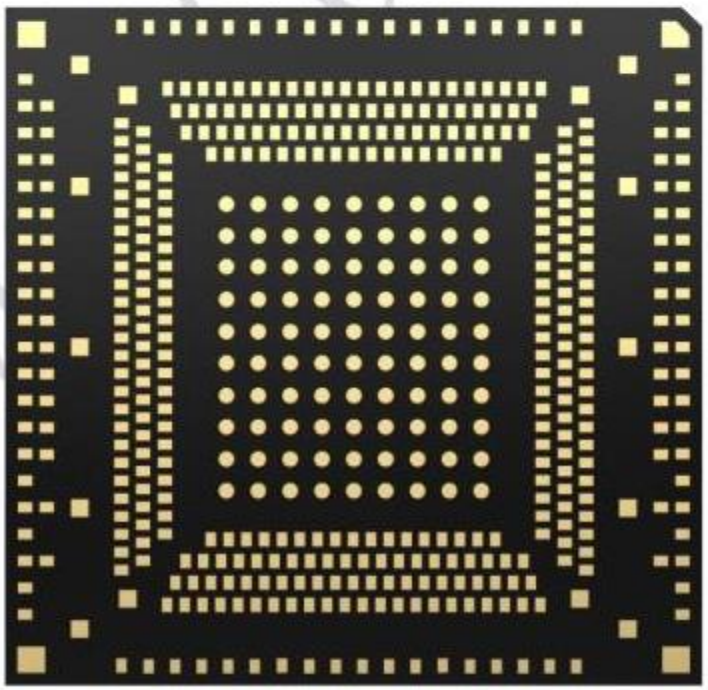


Figure 43 Bottom view of the module

7. Storage and Production

7.1 Storage

The MA922 ships in a vacuum-sealed bag. The storage of modules must comply with the following conditions:

1. When the ambient temperature is lower than 40 degrees Celsius and the air humidity is lower than 90%, the module can be stored in a vacuum-sealed bag for 12 months;
2. After the vacuum-sealed bag is opened, the module can be directly reflowed or other high-temperature processes if the following conditions are met:
   - Module storage air humidity is less than 10%;
   - The ambient temperature of the module is lower than 30 degrees Celsius, the air humidity is less than 60%, and the factory can complete the patch within 72 hours.
3. If the module is under the following conditions, it needs to be baked before placement:
   - When the ambient temperature is 23 degrees Celsius (the fluctuation of 5 degrees Celsius is allowed), the humidity displayed by the humidity indicator card is greater than 10%;
   - When the vacuum seal bag is opened, the ambient temperature of the module is lower than 30 degrees Celsius, and the air humidity is less than 60%, but the factory failed to complete the patch within 168 hours;
   - When the vacuum-sealed bag is opened, the module storage air humidity is greater than 10%.
4. bake it for 8 hours at 125°C (allow 5°C fluctuations up and down).

Remarks :

The mod's packaging cannot withstand such high temperatures, please remove the mod's packaging before the mod is baked.

7.2 Production Welding

Figure 44 Reflow Soldering Temperature Curve

7.3 Package

The MA922 is packaged in a tray. The packaging size of the tray is 310*200*20mm (**PCS) and placed as follows:

Figure 45 Pallet Packaging(undetermined)

8. Appendix A Reference Documents and Term Abbreviations

8.1 Reference Document

- MA922 module specifications;
- MA922 AT command set;
- MA922 EVB User Manual;
- MA922 reference design circuit;
- MA922 Application Business Process Manual.

8.2 Term Abbreviation

Table 34 Abbreviations of terms

Abbreviation	English description	Chinese description
AMR	Adaptive Multi-rate	自适应多速率
BER	Bit Error Rate	误码率
BTS	Base Transceiver Station	基站收发信台
PCI	Peripheral Component Interconnect	外设部件互连
CS	Circuit Switched (CS) domain	电路域
CSD	Circuit Switched Data	电路交换数据
DCE	Data communication equipment	数据电路终端设备
DTE	Data terminal equipment	数据终端设备
DTR	Data Terminal Ready	数据终端就绪
EDGE	Enhanced Data rates for GSM Evolution	增强型GPRS
EFR	Enhanced Full Rate	增强型全速率
EGSM	Enhanced GSM	增强型GSM
EMC	Electromagnetic Compatibility	电磁兼容性
ESD	Electrostatic Discharge	静电释放
FR	Frame Relay	帧中继
GMSK	Gaussian Minimum Shift Keying	高斯最小移频键控
GPIO	General Purpose Input Output	通用输入/输出
GPRS	General Packet Radio Service	通用分组无线系统
GSM	Global Standard for Mobile Communications	全球标准移动通信系统
HR	Half Rate	半速
HSDPA	High Speed Downlink Packet Access	高速下行分组接入
HSUPA	High Speed Uplink Packet Access	高速上行分组接入
HSPA	HSPA High-Speed Packet Access	高速分组接入
HSPA+	HSPA High-Speed Packet Access+	增强型高速分组接入

IEC	International Electro-technical Commission	国际电工技术委员会
IMEI	International Mobile Equipment Identity	国际移动设备标识
MEID	Mobile Equipment Identifier	CDMA终端的身份识别码
I/O	Input/Output	输入/输出
ISO	International Standards Organization	国际标准化组织
ITU	International Telecommunications Union	国际电信联盟
bps	bits per second	比特每秒
led	Light Emitting Diode	发光二极管
M2M	Machine to machine	机器到机器
MO	Mobile Originated	移动台发起的
MT	Mobile Terminated	移动台终止的
NTC	Negative Temperature Coefficient	负温度系数
PC	Personal Computer	个人计算机
PCB	Printed Circuit Board	印制电路板
PCS	Personal Cellular System	个人蜂窝系统
PCM	Pulse Code Modulation	脉冲编码调制
PCS	Personal Communication System	GSM1900
PDU	Packet Data Unit	分组数据单元
PPP	Point-to-point protocol	点到点协议
PS	Packet Switched	分组交换
QPSK	Quadrate Phase Shift Keying	正交相位移频键控
SIM	Subscriber Identity Module	用户识别模组
TCP/IP	Transmission Control Protocol/ Internet Protocol	传输控制协议/互联网协议
UART	Universal asynchronous receiver-transmitter	通用异步收/发器（机）
USIM	Universal Subscriber Identity Module	通用用户识别模组
UMTS	Universal Mobile Telecommunications System	通用移动通信系统
USB	Universal Serial Bus	通用串行总线
WCDMA	Wideband Code Division Multiple Access	宽带码分多址
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access	时分同步码分多址
TDD-LTE	Time Division Long Term Evolution	时分长期演进
FDD-LTE	Frequency Division Duplexing Long Term Evolution	频分长期演进
Vmax	Maximum Voltage Value	最大电压值
Vnorm	Normal Voltage Value	典型电压值
Vmin	Minimum Voltage Value	最小电压值
V_{IH} max	Maximum Input High Level Voltage Value	输入高电平的最大电压
V_{IH} min	Minimum Input High Level Voltage Value	输入高电平的最小电压
V_{IL} max	Maximum Input Low Level Voltage Value	输入低电平的最大电压
V_{IL} min	Minimum Input Low Level Voltage Value	输入低电平的最小电压
V_{OH} max	Maximum Output High Level Voltage Value	输出高电平的最大电压
VOH min _	Minimum Output High Level Voltage Value	输出高电平的最小电压
V_{OL} max	Maximum Output Low Level Voltage Value	输出低电平的最大电压
VOL min _	Minimum Output Low Level Voltage Value	输出低电平的最小电压