FCC ID: QIWPRX7-1

Technical Description :

The brief circuit description is listed as follows :
- U101, X101 and associated circuit act as RF Module.
- U11, X2 and associated circuit act as Central Processing Unit.

For control signal of the PS2 controller is transmitted via the socket of GP4 or GP5 to the MCU. The MCU EM78P4510 will transfer the control signal to the RF Modules for the RF transmission. The technical description of the RF Modules RF09325 can refer to the specification of the modules attached. And then, RF modules, RF09325 also can receive the RF control signal and demodulate to the control signal which is process by MCU EM784510 and send to the controller via GP4 & GP5. And the MCU, EM784510 also controls the RF modules and provide the status of this wireless adaptor via four LEDS.

Antenna Used :

A permanent wire antenna has been used.

AWICS-09325

Low Cost Single-Chip RF Transceiver ASIC Specification

Preliminary

JS Technologies, Corp.
151 West St., #202
Annapolis, MD 21401
USA
(410) 295-5452

Revision	Date	Author	Comment
1	5/29/00	J. Kriz	• Draft – Design goals prior fabrication • All data subject to change. • Digital architecture / being redesigned – descriptions no longer valid
2	7/20/01	J. Kriz/T. Romanko	Updated Digital section and ASIC pinout
3	7/27/01	S Harris	Revised/approved for preliminary distribution
4	11/16/01	J. Gluckman	Revised w/Appendices for preliminary distribution
5	6/17/02	S Harris	Revised Rx sensitivity from field msmts

1 Scope

This document provides advanced product and planning information regarding the AWICS I transceiver Application Specific Integrated Circuit (ASIC). It is aimed at providing information for the user to understand the functionality and performance of the ASIC for wireless communication applications.

1.1 Features and Design Goals

RF System

- Single-Chip RF Transceiver for 434MHz, 868MHz, and 915MHz ISM Bands.
- 300MHz to 1000 MHz operation.
- Binary FSK Modulation.
- Low cost fully integrated RF solution requiring minimal external components.
- Programmable data rates up to 28.8 Kbits/sec.
- Internal Manchester Encoding/Decoding selectable
- On-chip filters baseband active filter.
- On-Chip PLL/VCO capable of 2kHz programmable increments at 1GHz VCO frequency.
- Integrated direct conversion receiver with over –72dBm sensitivity.
- Greater than 70dB instantaneous receiver dynamic range.
- Low noise figure of Rx path (NF_{RxSYS} < 10dB).
- Capable of frequency agile communications.
- Adjustable Tx power levels from –20dBm up to +3dBm.
- 2.4V to 3.3V operation.

Peripherals

- Serial Peripheral Interface for configuration, Tx/Rx data transfer, program Tx power level and PLL frequency.
- Oversampled synchronization with bit-wise binary analog to digital coverversion of recevied data stream.

CMOS Technology

- Low-power consumption

- < TBD μA standby current

- Single supply operation.
- Advanced 0.35μm CMOS fabrication geometry.

2.0 Typical Applications

- Wireless Data Transceiver
- Wireless Security Intrusion Sensor Systems
- Battery Powered Portable Systems
- Wireless Meter Reading
- Home and Building Control Networks
- Keyless Entry and Tracking Device
- Intrusion Sensors.
- Key Fobs
- Wireless Controllers (i.e. Fireplace/HVAC Controllers)
- Asset Tracking and RFID Applications
- Zoning Systems
- Under Floor HVAC Controllers

3.0 General Description

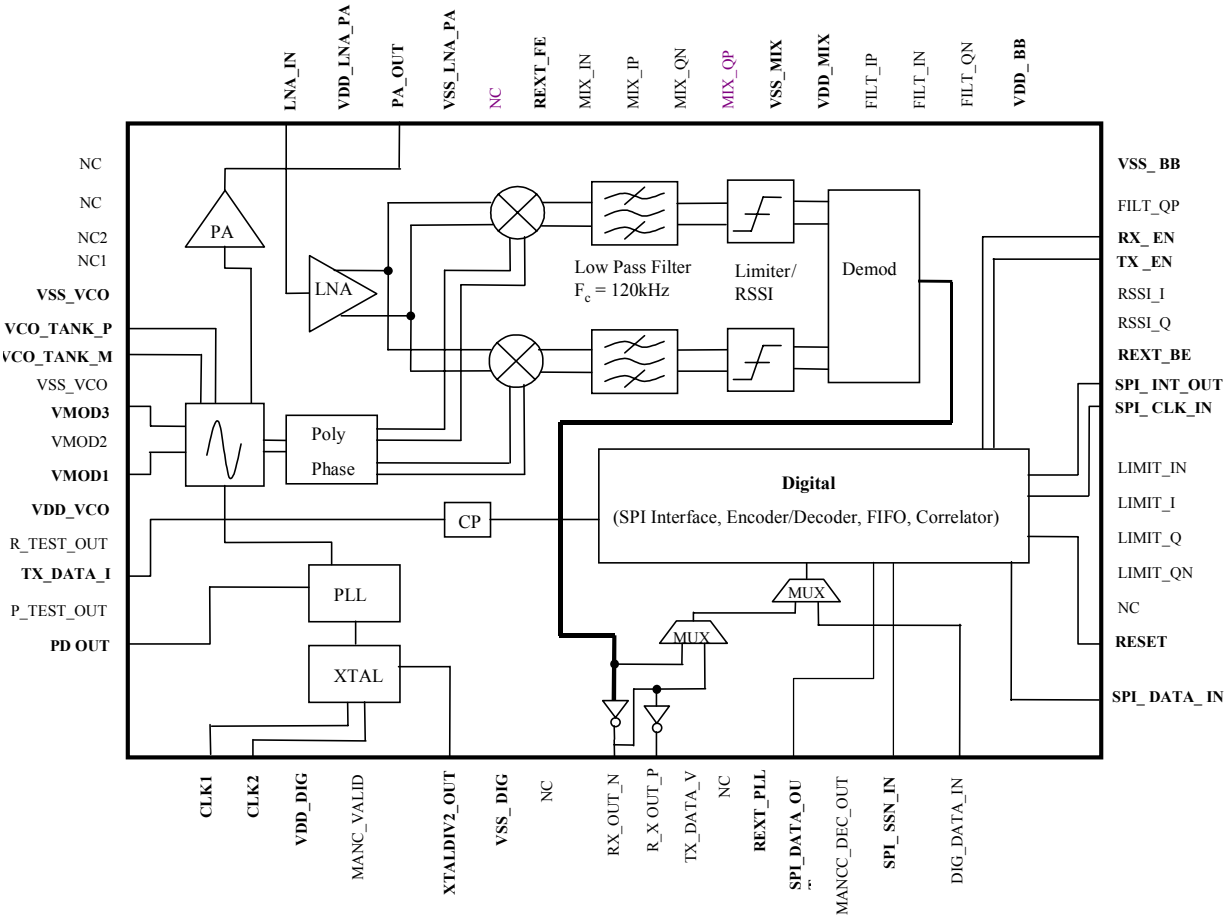
The Narrow Band Transceiver ASIC provides a half-duplex transceiver radio data link capable of statistical frequency-spread transmissions.

Applicable standards for many worldwide applications are shown below. Users will need to adjust values of external components to provide necessary filtering/frequency adjustment to meet these standards. Values shown below are intended to illustrate the range of potential operating conditions and are not warranted to represent current governing regulations. Current regulations should be obtained from the proper regulating agency and final products tested to conformance limits.

United States	United Kingdom	Europe
FCC Title 47 Part 15.231 • 260-470MHz ±0.25% • For 433.92MHz, 4400 uV/m continuous (44,000 uV/m for 10ms)	MPT 1340 • 418.00 ±0.10MHz • 0.25 mW ERP	ETS-300-220 • 433.92 ±0.87MHz • 25mW ERP Class I Device
FCC Title 47 Part 15.249 • 902-928MHz continuous at 50,000uV/m • Harmonics @ 500uV/m		ETS-300-220-Annex • New 868-870 MHz Band allowing both narrow and wideband operation. • Sub-Band A From 868.00 to 868.60MHz. • ERP = 25mW. • Duty cycle <1.0% • Sub-Band B • From 868.70 to 869.20MHz. • ERP = 25mW. • Duty cycle <0.1% • Sub-Band C • From 869.30 to 869.65MHz. • ERP = 500mW. • Duty cycle <10.0% • Sub-Band D → From 869.70 to 870.00MHz. → ERP = 5mW. → Duty cycle 100.0%

4.0 Architectural Overview

The basic architecture of the Direct-Conversion Narrowband FSK Transceiver ASIC is shown in Figure 1 below. Bold names represent potential signals for a 32 pin package.



The ASIC main sections are a digital data interface, frequency synthesizer, transmitter (Tx) and receiver (Rx). The digital and frequency synthesizers both interface the Tx and Rx. To complete the transceiver function, several off chip components are required. The off chip components include:

- Crystal (which can be shared with the application's microprocessor – the transceiver will drive the tolerance of the crystal)
- Transmitter and Receiver LC impedance matching and filtering components,
- LC tank circuit for tuning the PLL/VCO
- Capacitors for filtering supply noise
- Passive components for controlling bias points and loop filtering
- Separate transmit and receive anntennas or a tx/rx switch and a single antenna
- Regulated DC power source

4.1 Direct Conversion Zero-IF Transceiver

The receiver design is based on the direct down conversion principle where a local oscillator on the signal frequency mixes the input signal directly down to the baseband (zero IF). Two complete signal paths with signals of 90 degrees phase difference are used to demodulate the signal. The built-in filters provide sufficient channel selectivity for many applications.

4.1.1 Frequency Synthesizer

4.1.1.1 Voltage Controlled Oscillator (VCO)

The VCO is the source of the RF signals that drive the transmitter, receiver, and PLL. The VCO requires an external resonator to set up general frequency of operation. There are three on-chip varactors to tune and modulate the VCO. The VCO outputs include signals which drive the single ended transmitter power amplifier, receiver I and Q differential mixers, and carrier frequency to the PLL.

4.1.1.2 Phase Lock Loop (PLL)

The PLL function controls the VCO carrier frequency by comparing the phase and frequency of the divided down VCO output to the divided down crystal reference. It consists of a crystal oscillator reference, prescaler, programmable frequency dividers, a phase detector, and a two-level charge pump. The two level charge pump allows for increased bandwidth of the PLL loop filter without changing external components. Its output drives an off chip passive “loop filter” and then returns to the VCO tuning varactor. The PLL also supplies the digital section with a clock signal based on a pre-scaled version of the VCO carrier frequency.

4.1.1.3 Crystal Oscillator

The crystal oscillator circuitry is designed to operate with crystals ranging from 32 kHz to 16 MHz. For proper operation of the PLL and other timing circuitry, the crystal oscillator operating frequency must be indicated/programmed through the SPI bus. For best system phase noise, the highest possible fundamental crystal reference should be used.

4.1.2 Transmitter

The transmitter consists of the PLL/VCO frequency synthesizer and an adjustable power amplifier. The modulated VCO drives the power amplifier. The power amplifier has programmable output power that can be set through the digital SPI interface. Current consumption is minimized at lower output power settings.

4.1.3 Receiver

In receive mode, the PLL/VCO synthesizer generates the local oscillator (LO) signal. The receiver is a direct downconvert/zero intermediate frequency (IF) type in order to eliminate the need for an additional off chip filters. The receiver consists of a low noise amplifier (LNA) that differentially drives a quadrature mixer pair. The mixer differential outputs feed two identical signal channels in phase quadrature. The mixers each have a differential second order highpass 2.5kHz filter on the outputs. Each baseband channel is differential and includes the second order highpass filter at the output of the mixer, a ninth-order modified Chebychev active lowpass filter with 100kHz corner frequency, and a 100dB limiter.

Following the limiter, binary FSK demodulation and analog to digital data conversion is implemented. Using the relative phase difference of the I and Q channel signals, if the I channel signal leads the Q channel, the FSK tone frequency lies above the tone frequency (data '1'). If the I channel signal lags the Q channel, the FSK tone frequency lies below the tone frequency (data '0').

In addition to accessing the digitally filtered receiver data via the SPI port, the "raw" analog demodulated baseband data is also available.

4.1.4 Digital Interface

A five pin Serial Peripheral Interface (SPI) bus is used to interface the transceiver to its host processing device. The main functions of the digital section are:

- Programming the configuration registers of the ASIC
- Load data from host device into 64 byte FIFO for transmission
- Sample digital data from demodulator
- Hold data from receiver in 64 byte FIFO until host device is ready to process data
- Providing enable signals, select operational modes, and set power levels of the other ASIC functional blocks

Prior to starting data transmission, the host processor must configure the ASIC over the SPI bus. This includes data rate, frequency synthesizer registers, Tx output power, crystal oscillator frequency, FIFO configuration, and correlator configuration. To send information, data bytes are written to the FIFO over the SPI. The transmitter reads data from the FIFO, serializes the data, and automatically encodes it. Then the serial data is shifted out to the RF transmitter. The FIFO generates Programmable Almost Empty (PAE) status flag to the SPI interrupt pin. The host processor can monitor the SPI interrupt pin to write additional data into the FIFO before it empties (important for continuous transmission).

Prior to receiving transmitted data, the host processor must configure the ASIC over the SPI bus. This includes data rate, frequency synthesizer registers, demodulator output polarity and source selection, crystal oscillator frequency, FIFO configuration, and correlator configuration, and ADC glitch filter configuration. The incoming data from the on-chip demodulator is de-glitched, sampled, decoded, detected for correlation coefficient (if enabled), then the data is sent to the FIFO. The FIFO generates Programmable Almost Full (PAF) status flag to the SPI interrupt pin. The host processor can monitor the SPI interrupt pin to be notified that data is filling the FIFO.

4.1.5 Pinout Definition

Transceiver ASIC Pinout – Functional Description - A 64 pin prototyping list is shown below. Production pin out is expected to consist of a 32 pin packaged configuration Bold names represent potential signals for a 32 pin package.

Pin #	Name	Type	ESD	Function
1	NC	NC	OUT	No Connect
2	NC	NC	OUT	No Connect
3	NC	X	OUT	Not Used.
4	NC	X	OUT	Not Used.
5	**VSS_VCO**	GND		Ground pin for the Voltage Controlled Oscillator.
6	**VCO_TANK_P**	Input	Internal to ckt	Connection for external VCO resonator LC tank circuit.
7	**VCO_TANK_M**	Input	Internal to ckt	Connection for external VCO resonator LC tank circuit.
8	VSS_VCO	GND	PWR	Ground pin for the Voltage Controlled Oscillator.
9	**VMOD3**	Input	OUT	Center frequency phase-locked loop voltage tune pin.
10	VMOD2	Input	OUT	Wideband FM modulation pin: signal input to control the Transmitter output frequency.
11	**VMOD1**	Input	OUT	Narrowband FM modulation pin: signal input to control the Transmitter output frequency.
12	**VDD_VCO**	PWR	PWR	Power source pin for VCO.
13	R_TEST_OUT	Output	OUT	Test signal output of the R-Divider.
14	**TX_DATA_I**	Output	OUT	Digital transmit data output pin (current mode) from digital section. The same data is present on TX_DATA_V pin. Tx_DATA_V is a voltage output.
15	P_TEST_OUT	Output	OUT	Test signal output of the N-Divider.
16	**PD_OUT**	Output	OUT	PLL phase detector output (Current source)used to tune synthesizer frequency. This signal drives into the loop filter prior to connecting to the VCO input.
17	**CLK1**	Input	OUT	Connection for the external crystal.
18	**CLK2**	Input	OUT	Connection for the external crystal.
19	**VDD_DIG**	PWR	OUT	Power source pin for the Digital and PLL.
20	MANCH_VALID	Output	OUT	Test pin for digital.
21	**XTALDIV2_OUT**	Output	OUT	A clock output which is half the frequency of the external crystal.
22	**VSS_DIG**	PWR	OUT	Ground for digital and PLL
23	NC	NC	OUT	
24	RX_OUT_N	Output	OUT	Inverted, pre-digitized data output from the demodulator.
25	RX_OUT_P	Output	OUT	Positive pre-digitized data output from the demodulator.

26	TX_DATA_V	Output	OUT	Digital transmit data output pin (voltage mode) from digital section. Same data as on IMOD100U pin (which is a current mode output)
27	NC	Output	OUT	No Connection
28	**REXT_PLL**	Output	OUT	Pin for external resistor to set bias current level.
29	**SPI_DATA_OUT**	Output	OUT	SPI output data signal
30	MANCH_DEC_OUT	Output	OUT	Test pin for digital.
31	**SPI_SSN**	Output	IN	Serial Peripheral Interface Slave Select Input.
32	DIG_DATA_IN	Input	IN	Data input to the digital receive logic. Used as a test input for the digital section allowing controlled data into digital receiver.
33	**SPI_DATA_ IN**	Input	IN	Serial Peripheral Interface Data Input.
34	**RESET**	Input	IN	Signal to Reset the digital section.
35	NC	NC	Out	NC
36	LIMIT_QN	Output	OUT	Test output of the quadrature channel limiter, inverted polarity.
37	LIMIT _Q	Output	OUT	Test output of the quadrature channel limiter,.
38	LIMIT_I	Output	OUT	Test output of the in-phase channel limiter.
39	LIMIT_IN	Output	OUT	Test output of the in-phase channel limiter, inverted polarity.
40	**SPI_CLK**	Input	IN	Serial Peripheral Interface Clock pin.
41	**SPI_INT_OUT**	Output	OUT	Serial Peripheral Interface Interrupt pin.
42	**REXT_BE**	Output	IN	Pin for external resistor to set bias current level.
43	RSSI_Q	Output	OUT	Received Strength Signal Indicator for the quadrature channel. This is a current mode output.
44	RSSI_I	Output	OUT	Received Strength Signal Indicator for the in-phase channel.
45	**TX_ENABLE_OUT**	Output	OUT	Output of the external PA_EN pin OR'd with the internal digital PA_EN bit. This output can be used as a control for an external Transmit/Receive switch.
46	**RX_ENABLE_OUT**	Output	OUT	Output of the external RX_EN pin OR'd with the internal digital RX_EN bit. This output can be used as a control for an external Transmit/Receive switch.
47	FILT_QP_TEST	Output	OUT	Test output to measure Baseband filter performance, Q channel, positive side.
48	**VSS_BB**	GND	OUT	Ground pin for the baseband filtering, limiter and demodulator.
49	**VDD_BB**	PWR	OUT	Power source pin for the baseband filtering, limiter and demodulator.
50	FILT_QN_TEST	Output	OUT	Test output to measure Baseband filter performance, Q channel, negative side.

51	FILT_IN_TEST	Output	OUT	Test output to measure Baseband filter performance, I channel, negative side.
52	FILT_IP_TEST	Output	OUT	Test output to measure Baseband filter performance, I channel, positive side.
53	**VDD MIX**	PWR	OUT	Power source pin for the mixers.
54	**VSS_MIX**	GND	OUT	Ground pin for the mixers.
55	MIX_QP_TEST	Output	IN_50	Test output to measure mixer performance, Q channel, positive side.
56	MIX_QN_TEST	Output	IN_50	Test output to measure mixer performance, Q channel, negative side.
57	MIX_IP_TEST	Output	IN_50	Test output to measure mixer performance, I channel, positive side.
58	MIX_IN_TEST	Output	IN_50	Test output to measure mixer performance, I channel, negative side.
59	**REXT_FE**	Output	OUT	Pin for external resistor to set bias current
60	NC	Output	OUT	No Connection
61	**VSS_PA**	GND	PWR	Ground pin for the LNA and PA.
62	**PA_OUT**	Output	PWR	Transmitter RF output pin.
63	**VDD_PA**	PWR	PWR	Power source pin for the LNA and PA.
64	**LNA_IN**	Input	OUT	Receiver RF input pin.

5.0 Operating Conditions

5.1 Absolute Maximum Operating Conditions

Symbol	Parameter	Conditions	Min.	Typical	Max.	Units
T_A	Operating Ambient Temp.		-40	-	+85	^oC
T_S	Storage Temp.		-40	-	+150	^oC
V_{DD}	Supply Voltage		2.4	3.0	3.6	V

5.2 Digital Inputs and Outputs - DC Specifications

Symbol	Parameter	Conditions	Min.	Typical	Max.	Units
V_I	Input Voltage		-0.5	-	V_{DD}+0.3	V
V_O	Output Voltage		-0.5	-	V_{DD}+0.3	V

V_{IL}				0.7	V
V_{IH}		1.7			V
V_{OH}	I_{OH}=X ma	2.0			V
V_{OL}	I_{OL}=X ma			0.4	V
Io			TBD		mA

5.3 Power Consumption

The Narrow Band Transceiver ASIC draws ~15-26mA (power level dependent) at 3.0V in transmit mode and ~28mA at 3.0V in receive mode. Switching between transmit, receive and SLEEP can reduce power consumption to a fraction of continuous operation. Lower carrier frequencies will reduce power dissipation.

5.4 Performance Specifications

Description of the electrical parameters varies significantly from pin to pin as the signal types include low level analog, RF, digital, and power. Since the ASIC was designed to work over a wide frequency range, the electrical parameters may also vary with frequency. In many cases, a schematic is presented to provide the user a look at the interface circuitry.

Parameter	Description	Min.	Typ.	Max.	Units	Conditions
Overall	RF Frequency Range	300	434 or 915	928	MHz	T=25 °C, Vdd=3.0V
	Supply Voltage	2.4	3.0	3.3	V	
	TX to RX and RX to TX Switching		TBD		μS	Application/pll loop filter dependent
Transmit Section	Modulation Rate	2.4	19.2	28.8	Kbps	Minimum frequency deviation of 20 KHz
	PA Max. TX Pout		+3		dBm	Vdd=3.0V
	Power Control Range		20		dB	
	Power Control Resolution		0.5		dB	64 level binary code
	Peak Freq. Deviation	+/-3	+/-43	+/-75	kHz	FM: Fc +/- deltaF
	Antenna Port Impedance		50 matched		Ω	TX_EN = "1", w/ external match
	Antenna Port VSWR		1.5:1	2:1	-	TX_EN = "1", w/ ext. match

	PA Harmonics (2^{nd})		-17 -23		dBc dBc	At +3dBm out At –9dBm out
	PA Spurious		-70		dBm	At fc+10MHz
Receiver Section						
	Cascaded Noise Figure			10	dB	Simulated/calculated front-end NF
	Cascaded P1dBin		-20		dBm	Linear compression point
	Rx Sensitivity		-72		dBm	SNR=12dB, 50 Ohm input Impedance, no external filtering
	Dynamic Range		70		dB	
	LO Leakage		-60		dBm	PA off, Rx on
VCO and PLL	Max operating frequency		>928		MHz	
	Prescaler Divide Ratio		32/33			Dual modulus
	Frequency Increment	2	100	900	kHz	
	Lock Time from “OFF”		TBD		ms	ext.filter controlled
	Lock Time: Freq. Change		TBD		ms	ext.filter controlled
	Phase Noise, unlocked		-90 at 50kHz offset		dBc/Hz	Fvco=915MHz, free-run VCO. Meas through PA.
	Phase Noise, PLL locked		-50 at 1kHz offset		dBc/Hz	Locked loop, Fvco=915MHz Fcomp=100kHz Fxtal=9.83MHz Meas through PA.
	Reference Frequency	0.032		16	MHz	Crystal oscillator
	Rcounter		14		Bits	
	Ncounter		19		Bits	
	Crystal Register		8		Bits	
	Linear Tune Voltage Range		1.0-2.5		V	Linear, neg. polarity

Linear Baseband Filter	Low Fc (–3dB) corner		5		kHz	
	High Fc (–3dB) corner	90	100	120	kHz	
Baseband Limiter						
	Differential Output		1.1		Vpp	0 to 0.5V square wave single-ended
Power Down Control	ON" Time from Wake-Up		TBD			
	"OFF" Time		TBD			

5.4.1 ESD Structures

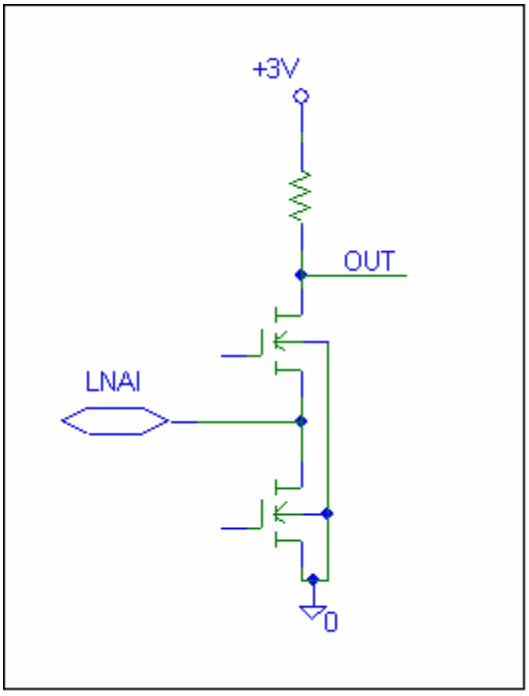
ESD structures are in place on all I/O pins. The circuits are protected to a minimum level as indicated for each type of strucutre. The definition of the protection on each pin is located in the "Pinout Definition" section above. There are five different structures.

ESD Strucutre	Protection Level
Input (IN)	TBD
Input 50 (IN_50)	TBD
Output (OUT)	TBD
Power (PWR)	TBD
Power Amp Output (PA_OUT)	TBD

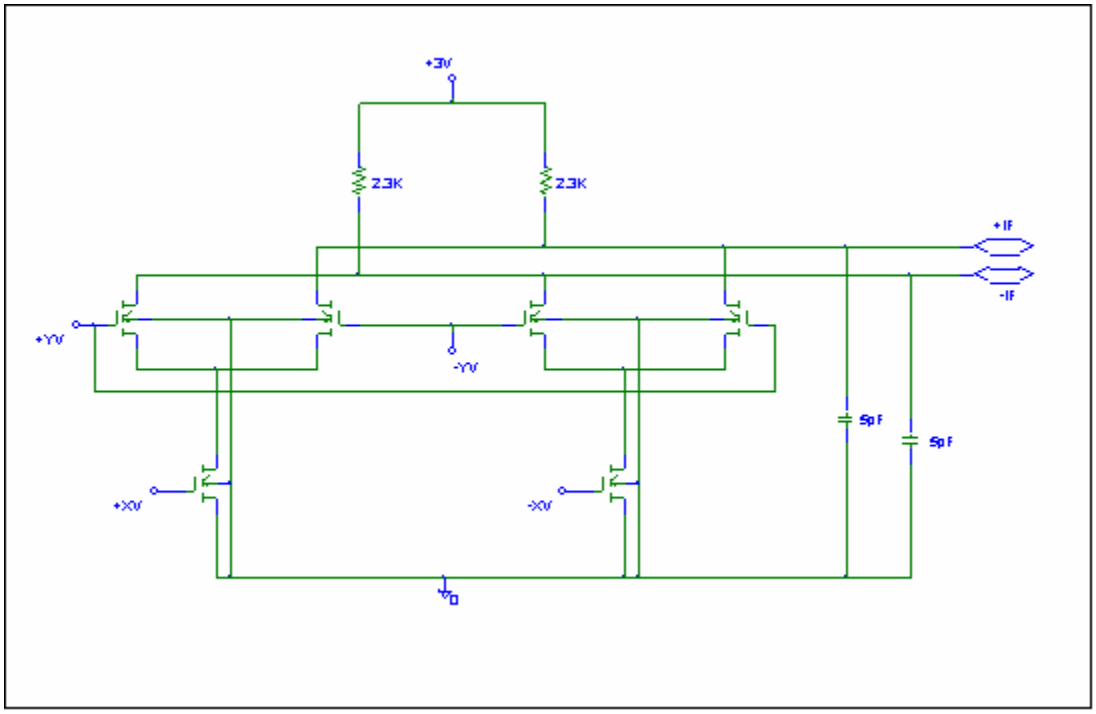
5.4.2 Analog and RF Interface Circuits

The following are circuit descriptions of the analog and RF inputs and outputs. The electrical characteristics are listed in the table above.

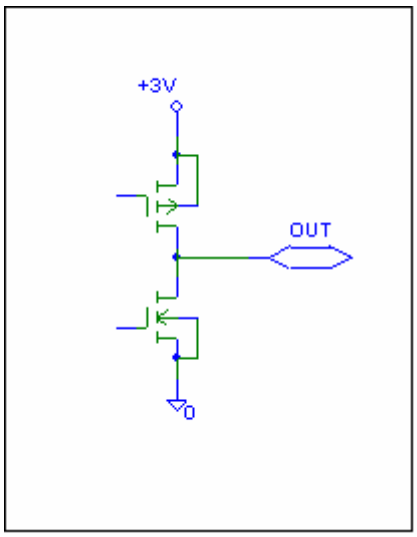
LNA INPUT ELECTRICAL DESCRIPTION:



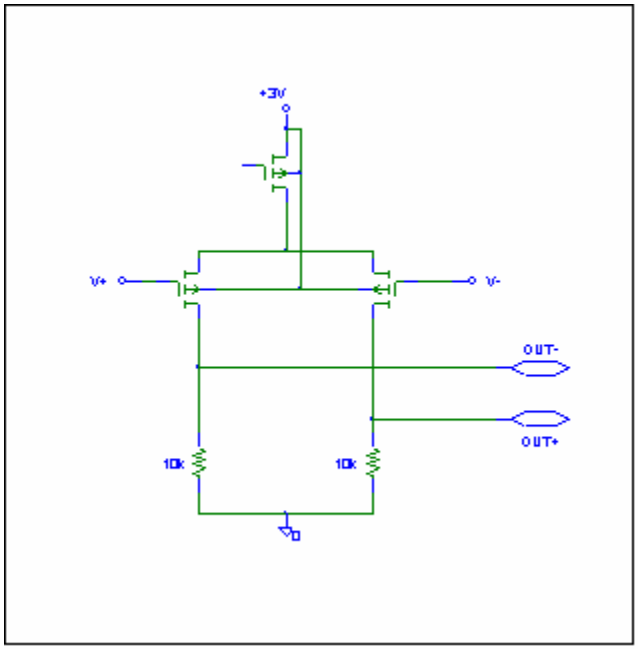
MIXER OUTPUT ELECTRICAL DESCRIPTION:



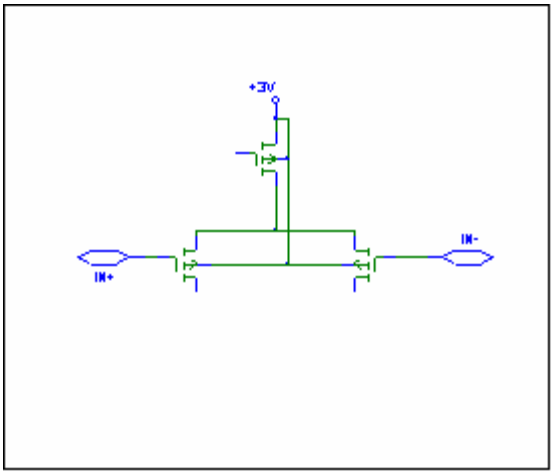
BASEBAND FILTER OUTPUT (BUFFERED) ELECTRICAL DESCRIPTION:



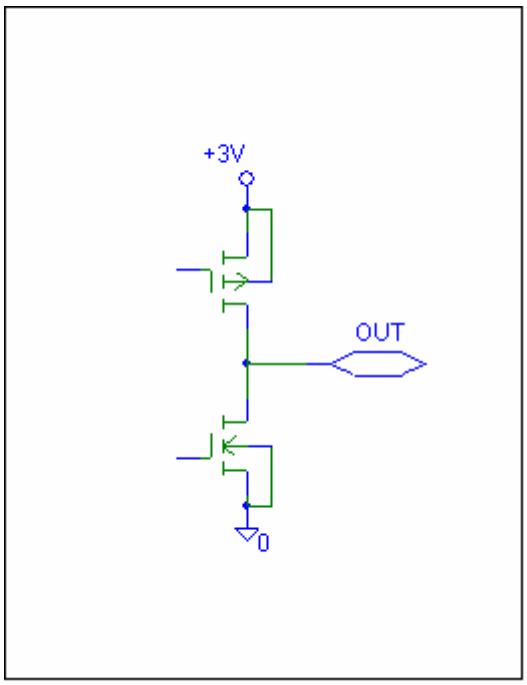
BASEBAND LIMITER OUTPUT ELECTRICAL DESCRIPTION:



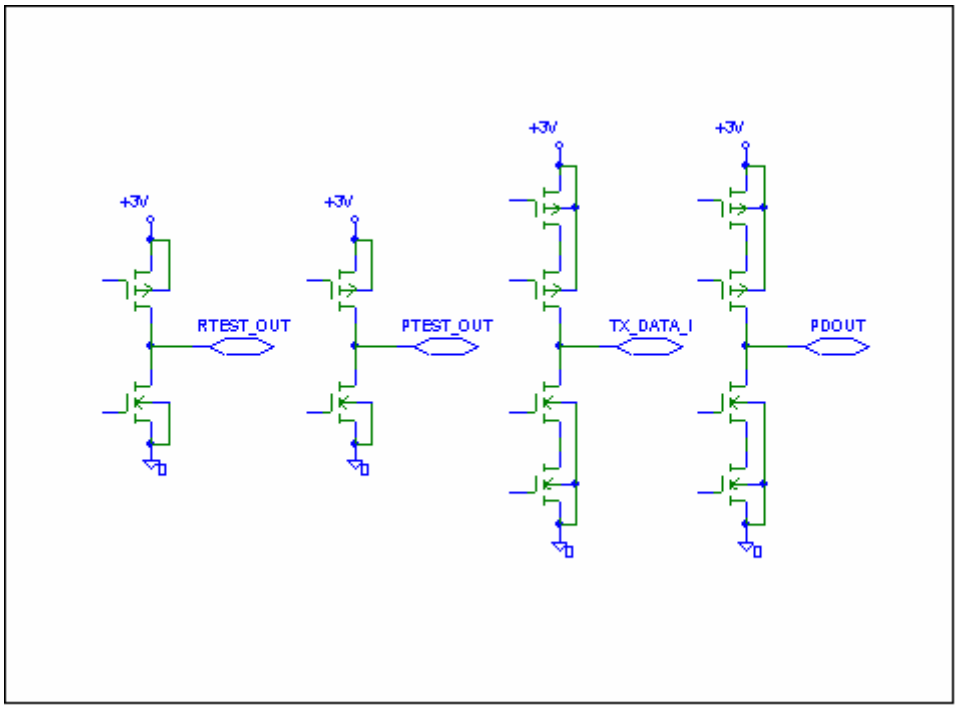
DEMOD INPUT ELECTRICAL DESCRIPTION:



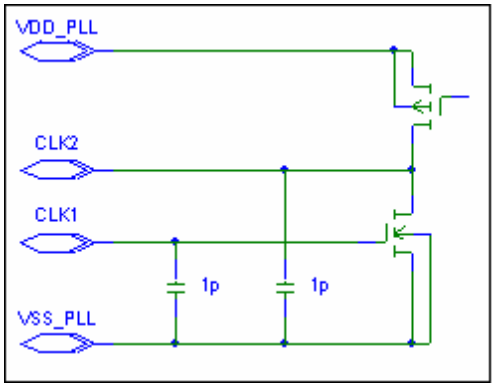
DEMOD OUTPUT ELECTRICAL DESCRIPTION:



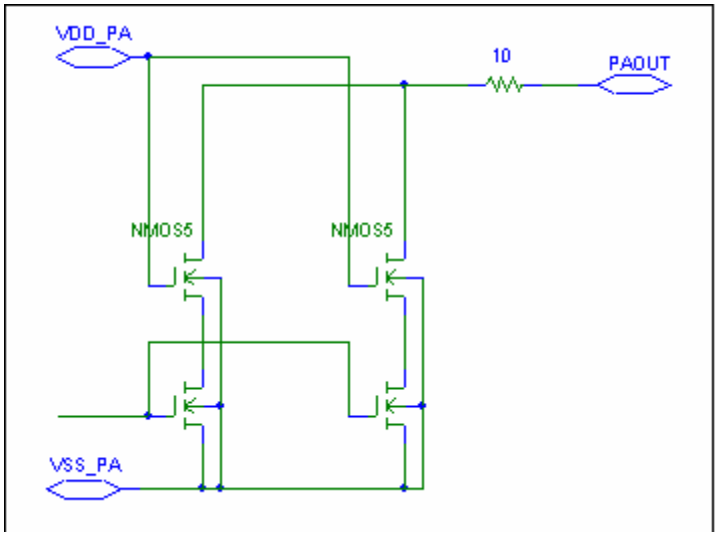
PLL OUTPUT ELECTRICAL DESCRIPTION:



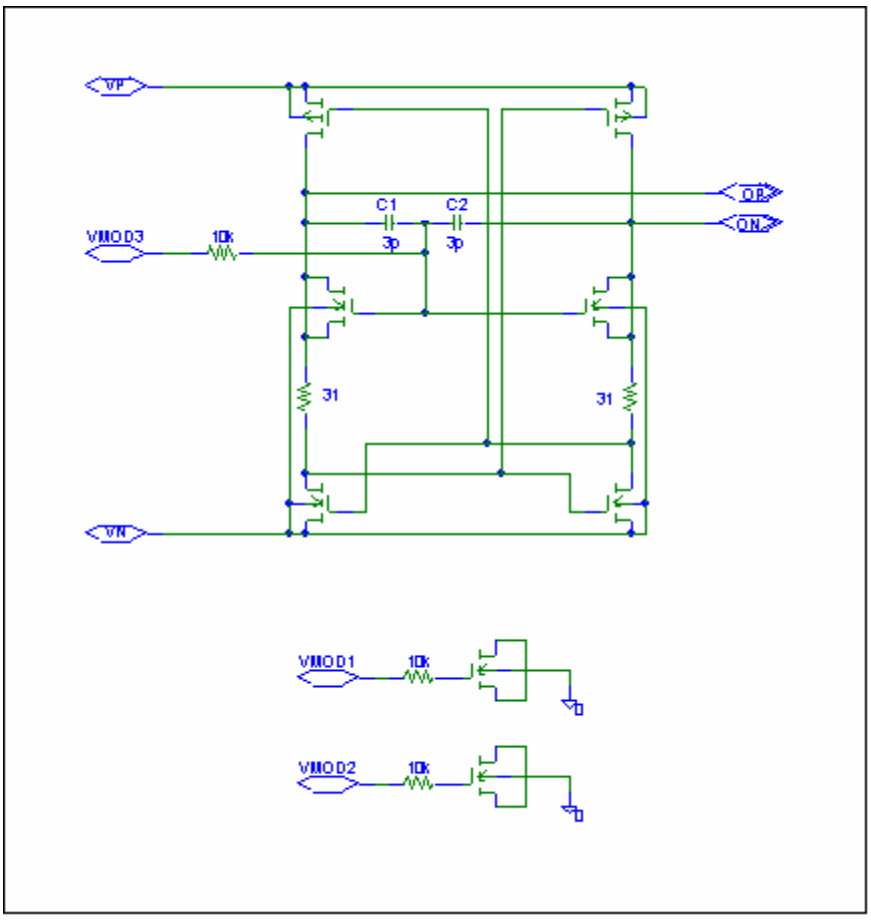
XTAL INPUT ELECTRICAL DESCRIPTION:



PA OUTPUT ELECTRICAL DESCTIPTION:



VCO OUTPUT ELECTRICAL DESCRIPTION:



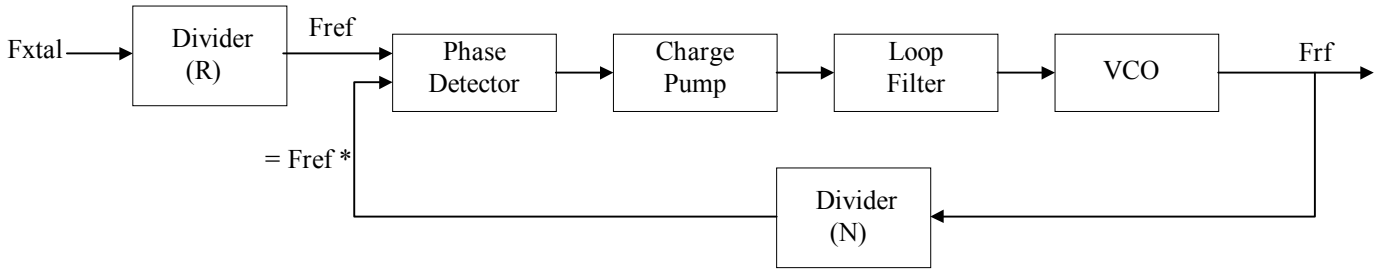
6 Transceiver ASIC Functional Description

The transceiver integrates all RF, IF, baseband, signal synthesis and digital processing components into a single monolithic solution. The various sub-sections below describe the CMOS circuits in each block of the transceiver.

Much of what drives the accuracy of a wireless transceiver link is the crystal oscillator accuracy. Using a +/-10ppm crystal in both the transmitter and receiver results in a possible +/-18.3kHz deviation when operating at 915MHz.

6.1 Phase Lock Loop and Voltage Controlled Oscillator (PLL/VCO)

The PLL provides the RF signal generation for the transmit output signal and in receive mode, supplies the receiver mixers with the differential I/Q Local Oscillator (LO) signals for down converting the incoming RF energy from the LNA. The basic block diagram of the PLL/VCO is shown below.



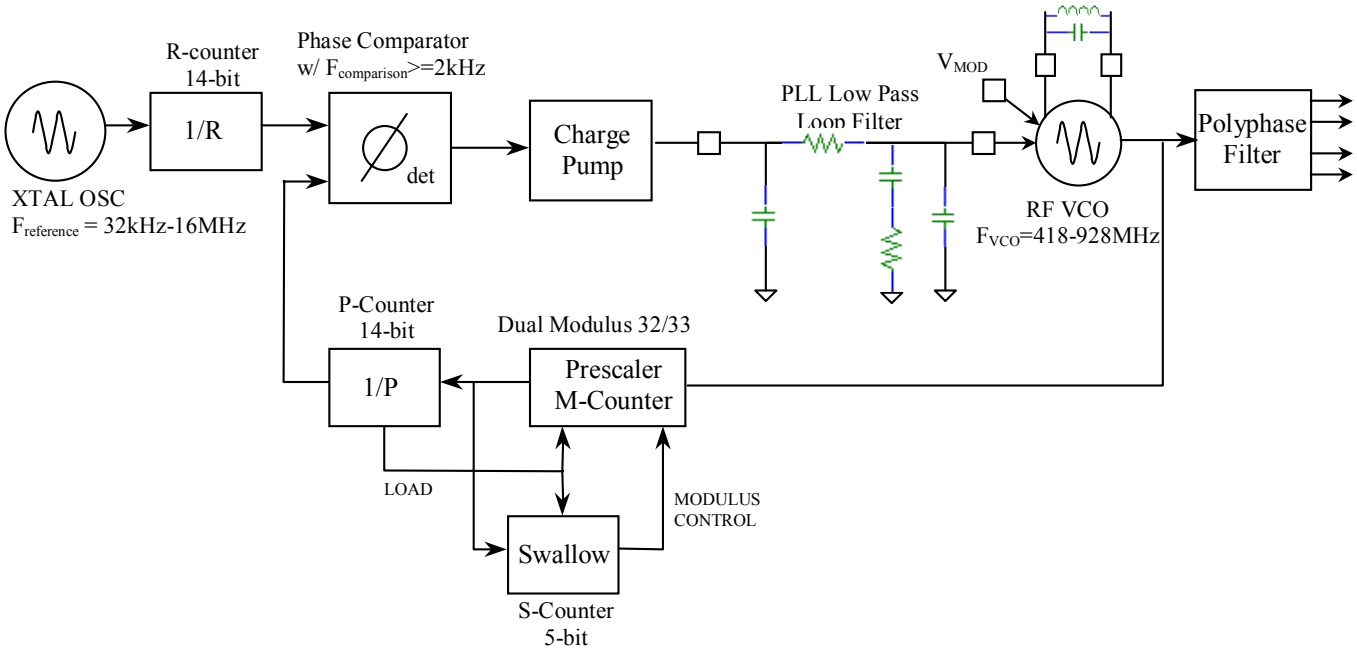
* : Frf/N=Fref when PLL is locked

Fref=Fxtal/R

Frf=Fref*N

Fref : Reference frequency
Fxtal : Crystal resonant frequency
Frf : RF frequency (result of locked PLL w/ chosen Fxtal and programmed R

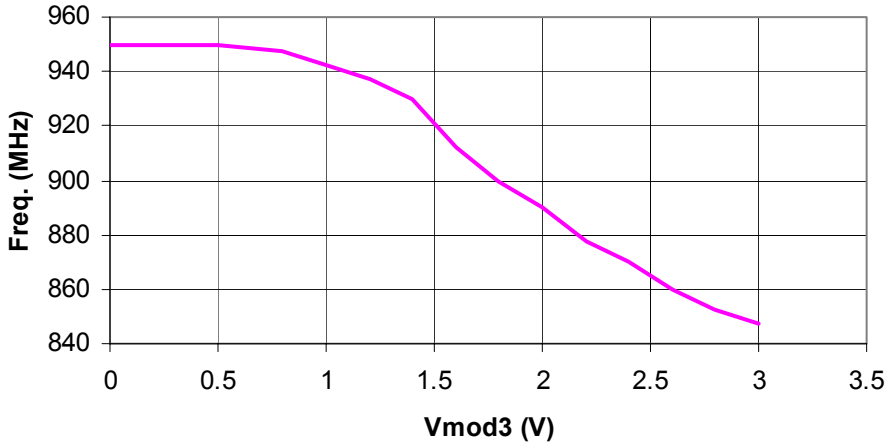
- Fully differential signals output to receiver. Single ended to the transmitter.
- Indirect synthesizer Frf = (N/R)*Fxtal, Fref=Fxtal/R
- Similar to LMX200 series from National Semiconductor.
- A minimum 2kHz programmable step index accuracy based on external loop filter.
- All registers are set in parallel with a single clock.
- Operation from 418MHz to 928MHz (>1000MHz PLL operation tested on Pass 2)
- >2% of center freq. tuning range.
- External tank circuit required to set general oscillation frequency.



f_{CKOUT} :Clock output frequency to phase detector for comparison with the reference clock.
f_{CKIN} :Desired 418MHz to 928MHz frequency
R :Crystal oscillator frequency divider count
M :Pre-scaler divide ratio (M=32)
P :Divider count
S :Swallow counter => S < P

Fckout= Fvco/ ((P*M)+S)) = Fvco/N

Depicted below are the graphs showing the voltage-controlled oscillation frequency output of the VCO.

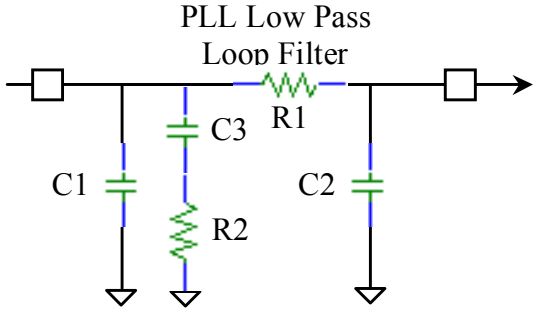


Simulated output frequency vs. tuning voltage. Measured response - TBD

6.1.1 Loop Filter Design

Correct design of the loop filter is of considerable importance to the optimal performance of the synthesizer and overall wireless link. The filter should be designed to achieve the required compromise between noise performance and switching time. The actual circuit will therefore depend upon the particular application implementation. The following design is a 3rd order low pass filter providing improved reference breakthrough rejection over a 2nd order design.

The loop filter input is driven by the PLL charge pump output and the output is connected to the VMOD line on the VCO.



The following loop parameters are first chosen:

Radio frequency: f_{RF}
Comparison frequency: f_C

Switching time:	t_S
VCO gain (rad/volt)	K_o
Phase comparator gain (amps/rad):	K_d
Phase margin:	φ
Breakthrough suppression (dB):	A

A good starting point for breakthrough suppression (A) is 20dB. Note that A should not be so large that $10 \cdot T_3 > T_1$.

Next, determine the loop bandwidth fn from $fn = 3/t_S$, then determine the main divider ratio N from $N = f_{RF} / f_C$

A loop filter has three time constants, these are:

$T_1 = C3 \cdot R2$

$T_2 = R2 \cdot C1 \cdot C3/(C3 + C1)$

$T_3 = C2 \cdot R1$

The 2nd order loop is designed by omitting R1 and C2 and uses the equations below:

$$T_2 = \frac{1/\cos(\varphi) - \tan(\varphi)}{\omega_n} \qquad \text{where;} \qquad \omega_n = 2\pi \cdot fn$$

$$T_3 = \sqrt{\frac{10^{(A/20)} - 1}{2\pi \cdot fc}}$$

$$\omega_{nc} = \frac{(T_2 + T_3)}{T_2^2} \cdot \tan(\varphi) \cdot \left(\sqrt{\left[1 + \frac{4 \cdot T_2^2}{\left(2 \cdot \tan(\varphi) \cdot (T_2 + T_3)\right)^2} \right]} - 1 \right)$$

$$T_1 = \frac{1}{\omega_{nc}^2 \cdot (T_2 + T_3)}$$

$$C3 + C1 = K \sqrt{\frac{1 + (\omega_{nc} \cdot T_1)^2}{\left(1 - \omega_{nc}^2 \cdot T_2 \cdot T_3\right)^2 + (T_2 \cdot T_3)/T_1}} \qquad \text{where;} \quad K = \frac{K_d \cdot K_o}{N \cdot \omega_n^2}$$

$$C1 = \frac{T_2 \cdot (C3 + C1)}{T_1}$$

$$C3 = (C3 + C1) - C1$$

$$C2 = C1/16$$

$$R2 = T_1/C3$$

$$R1 = T_3/C2$$

For a successful filter it is important that C3 >> C1 >> C2.

6.1.2 Modulation and Data Input

The transceiver was designed for use with FSK modulation. When FSK modulation is applied to the VCO, the RF carrier frequency (programmed by the PLL) is deviated above and below the RF carrier by an amount equal to the peak frequency deviation, which comes from the chosen FM modulation index and data information rate (also called the modulating frequency).

It is recommended that the data to be transmitted is DC balanced – the data should have no DC component. This means that the data should consist of equal numbers of '1's and '0's. A popular DC balanced coding scheme is the "Manchester code". For the transmit operation, the "Manchester" encoding can be accomplished by the external microprocessor prior to loading the tx_fifo via the SPI bus. For the receive operation, the reverse operation can be accomplished by the external microprocessor by decoding the "Manchester" encoded data obtained from the rx_fifo prior to using the information.

6.2 Basic Transmitter Operational Procedure

The basic operational procedure for the transmitting data is as follows:

1. The first operations are associated with writing to the configuration registers to set operating parameters. This begins with the data rate register, correlation N register, correlation coefficient, and FIFO PAE status flag. The manchester enable and the manchester LSB first enable must be set in the configuration register. Note: consult "Appendix A: PLL Frequency and Data Rate Register Tables" for the data rate register.

2. The PLL/VCO N and R registers are programmed for the desired transmit output frequency and PLL reference frequency. Detailed description of the register information can be found in the Digital Section as well as in Appendix A.

3. Set the desired transmit power level in the Transmitter Power Register. Refer to the TX Power Register definition in Table D2 of the Digital Section for typical TX output power levels and corresponding register values.

4. The PLL, VCO, and Crystal oscillator are enabled through the PLL_EN bit of the configuration register via the SPI bus.

5. The PLL and VCO must be turned on (enabled) and allowed to lock on the correct frequency defined by the configuration register.

6. The Power Amplifier and the TX driver buffer in the VCO output are enabled through the TX_EN bit of the configuration register via the SPI bus.

7. The data (<64 bytes) to be transmitted is written/loaded into the FIFO.

8. After completing the initial SPI FIFO write access, data automatically begins to be shifted serially out the TX_DATA_V port (pin 26) and the TX_DATA_I port (pin 14). An internal clock derived from the PLL (SYS_CLK derived) and not the SPI clock controls the shifting out of data.

9. On consecutive transmit operations the FIFO can be verified to be empty by reading the transmit FIFO empty status bit of the FIFO/RX Status Register. On continuous transmit operations the SPI interrupt pin can be monitored. When asserted, the programmable almost empty flag (PAE) is active. This indicates that more data can be written to the FIFO to ensure that the FIFO never goes empty (allowing the FIFO to completely empty will cause a pause in data transmission).

10. Monitor the FIFO Empty Flag bit in the FIFO Status Register until it goes high indicating completion of the data transmission.

11. Disable the Power Amplifier through the SPI bus.

12. Disable the VCO, PLL, Bias/Reference, and Crystal Oscillator.

Now the transmitter is in sleep mode.

6.3 Basic Receiver Operational Procedure

Operation procedure for the receiver is as follows:

1. The first operations are associated with writing to all the configuration registers to set operating parameters. This begins with the data rate register, correlation N register, correlation coefficient, correlation mask register, correlation threshold register, FIFO PAF status flag, and the glitch filter threshold. The manchester enable, the manchester LSB first enable, and the mask enable must be set in the configuration register. Note: consult "Appendix A: PLL Frequency and Data Rate Register Tables" for the data rate register.

2. The PLL/VCO N and R registers are programmed for the desired receive frequency and PLL reference frequency. Detailed description of the register information can be found in the Digital Section as well as in Appendix A.

3. The PLL, VCO, and Crystal oscillator are enabled through the PLL_EN bit of the configuration register via the SPI bus.

4. The LNA, Mixers, VCO mixer LO buffer, BBfilter, Limiter, demod, and digital serial receiver section are enabled by the internal RX_EN bit of the "Configuration Register".

5. Upon reception and transfer of the first byte into the FIFO, the FIFO Empty flag is set to indicate data is available. This can be monitored via the FIFO/RX Status Register. The FIFO programmable almost full (PAF) status flag causes the SPI_INT signal to be asserted. This indicates that data should be read from the FIFO, preventing the FIFO from overflowing (if FIFO becomes full, it will not overwrite, but all new data will be lost until FIFO space is made available).

6. The number of data bytes (up to 64) in FIFO can be obtained from the "FIFO/RX Status Register". (User does not have to do this operation because the PAF status flag provides information about the FIFO status more readily from the SPI interrupt pin).

7. Read data through SPI bus.

8. When the system application completes the read function, the receiver can be put into sleep mode by disabling the LNA, Mixers, VCO mixer LO buffer, BBfilter, Limiter, demod, and digital serial receiver by toggling the RX_EN bit of the configuration register. This can be followed by disabling the PLL, VCO, and Crystal oscillator by toggling the PLL_EN bit of the configuration register.

6.4 Digital Operation

A high-level block diagram of the digital portion of the RF ASIC is provided in Figure D1. The digital portion consists of mainly 4 blocks. The SPI slave controller, the FIFO, the serial transmitter, and the serial receiver.

The SPI slave controller provides an external interface to a SPI controller. The SPI interface provides the ability to transmit and receive data as well as configure the transceiver.

The transmit portion involves the FIFO block being loaded with data, via the SPI slave controller block, from the external SPI controller. Once the SPI FIFO access is completed the serial transmitter will begin outputting a training sequence of alternating 1,0's. The length of the training sequence is programmable in 8 bit increments up to 120 bits. After completing the training sequence the serial transmitter may append a synchronization word to the beginning of the serial data. After the synchronization word has been sent, the serial transmitter sends the data out of the FIFO. The serial transmitter may Manchester Encode the data prior to transmitting. A programmable flag in the FIFO will cause an SPI interrupt when the number of bytes in the FIFO falls below the Programmable Almost Empty (PAE) threshold. This will provide the capability of reloading the FIFO before it is empty, allowing continuous transmission.

The receive portion of the transceiver receives demodulated data and first removes glitches from the serial bit stream. Following the glitch removal, the bit determination is made. After the bit determination has been made the serial bit data may initially be correlated with a synchronization word. Once a valid synchronization word has been detected the data may be decoded. The decoded data is formed into bytes and then written into the FIFO. A programmable flag in the FIFO will cause an SPI interrupt when the number of bytes in the FIFO exceeds the Programmable Almost Full (PAF) flag.

A single FIFO is shared for both the reception and transmission of data. The transmit and receive enable signals define the direction of the FIFO and access to the FIFO. It will determine if the SPI can write (Tx mode) or read (Rx mode) and whether the serial transmitter or the receiver interfaces with the FIFO.

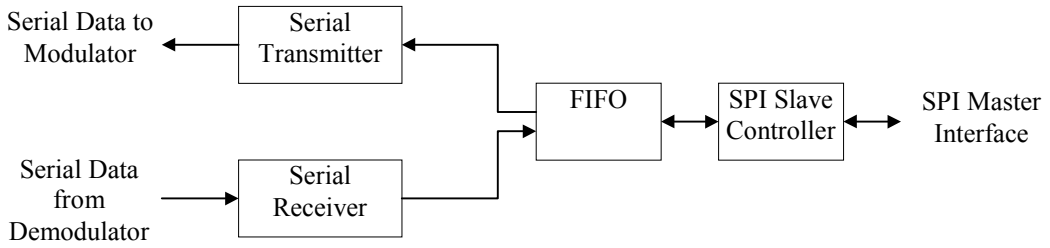


Figure D1. High Level Digital Block Diagram

6.1.1 Serial Peripheral Interface (SPI) Slave Controller

The transceiver contains a slave Serial Peripheral Interface (SPI) for configuration and exchange of data. The system's serial interface has input and output 8-bit shift registers that provide the conversion from parallel to serial and vice versa.

Below is a block diagram of the slave SPI circuitry.

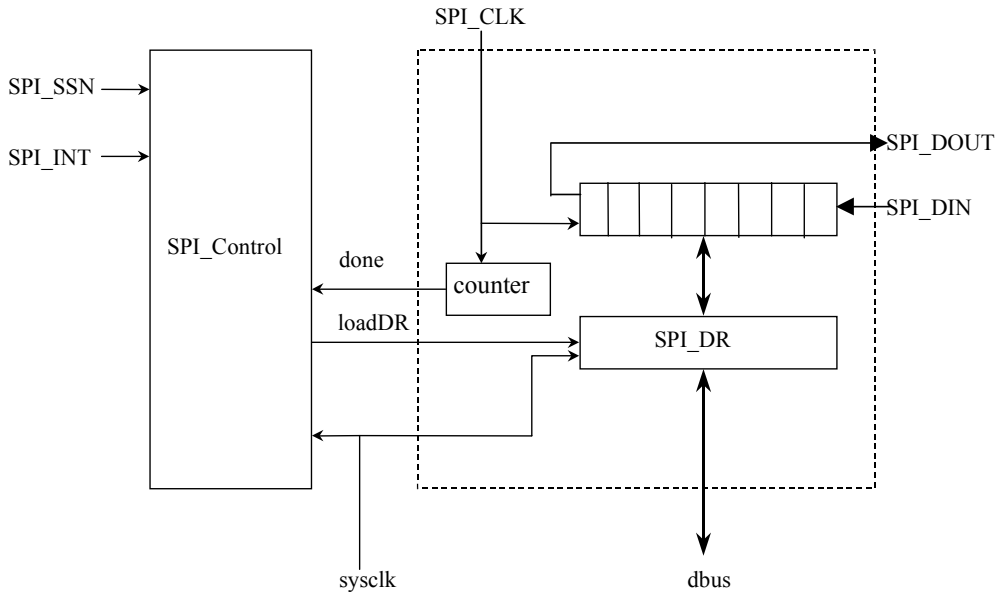


Figure D2. Slave Serial Peripheral Interface Block Diagram.

Signal Description:

- SPI_SSN SPI slave select pin used to enable Transceiver SPI interface.

- SPI_CLK serial clock used to latch data on the rising edge.
- SPI_DIN Receiving data port.
- SPI_DOUT Transmitting data port.
- SPI_INT Interrupt output signaling that the FIFO either is almost full in the receive mode or that it is almost empty in the transmit mode.
- SYSCLK Transceiver internally generated system clock
- dbus Internal data bus used to communicate to on chip registers and FIFO.

6.1.1.1 SPI Timing Diagrams

The SPI timing diagram in Figure D3, depicts the data valid relative to the SPI clock (sys_clk). On the rising edge of the SPI clock the SPI data in must be valid. The bit order loading is performed most significant bit first. Multiple byte accesses must occur most significant byte first. This holds true for both the input and output serial data of the SPI interface. Figures D4 and D5 depict the writing and reading of 2 byte words (example). The first byte of SPI transmission is always Instruction byte. This follows the SPI_SSN signal going low.

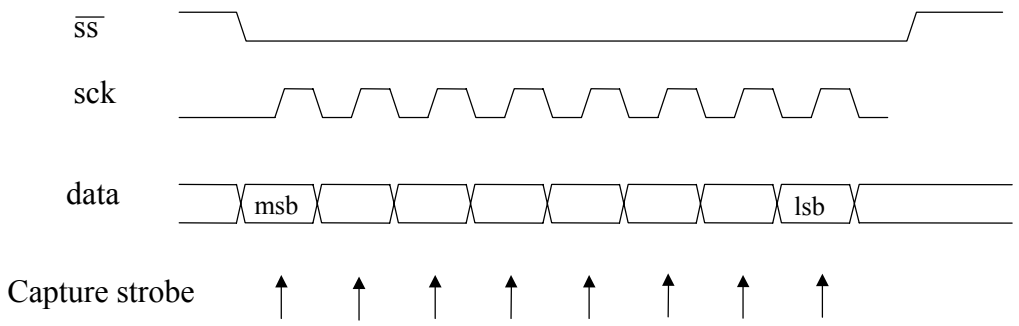


Figure D3. Timing Diagram Showing msb/lsb Relationship to SPI_SCK and SPI_SSN.

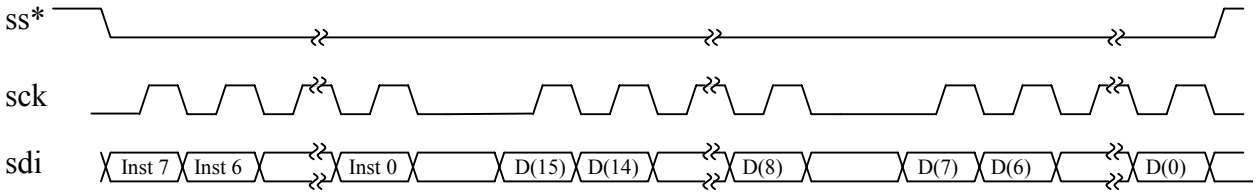


Figure D4. Write timing diagram showing two byte write MSB/LSB order.

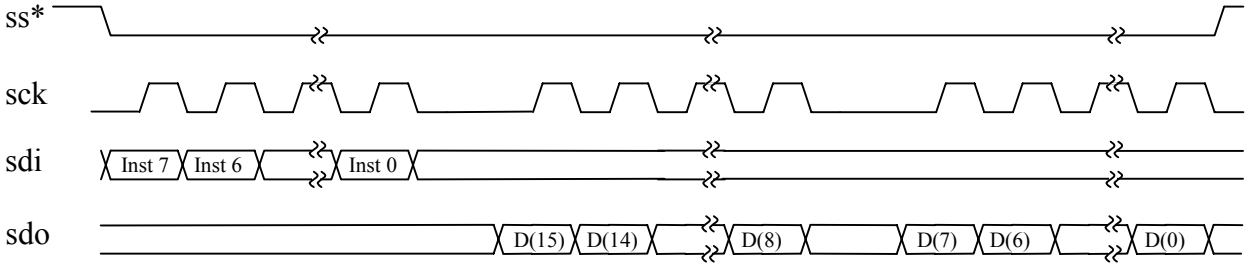
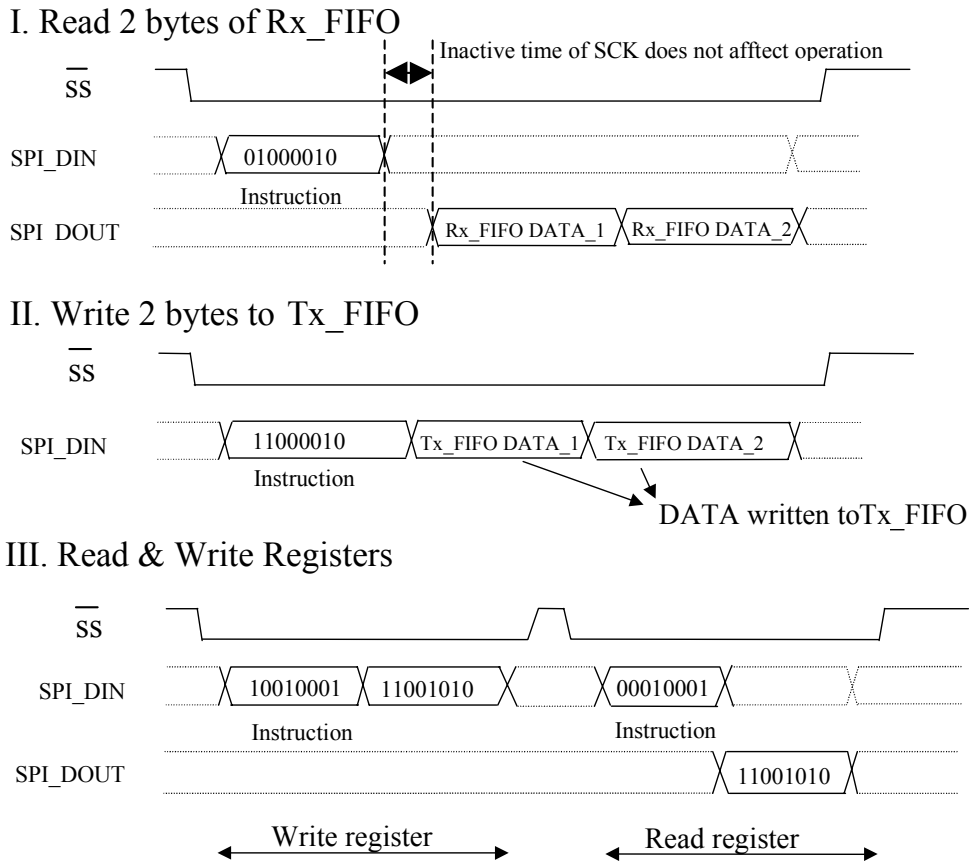


Figure D5. Read timing diagram showing two byte read MSB/LSB order.



6.1.2 Internal Registers

The transceiver has 17 internal registers as shown in table D6. The default operation after power up or reset will assume an input crystal reference frequency of 9.83MHz. A 9.83MHz crystal reference frequency will generate a 100.3kHz PLL reference frequency. The default value for the N register is 21D7 hex, to generate an 868.95MHz modulation frequency. The default value for the data rate register is 161 hex, to generate a 19.2kbps baud rate. After power up or reset all analog transceiver sections will be disabled.

Register Name	Address	Size
Instruction	No address location	8-bits used
Configuration	00h with 8-bits transferred	7 bits written, 8-bits read
FIFO/RX Status	01h with 16-bits transferred	12-bits used
Data Rate	02h with 16-bits transferred	11-bits used
PLL N	03h with 24-bits transferred (23-bits used)	23-bits used
PLL R	04h with 16-bits transferred	14-bits used

Register Name	Address	Size
Demodulator	05h with 8-bits transferred	8-bits used
Tx Power	06h with 8-bits transferred	6-bits used
Crystal	07h with 8-bits transferred	8-bits used
Correlator N	08h with 8-bits transferred	6-bits used
Correlator Mask	09h with 32-bits transferred	32-bits used
Correlator Coeff	0Ah with 32-bits transferred	32-bits used
Correlator Threshold	0Bh with 8-bits transferred	6-bits used
Glitch Filter Register	0Ch with 16-bits transferred	10-bits used
FIFO PAE	0Dh with 8-bits transferred	6-bits used
FIFO PAF	0Eh with 8-bits transferred	6-bits used
Training Bytes	0Fh with 8-transferred	4-bits used

Table D1. Transceiver internal registers.

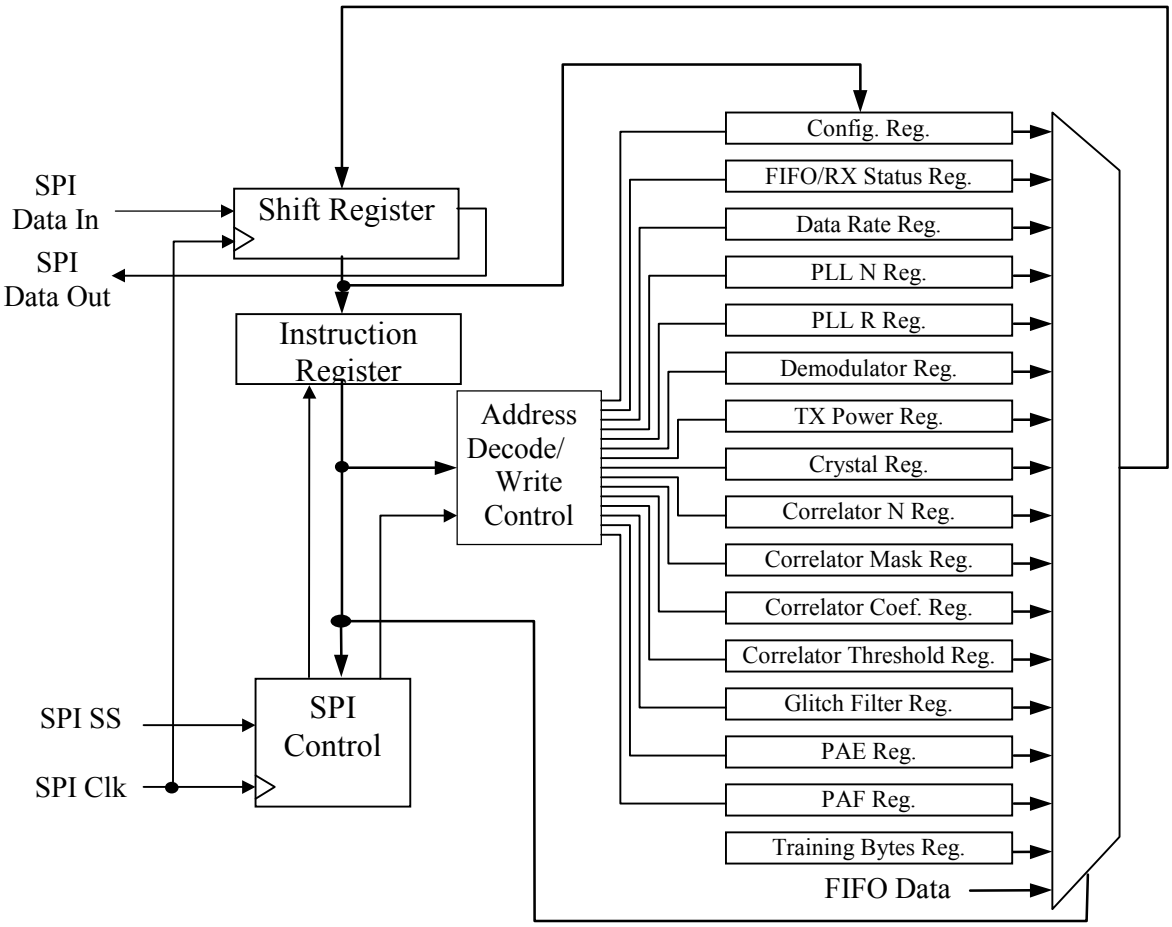


Figure D6. Block Diagram of SPI, Registers and Decoder.

6.1.2.1 Instruction Register Definition

The Instruction Register is the first byte received over the SPI bus from the microprocessor master SPI beginning all data exchanges.

R*/W	reg/fifo	a5/d5	a4/d4	a3/d3	a2/d2	a1/d1	a0/d0

R/W : 0 = read operation from either a register or the FIFO, provided the FIFO is configured to receive.

1 = write operation to either a register or the FIFO, provided the FIFO is configured to transmit.

reg/fifo: 0 = register operation

1 = FIFO operation

a5/d5-a0/d0: When reg/fifo = 0 a register operation has been initiated and these 6 bits provide the register address.

When reg/fifo = 1 a FIFO operation has been initiated and these 6 bits determine the number of bytes to transfer to/from the chosen FIFO selected by the R*/W bit of the instruction register.

A5	A4	A3	A2	A1	A0	Register
0	0	0	0	0	0	Configuration Register
0	0	0	0	0	1	FIFO Status Register
0	0	0	0	1	0	Data Rate Register
0	0	0	0	1	1	PLL N Register
0	0	0	1	0	0	PLL R Register
0	0	0	1	0	1	Demodulator Register
0	0	0	1	1	0	Transmit Power Register
0	0	0	1	1	1	Crystal Oscillator Register
0	0	1	0	0	0	Correlator N Register
0	0	1	0	0	1	Correlator Mask Register
0	0	1	0	1	0	Correlator Coefficient Reg.
0	0	1	0	1	1	Correlator Threshold Reg.
0	0	1	1	0	0	Glitch Filter Register
0	0	1	1	0	1	FIFO PAE Register

0	0	1	1	1	0	FIFO PAF Register
0	0	1	1	1	1	Training Bytes Register

Table D2. Register Addressing.

Instruction Register Operation and Bit Definition	R/W Bit_7	reg/fifo Bit_6	a5/d5 Bit_5	a4/d4 Bit_4	a3/d3 Bit_3	a2/d2 Bit_2	a1/d1 Bit_1	a0/d0 Bit_0
Read from Register Location	0	0	a5	a4	a3	a2	a1	a0
Write to Register Location	1	0	a5	a4	a3	a2	a1	a0
Read from FIFO	0	1	d5	d4	d3	d2	d1	d0
Write to FIFO	1	1	d5	d4	d3	d2	d1	d0

6.1.2.2 Configuration Register Definition

The Configuration Register is used to enable/disable functional areas of the Transceiver ASIC.

PLL CP Enabled	PLL Enable	TX Enable	RX Enable	Mask Enable	Manual PLL CP	Auto PLL CP	FIFO Reset

PLL CP enabled: 0 = PLL charge pump fast lock currently “disabled” (READ ONLY)

1 = PLL charge pump fast lock currently “enabled” (READ ONLY)

PLL enable: 0 = PLL/VCO/XTAL power “disabled” – default value

1 = PLL/VCO/XTAL power “enabled”

transmit enable: 0 = Transmitter PA/VCO PA Buffer power “disabled” – default value

1 = Transmitter PA/VCO PA Buffer power “enabled”

receive enable: 0 = Receiver LNA/Mixer/VCO Mixer LO Buffer/BBfilter/Limiter/Demod power “disabled” – default value

1 = Receiver LNA/Mixer/VCO Mixer LO Buffer/BBfilter/Limiter/Demod power “enabled”

mask enable: 0 = Correlator mask “disabled” – default value

1 = Correlator mask “enabled”

manual PLL CP: 0 = 100uA PLL phase-frequency detector charge pump output level – default value

1 = 400 uA PLL phase-frequency detector charge pump output level.

auto PLL CP: 0 = Automatic PLL high charge pump fast lock cycles “disabled” – default

1 = Automatic PLL high charge pump fast lock cycles “enabled”

FIFO reset: 0 = FIFO not reset – default value.

1 = FIFO reset.

6.1.2.3 FIFO/RX Status Register Definition

Not Used	Not Used	Not Used	Not Used	Manch. Error	FIFO PAE	FIFO PAF	Tx Complete

FIFO Empty	FIFO Full	FIFO Bytes(5)	FIFO Bytes(4)	FIFO Bytes(3)	FIFO Bytes(2)	FIFO Bytes(1)	FIFO Bytes(0)

The FIFO/RX Status Register is a read only register and provides the user with FIFO and receiver status information. After reset or power up the FIFO will be empty.

Manchester Error: 1 = Manchester error detected in data reception (READ ONLY).

0 = no Manchester error detected in data reception (READ ONLY).

FIFO PAE: 1 = number of bytes of data in FIFO is less than or equal to the programmable almost empty flag (PAE) register (READ ONLY).

0 = number of bytes of data in FIFO is greater than programmable almost empty flag (PAE) register (READ ONLY).

FIFO PAF: 1 = number of bytes of data in FIFO is greater than or equal to the programmable almost full flag (PAF) register (READ ONLY).

0 = number of bytes of data in FIFO is less than the programmable almost full flag (PAF) register (READ ONLY).

Tx Complete: 1 = Transmission of data complete, indicates that a transmission is not in progress.

0 = Transmission of data not complete, indicates that a transmission is currently in progress.

FIFO Empty: 1 = FIFO is empty and ready to accept data (READ ONLY).

0 = FIFO has data in it (READ ONLY).

FIFO Full: 1 = FIFO is full and will not accept more data (READ ONLY).

0 = FIFO is not full and will accept more data (READ ONLY).

FIFO Bytes (5..0): These 6 bits along with the FIFO Full flag define the number of bytes currently in the FIFO. When the FIFO is full these 6 bits will be 0 and the FIFO full flag will indicate 64 bytes. (READ ONLY)

6.1.2.4 Data Rate Register Definition

MSB	NU	NU	NU	NU	NU	Data Rate(10)	Data Rate(9)	Data Rate(8)
LSB	Data Rate(7)	Data Rate(6)	Data Rate(5)	Data Rate(4)	Data Rate(3)	Data Rate(2)	Data Rate(1)	Data Rate(0)

The Data Rate Register defines the transmit or the receive data baud rate based on the PLL prescaler output frequency. The value of the Data Rate Register should be set as shown in Appendix A for the desired transmit/receive frequencies and associated baud rates.

Data Rate(10..0): These 11 bits define the divide value loaded into the Data Rate Register. Default value = “00101100001” corresponding to 19.2kbps, using 868.95MHz RF frequency and 100.3kbps PLL reference frequency.

NU: Bit location Not Used.

6.1.2.5 PLL N Register Definition

MSB	NU	Fast Lock Cycles(3)	Fast Lock Cycles(2)	Fast Lock Cycles(1)	Fast Lock Cycles(0)	PLL N Reg(18)	PLL N Reg(17)	PLL N Reg(16)
MSB-1	PLL N Reg(15)	PLL N Reg (14)	PLL N Reg(13)	PLL N Reg(12)	PLL N Reg(11)	PLL N Reg(10)	PLL N Reg(9)	PLL N Reg(8)
LSB	PLL N Reg(7)	PLL N Reg(6)	PLL N Reg(5)	PLL N Reg(4)	PLL N Reg(3)	PLL N Reg(2)	PLL N Reg(1)	PLL N Reg(0)

The N register defines the divide count for the RF frequency divider.

Fast Lock Cycles(3..0): These 4-bits define how many reference clock cycles of high charge pump will be enabled after writing to the N regsiter. Possible values range from 0-15 cycles. The Automatic PLL CP must be enabled for these fast lock cycles to occur.

PLL N Reg(18..0): These 19-bits define the divide value loaded into the N-register for the PLL. Default value = “00000100001110101111” corresponding to 868.95 MHz modulation frequency with a 100 kHz reference frequency.

NU: Bit location Not Used.

6.1.2.6 PLL R Register Definition

MSB	NU	NU	PLL R Reg(13)	PLL R Reg(12)	PLL R Reg(11)	PLL R Reg(10)	PLL R Reg(9)	PLL R Reg(8)
LSB	PLL R Reg(7)	PLL R Reg (6)	PLL R Reg(5)	PLL R Reg(4)	PLL R Reg(3)	PLL R Reg(2)	PLL R Reg(1)	PLL R Reg(0)

The PLL R Register defines the divide ratio for the crystal oscillator input. The divided crystal oscillator output is used as the reference frequency or the PLL. The value of the PLL R Register should be set as shown in appendix A for the desired PLL reference frequency.

PLL R Reg(13..0): These 14-bits define the divide value loaded into the R-register. Default value = “00000001100010”, with a 9.83 MHz input crystal frequency will generate the desired 100kHz reference frequency.

NU: Bit location Not Used.

6.1.2.7 Demodulator Register Definition

Manch. LSB First	Mod. CP Select	En. BPF Test	VCO En. Sel.	Demod. Data Pol.	Demod. Out Sel.	Crystal Divide	Manch. Enable

Manchester LSB First: 0 = normal mode operation – default value.

1 = least significant Manchester coded bit received/transmitted first.

Modulation CP Select: Selects push/pull operation when '0' (+/-100uA) or push/tristate operation when '1' (+100uA/highZ) for the modulation charge pump output. This signal is used in the analog circuitry in conjunction with the PLL Enable and the Modulation CP Enable.

The Modulation CP Enable is a "gate/window" signal which is active when data is being sent out the FIFO.

The output state of the PLL Modulation Charge Pump is defined in the table below.

PLL Enable	Mod CP Select	Mod CP Enable	Mod CP Output State
1	1	X	Push/Tri-state
1	0	1	Push/Pull
1	0	0	Tri-state
0	X	X	Off (Tri-state)

Enable BPF Test: Enables buffered analog baseband filter test outputs (0 selects buffer off, 1 selects buffer on).

VCO Enable Select: Selects the enable that controls the VCO tank output buffer to the poly-phase filter and RX local oscillator (0 selects VCO_EN control, 1 selects RX_EN control).

Demod Data Polarity: Selects data polarity from internal analog demodulator output for use by the digital receiver (0 selects normal polarity, 1 selects inverted polarity).

Demod Output Select: Selects data input for digital receiver (0 selects internal analog demodulator output data, 1 selects external data from DIG_DATA_IN).

Crystal Divide: A crystal oscillator frequency divided by 2 buffered output is available from the XTAL_DIV2_OUT pad. (0 selects output on, 1 selects output off).

Manchester Enable: 0 = Manchester coding "disabled" –default value

1 = Manchester coding enabled

Default value = “00000000”

6.1.2.8 Tx Power Register Definition

NU	NU	TX Power(5)	TX Power(4)	TX Power(3)	TX Power(2)	TX Power(1)	TX Power(0)

The Transmitter Power Register programs the RF power amplifier output power level. Table D2 provides 5 (example) register values and the associated RF PA output transmit power value.

TX Power(5..0): These bit locations set the transmit power of the power amplifier with all “0”s being the lowest possible power level and all “1”s being the highest output power level. Default value = “111111”.

NU: Bit location Not Used.

TX Power Reg. Value	TX Power (dBm)
63	+6 dBm
20	-3 dBm
5	-13 dBm
0	-23 dBm

Table D2. TX power examples.

6.1.2.9 Crystal Register Word Definition

HCG	HMG	XTBF (2)	XTBF (1)	XTBF (0)	XTBIAS (2)	XTBIAS (1)	XTBIAS (0)

The crystal register controls the drive output of the crystal oscillator circuit. The variable drive feature allows the oscillator to be optimized for a wide variety of crystal load impedance and a wide variety of crystal resonant frequencies. The default value is set for a crystal oscillation frequency of 10MHz. The value of the Crystal Register should be set as shown in Appendix B: “Crystal Oscillator Configuration of Crystal Register”.

HCG: default value set to ‘0’ => 10MHz.

HMG: default value set to ‘1’ => 10MHz.

\XTBF(2..0): default value set to “001” => 10MHz.

XTBias(2..0): default value set to “110” => 10MHz.

6.1.2.10 Correlation N Register Definition

NU	NU	Correl. N Reg(5)	Correl. N Reg(4)	Correl. N Reg(3)	Correl. N Reg(2)	Correl. N Reg(1)	Correl. N Reg(0)

The correlation coefficient are fixed at 32 bits. The Correlation N Register defines the size of the synchronization word by allowing only N bits of the correlation coefficient to be transmitted and checks for N bits of the correlation coefficient for reception. The correlation coefficient bits are defined starting with the LSB.

Correlation N Reg(5..0): default value=”100000”.

6.1.2.11 Correlation Mask Register Definition

MSB	Correl. Mask Reg(31)	Correl. Mask. Reg(30)	Correl. Mask Reg(29)	Correl. Mask Reg(28)	Correl. Mask Reg(27)	Correl. Mask Reg(26)	Correl. Mask Reg(25)	Correl. Mask Reg(24)
	Correl. Mask Reg(23)	Correl. Mask Reg(22)	Correl. Mask Reg(21)	Correl. Mask Reg(20)	Correl. Mask Reg(19)	Correl. Mask Reg(18)	Correl. Mask Reg(17)	Correl. Mask Reg(16)
	Correl. Mask Reg(15)	Correl. Mask Reg(14)	Correl. Mask Reg(13)	Correl. Mask Reg(12)	Correl. Mask Reg(11)	Correl. Mask Reg(10)	Correl. Mask Reg(9)	Correl. Mask Reg(8)
LSB	Correl. Mask Reg(7)	Correl. Mask Reg(6)	Correl. Mask Reg(5)	Correl. Mask Reg(4)	Correl. Mask Reg(3)	Correl. Mask Reg(2)	Correl. Mask Reg(1)	Correl. Mask Reg(0)

The correlation mask register selects which of the N (Correlation N Register defined) LSB correlation coefficient bits are masked off during reception mode.

Definition: ‘0’ = corresponding correlation coefficient bit not masked off (bit is considered), ‘1’=corresponding correlation coefficient bit masked off (bit not considered).

Correlation Mask Reg(31..0): default value=”00000000000000000000000000000000”.

6.1.2.12 Correlation Coefficient Register Definition

MSB

Correl. Coeff. Reg(31)	Correl. Coeff. Reg(30)	Correl. Coeff. Reg(29)	Correl. Coeff. Reg(28)	Correl. Coeff. Reg(27)	Correl. Coeff. Reg(26)	Correl. Coeff. Reg(25)	Correl. Coeff. Reg(24)

Correl. Coeff. Reg(23)	Correl. Coeff. Reg(22)	Correl. Coeff. Reg(21)	Correl. Coeff. Reg(20)	Correl. Coeff. Reg(19)	Correl. Coeff. Reg(18)	Correl. Coeff. Reg(17)	Correl. Coeff. Reg(16)

Correl. Coeff. Reg(15)	Correl. Coeff. Reg(14)	Correl. Coeff. Reg(13)	Correl. Coeff. Reg(12)	Correl. Coeff. Reg(11)	Correl. Coeff. Reg(10)	Correl. Coeff. Reg(9)	Correl. Coeff. Reg(8)

LSB

Correl. Coeff. Reg(7)	Correl. Coeff. Reg(6)	Correl. Coeff. Reg(5)	Correl. Coeff. Reg(4)	Correl. Coeff. Reg(3)	Correl. Coeff. Reg(2)	Correl. Coeff. Reg(1)	Correl. Coeff. Reg(0)

The correlation coefficient register allows four unique bytes (32 bits) to be used during transmit mode and as comparison bytes during receive mode. The Correlation N Register determines how many of the 32 bits (starting with the LSB) are actually used. The Correlation Mask Register determines which of the N (Correlation N Register determined) bits are actually considered.

Correlation Coeff. Reg(31..0): These 32-bits define the correlation data sent during a transmission and compared with during reception. Default value = “10101010101010101010101010101010”.

6.1.2.13 Correlation Threshold Register Definition

NU	NU	Correl. Thrshld. Reg(5)	Correl. Thrshld. Reg(4)	Correl. Thrshld. Reg(3)	Correl. Thrshld. Reg(2)	Correl. Thrshld. Reg(1)	Correl. Thrshld. Reg(0)

The correlation threshold register defines how many of the un-masked N correlation coefficients must match to cause a detection during reception.

Correlation Threshold Reg(5..0): The default value=”100000”.

NU: Bit location not used.

6.1.2.14 Glitch Filter Register Word Definition

MSB	NU	NU	NU	NU	NU	NU	Glitch Filter Reg(9)	Glitch Filter Reg(8)
LSB	Glitch Filter Reg(7)	Glitch Filter Reg (6)	Glitch FIlter Reg(5)	Glitch Filter Reg(4)	Glitch Filter Reg(3)	Glitch Filter Reg(2)	Glitch Filter Reg(1)	Glitch Filter Reg(0)

The glitch filter register sets the amount of hysteresis in the glitch removal circuit. Refer to the Glitch Removal Filter description section for more information on its function and how to select appropriate values.

Glitch Filter Reg(9..0): The default value = “0011101110”.

NU: Bit location not used.

6.1.2.15 Programmable Almost Empty Flag Register Definition

NU	NU	PAE Reg(5)	PAE Reg(4)	PAE Reg(3)	PAE Reg(2)	PAE Reg(1)	PAE Reg(0)

The programmable almost empty flag register defines the maximum number of bytes of data in the FIFO during data transmission to cause the PAE flag to be asserted. This flag will also cause an SPI interrupt during data transmission, allowing for continuous data transmission. Note: the flag will not cause an SPI interrupt when TX_EN is disabled.

PAE Reg(5..0): default value=”100000”.

6.1.2.16 Programmable Almost Full Flag Register Definition

NU	NU	PAF Reg(5)	PAF Reg(4)	PAF Reg(3)	PAF Reg(2)	PAF Reg(1)	PAF Reg(0)

The programmable almost full flag register defines the minimum number of bytes of data in the FIFO during data reception to cause the PAF flag to be asserted. This flag will also cause an SPI interrupt during data reception, allowing for continuous data reception. Note: the flag will not cause an SPI interrupt when RX_EN is disabled.

PAF Reg(5..0): default value=”100000”.

6.1.2.17 Transmitter Training Cycles Register Definition

NU	NU	NU	NU	Tx Training Reg(3)	Tx Training Reg(2)	Tx Training Reg(1)	Tx Training Reg(0)

The Tx Training Cycles register defines how many training bytes will be transmitted prior to sending the synchronization word and message. A transmit training byte consists of 8-bits of alternating 1,0's. The rate the training bits are output will be the same as the baud rate of the data defined by the data rate register. Possible values are in the range from 0-15 bytes of transmitter training sequence.

Tx Training Cycles Reg(5..0): default value="0000".

6.1.3 Serial Transmitter

The SPI automatically generates a start signal to the serial transmitter after completing the initial SPI FIFO write access. After the serial transmitter has received a start transmission signal from the SPI section, a training sequence is output (the number of bytes of transmitter training is defined by the Tx training cycles register). Following the training sequence the synchronization word is output (if enabled). Once the entire synchronization word has been transmitted the serial transmitter reads the preloaded byte data from the FIFO. The byte data is then serialized and manchester encoded (manchester encoded if enabled). The serial transmitter monitors the FIFO empty status flag indicating the end of the transmission. The serial transmitter generates a transmit complete signal that is readable in the FIFO status register. The transmit complete signal being active indicates that the transmission is complete. Continuous transmission is possible by the SPI master monitoring the FIFO Almost Empty status flag or the SPI Interrupt (ASIC output pin). If set, the SPI Master can load additional data into the FIFO making certain that the FIFO never goes empty.

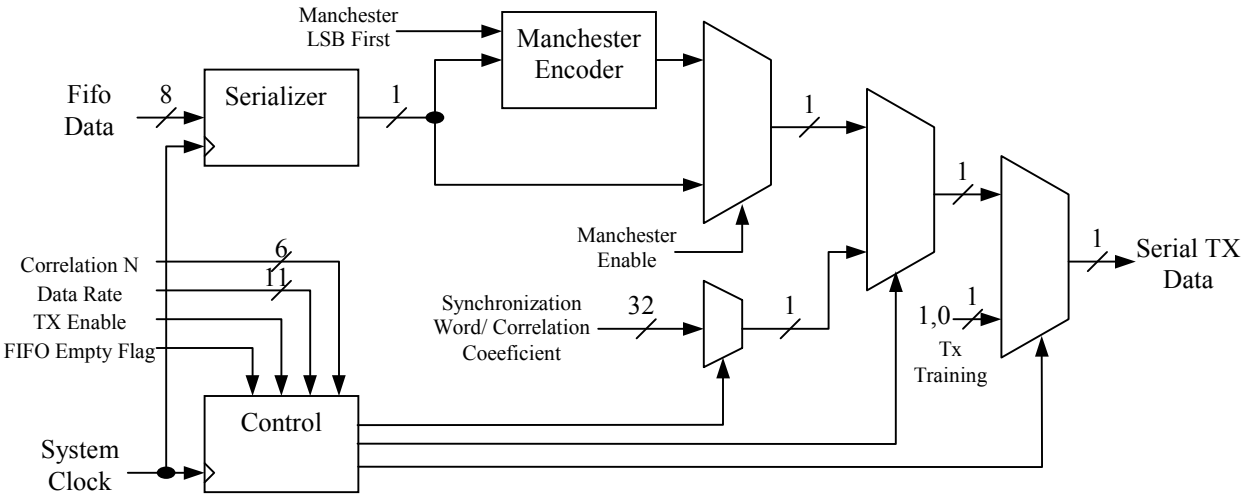


Figure D7. Block Diagram of Serial Transmitter.

6.1.3.1 Transmit Training Bytes

Prior to outputting the synchronization word or encoded data an alternating 1,0 sequence of training is output. The number of bits output are in multiple of 8 bits or a byte. The number of bytes of transmitter training are defined in the transmitter training bytes register. Following the transmitter training bytes the synchronization word is output (if enabled).

6.1.3.2 Synchronization Word

Prior to outputting encoded data a synchronization word is output (if enabled). The synchronization word is referred to as the Correlation Coefficient Register in the SPI register definition section. The synchronization word/Correlation Coefficient Register is 32 bits long and can be programmed to use from 0 to all 32 bits. The length of the synchronization word is determined by the value loaded in the Correlation N Register. The length and value of the synchronization word is pre-loaded by the SPI.

6.1.3.3 Manchester Encoding

The serial data may be manchester encoded. Manchester encoding is enabled by the manchester coding enable bit in the configuration register, defined in the SPI register definition section. The order of the manchester encoding is also programmed by the manchester LSB first bit in the configuration register. The configuration register is defined in the SPI register definition section.

6.1.4 Serial Receiver

The serial receiver first removes glitches from the serial data. The filtered data is then sampled to generate a serial bit stream. The serial bits are then correlated with a pre-loaded synchronization word (if enabled). When the correlation exceeds the correlation threshold (when enabled) the serial bit data is then deserialized to byte data and written into the FIFO.

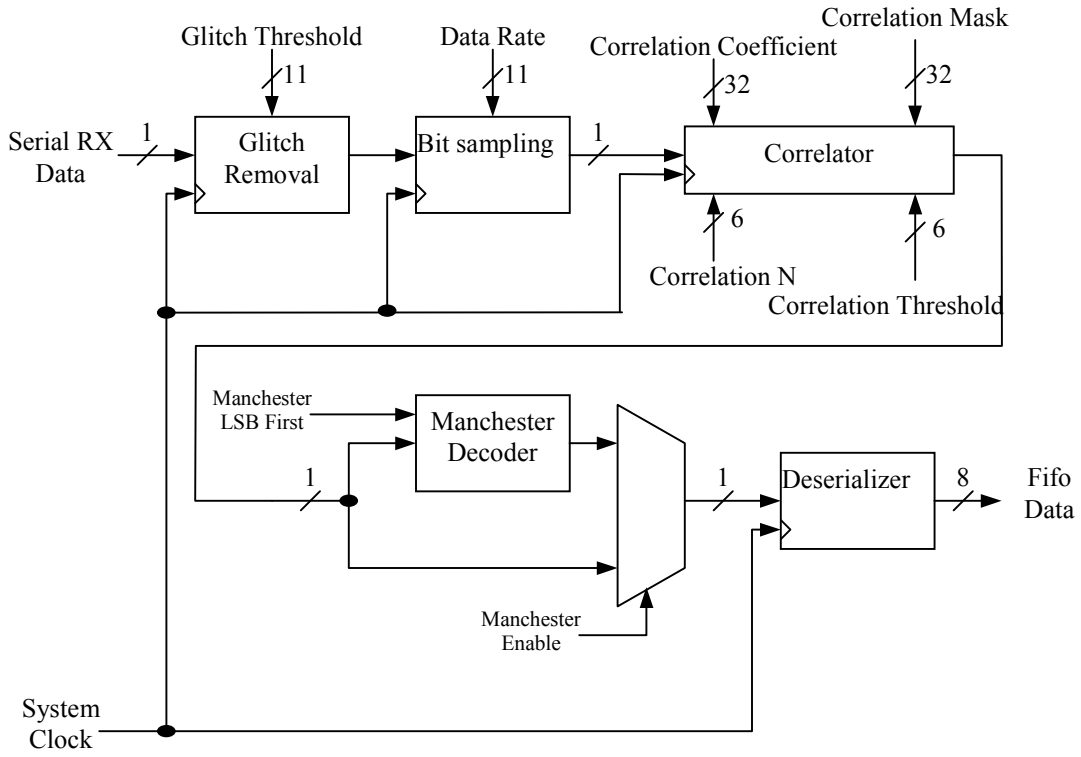
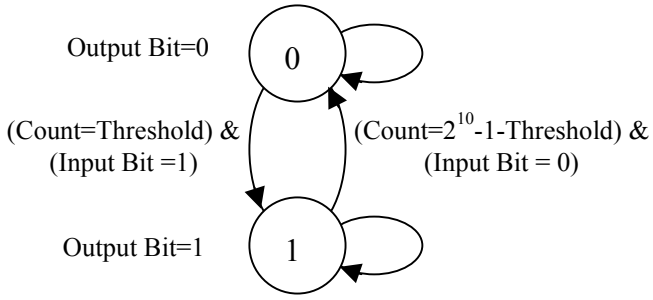


Figure D8. Block Diagram of Serial Receiver.

6.1.4.1 Glitch Removal Filter

Prior to bit determination the received serial digital data is filtered to remove any spurious noise. The method chosen to remove the spurious noise is to apply hysteresis to serial bit stream. The received serial bit digital data is sampled using the system clock. For each sample bit a counter is decremented/incremented based on the samples input bit value 0/1 respectively. The glitch threshold register, loaded from the SPI bus, defines the transition regions. If the count value is in the range 0 to "glitch threshold value" then the output bit value will be 0, corresponding to state 0. If the count value is in the range $(2^{10}\text{-}1)$ to $(2^{10}\text{-}1)$-"glitch threshold value" then the output bit value will be 1, corresponding to state 1. If the count value is the minimum 0 and the input bit value is 0 then the count will remain at the minimum, likewise when the count value is maximum $2^{10}-1$ and the input bit is a 1 then the count will remain at the maximum value. If the current state is state 0 and the count value is equal to the threshold value and the input bit value is 1 then the state machine will transition to state 1 and will also initialize the counter to the maximum value $2^{10}-1$. If the current state is state 1 and the count value is $2^{10}-1$-"glitch threshold value" and the input bit value is 0 then the state machine will transition to state 0 and will also initialize the counter to the minimum value 0. The range of the glitch threshold register is from 0 to 2^{10}-1, a glitch threshold value of 0 corresponds to no glitch removal. Increasing the glitch threshold value increases the amount of hysteresis. A graphical diagram of the state machine for the glitch removal filter is provided in the following figure.



6.1.4.2 Bit Determination

The bit determination circuit receives over sampled binary data from the glitch removal filter. A counter gets initialized (set to 0) whenever a transition of the incoming filtered serial bit stream occurs or whenever the counter reaches a modulus count, equal to the bit rate (defined by the system clock and the data rate register). When the count reaches half of the bit rate (this means that there has been no transitions for half a bit period) then a valid output is generated. This valid output value is the received serial bit value. Ideally this method will be capable of receiving serial data with up to 25% jitter. The bit determination circuit is synchronous to the system clock and the data rate register provides the number of system clock rate samples to define the bit rate.

6.1.4.3 Correlation

Prior to writing the data into the FIFO, the receiver must first detect the synchronization word (up to 32 bits). The correlator has four programmable features:

- **Length** – Select the number of bits in the correlator. Up to 32 bits (Correlator N Register)
- **Value** – Select the correlation pattern (Correlator Coefficient Register)
- **Mask** – Select the actual bits to be correlated. You may chose to mask bits off. (Correlator Mask Register)
- **Threshold** – Select the number of bits required for the correlator to match.

As the serial data begins to enter the correlator, it will compare data bits with the correlator value with the mask in place. Once enough bits are matched to reach the threshold, the data will then be sent into the FIFO. A block diagram is shown below.

6.1.4.4 Manchester Decoder

The serial data may be manchester decoded. Manchester decoding is enabled by the manchester coding enable bit in the configuration register, defined in the SPI register definition section. The

order of the manchester decoding is also programmed by the manchester LSB first bit in the configuration register. The configuration register is defined in the SPI register definition section.

6.1.5 FIFO

A single FIFO is used for both reception and transmission of data. The FIFO is 64 byte in length. Both the transmitter and receiver depending on the operational mode of the chip can access the FIFO.

1. When the transceiver is configured in transmit mode, the SPI will have write access to the FIFO and the serial transmitter will have read access to the FIFO.

2. When the transceiver is configured in the receive mode, the serial receiver will have write access to the FIFO and the SPI will have read access to the FIFO.

The FIFO generates several status flags indicating the current state of the FIFO. These flags include:

- **FIFO Empty** - Set to "1" when no data is in FIFO.
- **FIFO Full** - Set to "1" when the FIFO is full.
- **Programmable Almost Empty (PAE)** – Set to "1" when the number of bytes in the FIFO is less than the PAE register value. Transmitter mode.
- **Programmable Almost Full (PAF)** – Set to "1" when the number of bytes of data in the FIFO is greater than the PAF register value. Receiver mode.

These status flags are all accessible through the FIFO status register, defined in the SPI register definition section.

In the transmit mode, when the FIFO PAE status flag is set ("1"), it will cause the SPI_INT signal to change to a high state ("1") signaling the number of bytes in the FIFO has crossed the PAE threshold. Likewise, in the receive mode, when the FIFO PAF status flag is set ("1"), it will cause the SPI_INT signal to change to a high state ("1") signaling the number of bytes in the FIFO has crossed the PAF threshold.

6.1.6 SLEEP Mode

The SLEEP mode is achieved by disabling power to all circuitry. This is accomplished by setting the TX_EN, RX_EN, and PLL_EN enables to 0 state (disabled state) via the SPI interface. Note that in this mode of operation, the crystal oscillator is also shut down. As a result, the application must use an off-chip timer to tell the SPI master to enable the ASIC for operation.

7.0 Packaging

TBD

8.0 PCB Layout Guidelines

Proper layout of components and copper traces is required in order to attain optimal circuit performance. The following are some general guidelines that assist in proper layout design.

All RF circuits should be compact and close to the IC pin locations to which they are connected. Keep the loop area of an RF current path as small as possible to minimize radiation. This implies that components associated with the VCO resonator should be very close together as should the components relating the to transmitter power amplifier and receiver LNA. Capacitors for decoupling the individual supplies should be placed as close to the respective supply pin locations as possible. For best operation, it is important that coupling between RX_IN, TX_OUT and the VCO resonator is minimized.

9.0 Appendices

9.1 Appendix A: PLL Frequency and Data Rate Register Tables

A spreadsheet is available, called “pll_rfgrow3.xls” that provides the user R and N divider ratios (shown in decimal) from input desired RF and Reference frequencies (the PLL comparison frequency determines the minimum channel spacing and channel switching speeds of the PLL synthesizer). These divider ratios are provided for a wide range of available crystal oscillator frequencies. Note that the user-input columns have a blue background, and the outputs have a standard white background.

The spreadsheet also provides the Data Rate Register values needed to set up the transceiver data rate. These values can be found starting at H6 (Column/Row) and ending at AF23. The user inputs all the parameters used to obtain the R and N divider ratios, and then looks at the Data Rate Register value (shown in decimal) for the desired data rate. This is the value the user must enter into the GROW ASIC via the SPI interface. Data Rate Register values are tabulated for typical data rates ranging from 4.8kpbs to 120kbps. Note that data rates have only been demonstrated to 52.8kbps for the GROW chip.

The user in encouraged to use the spreadsheet, but a couple example outputs (not complete) are provided below.

Examples of divide ratios for 418Mhz with a 100.3kHz loop frequency using standard crystals.

Crystal tol.= 0 ppm < NOMINAL CASE.
Desired Frf= 418.000 MHz
Desired Fref= 100.300 kHz

Fxtal (MHz)	Reference Divide Ratio (R) {R>1}	Fref (kHz)	RF Divide Ratio (N) {N>992}	Frf achieved (MHz)	Frf Difference (kHz)	System_clk (MHz)
0.0327680	0	#DIV/0!	4167	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	10	100.0000	4167	416.7000	-1300.0000	3.25
1.2280000	12	102.3333	4167	426.4230	8423.0000	3.325833333
1.8432000	18	102.4000	4167	426.7008	8700.8000	3.328
2.0000000	20	100.0000	4167	416.7000	-1300.0000	3.25
2.4576000	25	98.3040	4167	409.6328	-8367.2320	3.19488
3.6864000	37	99.6324	4167	415.1683	-2831.6541	3.238054054
4.0000000	40	100.0000	4167	416.7000	-1300.0000	3.25
4.9152000	49	100.3102	4167	417.9926	-7.3796	3.260081633
5.0000000	50	100.0000	4167	416.7000	-1300.0000	3.25
5.0688000	51	99.3882	4167	414.1508	-3849.2235	3.230117647
6.0000000	60	100.0000	4167	416.7000	-1300.0000	3.25
8.0000000	80	100.0000	4167	416.7000	-1300.0000	3.25
9.8300000	98	100.3061	4167	417.9756	-24.3878	3.25994898
10.0000000	100	100.0000	4167	416.7000	-1300.0000	3.25
14.3181800	143	100.1271	4167	417.2298	-770.2373	3.254131818
16.0000000	160	100.0000	4167	416.7000	-1300.0000	3.25

Examples of Data Rate Register values (in decimal) for 418Mhz with a 100kHz loop frequency using standard crystals.

desired samples per bit time= 1

Crystal tol.= 0 ppm

Desired Frf= 418.000 MHz =((1/bps)/(1/Fsys_clk))/(desired samples each bit)

Desired Fref= 100.000 kHz

Fxtal (MHz)	System_clk (MHz)	4800	9600	14400	19200	24000	28800	33600	38400	43200	48000	52800
0.0327680	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
1.2280000	6.779583333	1412.41	706.21	470.80	353.10	282.48	235.40	201.77	176.55	156.93	141.24	128.40
1.8432000	6.784	1413.33	706.67	471.11	353.33	282.67	235.56	201.90	176.67	157.04	141.33	128.48
2.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
2.4576000	6.782976	1413.12	706.56	471.04	353.28	282.62	235.52	201.87	176.64	157.01	141.31	128.47
3.6864000	6.775005405	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.9152000	6.770938776	1410.61	705.31	470.20	352.65	282.12	235.10	201.52	176.33	156.73	141.06	128.24
5.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
5.0688000	6.783247059	1413.18	706.59	471.06	353.29	282.64	235.53	201.88	176.65	157.02	141.32	128.47
6.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
8.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
9.8300000	6.770663265	1410.55	705.28	470.18	352.64	282.11	235.09	201.51	176.32	156.73	141.06	128.23
10.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
14.3181800	6.783613252	1413.25	706.63	471.08	353.31	282.65	235.54	201.89	176.66	157.03	141.33	128.48
16.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31

Examples of divide ratios for 434.92Mhz with a 100.3kHz loop frequency using standard crystals.

Crystal tol.= 0 ppm < NOMINAL CASE.
Desired Frf= 434.920 MHz
Desired Fref= 100.300 kHz

Fxtal (MHz)	Reference Divide Ratio (R) {R>1}	Fref (kHz)	RF Divide Ratio (N) {N>992}	Frf achieved (MHz)	Frf Difference (kHz)	System_clk (MHz)
0.0327680	0	#DIV/0!	4336	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	10	100.0000	4336	433.6000	-1320.0000	3.375
1.2280000	12	102.3333	4336	443.7173	8797.3333	3.45375
1.8432000	18	102.4000	4336	444.0064	9086.4000	3.456
2.0000000	20	100.0000	4336	433.6000	-1320.0000	3.375
2.4576000	25	98.3040	4336	426.2461	-8673.8560	3.31776
3.6864000	37	99.6324	4336	432.0062	-2913.7730	3.362594595
4.0000000	40	100.0000	4336	433.6000	-1320.0000	3.375
4.9152000	49	100.3102	4336	434.9450	25.0449	3.385469388
5.0000000	50	100.0000	4336	433.6000	-1320.0000	3.375
5.0688000	51	99.3882	4336	430.9474	-3972.6118	3.354352941
6.0000000	60	100.0000	4336	433.6000	-1320.0000	3.375
8.0000000	80	100.0000	4336	433.6000	-1320.0000	3.375
9.8300000	98	100.3061	4336	434.9273	7.3469	3.385331633
10.0000000	100	100.0000	4336	433.6000	-1320.0000	3.375
14.3181800	143	100.1271	4336	434.1512	-768.7519	3.379290734
16.0000000	160	100.0000	4336	433.6000	-1320.0000	3.375

Examples of Data Rate Register values (in decimal) for 434.92Mhz with a 100kHz loop frequency using standard crystals.

desired samples per bit time= 1

Crystal tol.= 0 ppm

Desired Frf= 434.920 MHz =((1/bps)/(1/Fsys_clk))/(desired samples each bit)

Desired Fref= 100.000 kHz

Fxtal (MHz)	System_clk (MHz)	4800	9600	14400	19200	24000	28800	33600	38400	43200	48000	52800
0.0327680	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
1.2280000	6.779583333	1412.41	706.21	470.80	353.10	282.48	235.40	201.77	176.55	156.93	141.24	128.40
1.8432000	6.784	1413.33	706.67	471.11	353.33	282.67	235.56	201.90	176.67	157.04	141.33	128.48
2.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
2.4576000	6.782976	1413.12	706.56	471.04	353.28	282.62	235.52	201.87	176.64	157.01	141.31	128.47
3.6864000	6.775005405	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.9152000	6.770938776	1410.61	705.31	470.20	352.65	282.12	235.10	201.52	176.33	156.73	141.06	128.24
5.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
5.0688000	6.783247059	1413.18	706.59	471.06	353.29	282.64	235.53	201.88	176.65	157.02	141.32	128.47
6.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
8.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
9.8300000	6.770663265	1410.55	705.28	470.18	352.64	282.11	235.09	201.51	176.32	156.73	141.06	128.23
10.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
14.3181800	6.783613252	1413.25	706.63	471.08	353.31	282.65	235.54	201.89	176.66	157.03	141.33	128.48
16.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31

Examples of divide ratios for 868.95Mhz with a 100kHz loop frequency using standard crystals.

Crystal tol.= 0 ppm < NOMINAL CASE.
Desired Frf= 868.950 MHz
Desired Fref= 100.000 kHz

Fxtal (MHz)	Reference Divide Ratio (R) {R>1}	Fref (kHz)	RF Divide Ratio (N) {N>992}	Frf achieved (MHz)	Frf Difference (kHz)	System_clk (MHz)
0.0327680	0	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	10	100.0000	8690	869.0000	50.0000	6.775
1.2280000	12	102.3333	8491	868.9123	-37.6667	6.779583333
1.8432000	18	102.4000	8486	868.9664	16.4000	6.784
2.0000000	20	100.0000	8690	869.0000	50.0000	6.775
2.4576000	25	98.3040	8839	868.9091	-40.9440	6.782976
3.6864000	37	99.6324	8722	868.9941	44.0757	6.775005405
4.0000000	40	100.0000	8690	869.0000	50.0000	6.775
4.9152000	49	100.3102	8663	868.9873	37.2980	6.770938776
5.0000000	50	100.0000	8690	869.0000	50.0000	6.775
5.0688000	51	99.3882	8743	868.9513	1.3412	6.783247059
6.0000000	60	100.0000	8690	869.0000	50.0000	6.775
8.0000000	80	100.0000	8690	869.0000	50.0000	6.775
9.8300000	98	100.3061	8663	868.9519	1.9388	6.770663265
10.0000000	100	100.0000	8690	869.0000	50.0000	6.775
14.3181800	143	100.1271	8678	868.9033	-46.7410	6.783613252
16.0000000	160	100.0000	8690	869.0000	50.0000	6.775

Examples of Data Rate Register values (in decimal) for 868.95Mhz with a 100kHz loop frequency using standard crystals.

desired samples per bit time= 1

Crystal tol.= 0 ppm

Desired Frf= 868.950 MHz

Desired Fref= 100.000 kHz

=((1/bps)/(1/Fsys_clk))/(desired samples each bit)

Fxtal (MHz)	System_clk (MHz)	4800	9600	14400	19200	24000	28800	33600	38400	43200	48000	52800
0.0327680	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
1.2280000	6.779583333	1412.41	706.21	470.80	353.10	282.48	235.40	201.77	176.55	156.93	141.24	128.40
1.8432000	6.784	1413.33	706.67	471.11	353.33	282.67	235.56	201.90	176.67	157.04	141.33	128.48
2.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
2.4576000	6.782976	1413.12	706.56	471.04	353.28	282.62	235.52	201.87	176.64	157.01	141.31	128.47
3.6864000	6.775005405	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.9152000	6.770938776	1410.61	705.31	470.20	352.65	282.12	235.10	201.52	176.33	156.73	141.06	128.24
5.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
5.0688000	6.783247059	1413.18	706.59	471.06	353.29	282.64	235.53	201.88	176.65	157.02	141.32	128.47
6.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
8.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
9.8300000	6.770663265	1410.55	705.28	470.18	352.64	282.11	235.09	201.51	176.32	156.73	141.06	128.23
10.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
14.3181800	6.783613252	1413.25	706.63	471.08	353.31	282.65	235.54	201.89	176.66	157.03	141.33	128.48
16.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31

Examples of divide ratios for 902Mhz with a 100.3kHz loop frequency using standard crystals.

Crystal tol.= 0 ppm < NOMINAL CASE.
Desired Frf= 902.000 MHz
Desired Fref= 100.300 kHz

Fxtal (MHz)	Reference Divide Ratio (R) {R>1}	Fref (kHz)	RF Divide Ratio (N) {N>992}	Frf achieved (MHz)	Frf Difference (kHz)	System_clk (MHz)
0.0327680	0	#DIV/0!	8993	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	10	100.0000	8993	899.3000	-2700.0000	7.025
1.2280000	12	102.3333	8993	920.2837	18283.6667	7.188916667
1.8432000	18	102.4000	8993	920.8832	18883.2000	7.1936
2.0000000	20	100.0000	8993	899.3000	-2700.0000	7.025
2.4576000	25	98.3040	8993	884.0479	-17952.1280	6.905856
3.6864000	37	99.6324	8993	895.9945	-6005.5351	6.999178378
4.0000000	40	100.0000	8993	899.3000	-2700.0000	7.025
4.9152000	49	100.3102	8993	902.0897	89.6653	7.046791837
5.0000000	50	100.0000	8993	899.3000	-2700.0000	7.025
5.0688000	51	99.3882	8993	893.7984	-8201.6000	6.982023529
6.0000000	60	100.0000	8993	899.3000	-2700.0000	7.025
8.0000000	80	100.0000	8993	899.3000	-2700.0000	7.025
9.8300000	98	100.3061	8993	902.0530	52.9592	7.046505102
10.0000000	100	100.0000	8993	899.3000	-2700.0000	7.025
14.3181800	143	100.1271	8993	900.4433	-1556.6941	7.033931084
16.0000000	160	100.0000	8993	899.3000	-2700.0000	7.025

Examples of Data Rate Register values (in decimal) for 902.000Mhz with a 100kHz loop frequency using standard crystals.

desired samples per bit time= 1

Crystal tol.= 0 ppm

Desired Frf= 902.000 MHz =((1/bps)/(1/Fsys_clk))/(desired samples each bit)

Desired Fref= 100.000 kHz

Fxtal (MHz)	System_clk (MHz)	4800	9600	14400	19200	24000	28800	33600	38400	43200	48000	52800
0.0327680	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
1.2280000	6.779583333	1412.41	706.21	470.80	353.10	282.48	235.40	201.77	176.55	156.93	141.24	128.40
1.8432000	6.784	1413.33	706.67	471.11	353.33	282.67	235.56	201.90	176.67	157.04	141.33	128.48
2.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
2.4576000	6.782976	1413.12	706.56	471.04	353.28	282.62	235.52	201.87	176.64	157.01	141.31	128.47
3.6864000	6.775005405	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.9152000	6.770938776	1410.61	705.31	470.20	352.65	282.12	235.10	201.52	176.33	156.73	141.06	128.24
5.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
5.0688000	6.783247059	1413.18	706.59	471.06	353.29	282.64	235.53	201.88	176.65	157.02	141.32	128.47
6.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
8.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
9.8300000	6.770663265	1410.55	705.28	470.18	352.64	282.11	235.09	201.51	176.32	156.73	141.06	128.23
10.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
14.3181800	6.783613252	1413.25	706.63	471.08	353.31	282.65	235.54	201.89	176.66	157.03	141.33	128.48
16.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31

Examples of divide ratios for 928Mhz with a 100.3kHz loop frequency using standard crystals.

Crystal tol.= 0 ppm < NOMINAL CASE.
Desired Frf= 928.000 MHz
Desired Fref= 100.300 kHz

Fxtal (MHz)	Reference Divide Ratio (R) {R>1}	Fref (kHz)	RF Divide Ratio (N) {N>992}	Frf achieved (MHz)	Frf Difference (kHz)	System_clk (MHz)
0.0327680	0	#DIV/0!	9252	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	10	100.0000	9252	925.2000	-2800.0000	7.225
1.2280000	12	102.3333	9252	946.7880	18788.0000	7.393583333
1.8432000	18	102.4000	9252	947.4048	19404.8000	7.3984
2.0000000	20	100.0000	9252	925.2000	-2800.0000	7.225
2.4576000	25	98.3040	9252	909.5086	-18491.3920	7.102464
3.6864000	37	99.6324	9252	921.7993	-6200.7351	7.198443243
4.0000000	40	100.0000	9252	925.2000	-2800.0000	7.225
4.9152000	49	100.3102	9252	928.0700	70.0082	7.247412245
5.0000000	50	100.0000	9252	925.2000	-2800.0000	7.225
5.0688000	51	99.3882	9252	919.5400	-8460.0471	7.1808
6.0000000	60	100.0000	9252	925.2000	-2800.0000	7.225
8.0000000	80	100.0000	9252	925.2000	-2800.0000	7.225
9.8300000	98	100.3061	9252	928.0322	32.2449	7.247117347
10.0000000	100	100.0000	9252	925.2000	-2800.0000	7.225
14.3181800	143	100.1271	9252	926.3762	-1623.7667	7.23418535
16.0000000	160	100.0000	9252	925.2000	-2800.0000	7.225

Examples of Data Rate Register values (in decimal) for 928.000Mhz with a 100kHz loop frequency using standard crystals.

desired samples per bit time= 1

Crystal tol.= 0 ppm

Desired Frf= 928.000 MHz =((1/bps)/(1/Fsys_clk))/(desired samples each bit)

Desired Fref= 100.000 kHz

Fxtal (MHz)	System_clk (MHz)	4800	9600	14400	19200	24000	28800	33600	38400	43200	48000	52800
0.0327680	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!	#DIV/0!
1.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
1.2280000	6.779583333	1412.41	706.21	470.80	353.10	282.48	235.40	201.77	176.55	156.93	141.24	128.40
1.8432000	6.784	1413.33	706.67	471.11	353.33	282.67	235.56	201.90	176.67	157.04	141.33	128.48
2.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
2.4576000	6.782976	1413.12	706.56	471.04	353.28	282.62	235.52	201.87	176.64	157.01	141.31	128.47
3.6864000	6.775005405	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
4.9152000	6.770938776	1410.61	705.31	470.20	352.65	282.12	235.10	201.52	176.33	156.73	141.06	128.24
5.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
5.0688000	6.783247059	1413.18	706.59	471.06	353.29	282.64	235.53	201.88	176.65	157.02	141.32	128.47
6.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
8.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
9.8300000	6.770663265	1410.55	705.28	470.18	352.64	282.11	235.09	201.51	176.32	156.73	141.06	128.23
10.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31
14.3181800	6.783613252	1413.25	706.63	471.08	353.31	282.65	235.54	201.89	176.66	157.03	141.33	128.48
16.0000000	6.775	1411.46	705.73	470.49	352.86	282.29	235.24	201.64	176.43	156.83	141.15	128.31

9.2 Appendix B: Crystal Oscillator – Configuration of Crystal Register

Crystal Oscillator Operation

A Pierce IC Oscillator, with external RC and XTAL, is used to provide a stable reference for the on-chip PLL. The on-chip portion of the oscillator consists of the inverter (to provide 180 degrees of phase shift for the closed-loop phase) with a digitally controlled variable drive output. The variable drive feature exists to allow the oscillator to be optimized to a wide variety of crystal load impedance and a wide variety of crystal resonant frequencies (32 kHz-16MHz). Because crystal drive requirements are different for different crystals (different manufacturer, packaging, or resonant frequency), there is not a specific setting for a specific crystal resonant frequency. This requires an empirical approach to optimizing the variable drive setting.

The crystal oscillator circuit has an Automatic Gain Control (AGC) that regulates the current drive (and applied voltage) to the crystal oscillator. Crystal drive regulation is necessary for optimum oscillator performance. Over-driving a crystal will cause distortion of the oscillator output signal. Under-driving a crystal may cause it to not

oscillate. The drive level required is different for different crystals. The AGC circuitry can be digitally tuned (via the SPI bus) to allow the application designer the ability to optimize oscillator drive for any particular application.

Refer to the "Crystal Oscillator: Simplified Functional Schematic" figure for the discussion on the AGC functions/control below.

Capacitor Divider

The crystal oscillator AGC has a capacitor divider that taps the oscillator inverter output. The capacitor divider ratio is programmable by the user through the XTHCG bit. A larger capacitor ratio (XTHCG="0") allows more signal attenuation if needed to prevent the AGC loop components from saturating. If the AGC loop components were allowed to saturate, then they would not be able to regulate the crystal drive.

Rectifier Circuit

The capacitor divider output voltage drives the NFET in the rectifier circuit. The NFET is driven in a semi-switching (large-signal analog) fashion. The NFET output is tied to a shunt RC and a current source. Both a large input signal and a smaller input signal are discussed to demonstrate the rectifier operation.

When the positive portion of a large signal appears at the input of the NFET, the NFET output will pull the rectifier circuit output very close to ground. This will cause the capacitor to mostly discharge and the current source to shunt most of its current to ground (rather than used to charge the capacitor). When the negative portion of a large signal appears at the input of the NFET, the NFET acts essentially like an open switch. This will cause the current source to slowly bias the capacitor. This discharge and charge cycle continues indefinitely while the crystal oscillator circuit is enabled.

When the positive and negative portions of a smaller signal appear at the input of the NFET, the same effects occur as for the large input signal. The difference is that during positive portions of the input signal, the NFET will pull the output only slightly toward ground. Thereby discharging the capacitor only slightly. During negative portions of the input signal, the current source will charge the capacitor at the same rate as for the large signal case. The difference is that the small signal case starts charging at a higher initial voltage (since the NFET did not discharge the capacitor as completely as it did for the large input signal case). The maximum capacitor charge level for the small signal case is, therefore, higher than that for the large signal case (because the small signal case charges for the same amount of time at the same rate, but starts the charging from a higher initial voltage level).

The maximum voltage achieved across the capacitor over any given input signal cycle depends on the fixed R and C components as well as the user programmable Ibias level. Ibias is controlled by the user through the XTBIAS[2:0] bits. Ibias controls the gm of the oscillator inverter in conjunction with the oscillator current

driver source mirror gain control (as will be shown later in this description). An increase in the XTBIAS[2:0] value causes an increase in the oscillator inverter gm. Ibias should be adjusted such that the crystal drive level allows stable oscillation, but the drive level should not be so high that the oscillation shows distortion.

LPF

This “half-wave rectified” signal is then low-pass filtered. The low-pass filtered signal is a quasi-static voltage level that is proportional to the oscillator amplitude.

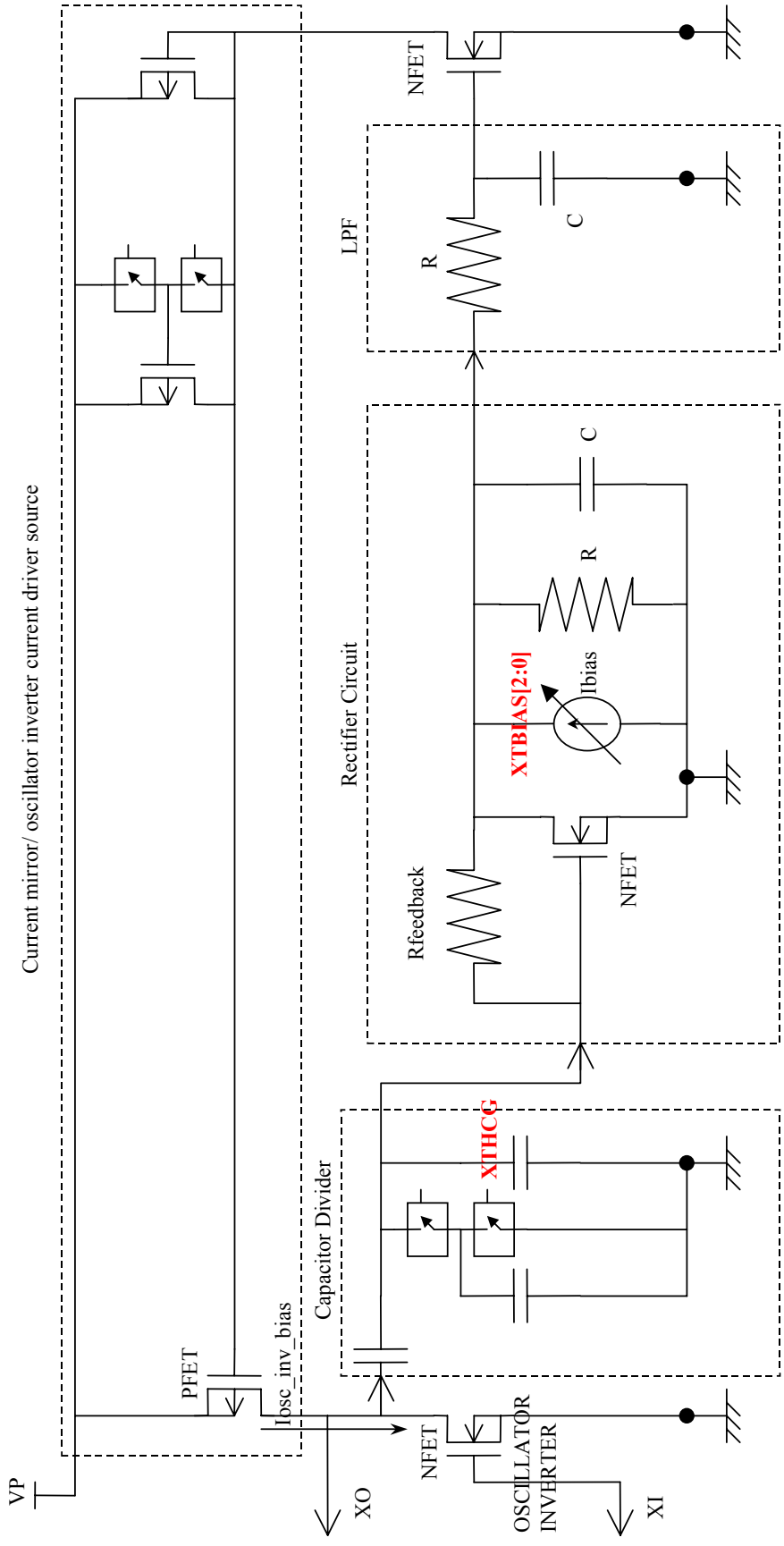
Current mirror/oscillator inverter current driver source

The current mirror circuit uses the output of the LPF output NFET as a current source. The current mirror gain is digitally programmable through the XTHMG bit. The current mirror gain can be reduced by switching in the extra current reference stages (by setting XTHMG=”0”). Reduction of current gain will directly reduce the bias current provided to the oscillator inverter. This, in turn, reduces the gain of the oscillator inverter.

Buffer (not shown on functional schematic)

The crystal oscillator circuit, as it is shown in the simplified functional schematic, is unbuffered. Any loads attached to the crystal resonator (across the XI and XO pins) would load the crystal oscillator. This loading would cause frequency shifts, distortion, and may even cause the oscillation to damp out (terminate). An on-chip buffer has been added across the XI and XO pins to provide an isolated oscillator source for the rest of the chip. The buffer consists of a high input impedance differential comparator with hysteresis and several stages of series-connected inverters. The current supply to the differential comparator is digitally programmable through the XTBFI[2:0] bits. Tuning the current supply will tune the oscillator output duty cycle.

Crystal Oscillator: Simplified Functional Schematic

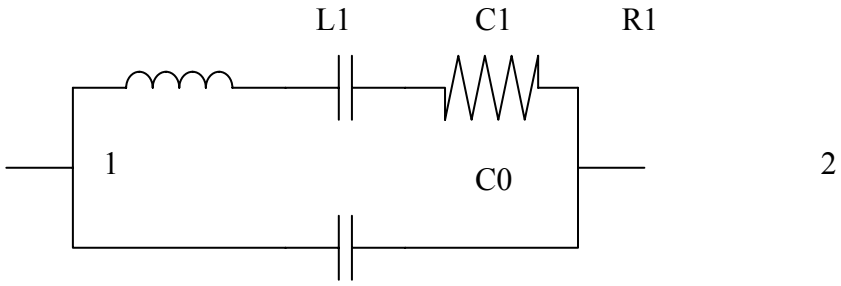


Procedure for optimizing the variable drive setting of the Pierce oscillator

1. Choose a setting from table of known settings, based on an extrapolation to the resonant frequency for the application.

CRYSTAL REGISTER (XT_REG[0:7]): RECOMMENDED CONTROL SETTINGS						
		Oscillation Frequency				
		32 kHz	100 kHz	1 MHz	10 MHz	16 MHz
Register	Familiar name					
XT_REG[2:0]	XTBIAS[2:0]	0	0	3	5	?
XT_REG[5:3]	XTBF[2:0]	0	0	0	1	?
XT_REG[6]	XTHMG	0	1	1	1	?
XT_REG[7]	XTHCG	1	1	1	1	?

2. Obtain the SPICE model for the crystal. The SPICE model parameters of interest include the electrical equivalent of the mechanical parameters of inertia, restoring force, and friction. Also of interest is the shunt capacitance between terminals and the sum of the electrode capacitance of the crystal and package capacitance. These parameters define the electrical equivalent circuit of the crystal.



L1 electrical equiv. (mechanical), inertia
C1 electrical equiv. (mechanical), restoring
R1 electrical equiv. (mechanical), friction
C0 terminal shunt capacitance, electrode capacitance, package capacitance

3. Attach the SPICE model for the crystal to the SPICE model for the on-chip inverter/crystal driver circuitry and perform the closed-loop simulation. SPICE ".TRAN" transient analysis will require a very long simulation time because the crystal Q (which is typically on the order of 10,000) causes a long start-up time. *As a practical alternative to transient analysis, DC analysis and gm curves should be analyzed for oscillator performance????(explain the simulation, output plots needed, and output plot interpretation for oscillator optimization: i.e. "what to simulate, what simulation outputs to look at, and what to do with the simulation outputs", Jim).* Empirically change the XT_REG register values to optimize the oscillation frequency and stability. Simulate frequency pulling and change the XTAL register values to minimize pulling effects.

There are several separate control vectors that may be used to tune the inverter/crystal driver circuitry. Their control names and descriptions follow:

XTBIAS[2:0] Controls (indirectly) gm of the crystal oscillator inverter. A crystal has a minimum and maximum drive requirement in order to establish and maintain stable oscillation. XTBIAS [2:0] should be adjusted such that the crystal drive level allows stable oscillation, but the drive level should not be so high that the oscillation shows distortion. Increasing XTBIAS[2:0] increases the crystal oscillator inverter gm, which increases the drive to the crystal.

XTBF[2:0] Controls the duty cycle of the oscillator buffer output. The duty cycle is controlled by tuning the buffer current supply through the XTBFI[2:0] bits. Increasing XTBF[2:0] increases the buffer current, which *??????* *(increases or decreases??, Jim?)* the crystal oscillator buffer output duty cycle. XTBF[2:0] should be kept as small as possible for low current draw.

XTHMG Controls current mirror gain of the crystal oscillator inverter bias source. This, in turn, controls the gm of the oscillator inverter. Use to set loop gain for stability. Tune to eliminate unintentional FM or AM modulation of the oscillator. Tune to encourage start-up of oscillation if oscillator is over-damped. XTHMG="0" sets current mirror gain to "low" setting. XTHMG="1" sets current mirror gain to "high" setting.

XTHCG Controls capacitor divide ratio for capacitor tap of the oscillator AGC loop. Use to prevent the AGC loop components from saturating (from too much capacitor gain) and causing loss of oscillator signal regulation. Used to improve stability. Tune to reduce frequency-pulling effects. Use to tune oscillation frequency. Tune to increase feedback to crystal. XTHCG="0" sets capacitor divide ratio to "low gain" setting. XTHCG="1" sets capacitor divide ratio to "high gain" setting.

4. After performing a SPICE optimization, enter the XT_REG[7:0] register values from SPICE into the actual chip through the SPI bus. Measure the start-up characteristics, oscillation amplitude and stability characteristics, and current draw of the oscillator. Use the same register controls that were used in SPICE to optimize the actual crystal oscillator. All XT_REG[7:0] register changes to the real chip must be done through the SPI bus.

9.3 Appendix C: PLL Loop Filter Design, with consideration for 1/f noise reduction

When designing of the PLL filter, it is necessary to consider the effects of reference frequency multiplication on overall PLL noise level. For purposes of the Grow PLL, the estimated oscillator phase noise floor at the phase detector comparison frequency (reference frequency) is ~-120dBm/Hz. This can be used to determine the minimum noise shelf of the PLL as given by Eq. 9.1.1.

$$P_{noise} = 6 + 20 * \log[N] + P_{reference} \text{ (dBm/Hz)} \qquad (9.1.1)$$

where N= (carrier frequency)/(reference frequency)
= carrier frequency divider ratio in PLL counter

By noise shelf, we mean the minimum noise level of the PLL inside the PLL loop filter bandwidth. This is shown in Figure 9.1.1.

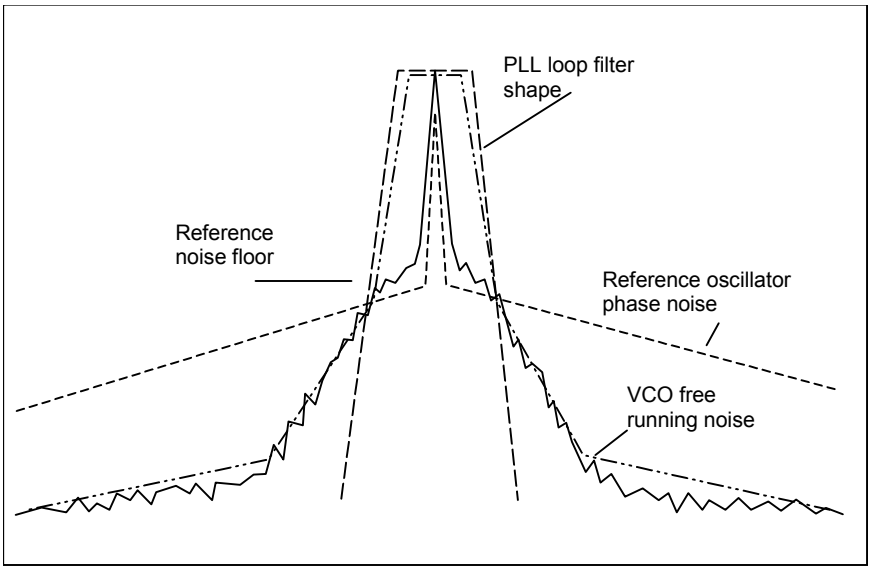


Figure 9.1.1. PLL phase noise spectrum and the origin of various components of the noise spectrum.

Figure 9.1.1 shows the spectrum of a typical PLL. In the case of the Grow PLL, the VCO free running noise has a strong 1/f component and the noise rises more near the carrier than it would with a lower noise VCO. However, the PLL is able to largely track out the VCO free running noise within the loop filter bandwidth.

As the loop bandwidth narrows, the free running noise rises higher than the noise floor from the reference as shown in Figure 9.1.2. As a practical matter, for very narrow loop bandwidths, the apparent noise floor of the PLL increases to the top of the noise peaks at the edges of the loop bandwidth as it becomes a practical impossibility to separate the carrier from the noise sidebands at the edge of the loop bandwidth.

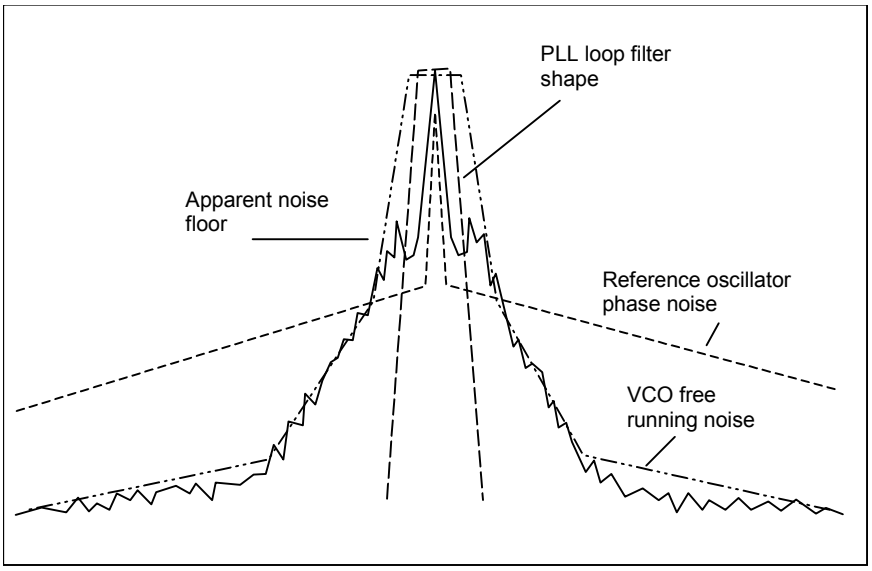


Figure 9.1.2. PLL phase noise spectrum and the origin of various components of the noise spectrum at reduced loop bandwidth.

For FM signals, one would ideally wish to minimize the contribution of the PLL noise to the detector output noise. Generally speaking, this can be accomplished with a PLL noise shelf about 10 to 15dB lower than the SNR required for demodulation at a given bit error rate. For example, if we require a SNR of 12dB to achieve a bit error rate of 10^{-4} a PLL noise floor of –22dBc for the transmitter PLL would negligibly degrade the performance of the system. If the receiver has a similar PLL noise floor, the root-sum-square of the PLL noise from the transmitter and receiver will result in an equivalent noise floor 8.5dB lower than the minimum required SNR of 12dB for an overall SNR due to PLL noise of –20.5dB. This is far below the required SNR, but the effect on bit error rate may no longer be entirely negligible.

For purposes of this example, if the multiplied up reference noise results in a reference noise floor higher than –22dBc, there is no choice but to increase the reference frequency so as to lower the multiplication factor, N. This can cause great inconvenience in selecting main and reference divider values that result in carriers on or very near the desired channel frequency, but failure to do so will result in inadequate SNR at the demodulator output and consequently, higher bit error rates.

Selecting a loop bandwidth also requires compromises. The PLL loop bandwidth must be sufficiently narrow as to provide adequate rejection of the reference oscillator phase noise, yet it must also be wide enough to allow the VCO free running noise to be tracked out. The optimum bandwidth of the PLL loop filter occurs where the free running VCO noise and the reference oscillator phase noise are the same. Increasing the loop bandwidth beyond this only degrades the PLL SNR as the wider filter bandwidth allows more reference oscillator phase noise into the loop. A narrower loop filter can also degrade the PLL SNR, as the PLL will be unable to track out the VCO free running noise outside the loop bandwidth. Thus, PLL noise

will increase outside the loop bandwidth but may still be within the receiver passband and thereby contribute to degraded SNR in the receiver. Also requiring consideration is the application's maximum worst case channel switch time. The loop filter bandwidth must be wide enough to allow for the VCO tune voltage transient upon a programmable divider change (initiated by the application via the SPI interface) to settle out to an acceptably low center frequency error before the VCO is considered to be "on frequency".

A third consideration occurs when one attempts to FM modulate the PLL. FM modulation perturbs the PLL and the loop attempts to track it out as soon as it can. The common rule of thumb is that the loop filter must be at least 10 times narrower than the minimum modulating frequency. Experimentally, it has been determined that this ratio of loop bandwidth to signal frequency works adequately for sinusoidal modulation and is less than ideal for binary modulation as the PLL can introduce considerable tilt to the modulation. An example is shown in Figure 9.1.3.

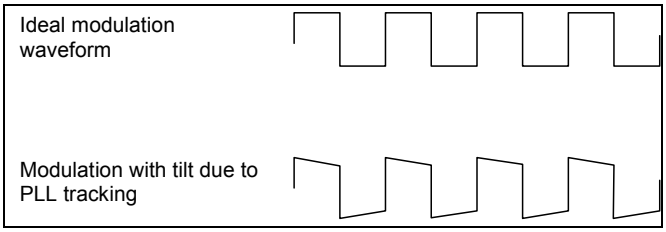


Figure 9.1.3. Ideal binary FM and modulation with tilt due to the PLL attempting to track out the modulation.

The tilt on the modulation can be thought of as reducing the SNR of the detected waveform or closing the eye pattern. In either case, the result is reduced data integrity. Tilt is reduced to an acceptable level (< 10%) when the loop filter is between 15 and 20 times narrower than the lowest modulating frequency. Loop filters as narrow as $1/20^{th}$ the lowest modulating frequency tend to have higher noise as the VCO noise at the edges of the loop filter is higher than the reference frequency noise. This, in turn, degrades the SNR of the detected signal.

In order to improve the performance of a receiver-transmitter pair, it may be optimal to have unmatched receiver and transmitter PLL noise characteristics. The transmitter loop filter can be narrower and suffer a slightly higher effective noise floor in order to improve the modulated signal characteristics while the receiver loop filter bandwidth can be wider and have a lower noise floor so that the receiver VCO noise contribution to the demodulated signal is reduced.

The characteristics of the loop filter can be altered by changing the charge pump current. Higher currents result in wider loop filters. In the Grow chip, the charge pump currents can be digitally controlled through the SPI bus to 100uA or 1mA (a factor of 10) via the "Charge Pump Select" register bit toggle. A loop filter designed for optimum performance at low charge pump currents will degrade significantly at high charge pump gains and may actually become unstable.

The key to designing a loop filter that is stable at both low and high charge pump gains is to design to the geometric mean of the charge pump current and the geometric mean of the loop filter bandwidth. For example, if we wanted a 300Hz loop filter for transmit and a 3kHz loop filter for receive, we would design for a loop filter bandwidth of

$$BW_{loop} = \sqrt{BW_{low} * BW_{high}} \qquad (9.1.2)$$

or, 948 Hz. Similarly, we would design to the geometric mean of the charge pump currents. That is,

$$I_{cp} = \sqrt{I_{high} * I_{low}} \qquad (9.1.3)$$

which, for 100μA and 1mA currents becomes 0.316mA. If we assume operation with a 100.3kHz reference frequency and a 435.2MHz operating frequency, we have an N-divider value of 4340 (use "pll_rfgorw3.xls" Excel spreadsheet and "Appendix A: PLL Frequency and Data Rate Register Tables" from this document for easy selection of achievable reference frequency and resultant N-divider). We now have almost everything needed to design the loop filter, except the phase margin of the loop. The optimized phase margin function for a 2nd order loop filter is nearly parabolic about the design frequency on a log frequency scale. Above and below the design frequency, the phase margin falls off. The amount of this fall off at frequencies ~3X above and below the design frequency is ~10°. Thus, a design phase margin of 70° results in ~60° of phase margin when the filter design is analyzed at charge pump currents of 100μA and 1mA. To determining specific values of the loop filter, we need the VCO gain (tune sensitivity) in MHz/V. For this example, we will use 9 MHz/Volt which happens to be the VCO gain of the obsolete second pass RFGROW ASIC. The results are shown in Figure 9.1.4.

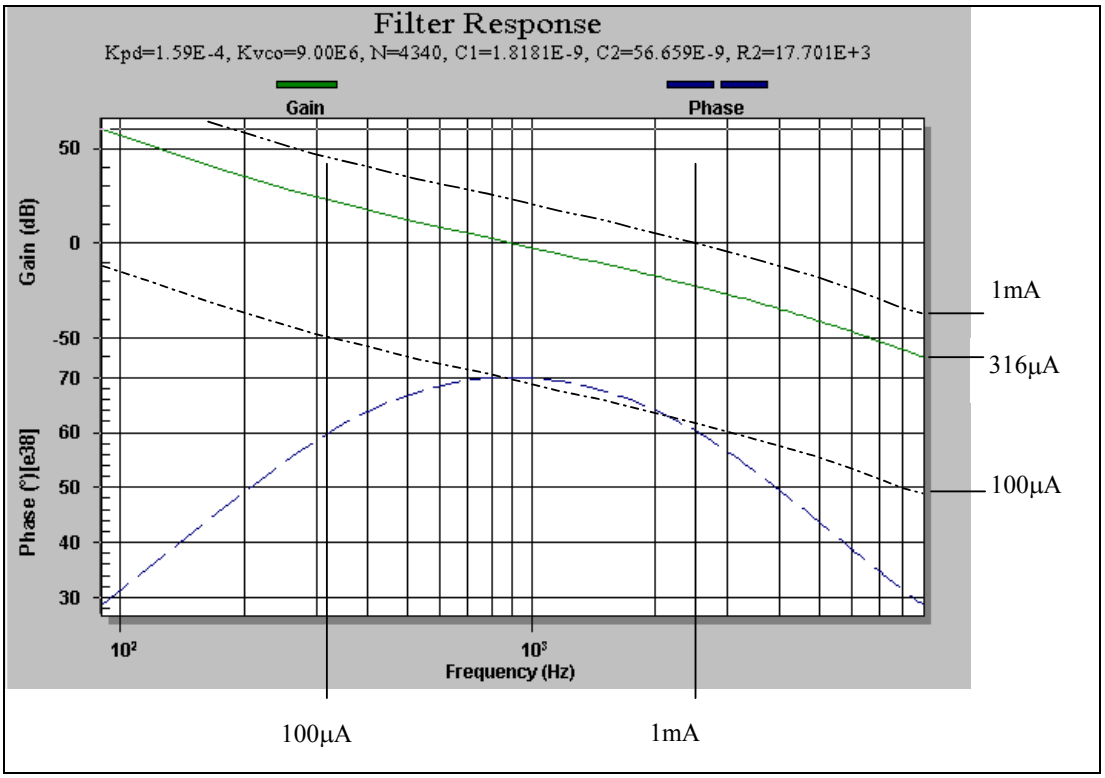


Figure 9.1.4. 2nd order PLL loop filter design. Bandwidth and phase margin at 100µA and 1mA are determined from separate simulations run at these currents and the 0dB gain crossover point.

At this point, the loop filter design may also be analyzed using actual component values. Overall, the design of the filter is now complete.

9.4 Appendix E: PLL Loop Filter Data Injection Pre-emphasis Filtering for Low Data Rates

One of the issues brought up in section 9.1 was the effect of loop bandwidth on the modulated waveform. In particular, the problem of low modulating frequencies forcing narrow PLL loop filter bandwidths can result in loop filters so narrow that the VCO free running noise is higher than the reference frequency noise. The result is an apparent increase in the noise floor of the PLL and consequent degradation of the SNR of the transmitted or received signal. Some relief from this limitation can be achieved by pre-emphasizing the modulating signal.

Determining a pre-emphasis network begins with determining the minimum acceptable SNR of the transmitted signal consistent with the system bit error rate. Assume a bit error rate of 10^{-5}. The required SNR for binary FSK is ~13dB. Given the VCO free running noise, assume the loop filter bandwidth set to the point where the free running noise and the reference noise match. If this bandwidth is wider than ~$1/10^{th}$ the minimum modulating frequency, it may not be possible to compensate PLL track-out of the modulating signal with this filter. In this case, one would be forced to set the loop filter bandwidth to $1/10^{th}$ the minimum modulating frequency.

At this point, it is necessary to determine if the resulting PLL SNR is adequate to support the required bit error rate. The composite curve of VCO free running noise and reference frequency noise can be integrated over the receiver bandwidth to determine if there is adequate SNR in the transmitted signal. In general, the required SNR will be higher than the minimum SNR for a given bit error rate so as to allow some degradation due to receiver phase noise. If sufficient SNR is not available, the reference frequency may have to be increased, the loop filter bandwidth may have to be relaxed, or a quieter VCO may be required.

For purposes of the discussion, we will assume that we can achieve the required transmit SNR. The effect of the PLL on the modulation can be modeled using a non-linear simulation tool, such as SPICE. A sample SPICE PLL model is shown in Figure 9.2.1.

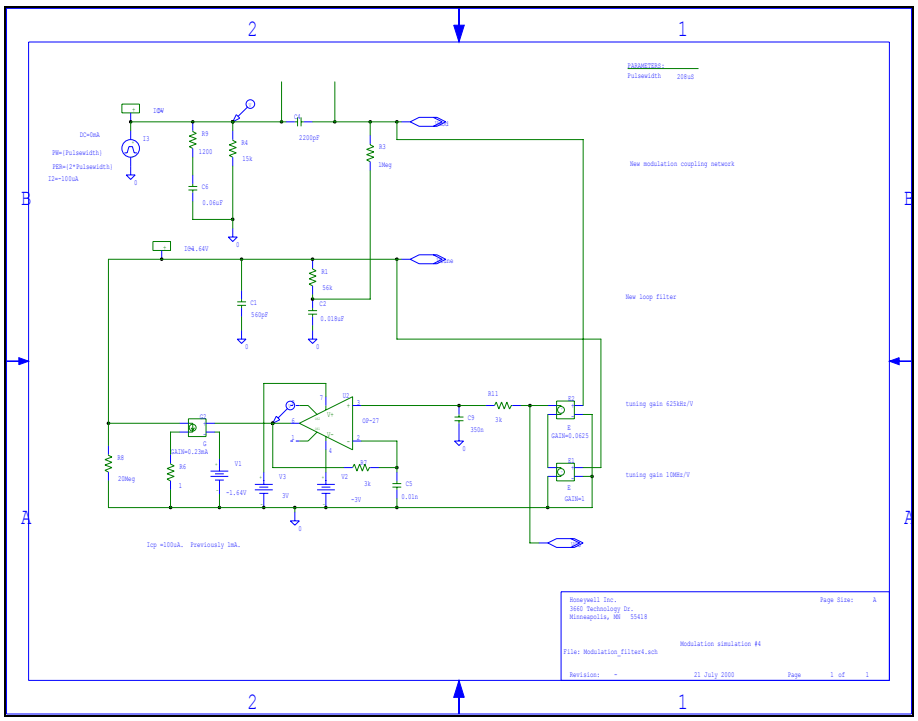


Figure 9.2.1. Pspice schematic of PLL simulation.

In the course of modeling the PLL, it was easier to simulate the limited excursion of the charge pump output by using a real op-amp followed by a voltage to current converter. The PLL gain is set by

$$A_{PLL} = \frac{K_{PD}(radians) * K_{VCO}(Volts/MHZ) * 2\pi}{N}$$

where K_{PD} is the phase detector gain, K_{VCO} is the VCO gain, and N is the main divider value at the operating frequency. For the RF GROW ASIC, K_{PD} = 0.159mA (1mA/(2*pi)) for "Charge Pump Select"=1 and K_{PD} = 0.0159mA (100uA/(2*pi)) for "Charge Pump Select"=0. For K_{PDA} = 0.0159mA, K_{VCO} = 10MHz/V, and N = 4340, the PLL loop gain is 0.23 . This is the number associated with the voltage-to-current converter in the schematic. The R-C network R7/C5 is effectively out of circuit (R7/C5 can be removed and replaced with a short across R7 and an open for C5). The R-C network R11/C9 was determined experimentally to model the transportation lag through the man divider and the VCO V_{tune} response. The two voltage controlled voltage sources represent the normalized VCO gain and normalized VCO modulation input.

The loop filter values were calculated using the method described in Sect. 9.1 using National Semiconductor's PLL loader software (the user can obtain a copy of the software from www.national.com. The older version is more straight-forward and has less software bugs: the primary bug is the user must enter Icp/(2*pi) rather than intended Icp before hitting calculate). Note that the bias for the modulation input is connected to the pole-zero compensation capacitor. This was done because this node is better decoupled from the instantaneous variations of the VCO V_{tune} line than would be a direct connection to the filter output.

The modulation network R9/C6 is the actual pre-emphasis network. R4 is necessary to establish a DC operating point for this network. The network actually functions almost identically for R4 values from 15k to as high as 100K. The values for R9/C6 were determined experimentally for best modulation waveshape. The loop filter is a two-pole network and the uncompensated modulation has some ringing-up before decaying that is typically of this type of network. The single pole compensation network does not have this ringing and the result is some overshoot of the modulation waveform. R9 predominantly determines deviation and C6 determines the slope of the compensation.

For the loop modeled in Figure 9.2.1, the resulting compensation modulation is shown in Figure 9.2.2.

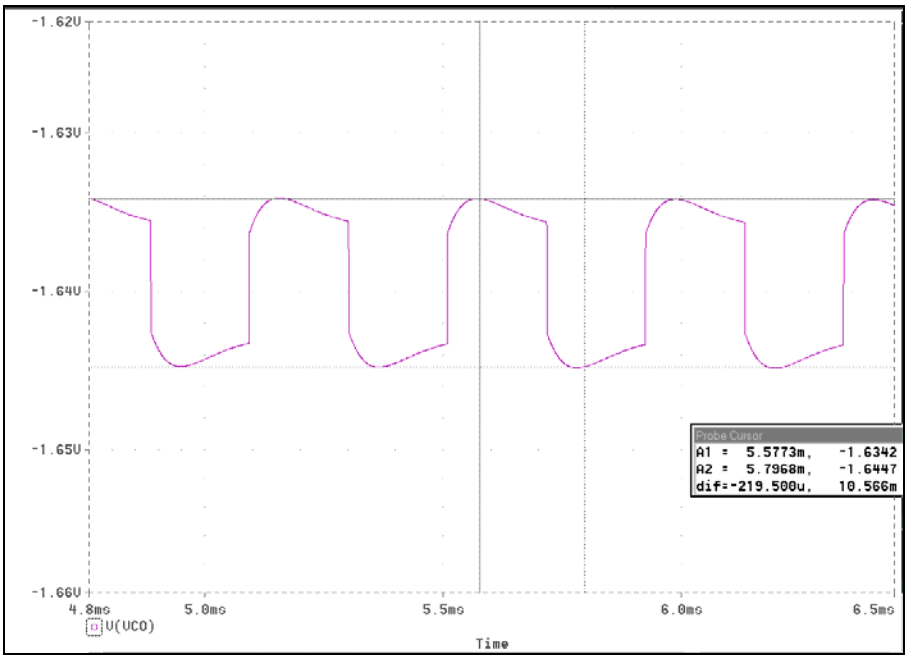


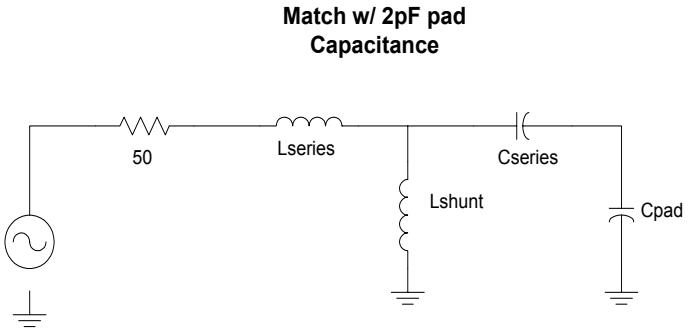
Figure 9.2.2. Plot of VCO V_{tune} output using single pole compensated modulation .

Note that the modulation is not flat. The peaks represent ~106kHz peak-to-peak deviation while the ends of the peaks are 77kHz p-p deviation. The average peak-to-peak deviation is ~90kHz for an average deviation of 45kHz. This is quite close to the target deviation of 43kHz and the overshoot and droop are within acceptable limits.

9.5 Appendix F: LNA Front End Matching Networks

LNA IMPEDANCE MATCHES
FOR 915MHz, 868MHz, and 434MHz

1. Match for 915MHz



Zin= 29.82-56.2j
Zin(nor)=.5964-1.12j

$$Lseries = \frac{X * 50}{w} = 11.5nH$$

$$Lshunt = \frac{50}{w * B} = 39nH$$

$$Cseries = 100\,pF$$
$$Cpad = 2\,pF$$

2. Match for 868MHz

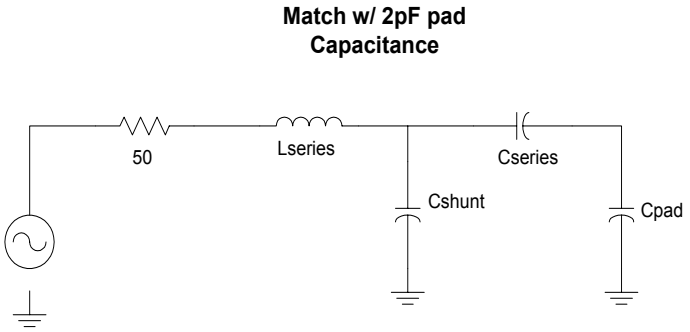
Zin= 31.5-56.5j
Zin(nor)=.63-1.13j

$$Lseries = \frac{X * 50}{w} = 12nH$$

$$Lshunt = \frac{50}{w * B} = 49nH$$

$$Cseries = 100\,pF$$
$$Cpad = 2\,pF$$

3. Match for 434MHz



Zin= 69.8-71.8j
Zin(nor)=1.396-1.436j

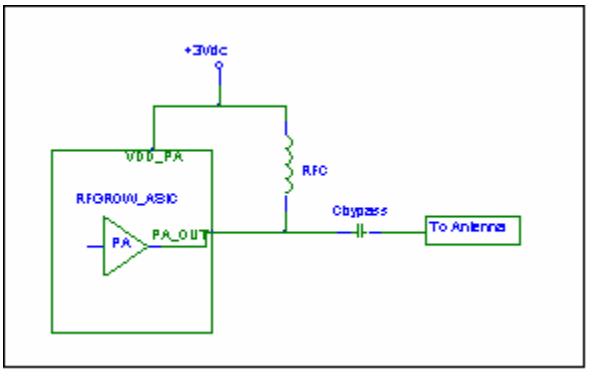
$$Lseries = \frac{X * 50}{w} = 26nH$$

$$Cshunt = \frac{B}{w * 50} = .74pF$$

$$Cseries = 100pF$$
$$Cpad = 2pF$$

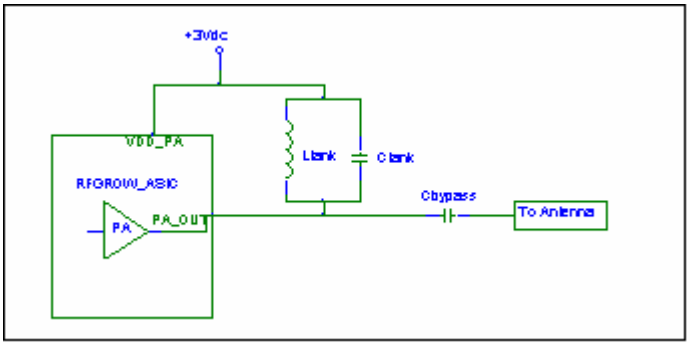
9.6 Appendix G: PA Output Bias, Matching, and Harmonic Suppression Filtering

For minimum external parts count (and minimum external parts cost), one can simply provide an external RF choke and series dc blocking capacitor. This architecture is shown below:

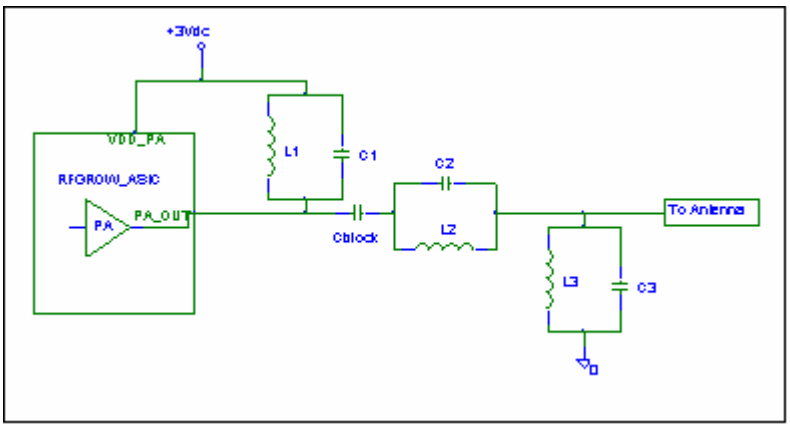


For nominal second harmonic suppression, the external parts count can be extended to include a capacitor as part of a shunt LC tank. The extra benefit of this is that Ltank may be smaller than

the RF choke of above – as long as it resonates with Ctank at the intended carrier frequency. This architecture is shown below:



For extra second harmonic suppression, the external parts count can be extended to include a series and a shunt LC trap. This may be excessive; the lesser parts count options above should be investigated first before committing to the greater parts count shown here. This architecture is shown below:



9.7 Appendix H: ASIC Digital to ASIC Analog Interface

9.7.1 Digital to VCO Off-chip Interface

Once the digital section begins transmission of the data, it must be filtered and input to the VCO. The digital section drives the data off-chip to the external filter on either the TX_DATA_V port (voltage output, pin 26) or the TX_DATA_I port (current output, pin 14) to one of the VCO's VMOD input ports (typically VMOD1) to FM modulate the transmitted carrier generated by the VCO. The VCO then sends the FM modulated carrier to the PA which sources energy to the antenna for radiating.

The TX_DATA_V port is a direct voltage output of the encoded serial data for transmission. TX_DATA_V can be externally connected to the VMOD1 input port (pin 11) for narrowband FM modulation or VMOD2 (pin 10) input port for wideband FM modulation, with a resistive divider used for voltage division prior to the chosen VMOD port.

The TX_DATA_I port is a current-mode version of the TX_DATA_V port. The internal encoded serial data signal that is connected to the TX_DATA_V port is also routed to an internal buffer and charge-pump, where it is converted from a voltage signal to a current-mode signal. The charge pump push/pull value of TX_DATA_I is set to 100uA. TX_DATA_I can be externally connected to the VMOD1 input port or the VMOD2 input port of the VCO, just like would be done with TX_DATA, except that a voltage-to-current converting resistor and ac coupling capacitor (or use a capacitive divider) would be used instead of a resistive divider prior to the chosen VMOD port. Note that if using an ac coupling capacitor, the VMOD port will need linear mid-range tune biasing supplied from elsewhere. The linear region is shown on the VCO tuning plot in the Phase Lock Loop and VCO section of the Transceiver ASIC Functional Description section. It is recommended that the PLL filtered VCO tune voltage be used as the basis of bias for the modulation VMOD port, since the phase-locked tune voltage level is usually in the middle of the linear tune range of VMOD1 and VMOD2 and has excellent power supply rejection.

A connection shall not simultaneously be made from both the TX_DATA_V port and the TX_DATA_I port to the VMOD pins. The applications engineer must decide whether a voltage-based or current-based modulation source is desired, and then connect the proper transmission data port to the chosen VMOD. The current-based modulation method would have the least change in FM peak frequency deviation over changes in supply voltage because the current output is based off an internal bandgap reference with excellent power supply rejection where-as the voltage output has almost no power supply rejection.

The applications engineer must decide which VMOD input port to select depending on the peak frequency deviation required for the application's FM modulated signal. VMOD1 typically has more than enough tune sensitivity to handle reasonable peak frequency deviations required to FM modulate a signal within the 100kHz baseband filter bandwidth.

9.7.2 RX Demodulator to Digital Interface .

The analog demodulator output is internally routed to the digital serial receiver via two MUX's. The first MUX determines the polarity of the data going to the digital receiver This MUX is controlled by the Demod Data Polarity bit (0 selects normal polarity, 1 selects inverted polarity) of the Demodulator Register. Note that both analog demodulator polarities are available external to the chip as well (pins 24 and 25, for the 64 pin configuration). The second MUX determines whether to use the internal analog demodulator output as the data source or to use external data (from DIG_DATA_IN, pin 32 for the 64 pin configuration) for the digital serial receiver input. This MUX is controlled by the Demod Output Select bit (0 selects internal analog demodulator output data, 1 selects external data from DIG_DATA_IN) of the Demodulator Register. This is how the analog receiver data is input to the receiver section of the digital circuitry. The digital will then detect and validate the data and transfer it into the FIFO for use by the application via the SPI interface.