Datasheet

Vela IF820

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	10 Oct 2023	Initial release	Li Yuan Chang Mark Duncombe Rikki Horrigan Ryan Erickson	Jonathan Kaye

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TABLES

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1 SCOPE

This document describes the key hardware aspects of the Laird Connectivity Vela IF820 Series wireless modules providing high-speed 4-wire UART interface for Bluetooth® / Bluetooth® LE connections. This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from several sources and includes information found in the Infineon CYW20820 data sheet issued on September 26, 2022 along with other documents provided by Infineon.

Note: **The information in this document is subject to change.** Please contact Laird Connectivity to obtain the most recent version of this document.

2 GENERAL DESCRIPTION

Ensure your estate of Classic Bluetooth devices don't get left behind in a growing environment of Bluetooth LE-only wireless options. Our Vela IF820 series being dual mode allows a single module to cover legacy Classic Bluetooth and migration to Bluetooth LE with a single part. This innovative series is based on **Infineon Technologies AIROC™ CYW20820** silicon. This range of flexible modules, adapters and DVKs marries all the benefits of the CYW20820 hardware, software, and tools offerings with our added value application software, services, certification, and support capabilities. The Vela IF820 series provides OEMs with multiple software development options suited to their resources and skillsets, with close attention to providing forward-looking replacement products for some of Laird Connectivity's legacy Bluetooth product portfolio.

The Vela IF820 includes multiple small form factor PCB modules to suit any host board footprint and targets both hosted and hostless applications. They're accompanied by low cost, easy to use development kits and the addition of a certified, packaged USB Adapter to add Classic Bluetooth and Bluetooth LE connectivity to a variety of additional products in your Bluetooth portfolio. Together, Infineon and Laird Connectivity drive down your total cost of ownership, design complexity and risk, while ensuring you the fastest time to market for your next dual mode Bluetooth IoT design.

Table 1: Product ordering information

Part	Description
453-00171R	Vela IF820 - Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) - Tape / Reel
453-00171C	Vela IF820 - Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) – Cut / Tape
453-00172R	Vela IF820 - Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) - Tape / Reel
453-00172C	Vela IF820 - Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) – Cut / Tape
453-00171-K1	Vela IF820 - Development Kit with integrated chip antenna
453-00172-K1	Vela IF820 - Development Kit with MHF4 Connector
450-00185	Vela IF820 - Dual Mode Bluetooth USB Adapter with integrated antenna variant (Infineon CYW20820)

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3 FEATURES SUMMARY

The Laird Connectivity Vela IF820 series device features are described in Table 2.

Table 2: Vela IF820 series wireless module features

Feature	Description
Variants	▪ Integrated antenna variant ▪ MHF4 connector variant ▪ USB Adapter
Bluetooth subsystem	▪ Complies with Bluetooth® core specification version 5.4 ▪ Includes support for basic data rate (BR), EDR 2 Mbps and 3 Mbps, extended synchronous connection-oriented ▪ Bluetooth® LE 1MPHY & 2 MPMY. ▪ Up to 10dBm EIRP output power ▪ Excellent receiver sensitivity (-94dBm for Bluetooth® LE 1 Mbps)
Microcontroller (MCU)	▪ Powerful Arm® Cortex®-M4 core with a maximum speed of 96 MHz ▪ Bluetooth® stack in ROM allowing standalone operation without any external MCU ▪ 256-KB on-chip flash ▪ 176-KB on-chip RAM Bluetooth® stack, peripheral drivers, security functions built into ROM (1 MB) allowing application to efficiently use on-chip flash ▪ AES-128 and true random number generator (TRNG) ▪ Security functions in ROM including elliptic curve digital signature algorithm (ECDSA) signature verification ▪ Over-the-air (OTA) firmware updates
Peripherals	▪ Up to 22 GPIOs ▪ I2C, I2S, UART, and PCM interfaces ▪ Two Quad-SPI interfaces ▪ Auxiliary ADC with up to 28 analog channels ▪ Programmable key scan 20 ´ 8 matrix ▪ Three-axis quadrature signal decoder ▪ General-purpose timers and pulse width modulation (PWM) ▪ Real-time clock (RTC) and watchdog timer (WDT) ▪
Power management	▪ On-chip power-on reset (POR) ▪ Integrated buck (DC-DC) and low drop out (LDO) regulators ▪ On-chip software controlled power management unit ▪ On-chip 32 kHz low power oscillator (LPO) with optional external 32 kHz crystal oscillator support

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4 SPECIFICATIONS

Table 3: Vela IF820 Specifications

Feature		Description
Physical Interface		54-pin LGA package for integrated antenna variant 44-pin LGA package for MHF4 connector variant
Bluetooth/BLE Interface		Host Controller Interface (HCI) using high speed UART
Main Chip		Infineon CYW20820
Input Voltage Requirements		3V Typ, 2.6V Min, 3.3V Max
I/O Signalling Voltage		Set to 3V or 1.8V, by the power domains connected to VDDIO
Operating Temperature		-40° to +85°C (-40° to +185°F)
Operating Humidity		Less than 85% RH (non-condensing)
Storage Temperature		-40° to +85°C (-40° to +185°F)
Storage Humidity		Less than 60% RH (non-condensing)
MSL (Moisture Sensitivity Level)		4 (module) N/A (USB Adapter)
Maximum Electrostatic Discharge		4kV Indirect application (In compliance with EN 301489)
Size – mm		Integrated Antenna variant: 9.3mm x 12.5mm x 2.15 mm MHF4 Connector variant: 7.5mm x 7.5mm x 2.15 mm USB Adapter: 18.39mm x 50.74mm x 11mm
Weight – g (oz.)		0.0003g (Integrated Antenna) 0.0001g (MHF4)
Bluetooth Media		Frequency Hopping Spread Spectrum (FHSS)
Bluetooth Standards		Bluetooth 5.4
Bluetooth Data Rates Supported		1, 2, 3 Mbps
Bluetooth Modulation	GFSK@ 1 Mbps Pi/4-DQPSK@ 2 Mbps (EDR)	8-DPSK@ 3 Mbps (EDR) BLE 1 Mbps, 2Mbps
Regulatory Certifications		FCC, IC, CE, UKCA, RCM, Japan, and Korea, Bluetooth SIG

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Compliance	**ACMA** AS/NZS 2772.2:2016 Amd 1:2018 AS/NZS 4268:2017+Amd 1:2021 **CE** EN 62479:2010 EN 50663:2017 EN 300 328 V2.2.2 EN 62368-1 **EMC** ICES-003 Issue 7, Class B EN 301 489-1 V2.2.3 EN 301 489-17 V3.2.4	**FCC** FCC Part 15, Subpart B, ClassB 47 CFR FCC Part 2.1091 47 CFR FCC Part 15.247 **Japan** Article 2 Paragraph 1 Item 19 **Korea** TBD
Certifications	***Bluetooth*® SIG Qualification**	
Warranty	One Year Warranty	

All specifications are subject to change without notice

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5 BLOCK DIAGRAM

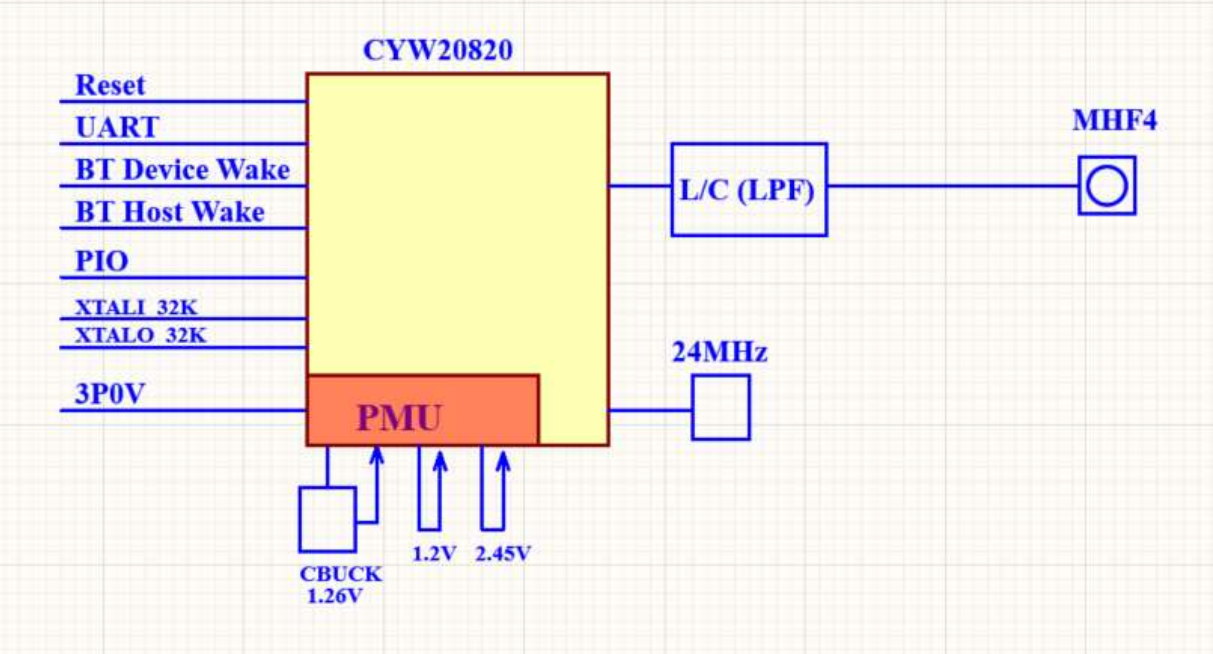

Figure 1: MHF4 connector variant diagram

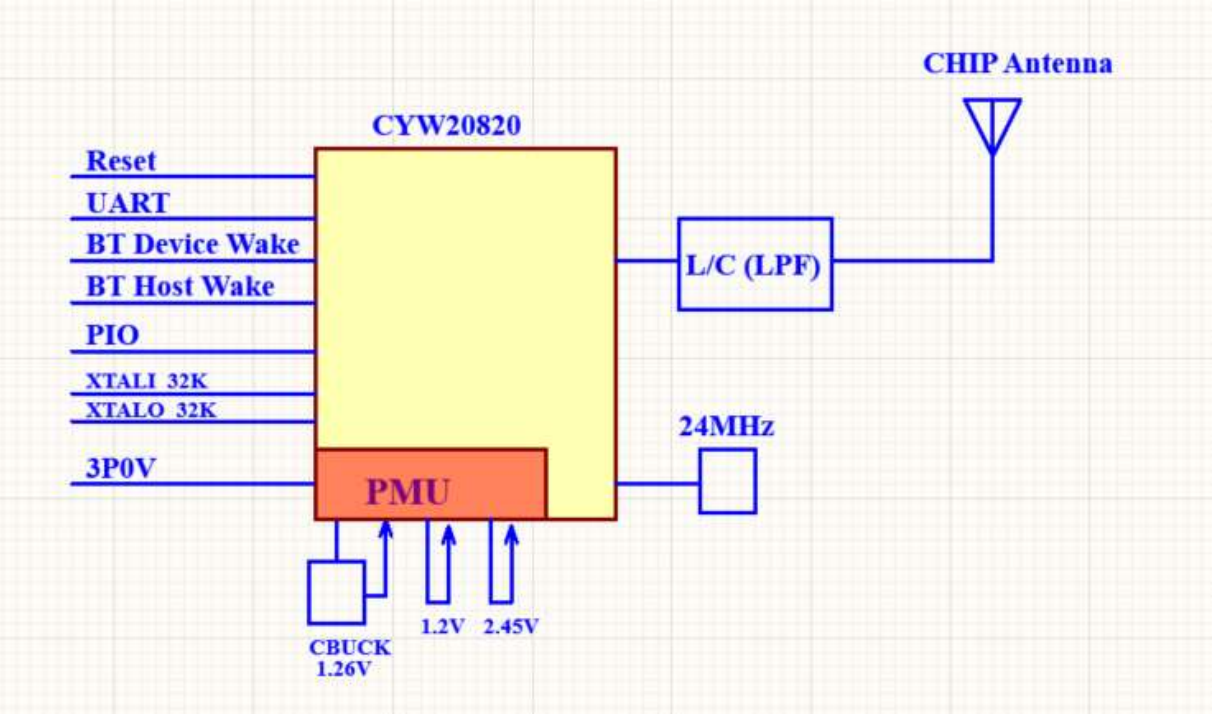

Figure 2: Integrated antenna variant diagram.

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6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 4 summarizes the absolute maximum ratings and Table 5 lists the recommended operating conditions for the Vela IF820 series wireless module. Absolute maximum ratings are those values beyond which damage to the device can occur. Operating this device outside of the listed maximum ratings and operating conditions may damage the device and void the warranty.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 4: Absolute maximum ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3P0V	Power supply for Internal Regulators	-0.5		3.45	V
VDDIO	DC supply voltage for digital I/O	-0.5		3.45	V

6.2 Recommended Operating Conditions

Table 5: Recommended operating conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
3P0V	Power supply for Internal Regulators	2.6	3.0	3.3	V
VDDIO	DC supply voltage for digital I/O	1.71	1.8/3.0	3.3	V
T-ambient	Ambient temperature	-40	25	85	°C

6.3 General DC Electrical Characteristics

Table 6 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 6: General DC electrical characteristics (For 1.8V or 3V operation VIO)

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input low voltage (VDDIO = 3V)	—	—	0.8	V
VIH	Input high voltage (VDDIO = 3V)	2.4	—	—	
VIL	Input low voltage (VDDIO = 1.8V)	—	—	0.4	
VIH	Input high voltage (VDDIO = 1.8V)	1.4	—	—	
VOL	output low voltage	—	—	0.4	
VOH	output high voltage	VDDIO-0.4V	—	—	
IIL	input low current	—	—	1	uA
IIH	input high current	—	—	1	
IOL	output low current (VDDIO = 3V, VOL = 0.4V)	—	—	4	mA
IOL	output low current (VDDIO = 3V, VOL = 1.8V)	—	—	2	
IOH	output high current (VDDIO = 3V, VOH = 2.6V)	—	—	8	
IOH	output high current (VDDIO = 1.8V, VOH = 1.4V)	—	—	4	
CIN	Input capacitance	—	—	0.4	pF

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7 RF CHARACTERISTICS

7.1 Bluetooth Radio Characteristics

Table 7 through 錯誤! 找不到參照來源。 describe the Bluetooth Basic Rate (BR) / BLE transmitter performance, Basic Rate (BR) / BLE receiver performance, Enhanced Data Rate (EDR) receiver performance, and current consumption conditions at 25°C.

Table 7: Basic Rate (BR) transmitter performance temperature at 25°C (3V)

Test Parameter		Min	Typ	Max	BT Spec.	Unit
RF Output Power[4] (test at MHF4 connector)	BR	—	6	7.5	0 ~ +20	dBm
	EDR 2M	—	1.5	2.5		
	EDR 3M	—	0.5	1.5		
Max EIRP (Integrated antenna variant)				10		dBm
Frequency Range		2.4	—	2.480	2.4 ≤ f ≤ 2.480	GHz

Table 8: Basic Rate (BR) receiver performance at (3V)

Test Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Sensitivity (1DH5)	BER ≤ 0.1%	—	-90	-87	≤ -70	dBm
Maximum Input	BER ≤ 0.1%	—	—	-20	≥ -20	dBm

Table 9: Enhanced Data Rate (EDR) receiver performance (3V)

Test Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Sensitivity (BER ≤ 0.01%)	π/4-DQPSK	—	-92.5	-89.5	≤ -70	dBm
	8-DPSK	—	-86	-83	≤ -70	dBm

Table 10: Bluetooth LE RF Specifications (3V)

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	—	2402	—	2480	MHz
Rx sensitivity[3]	GFSK, 30.8% PER, 1Mbps	—	-94	-91	dBm
	GFSK, 30.8% PER, 2Mbps	—	-90	-87	dBm
RF Output Power[4] (test at MHF4 connector)	1M	—	6	7.5	dBm
	2M		6	7.5	dBm
Max EIRP (Integrated antenna variant)				10	dBm

Note[3]: Dirty TX is Off.

Note[4]: The Bluetooth LE TX power cannot exceed 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.

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7.2 Bluetooth Current Consumption

Table 11: Bluetooth current consumption, VBAT=3V VDDIO=3V, MHF4 connector variant

Operating Mode	Data Rate	Module 3V	Unit
TX	DH1	13.5	mA
	DH3	13.5	
	DH5	13.5	
	2DH1	20.2	
	2DH3	20	
	2DH5	20.1	
	3DH1	19.8	
	3DH3	20	
	3DH5	20.1	
	LE1M	13.3	
	LE2M	13.3	
RX	DH5	6.2	mA
	LE1M	6.4	
	LE2M	7.4	

Table 12: Bluetooth current consumption, VBAT=3V VDDIO=3V, Integrated antenna variant

Operating Mode	Data Rate	Module 3V	Unit
TX	DH1	14.4	mA
	DH3	14.5	
	DH5	14.5	
	2DH1	19.9	
	2DH3	20.4	
	2DH5	20.4	
	3DH1	20.2	
	3DH3	20.1	
	3DH5	20.1	
	LE1M	16.4	
	LE2M	16.3	
RX	DH5	6.2	mA
	LE1M	6.4	
	LE2M	7.4	

Note: Current consumption is measured at average of the TX-on time

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8 HOST INTERFACE SPECIFICATIONS

8.1 High-Speed UART Specifications

Table 13: UART timing specifications

Reference	Characteristics	Min	Typ	Max	Units
1	Delay time, UART_CTS_N LOW to UART_TXD valid.	—	—	1.5	Bit periods
2	Setup time, UART_CTS_N HIGH before midpoint of stop bit.		—	0.67	
3	Delay time, midpoint of stop bit to UART_RTS_N HIGH.	—	—	1.33	

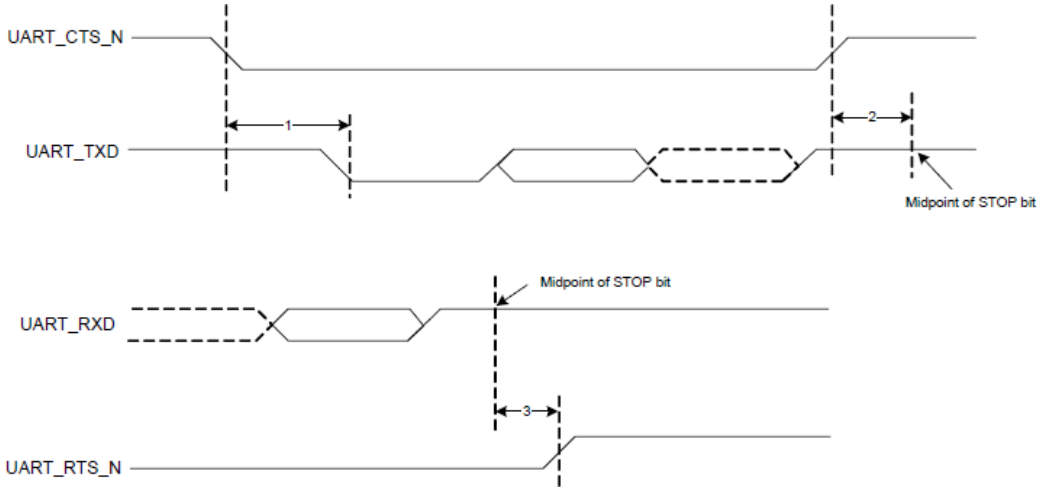

Figure 3: UART timing diagram

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8.2 SPI timing

Table 14: SPI mode 0 and 2

Reference	Characteristics	Min	Max	Units
1	Time from master assert SPI_CSN to first clock edge	45	—	ns
2	Setup time for MOSI data lines	6	1/2 SCK	
3	Idle time between subsequent SPI transactions	1 SCK	—	

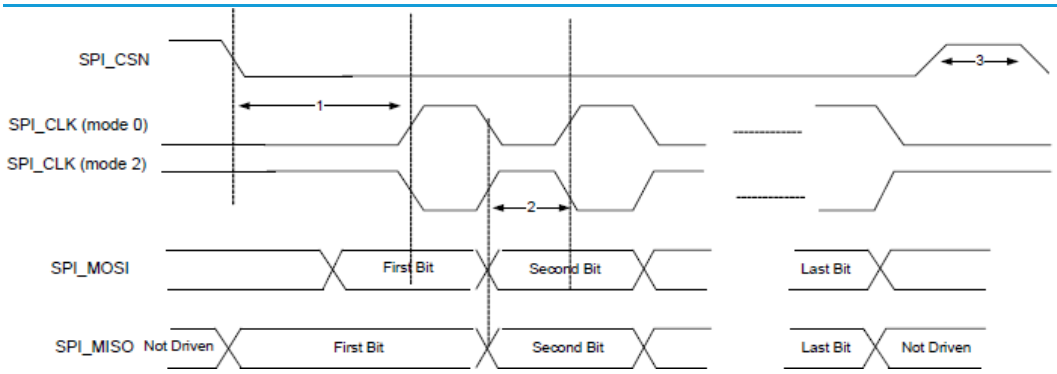

Figure 4: SPI timing, mode 0 and 2

Table 15: SPI mode 1 and 3

Reference	Characteristics	Min	Max	Units
1	Time from master assert SPI_CSN to first clock edge	45	—	ns
2	Setup time for MOSI data lines	6	1/2 SCK	
3	Idle time between subsequent SPI transactions	1 SCK	—	

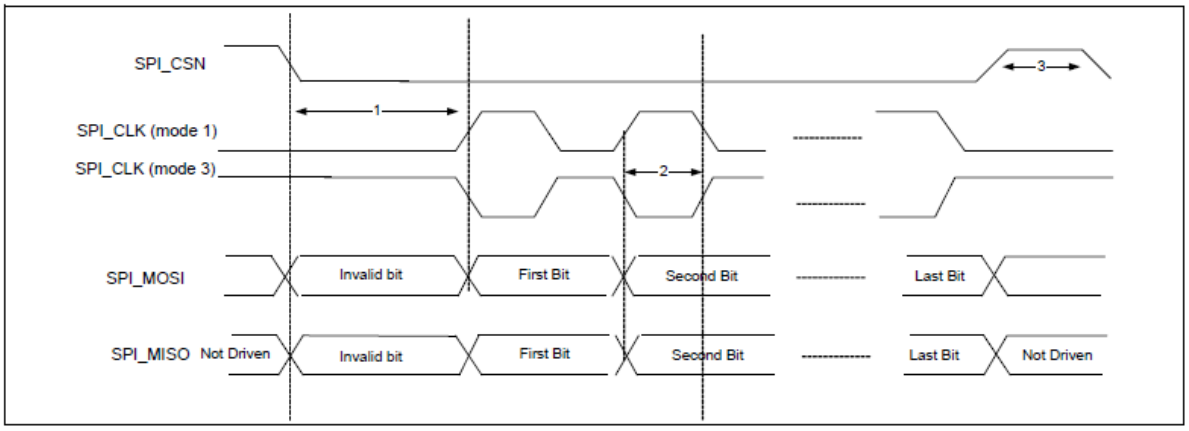

Figure 5: SPI timing, mode 1 and 3

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8.3 I²C timing

Table 16: I2C interface timing specifications (up to 1 MHz)

Reference	Characterstics	Min	Max	Units
1	Clock frequency	—	100 400 800 1000	KHz
2	START condition setup time	650	—	us
3	START condition hold time	280	—	
4	Clock low time	650	—	
5	Clock high time	280		
6	Data input hold time[1]	0	—	
7	Data input setup time	100	—	
8	STOP condition setup time	280		
9	Output valid from clock	—	400	
10	Bus free time[2]	650	—	

Notes: 1. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2. Time that the CBUS must be free before a new transaction can start.

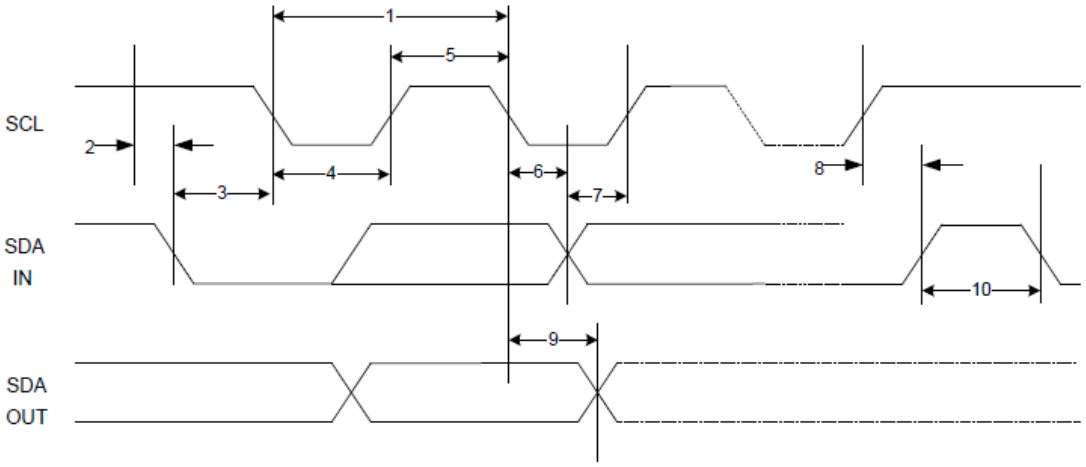

Figure 6: I²C interface timing diagram

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8.4 I²S timing

Table 17: Timing for I2S transmitters and receivers

	Transmitter				Receiver				Notes
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	-	-	-	T_r	-	-	-	[3]
Master mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	0.35 x T_{tr}	-	-	-	0.35 x T_{tr}	-	-	-	[4]
LOW t_{LC}	0.35 x T_{tr}	-	-	-	0.35 x T_{tr}	-	-	-	[4]
Slave mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	-	0.35 x T_{tr}	-	-	-	0.35 x T_{tr}	-	-	[3]
LOW t_{LC}	-	0.35 x T_{tr}	-	-	-	0.35 x T_{tr}	-	-	[3]
Rise time t_{RC}	-	-	0.15 x T_{tr}	-	-	-	-	-	[4]
Transmitter									
Delay t_{dtr}	-	-	-	0.8 x T	-	-	-	-	[5]
Hold time t_{htr}	0	-	-	-	-	-	-	-	[4]
Receiver									
Setup time t_{sr}	-	-	-	-	0.2 x T_{tr}	-	-	-	[6]
Hold time t_{hr}	-	-	-	-	0.2 x T_{tr}	-	-	-	[6]

Notes: [3] The system clock period T must be greater than Ttr and Tr because both the transmitter and receiver have to be able to handle the data transfer rate.

[4] At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, tHC and tLC are specified with respect to T.

[5]In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35Tr, any clock that meets the requirements can be used.

[6]Because the delay (tdtr) and the maximum transmitter speed (defined by Ttr) are related, a fast transmitter driven by a slow clock edge can result in tdtr not exceeding tRC which means thtr becomes zero or negative. Therefore, the transmitter has to guarantee that thtr is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than tRCmax, where tRCmax is not less than 0.15Ttr.

[7] To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.

[8] The data setup and hold time must not be less than the specified receiver setup and hold time.

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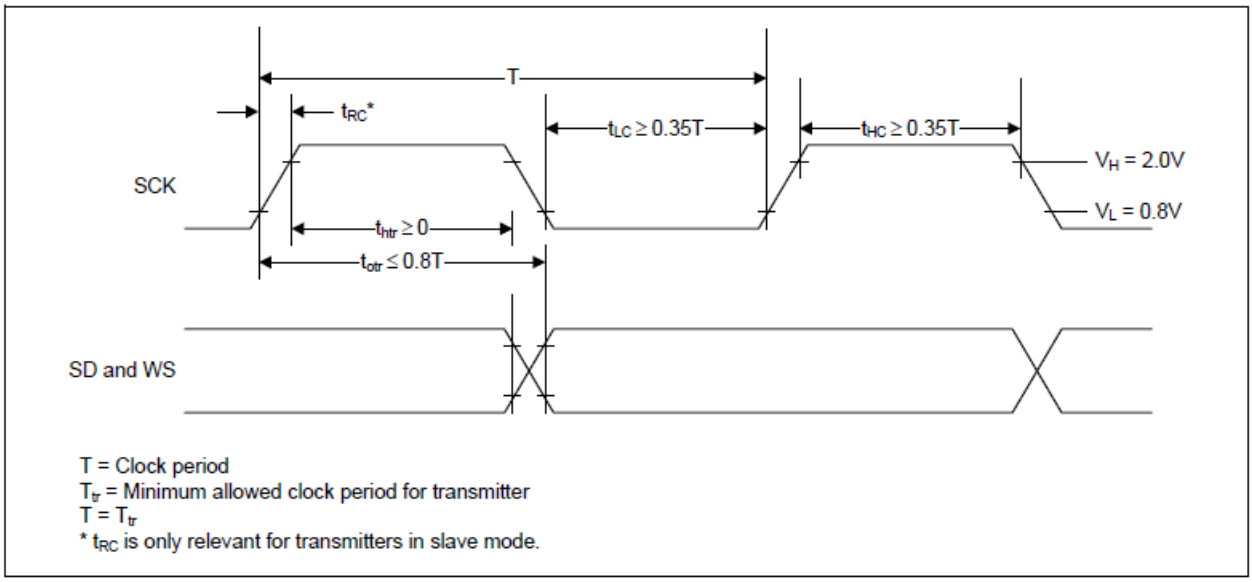

Figure 7: I²S transmitter timing

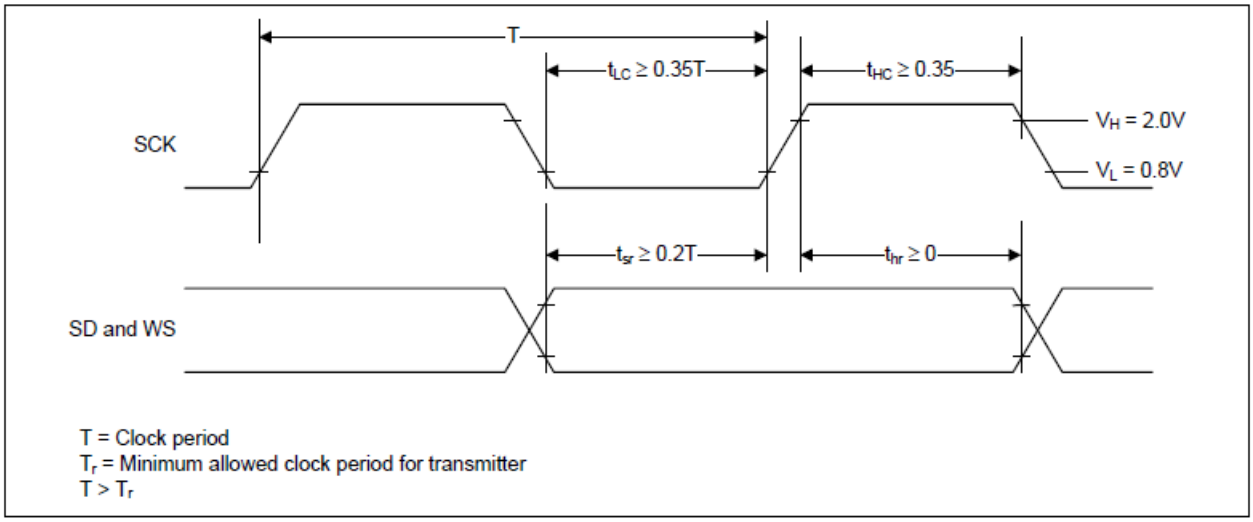

Figure 8: 2S receiver timing

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9 MHF4 Connector Variant Footprint and Pin Definitions

Note: The following footprint and pin definitions apply to the Vela IF820. There are two module footprints, depending on which variant of the module is used. *It is important to ensure you are using the correct version on your design*.

9.1 MHF4 connector variant Mechanical Definition

Module dimensions of MHF4 connector variant module is 7.5 x 7.5 x 2.15 mm. Detail drawings are shown in Figure 9.

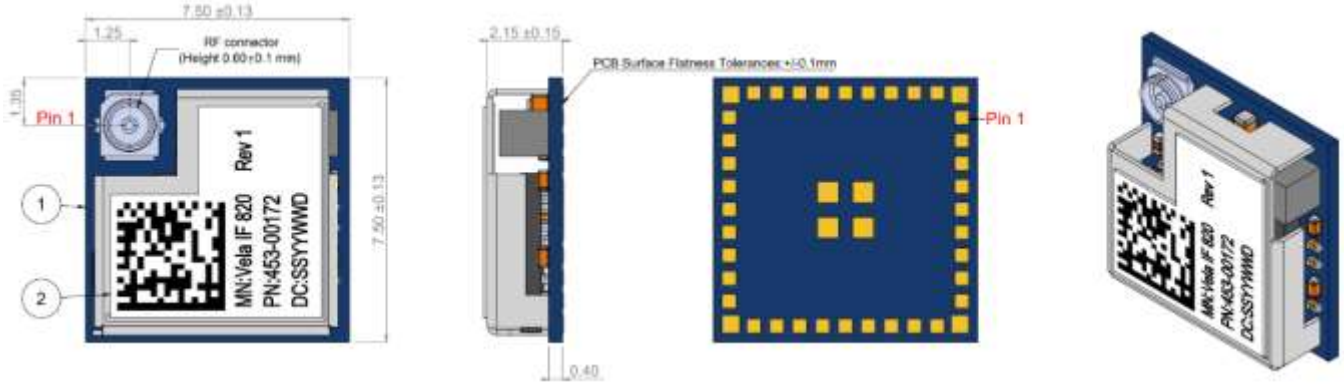

Figure 9: Mechanical Details – MHF4 Variant (453-00172)

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9.2 MHF4 connector variant Module Footprint

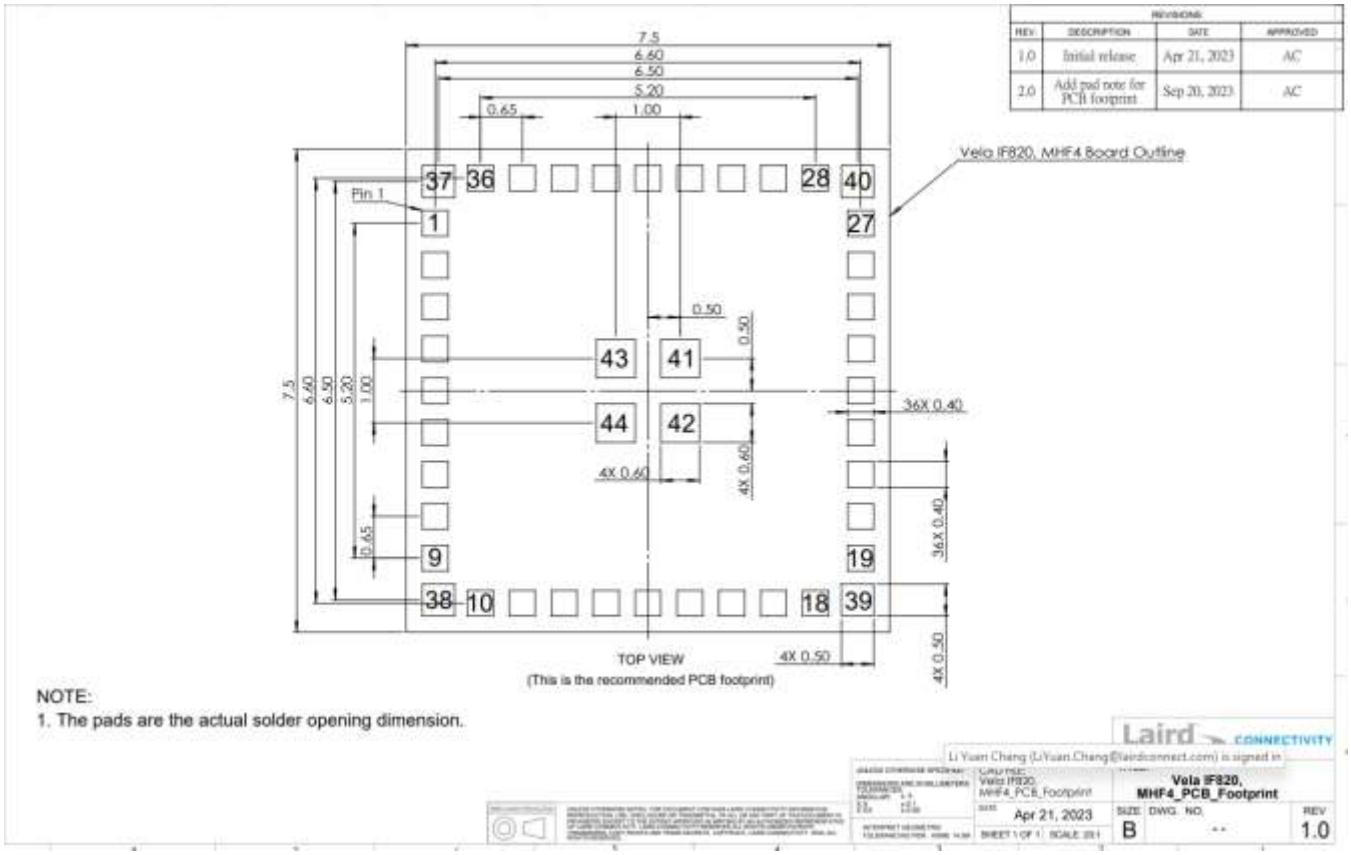

Figure 10: MHF4 connector variant module pinout (top view)

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9.3 MHF4 connector variant Module Pin Definition

Table 18: Pin definitions of MHF4 connector variant module

Pin #	Name	I/O	Voltage Ref.	Description
1	BT_DEV_WAKE	I	VDDIO	A signal from the CYW20820 device to the host indicating that the Bluetooth® device requires attention.
2	BT_HOST_WAKE	O	VDDIO	A signal from the host to the CYW20820 indicating that the host requires attention.
3	GND	-	-	NA
4	P28	I/O	VDDIO	Recommended functions for P28 ▪ PWM2 ▪ SCL3 (master and slave) ▪ Optical control output: QOC2 ▪ A/D converter input 11 ▪ Current: 16 mA sink P28 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
5	P4	I/O	VDDIO	Recommended functions for P4 ▪ Keyboard scan input (row): KSI4 ▪ Quadrature: QDY0 ▪ SPI_1: MOSI (master only) P4 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
6	P2	I/O	VDDIO	Recommended functions for P2 ▪ Keyboard scan input (row): KSI2 ▪ Quadrature: QDX0 ▪ SPI_1: MOSI (master only) ▪ UART1_RTS_N P2 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
7	P15	I/O	VDDIO	Recommended functions for P15 Keyboard scan output (column): KSO7 A/D converter input 20 P15 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.

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Pin #	Name	I/O	Voltage Ref.	Description
8	P5	I/O	VDDIO	Recommended functions for P5 ▪ Keyboard scan input (row): KSI5 ▪ Quadrature: QDY1 ▪ Peripheral UART: puart_tx ▪ SPI_1: MISO (slave only) ▪ I2C: SDA P5 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
9	P8	I/O	VDDIO	Recommended functions for P8 ▪ Keyboard scan output (column): KSO0 ▪ A/D converter input 27 ▪ External T/R switch control: ~tx_pd P8 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
10	VDDIO	I	VDDIO	1.71V to 3.3V is recommended to supply for digital I/O
11	GND	-	-	NA
12	XTALI_32K	I	VDDIO	Low-power oscillator input
13	XTALO_32K	O	VDDIO	Low-power oscillator output
14	P3	I/O	VDDIO	Recommended functions for P3 ▪ Keyboard scan input (row): KSI3 ▪ Quadrature: QDX1 ▪ UART1_CTS_N ▪ SPI_1: SPI_CLK (master only) P3 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
15	P6	I/O	VDDIO	Recommended functions for P6 ▪ Keyboard scan input (row): KSI6 ▪ Quadrature: QDZ0 ▪ Peripheral UART: puart_rts ▪ PWM2 P6 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
16	P17	I/O	VDDIO	Recommended functions for P17 ▪ Keyboard scan output (column): KSO9 ▪ A/D converter input 18 P17 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
17	P9	I/O	VDDIO	Recommended functions for P9 ▪ Keyboard scan output (column): KSO1 ▪ A/D converter input 26 ▪ External T/R switc0h control: tx_pd P9 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.

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Pin #	Name	I/O	Voltage Ref.	Description
18	P12	I/O	VDDIO	Recommended functions for P12 ▪ Keyboard scan output (column): KSO4 ▪ A/D converter input 23 P12 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
19	P13	I/O	VDDIO	Recommended functions for P13 ▪ Keyboard scan output (column): KSO5 ▪ A/D converter input 22 ▪ PWM3 P13 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
20	P1	I/O	VDDIO	Recommended functions for P1 ▪ Keyboard scan input (row): KSI1 ▪ A/D converter input 28 ▪ Peripheral UART: puart_rts ▪ SPI_1: MISO (slave only) ▪ UART1_RXD Can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
21	P11	I/O	VDDIO	Recommended functions for P11 ▪ Keyboard scan output (column): KSO3 ▪ A/D converter input 24 P11 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
22	P10	I/O	VDDIO	Recommended functions for P10 ▪ Keyboard scan output (column): KSO2 ▪ A/D converter input 25 ▪ External PA ramp control: PA_Ramp P10 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
23	P27	I/O	VDDIO	Recommended functions for P27 ▪ Keyboard scan output (column): KSO19 ▪ PWM1 ▪ SPI_1: MOSI (master only) ▪ Optical control output: QOC1 ▪ Current: 16 mA sink P27 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
24	RST	I	VDDIO	Active-low system reset with internal pull-up resistor.

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Pin #	Name	I/O	Voltage Ref.	Description
25	P0	I/O	VDDIO	Recommended functions for P0 ▪ Keyboard scan input (row): KSI0 ▪ A/D converter input 29 ▪ Peripheral UART: puart_tx ▪ SPI_1: MOSI (master only) ▪ UART1_TXD P0 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
26	P37	I/O	VDDIO	Recommended functions for P37 ▪ A/D converter input 2 ▪ Quadrature: QDZ1 ▪ SPI_1: MISO (slave only) ▪ Auxiliary clock output: ACLK1 ▪ I2C: SCL P37 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
27	P32	I/O	VDDIO	Recommended functions P32 ▪ A/D converter input 7 ▪ Quadrature: QDX0 ▪ Auxiliary clock output: ACLK0 ▪ Peripheral UART: puart_tx P32 Can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
28	P14	I/O	VDDIO	Recommended functions for P14 ▪ Keyboard scan output (column): KSO6 ▪ A/D converter input 21 ▪ PWM2 P14 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
29	P29	I/O	VDDIO	Recommended functions for P29 ▪ PWM3 ▪ SDA3 (master and slave) ▪ Optical control output: QOC3 ▪ A/D converter input 10 ▪ Current: 16 mA sink P29 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
30	P26	I/O	VDDIO	Recommended functions for P26 ▪ Keyboard scan output (column): KSO18 ▪ PWM0 ▪ SPI_1: SPI_CS (slave only) ▪ Optical control output: QOC0 ▪ Current: 16 mA sink P26 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.

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Pin #	Name	I/O	Voltage Ref.	Description
31	3P0V	I	3V	Power supply input
32	GND	-	-	Ground
33	BT_UART_RTS	O, PU	VDDIO	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.
34	BT_UART_TXD	O, PU	VDDIO	UART serial output. Serial data output for the HCI UART interface.
35	BT_UART_RXD	I	VDDIO	UART serial input. Serial data input for the HCI UART interface.
36	BT_UART_CTS	I, PU	VDDIO	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.
37	GND	-	-	Ground
38	GND	-	-	Ground
39	GND	-	-	Ground
40	GND	-	-	Ground
41	GND	-	-	Ground
42	GND	-	-	Ground
43	GND	-	-	Ground
44	GND	-	-	Ground

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9.4 Reference schematic design

Note: ***It is recommended to put a 100nF bypass capacitor in the 3P0V (pin31) and VDDIO (pin10).***

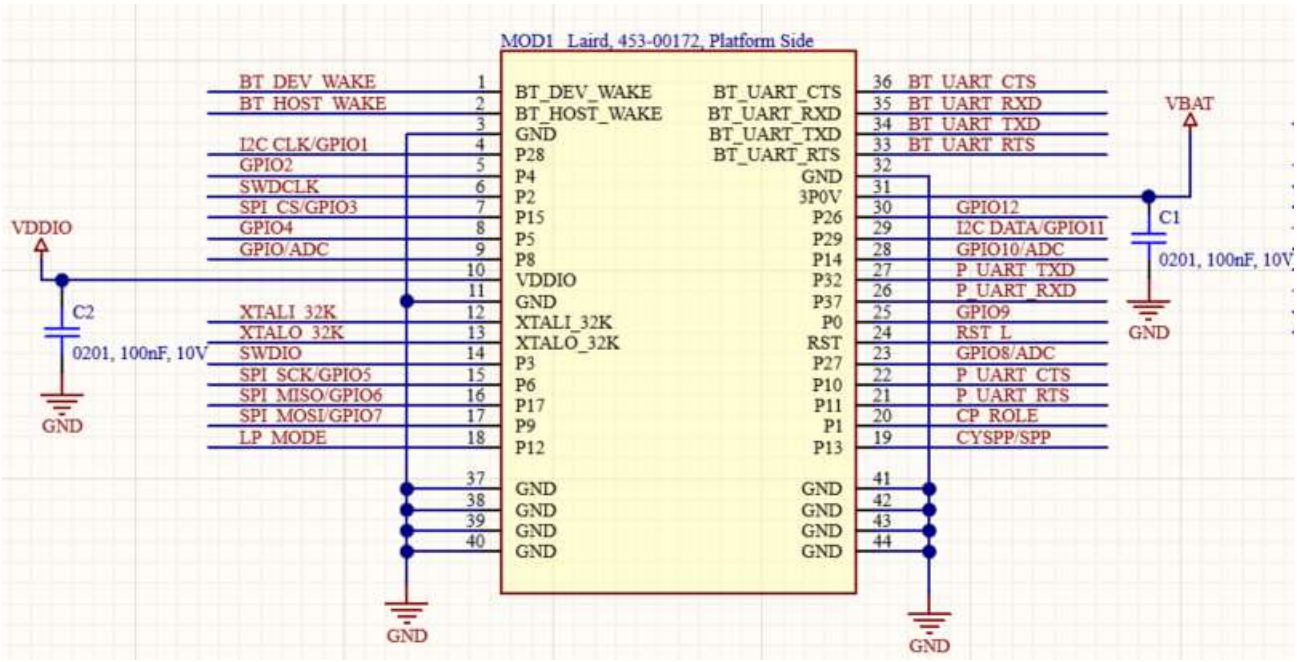

Figure 11: MHF4 connector variant schematic

9.5 Supermux I/O function defined table

Table 19: GPIO supermux input functions

	Input	
SWDCK	**SPI2_CS**	**SCL2**
SWDIO	**SPI2_MOSI**	**SDA2**
SPI1_CLK	**SPI2_MISO**	**PCM_IN**
SPI1_CS	**SPI2_IO2**	**PCM_CLK**
SPI1_MOSI	**SPI2_IO3**	**PCM_SYNC**
SPI1_MISO	**SPI2_INT**	**I2S_DI**
SPI1_IO2	**puart_rx**	**I2S_WS**
SPI1_IO3	**puart_cts_n**	**I2S_CLK**
SPI1_INT	**SCL**	**PDM_IN_Ch_1**
SPI2_CLK	**SDA**	**PDM_IN_Ch 2**

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Table 20: GPIO supermux output functions

Output			
do_P# (data out of GPIO. For example: P0)	**kso4**	**kso19**	**SCL2**
do_PCM_IN	**kso5**	**do_P# pwm0**	**puart_tx (uart2_tx)**
do_PCM_OUT	**kso6**	**do_P# pwm1**	**puart_rts_n (uart2_rts_n)**
do_PCM_CLK	**kso7**	**do_P# pwm2**	**SPI1_CLK**
do_PCM_SYNC	**kso8**	**do_P# pwm3**	**SPI1_CS**
do_I2S_DO	**kso9**	**do_P# pwm4**	**SPI1_MOSI**
do_I2S_DI	**kso10**	**do_P# pwm5**	**SPI1_MISO**
do_I2S_WS	**kso11**	**aclk0**	**SPI1_IO2**
do_I2S_CLK	**kso12**	**aclk1**	**SPI1_IO3**
do_CLK_REQ	**kso13**	**HID_OFF**	**SPI2_CLK**
IR_TX	**kso14**	**pa_ramp**	**SPI2_CS**
kso0	**kso15**	**tx_pd**	**SPI2_MOSI**
kso1	**kso16**	**~tx_pd**	**SPI2_MISO**
kso2	**kso17**	**SWDIO**	**SPI2_IO2**
kso3	**kso18**	**SDA2**	**SPI2_IO3**

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10 INTEGRATED ANTENNA VARIANT FOOTPRINT & PIN DEFINITIONS

10.1 Integrated Antenna variant Mechanical Definition

Module dimensions of integrated antenna variant module is 12.5 x 9.3 x 2.15 mm. Detail drawings are shown in Figure 9.

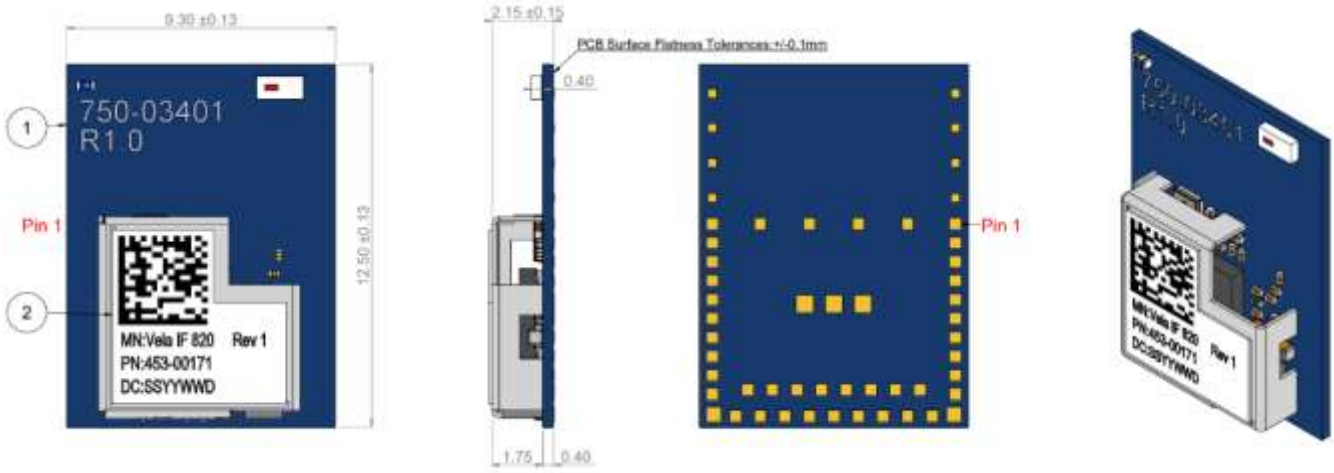

Figure 12: Mechanical Details – Integrated Antenna Variant (453-00171)

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10.2 Integrated Antenna variant Module Footprint

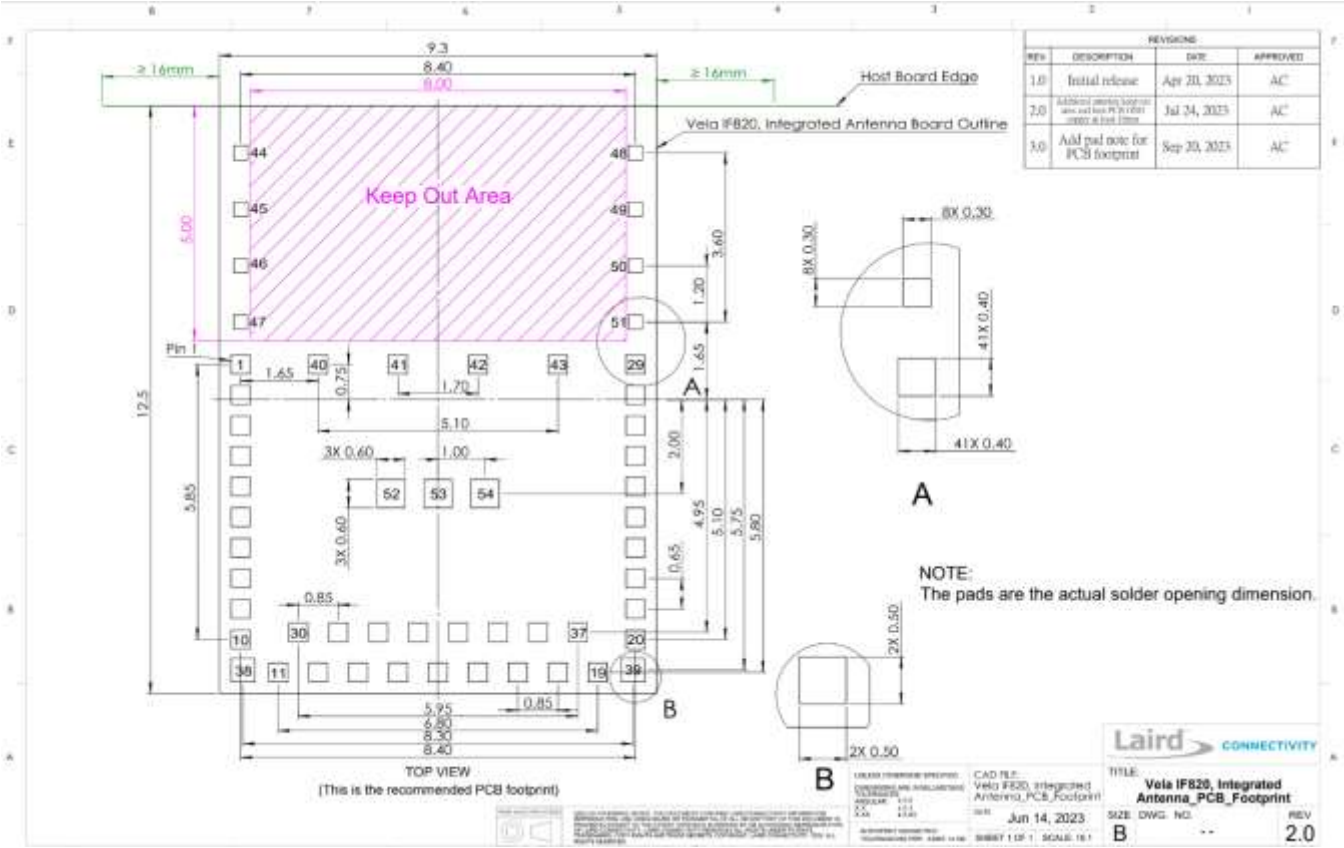

Figure 13: Integrated antenna variant module pinout (top view)

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10.3 Integrated Antenna variant Module Pin Definition

Table 21: Pin definitions of Vela IF820 chip Antenna module

Pin #	Name	I/O	Voltage Ref.	Description
1	GND	-	-	Ground
2	VDDIO	I	VDDIO	1.71V to 3.3V is recommended to supply for digital I/O
3	GND	-	-	Ground
4	XTALI_32K	I	VDDIO	Low-power oscillator input
5	XTALO_32K	O	VDDIO	Low-power oscillator output
6	P15	I/O	VDDIO	Recommended functions for P15 ▪ Keyboard scan output (column): KSO7 ▪ A/D converter input 20 P15 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
7	P8	I/O	VDDIO	Recommended functions for P8 ▪ Keyboard scan output (column): KSO0 ▪ A/D converter input 27 ▪ External T/R switch control: ~tx_pd P8 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
8	P2	I/O	VDDIO	Recommended functions for P2 ▪ Keyboard scan input (row): KSI2 ▪ Quadrature: QDX0 ▪ SPI_1: MOSI (master only) ▪ UART1_RTS_N P2 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
9	P3	I/O	VDDIO	Recommended functions for P3 ▪ Keyboard scan input (row): KSI3 ▪ Quadrature: QDX1 ▪ UART1_CTS_N ▪ SPI_1: SPI_CLK (master only) P3 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
10	P6	I/O	VDDIO	Recommended functions for P6 ▪ Keyboard scan input (row): KSI6 ▪ Quadrature: QDZ0 ▪ Peripheral UART: puart_rts ▪ PWM2 P6 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.

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11	P17	I/O	VDDIO	Recommended functions for P17 ▪ Keyboard scan output (column): KSO9 ▪ A/D converter input 18 P17 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
12	P13	I/O	VDDIO	Recommended functions for P13 ▪ Keyboard scan output (column): KSO5 ▪ A/D converter input 22 ▪ PWM3 P13 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
13	P9	I/O	VDDIO	Recommended functions for P9 ▪ Keyboard scan output (column): KSO1 ▪ A/D converter input 26 ▪ External T/R switc0h control: tx_pd P9 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
14	P10	I/O	VDDIO	Recommended functions for P10 ▪ Keyboard scan output (column): KSO2 ▪ A/D converter input 25 ▪ External PA ramp control: PA_Ramp P10 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
15	P37	I/O	VDDIO	Recommended functions for P37 ▪ A/D converter input 2 ▪ Quadrature: QDZ1 ▪ SPI_1: MISO (slave only) ▪ Auxiliary clock output: ACLK1 ▪ I2C: SCL P37 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
16	P11	I/O	VDDIO	Recommended functions for P11 ▪ Keyboard scan output (column): KSO3 ▪ A/D converter input 24 P11 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
17	P32	I/O	VDDIO	Recommended functions P32 ▪ A/D converter input 7 ▪ Quadrature: QDX0 ▪ Auxiliary clock output: ACLK0 ▪ Peripheral UART: puart_tx P32 Can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.

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18	P14	I/O	VDDIO	Recommended functions for P14 ▪ Keyboard scan output (column): KSO6 ▪ A/D converter input 21 ▪ PWM2 P14 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
19	P5	I/O	VDDIO	Recommended functions for P5 ▪ Keyboard scan input (row): KSI5 ▪ Quadrature: QDY1 ▪ Peripheral UART: puart_tx ▪ SPI_1: MISO (slave only) ▪ I2C: SDA P5 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
20	P28	I/O	VDDIO	Recommended functions for P28 ▪ PWM2 ▪ SCL3 (master and slave) ▪ Optical control output: QOC2 ▪ A/D converter input 11 ▪ Current: 16 mA sink P28 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
21	GND	-	-	Ground
22	3P0V	I	3V	Power supply input
23	GND	-	-	Ground
24	BT_UART_RTS	O, PU	VDDIO	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.
25	BT_UART_TXD	O, PU	VDDIO	UART serial output. Serial data output for the HCI UART interface.
26	BT_UART_RXD	I	VDDIO	UART serial input. Serial data input for the HCI UART interface.
27	BT_UART_CTS	I, PU	VDDIO	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.
28	BT_DEV_WAKE	I	VDDIO	A signal from the CYW20820 device to the host indicating that the Bluetooth® device requires attention.
29	BT_HOST_WAKE	O	VDDIO	A signal from the host to the CYW20820 indicating that the host requires attention.
30	P12	I/O	VDDIO	Recommended functions for P12 ▪ Keyboard scan output (column): KSO4 ▪ A/D converter input 23 P12 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.

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31	P1	I/O	VDDIO	Recommended functions for P1 ▪ Keyboard scan input (row): KSI1 ▪ A/D converter input 28 ▪ Peripheral UART: puart_rts ▪ SPI_1: MISO (slave only) ▪ UART1_RXD Can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
32	P0	I/O	VDDIO	Recommended functions for P0 ▪ Keyboard scan input (row): KSI0 ▪ A/D converter input 29 ▪ Peripheral UART: puart_tx ▪ SPI_1: MOSI (master only) ▪ UART1_TXD P0 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
33	P27	I/O	VDDIO	Recommended functions for P27 ▪ Keyboard scan output (column): KSO19 ▪ PWM1 ▪ SPI_1: MOSI (master only) ▪ Optical control output: QOC1 ▪ Current: 16 mA sink P27 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
34	RST	I	VDDIO	Active-low system reset with internal pull-up resistor.
35	P29	I/O	VDDIO	Recommended functions for P29 ▪ PWM3 ▪ SDA3 (master and slave) ▪ Optical control output: QOC3 ▪ A/D converter input 10 ▪ Current: 16 mA sink P29 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
36	P26	I/O	VDDIO	Recommended functions for P26 ▪ Keyboard scan output (column): KSO18 ▪ PWM0 ▪ SPI_1: SPI_CS (slave only) ▪ Optical control output: QOC0 ▪ Current: 16 mA sink P26 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.

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37	P4	I/O	VDDIO	Recommended functions for P4 ▪ Keyboard scan input (row): KSI4 ▪ Quadrature: QDY0 ▪ SPI_1: MOSI (master only) P4 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
38	GND	-	-	Ground
39	GND	-	-	Ground
40	GND	-	-	Ground
41	GND	-	-	Ground
42	GND	-	-	Ground
43	GND	-	-	Ground
44	GND	-	-	Ground
45	GND	-	-	Ground
46	GND	-	-	Ground
47	GND	-	-	Ground
48	GND	-	-	Ground
49	GND	-	-	Ground
50	GND	-	-	Ground
51	GND	-	-	Ground
52	GND	-	-	Ground
53	GND	-	-	Ground
54	GND	-	-	Ground

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10.4 Reference schematic design

Note: It is recommended to put bypass capacitors 100nF in the 3P0V (pin22) and VDDIO (pin2).

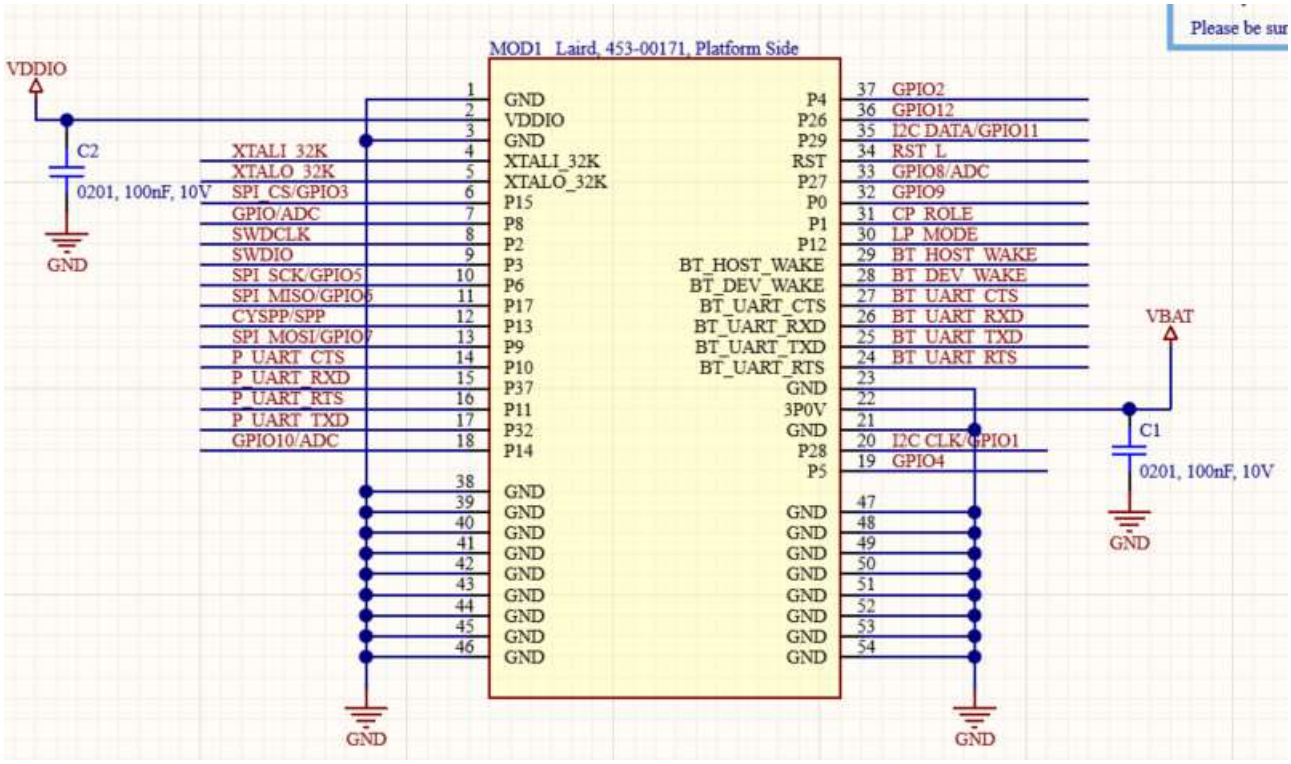

Figure 14: Integrated antenna variant schematic

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11 RF LAYOUT DESIGN GUIDELINES

11.1 General consideration

The following is a list of RF layout design guidelines and recommendation when installing a Laird Connectivity radio into your device.

- Do not run antenna cables directly above or directly below the radio.
- Do not place any parts or run any high-speed digital lines below the radio.
- If there are other radios or transmitters located on the device (such as a Bluetooth radio), place the devices as far apart from each other as possible. Also, make sure there is at least 25 dB isolation between these two antennas.
- Ensure that there is the maximum allowable spacing separating the antenna connectors on the Laird Connectivity radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Laird Connectivity recommends the use of a double-shielded cable for the connection between the radio and the antenna elements.
- Be sure to put a 100nF capacitor on EACH power pin. Also, place that capacitor to the pin as close as possible to make sure the internal PMU working correctly.

Use proper electro-static-discharge (ESD) procedures when installing the Laird Connectivity radio module. To avoid negatively impacting Tx power and receiver sensitivity, do not cover the antennas with metallic objects or components.

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11.2 Layout recommendations for integrated antenna variant

The following are recommended for layout of the integrated antenna variant of the Vela IF820:

1. Align module edge with PCB edge
2. In order to maintain antenna radiation efficiency, keep at least 15mm width of the GND plane to the sides the module.

Please see Figure 15 for a layout example.

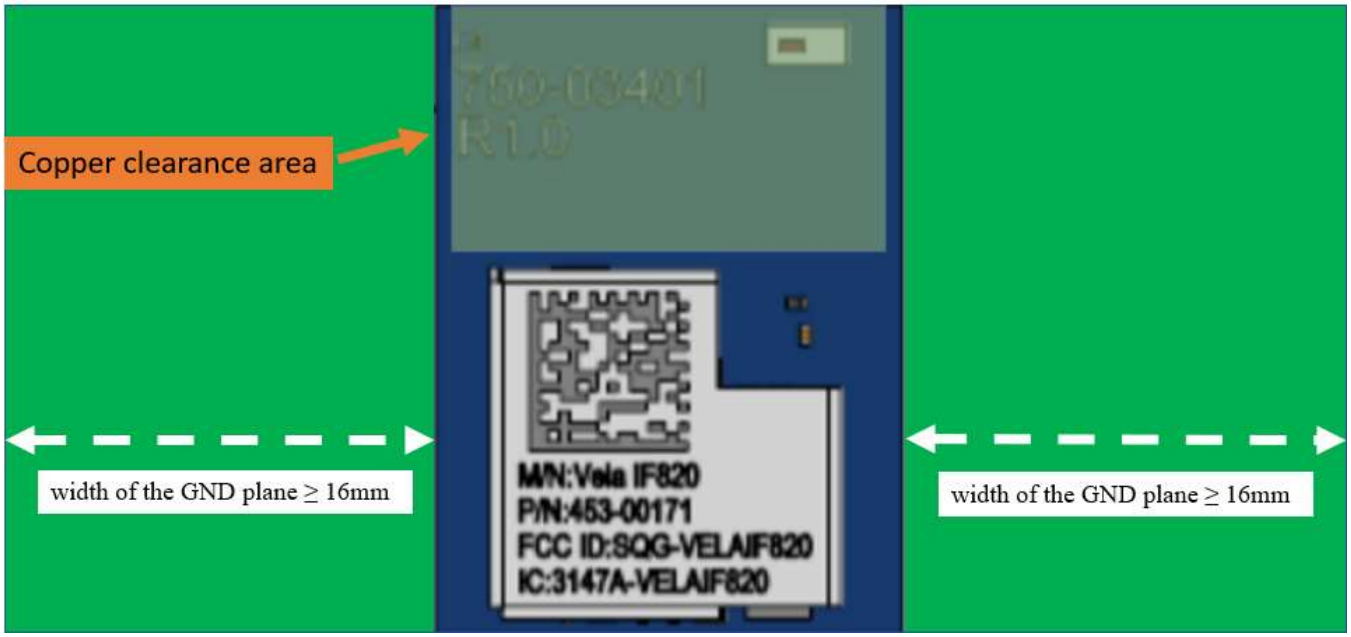

Figure 15: Integrated antenna variant layout suggestion example

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12 Application Note for Surface Mount Modules

12.1 Introduction

Laird Connectivity's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

Vela IF820 part numbers – 453-00171**R** and 453-00172**R** are shipped as Tape / Reel, with a reel containing 1,000 pcs.

12.2 Module Packaging Configuration

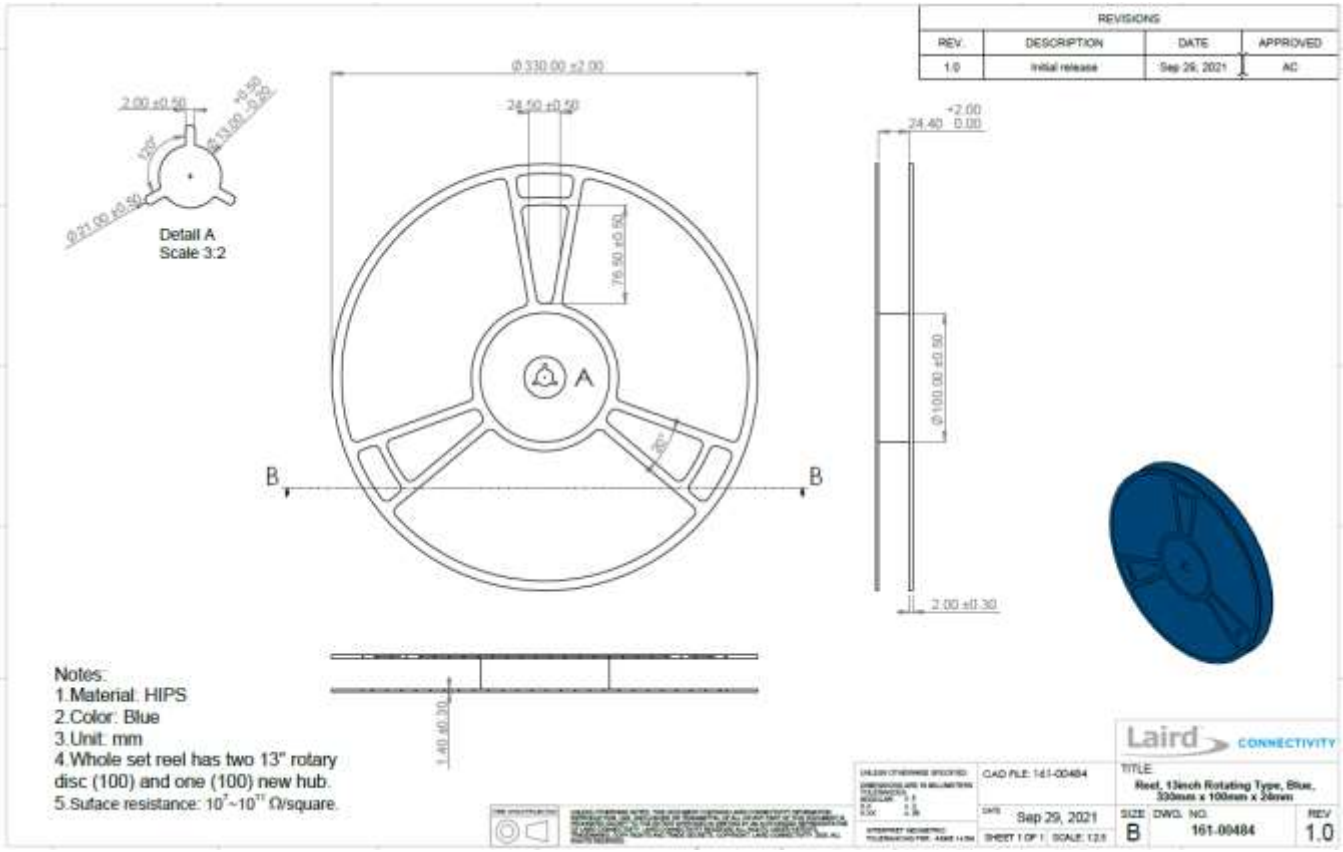

Figure 16: Reel specifications – 1,000 pieces per Reel

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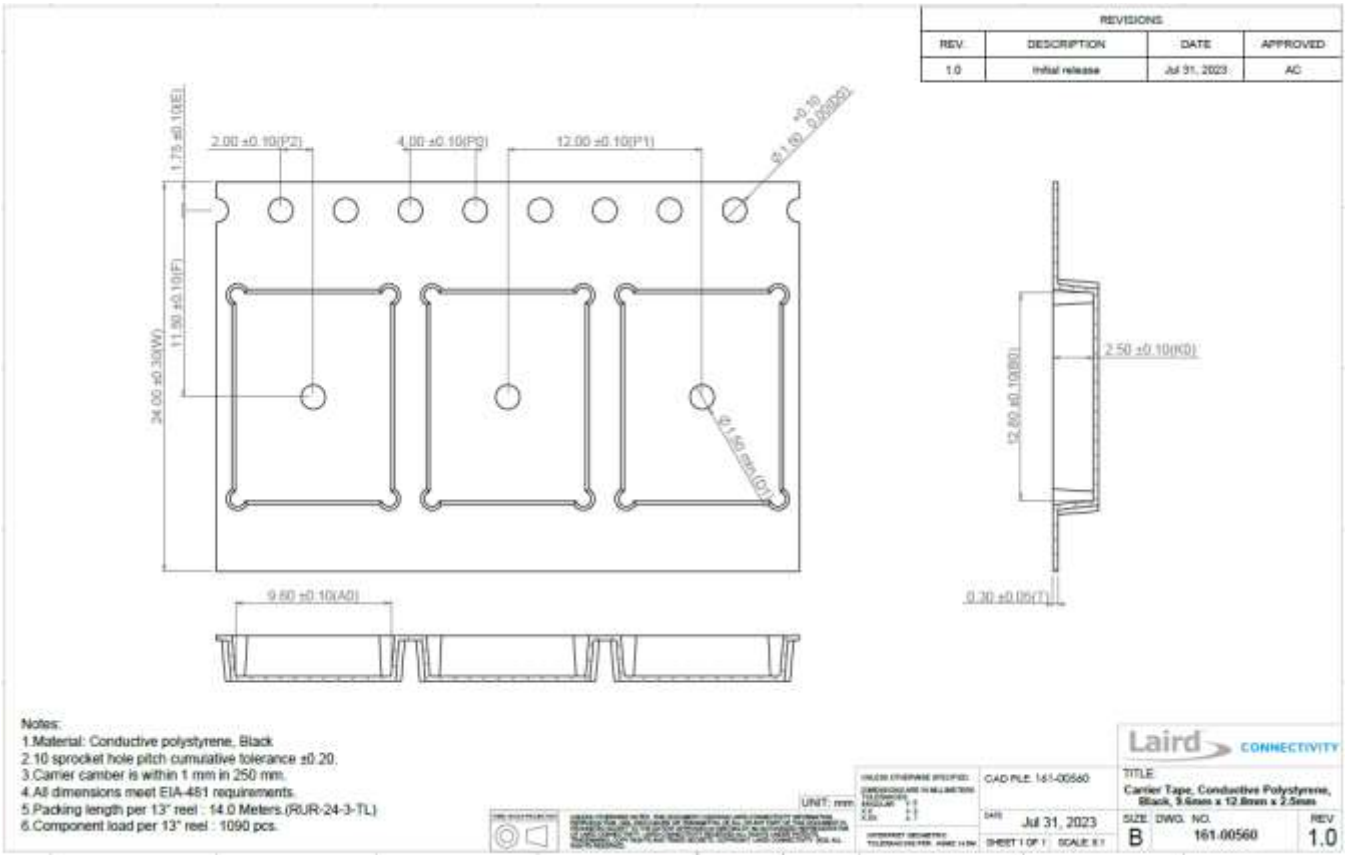

Figure 17: Carrier Tape specifications for Integrated Antenna Variant

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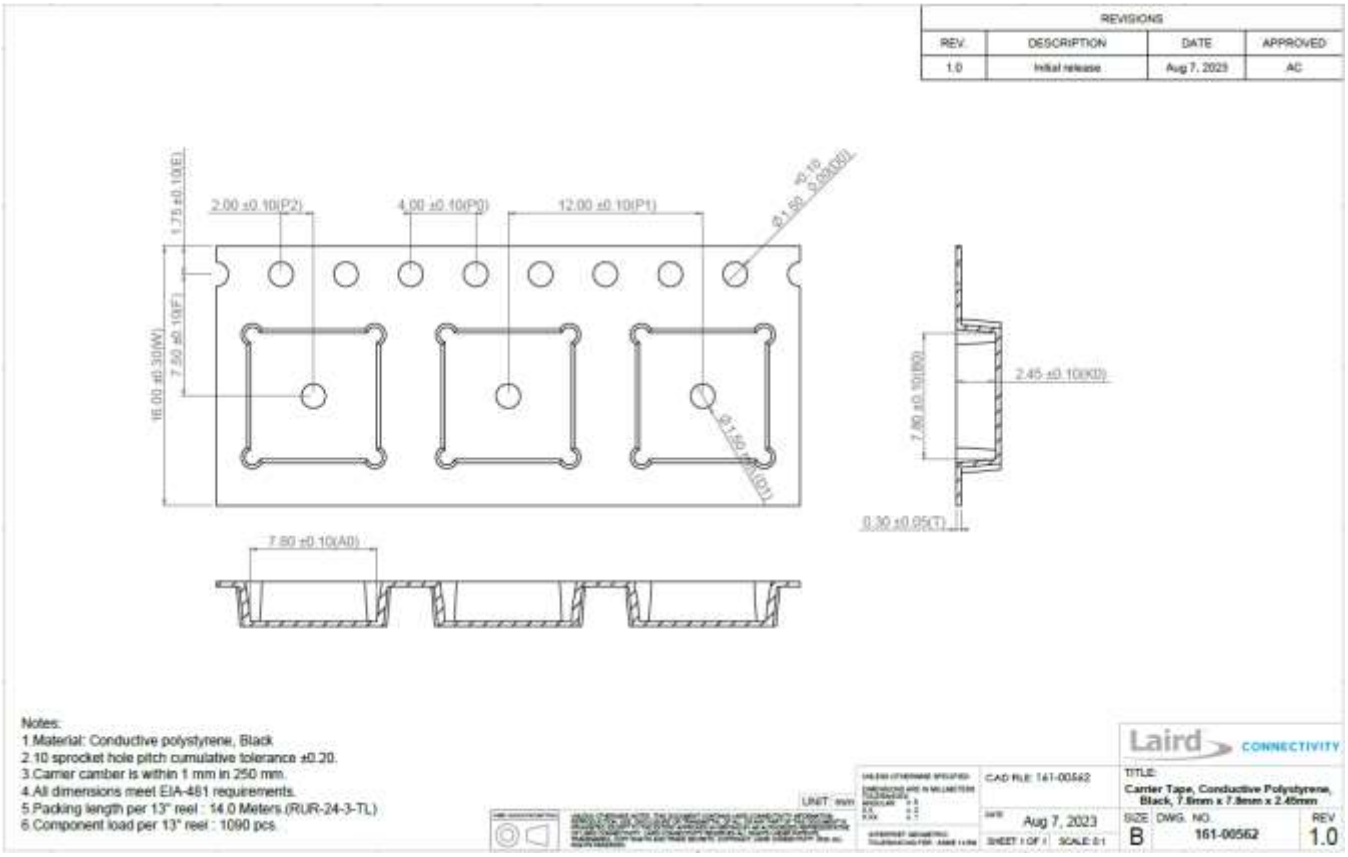

Figure 18: Carrier Tape Specifications for MHF4 Variant

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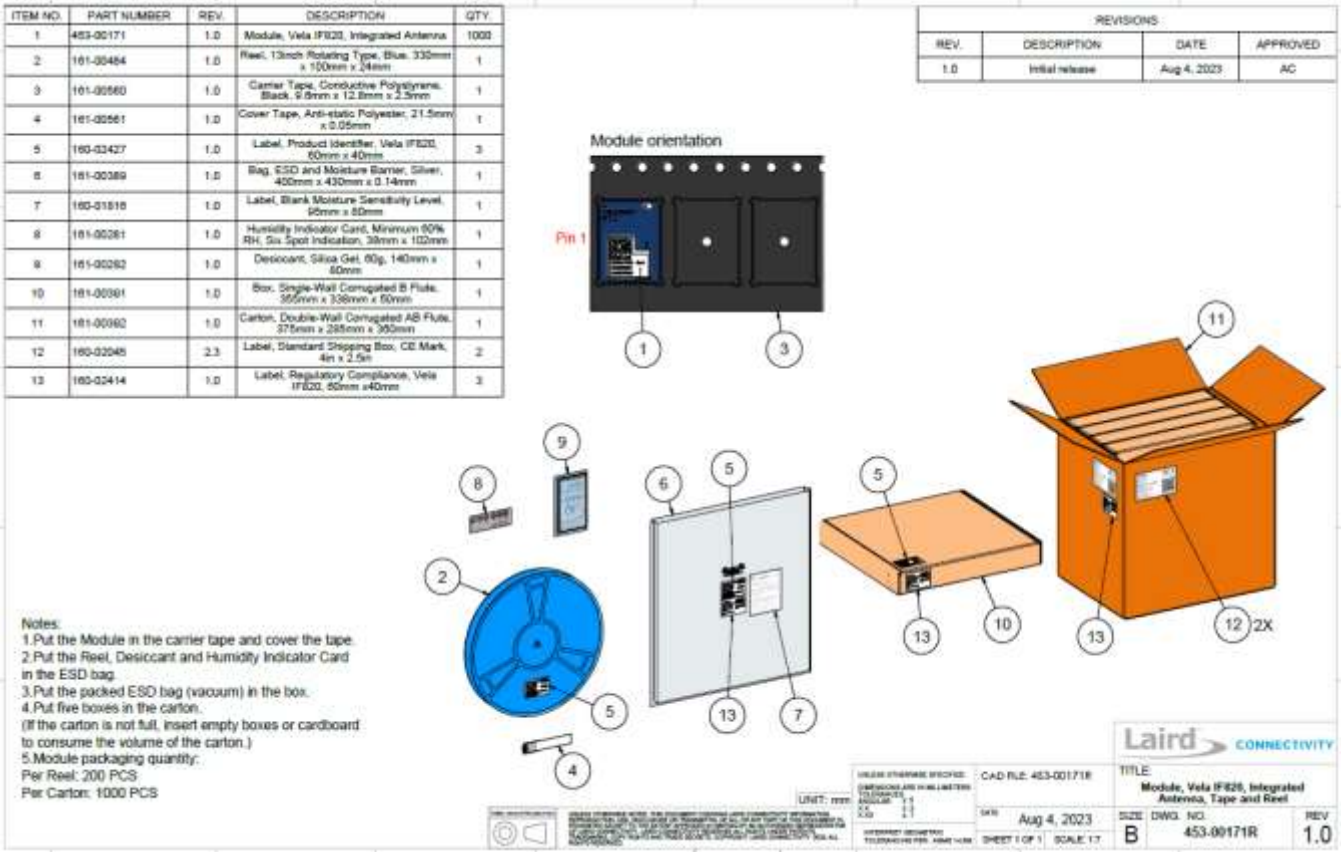

Figure 19: Vela IF820 Packaging Process for Integrated Antenna Variant

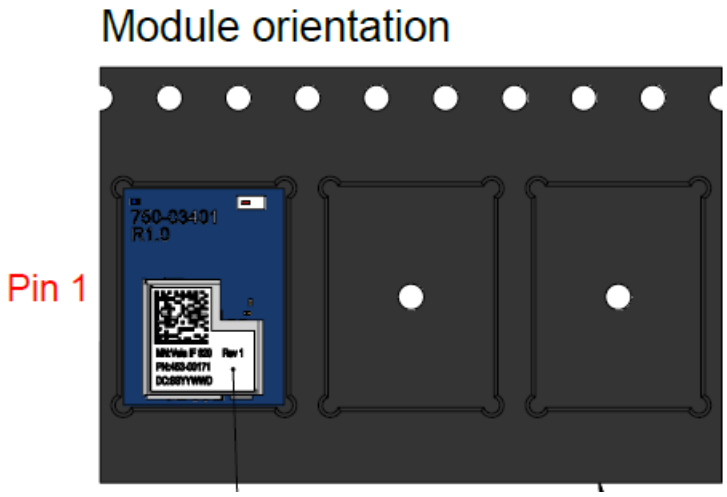

Figure 20: Module Orientation in Carrier Tape Pocket, Integrated Antenna Variant

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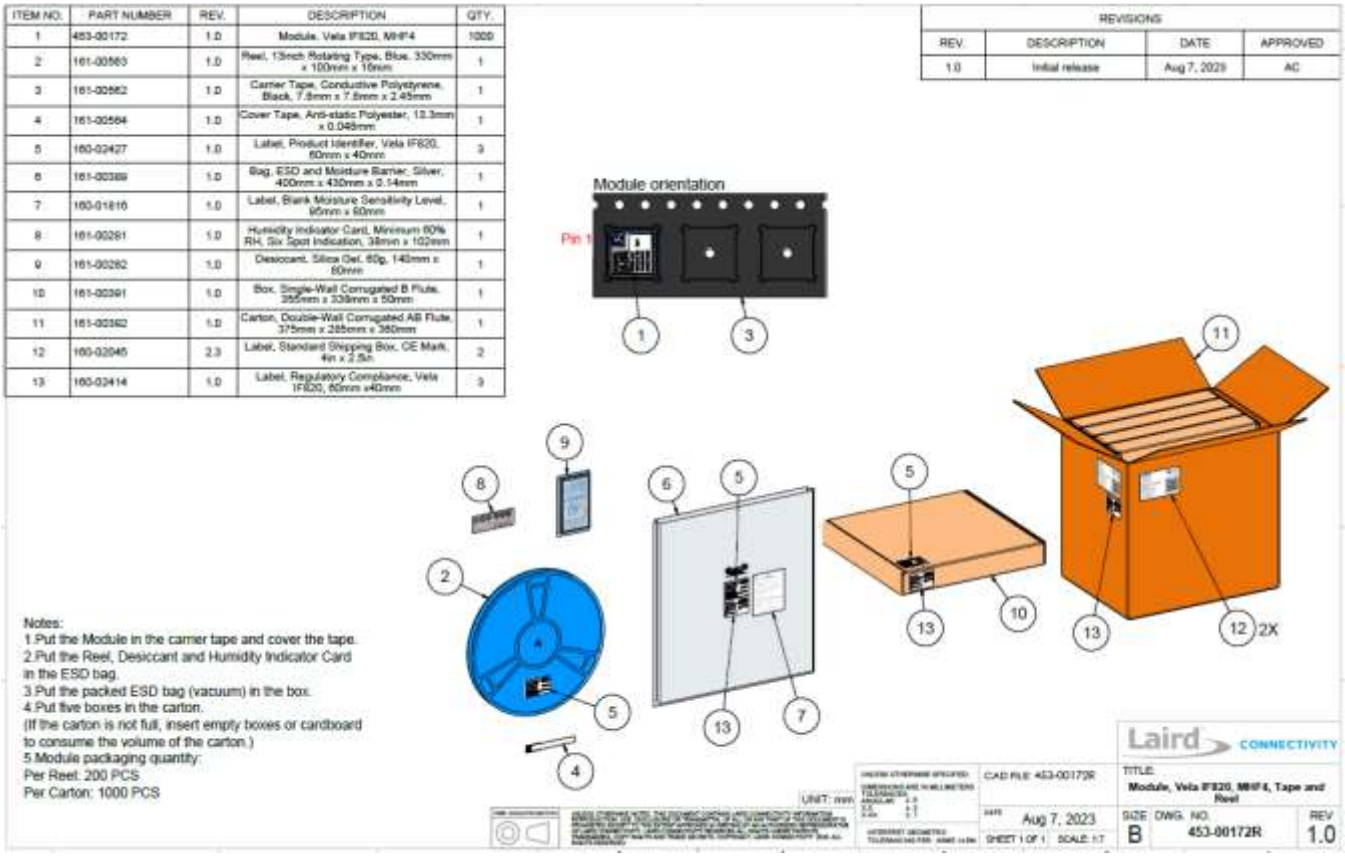

Figure 21: Vela IF820 Packaging Process for MHF4 Variant

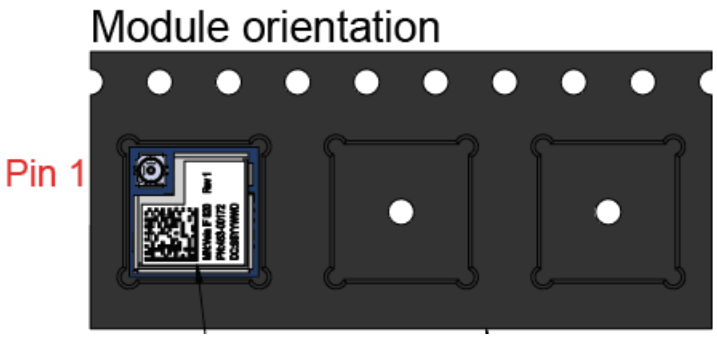

Figure 22: Module Orientation in Carrier Tape Pocket, MHF4 Variant

12.3 Module Shipping

All modules are shipped in tape and reel package and sealed in ESD Bags.

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12.4 Labelling

The following labels are placed on the anti-static bag. The Vela IF820 solder-down modules are classified as MSL4 devices.

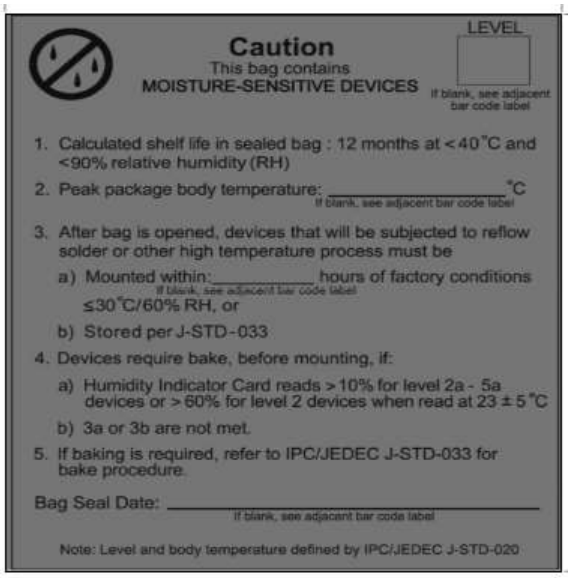

Figure 23: Moisture Sensitivity Level Label

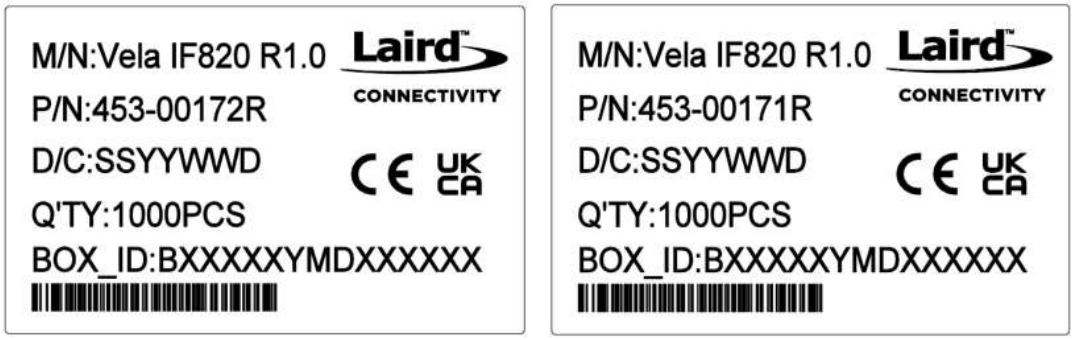

Figure 24: Product Identifier Label

Figure 25: Regulatory Compliance Label

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The following labels are placed on the pizza box.

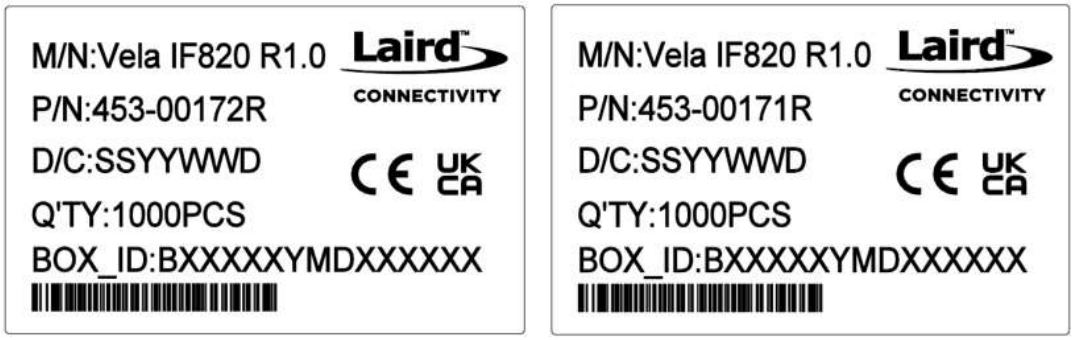

Figure 26: Product Identifier Label

Figure 27: Regulatory Compliance Label

The following labels are placed on the master shipping carton.

Figure 28: Standard Shipping Carton Label

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Figure 29: Regulatory Compliance Label

12.5 Required Storage Conditions

12.5.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior* to opening the dry packing**:

- Normal temperature: 5~40˚C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means relative humidity.

12.5.2 After Opening the Dry Packing

The following are required storage conditions ***after* opening the dry packing** (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: 72 hours or less after opening
- Storage conditions for two-time soldering
  - Storage conditions following opening and prior to performing the 1st reflow:
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: A hours or less after opening
  - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: B hours or less after completion of the 1st reflow

---

Note: Should keep A+B within 72 hours.

12.5.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

- Storage temperature and humidity:

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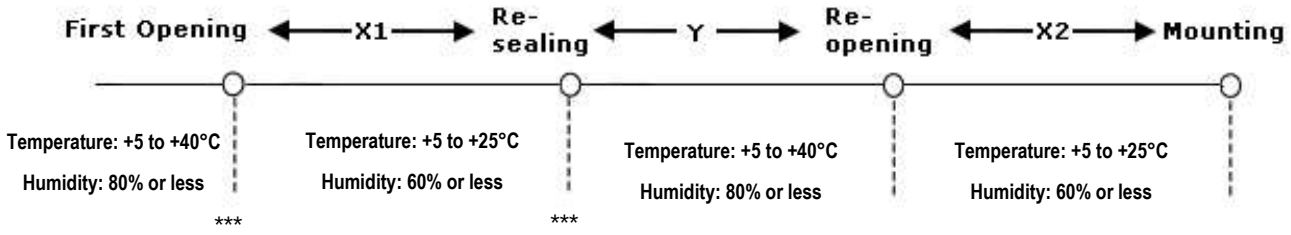

*** - External atmosphere temperature and humidity of the dry packing

- Storage period:
  - X1+X2 – Refer to After Opening the Dry Packing storage requirements. Keep is X1+X2 within 72 hours.
  - Y – Keep within two weeks or less.

12.6 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the SiP must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30˚C and <60% relative humidity.
- If the SiP is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125 ˚C (±5 ˚C).

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12.7 Surface Mount Conditions

The following soldering conditions are recommended to ensure device quality.

12.7.1 Soldering

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:

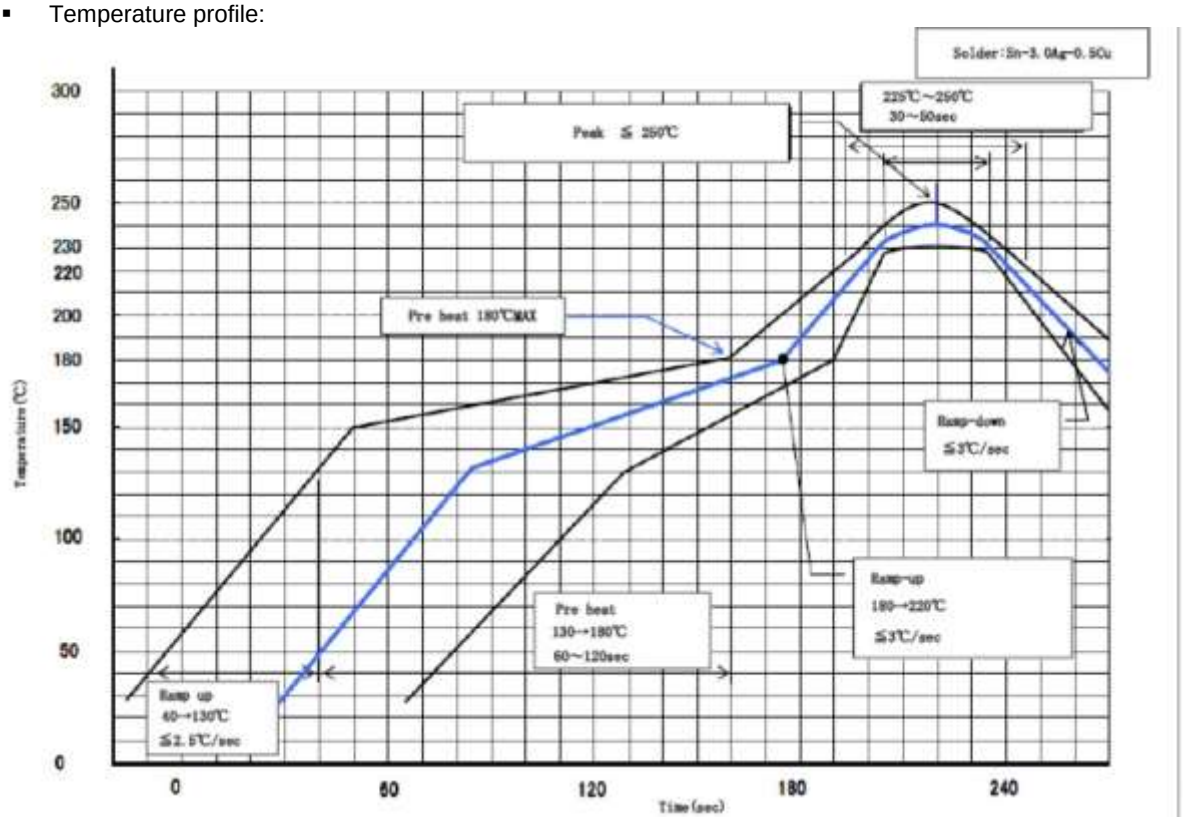

Figure 30: Temperature profile

- Ramp-up: 40-130˚C. Less than 2.5˚C/sec
- Pre heat: 130-180˚C 60-120 sec, 180˚C MAX
- Ramp-up: 180-220˚C. Less than 3˚C/sec
- Peak Temperature: MAX 250˚C
  - 225˚C ~ 250˚C, 30 ~ 50 sec
- Ramp-down: Less than 3˚C/sec

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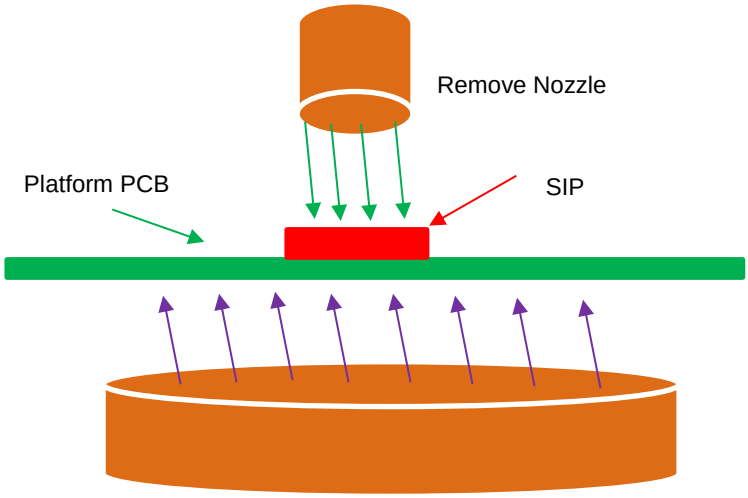
12.7.2 Cautions When Removing the SIP from the Platform for RMA

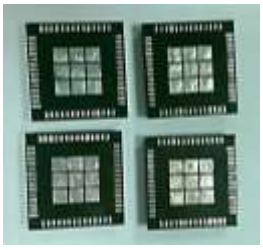
- Bake the platform before removing the SIP from the platform. Reference baking conditions.
- Remove the SIP by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

- One-side component platform:
  - Set the hot plate at 280°C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.
- Two-side components platform:
  - Use two hot air guns
  - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250°C) at a suitable distance from the platform PCB.
  - On the top side, apply a remove nozzle (temperature setting of 330°C). Heat the SIP until it can be removed from platform PCB.



- Remove the residue solder under the bottom side of SIP. (Note: Alternate module pictured as an example)



(Not accepted for RMA)

Example SIP with residue solder on the bottom

(Accepted for RMA analysis)

Example Module, no residue solder

- Remove and clean the residue flux as needed.

12.7.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.
- The Vela IF820 modules are MSL 4 rated.

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13 RELIABILITY TEST

13.1 Climatic And Dynamic Reliability Test

Table 22: Climatic and Dynamic Reliability Test Results for Vela IF820 Modules

Test Item	Specification	Standard	Test Result
Thermal Shock	Temperature: -40 ~ 85℃ Ramp time: Less than 10 seconds. Dwell Time: 10 minutes Number of Cycles: 350 times	*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles	Pass
Vibration Non-operating Unpackaged device	Vibration Wave Form: Sine Waveform Vibration frequency / Displacement: 20-80 Hz/1.5mm Vibration frequency / Acceleration: 80-2000 Hz/20g Cycle Time: 4 min/cycle Number of Cycles: 4 cycle/axis Vibration Axes：X, Y and Z (Rotate each axis on vertical vibration table)	JEDEC 22-B103B (2016)	Pass
Mechanical Shock Non-operating Unpackaged device	Pulse shape: Half-sine waveform Impact acceleration: 1500 g Pulse duration: 0.5 ms Number of shocks: 30 shocks (5 shocks for each face) Orientation: Bottom, top, left, right, front and rear faces	JEDEC 22-B110B.01 (2019)	Pass

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13.2 Reliability MTBF Prediction

Table 23: MTBF Predictions for Vela IF820 Modules

Laird Connectivity Part Number	Environment	Standard	Test Result 45 ℃ (Hours)
453-00171R 453-00171C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	7,920,607
453-00172R 453-00172C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	8,084,775
450-00185	Ground, Fixed, Uncontrolled	Telcordia Issue 3	1,114,640.34
453-00171R 453-00171C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	2,970,228
453-00172R 453-00172C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	3,031,791
450-00185	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	181,815.09
Laird Connectivity Part Number	**Environment**	**Standard**	**Test Result 85 ℃ (Hours)**
453-00171R 453-00171C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	1,839,958
453-00172R 453-00172C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	1,8537,738
450-00185	Ground, Fixed, Uncontrolled	Telcordia Issue 3	2,549,301.59
453-00171R 453-00171C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	689,984
453-00172R 453-00172C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	696,652
450-00185	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	440,892.82

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14 REGULATORY

Full regulatory information on the Vela IF820, including the Regulatory Information Guide, grants, and test reports are available on the Vela IF820 product page (coming soon).

The Vela IF820 holds current certifications in the following countries:

Table 24: Vela IF820 Certifications

Country/Region	Regulatory ID
USA (FCC)	SQG-VELAIF820
EU (ETSI)	N/A (No ID Number Required)
UKCA	N/A (No ID Number Required)
Canada (ISED)	3147A-VELAIF820
Japan (MIC)	201-230307
Australia (RCM)	N/A
New Zealand (RCM)	N/A
Korea	R-C-L8C-VELAIF820

Table 25: Certified Antennas for Vela IF820 Modules

Model	MPN	Manufacturer	Type	Connector	Peak Gain (2400 – 2500 MHz)
NanoBlue	EBL2400A1-10MH4L	Laird Connectivity	PCB Antenna	IPEX MHF4	2 dBi
FlexPIFA	001-0022	Laird Connectivity	Planar Inverted-F Type	IPEX MHF4	2 dBi
EDA-8709-2G4C1-B27-CY	EDA-8709-2G4C1-B27-CY (Laird Part#0600-00057)	MAG.LAYERS	Dipole	IPEX MHF4	2 dBi
mFlexPIFA	EFA2400A3S-10MH4L	Laird Connectivity	Planar Inverted-F Type	IPEX MHF4	2.32 dBi
AD1608	AD1608-A2455AAT/LF	ACX	Chip Antenna	N/A	1.0 dBi

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15 ORDERING INFORMATION

Table 26: Vela IF820 Ordering Part Numbers

Part	Description
453-00171R	Vela IF820 - Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) - Tape / Reel
453-00171C	Vela IF820 - Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) – Cut / Tape
453-00172R	Vela IF820 - Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) - Tape / Reel
453-00172C	Vela IF820 - Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) – Cut / Tape
453-00171-K1	Vela IF820 - Development Kit with integrated chip antenna
453-00172-K1	Vela IF820 - Development Kit with MHF4 Connector
450-00185	Vela IF820 - Dual Mode Bluetooth USB Adapter with integrated antenna variant (Infineon CYW20820)

15.1 General Comments

This is a preliminary datasheet. Please check with Laird Connectivity for the latest information before commencing a design. If in doubt, ask. For additional information visit Vela IF820 product page.

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16 BLUETOOTH SIG QUALIFICATION

16.1 Overview

The Vela IF820 module is listed on the Bluetooth SIG website as a qualified Controller Subsystem.

Design Name	Owner	Reference QDID	Description
453-00171R	Laird	217016	Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) - Tape / Reel
453-00171C	Laird	217016	Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) – Cut / Tape
453-00172R	Laird	217016	Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) - Tape / Reel
453-00172C	Laird	217016	Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) – Cut / Tape
453-00171-K1	Laird	217016	Development Kit with integrated chip antenna
453-00172-K1	Laird	217016	Development Kit with MHF4 Connector

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to register as a member of the Bluetooth SIG – www.bluetooth.org

The following is a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

To purchase a new Declaration ID for your design, please follow the link below, (login is required to access this page):

Launch Studio - Manage Declaration ID (bluetooth.com)

16.2 Qualification Steps When Referencing a Laird Controller Subsystem Design

To qualify your product when referencing a Laird Controller Subsystem design, follow these steps:

1. To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

   Note: A user name and password are required to access this site.

2. Select the option, 'Start the Bluetooth Qualification Process with **No Required Testing**'.
3. Enter your Project Name, this is a project name which can be the same as the product name or a top level project name if adding multiple End Products.
4. Enter *217016* in the Controller Subsystem table entry.
5. Enter your complimentary Host Subsystem and optional Profile Subsystem in the table entry, (refer to the table at the end of this section for suggested QDID).
6. On the Product Declaration Page and the Listing Date, then add each End Product that uses the Subsystem combination
7. On the Declaration ID page, select your pre-paid Declaration ID from the drop down menu or hit the 'Pay Declaration Fee' button.

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Note:	Unless the Declaration ID is pre-paid or purchased with a credit card, you cannot proceed until the SIG invoice is paid.

8. The End Products are now ready to list, on the Review and Submit tab, make sure the project status is all confirmed with a green tick. Check and confirm all tick boxes and enter your name in the signature box. To finalise hit the 'Signature Confirmed – Complete Project & Submit Products(s) for Qualification.

   Your new design will be listed on the SIG website and you can download your SDoC which should be placed in your compliance folder.

16.3 Complimentary Host Subsystem QDID

Design Name	Owner	QDID	Description
Infineon AIROC™ Bluetooth Host Software Stack	Cypress Semiconductor	223736	The Infineon AIROC™ Bluetooth Host Software Stack is a generic Bluetooth application package and is designed for implementation on hosted platforms as well as embedded Bluetooth or Wi-Fi/Bluetooth SoC's from Infineon. The Infineon AIROC™ Bluetooth Host Software Stack is Bluetooth v5.4 core spec compliant.

For further information please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

If you require assistance with the qualification process please contact our recommended Bluetooth Consultant, Steve Flooks, steve.flook@eurexuk.com.

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17 453-00171 Integrated Chip Antenna Performance

The following are details and plots of the measured radiation performance of the chip antenna on the Vela IF820 module with integrated antenna (part numbers 453-00171R and 453-00171C).

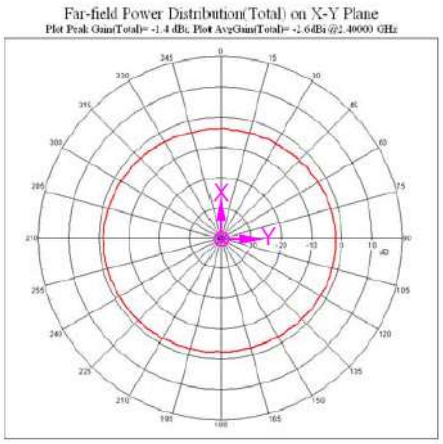
17.1 Summary of Antenna Performance

Unit in dBi	XY-plane		XZ-plane		YZ-plane		Efficiency
	Peak	Avg.	Peak	Avg.	Peak	Avg.	
@2400MHz	-1.4	-2.6	-2.1	-5	0.1	-2.8	45%
@2440MHz	-1.5	-2.3	-1.2	-4.3	0.6	-2.3	51%
@2480MHz	-2.1	-2.7	-1.8	-4.4	0.2	-2.7	48%

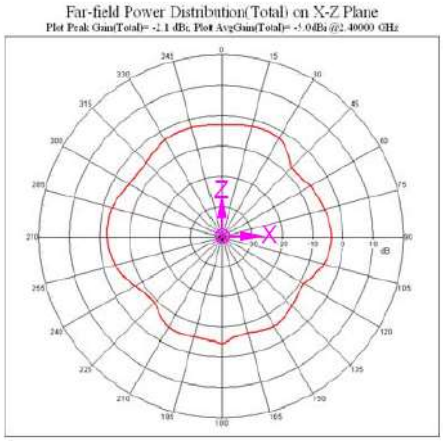
Note: The result is measured with Laird DVK part # 453-00171-K1.

17.2 2.4GHz Radiated Performance

XY-plane



XZ-plane



YZ-plane

Figure 31: 2400 MHz radiation pattern

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XY-plane XZ-plane YZ-plane

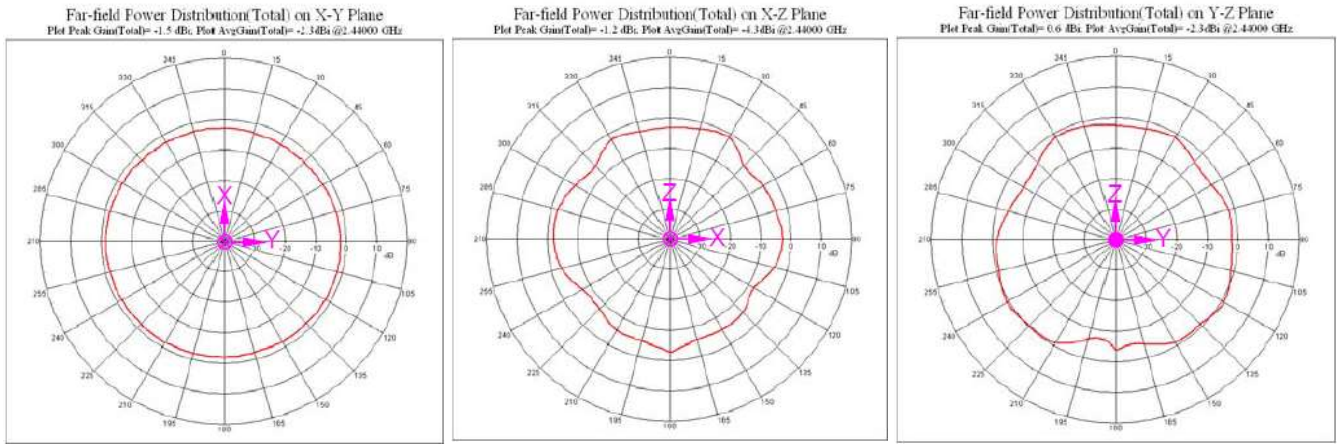

Figure 32: 2440 MHz radiation pattern

XY-plane XZ-plane YZ-plane

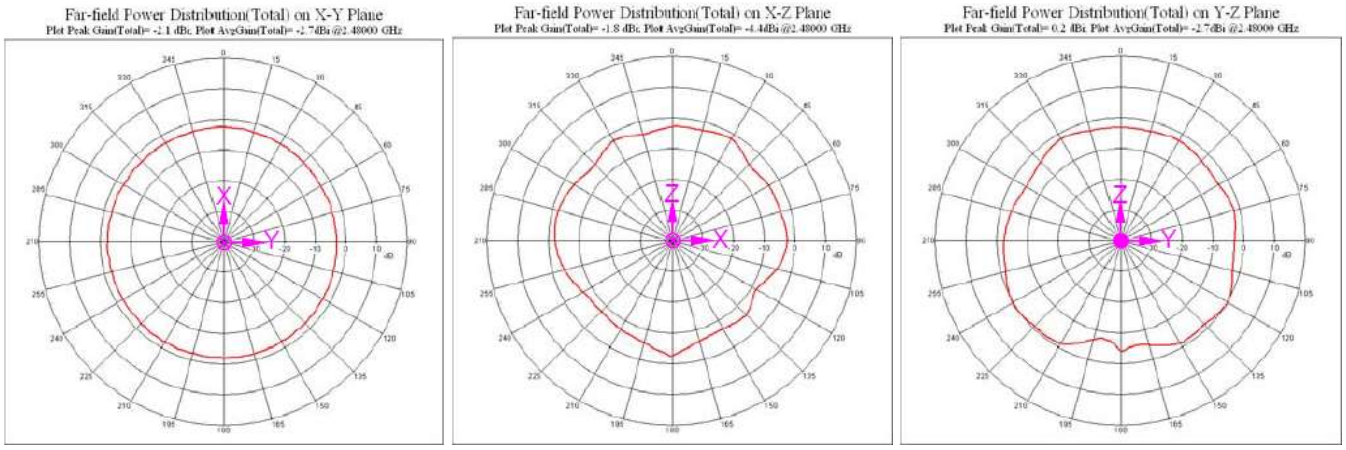

Figure 33: 2480 MHz radiation pattern

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18 453-00185 USB Adapter Integrated Antenna Performance

The following are details and plots of the measured radiation performance of the integrated antenna on the Vela IF820 USB adapter (part number 453-00185).

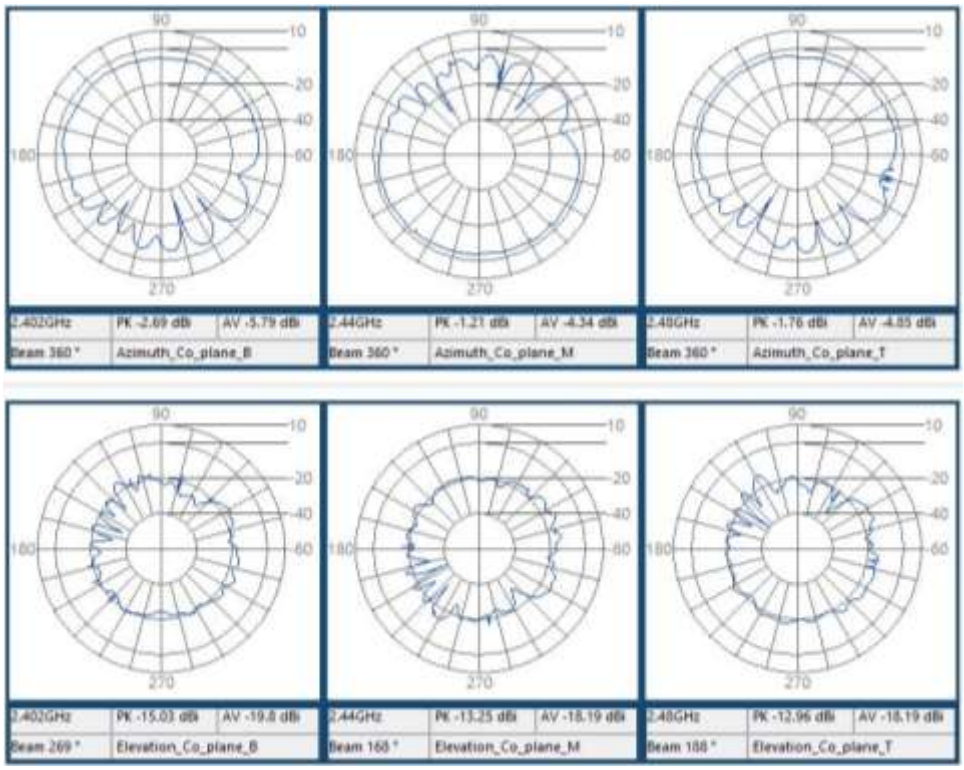
18.1 Summary of Antenna Performance

Unit in dBi	XY-plane		XZ-plane		YZ-plane	
	Peak	Avg.	Peak	Avg.	Peak	Avg.
@2400MHz	-2.69	-5.79	-4.47	-9.66	-4.92	-8.14
@2440MHz	-1.21	-4.34	-3.39	-8.67	-2.62	-5.35
@2480MHz	-1.76	-4.85	-3.71	-9.47	-2.27	-5.82

Note: The result is measured with USB adapter (part # 450-00185).

18.2 2.4GHz Radiated Pattern

18.2.1 X-Axis



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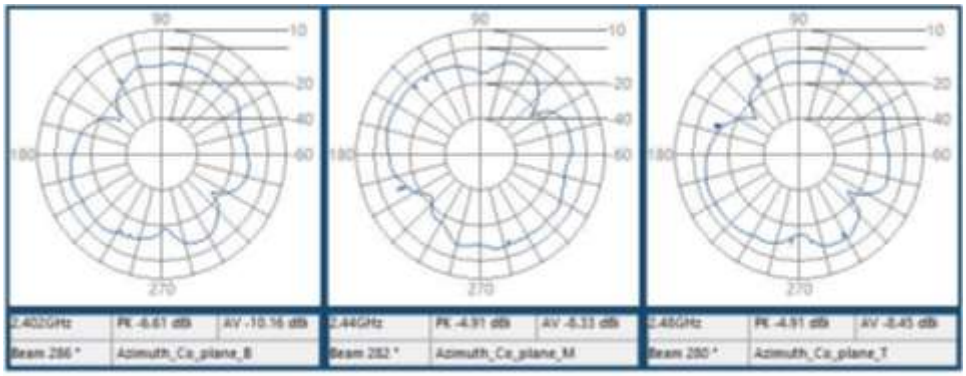
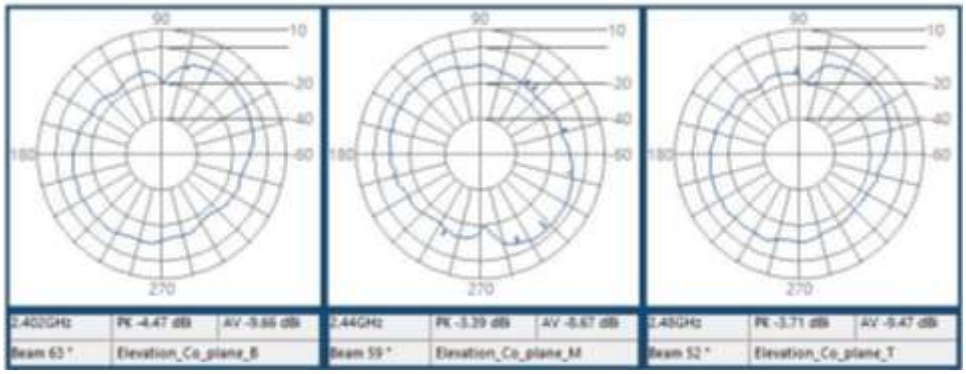
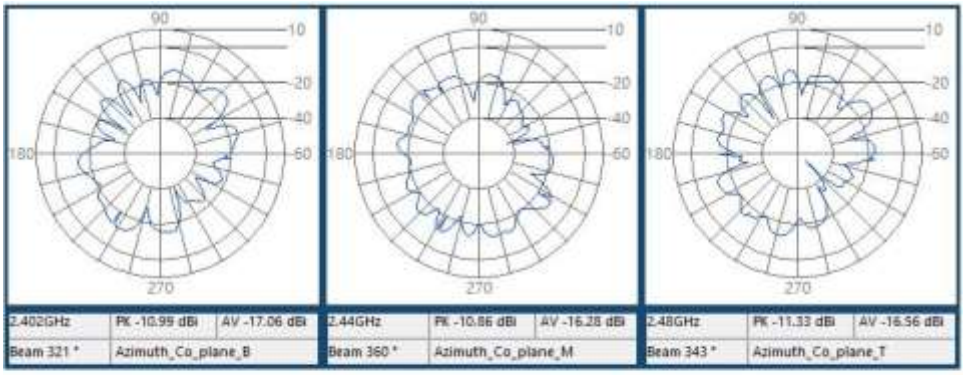
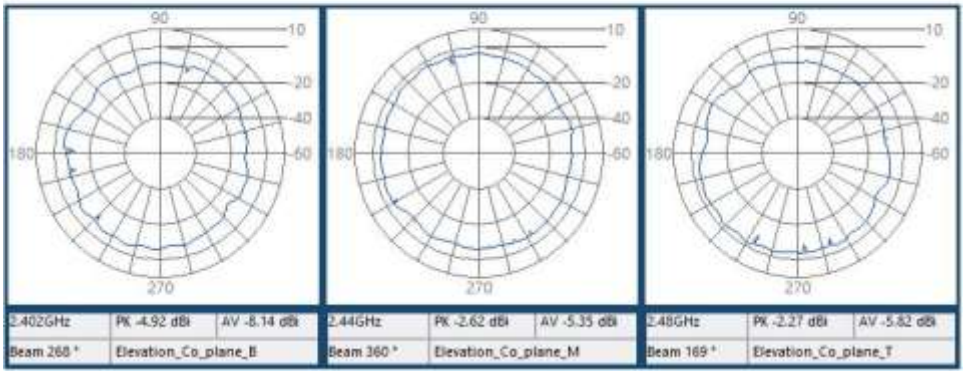
18.2.2 Y-axis





18.2.3 Z-axis





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19 ADDITIONAL INFORMATION

Please contact your local sales representative or our support team for further assistance:

Headquarters	Laird Connectivity 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Phone	Americas: +1-800-492-2320 Europe: +44-1628-858-940 Hong Kong: +852-2762-4823
Website	www.lairdconnect.com/
Technical Support	www.lairdconnect.com/resources/support
Sales Contact	www.lairdconnect.com/contact

Note: Information contained in this document is subject to change.

Laird Connectivity's products are subject to standard Terms & Conditions.

sales@lairdconnect.com
support@lairdconnect.com
www.lairdconnect.com

Federal Communication Commission Interference Stateme

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

Radiation Exposure Statement:

The product comply with the US portable RF exposure limit set forth for an uncontrolled environment and are safe for intended operation as described in this manual. The further RF exposure reduction can be achieved if the product can be kept as far as possible from the user body or set the device to lower output power if such function is available.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.\

Industry Canada statement:

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

(1) This device may not cause interference
(2) This device must accept any interference, including interference that may cause undesired operation of the device

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L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) L*'appareil ne doit pas produire de brouillage;*
(2) L'*appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.*

Radiation Exposure Statement:

The product comply with the Canada portable RF exposure limit set forth for an uncontrolled environment and are safe for intended operation as described in this manual. The further RF exposure reduction can be achieved if the product can be kept as far as possible from the user body or set the device to lower output power if such function is available.

Déclaration d'exposition aux radiations:
Le produit est conforme aux limites d'exposition pour les appareils portables RF pour les Etats-Unis et le Canada établies pour un environnement non contrôlé. Le produit est sûr pour un fonctionnement tel que décrit dans ce manuel. La réduction aux expositions RF peut être augmentée si l'appareil peut être conservé aussi loin que possible du corps de l'utilisateur ou que le dispositif est réglé sur la puissance de sortie la plus faible si une telle fonction est disponible.

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