SIM8260A Hardware Design

5G Module

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Version History

Date	Version	Description of change	Author
2021-9-27	1.00	Release	Yaling Wang Yi Zheng Chen Cheng
2021-11-26	1.01	1.Correct the PIN H39 to AH39 in table 5 2.Change some information about the baud rate frequency band supported by the serial port in the NOTE of 3.11 UART Interface. 3.Delete the PIN BA29 of the GND column in Table 5. 4.Add the power consumption current 120uA of the Power off mode in Table 62. 5. Change PIN W1 to RFU and PIN AM7 to GPIO, correct the information about ant interface in table 5 6.Add information about the conditions for the software with chip PM7250B to start up at 3.3V in the note of 3.1 Power Supply. 7.Correct some information about Frequency bands of SIM8260E and SIM8260A in the table, and data transmission throughput of 5G NR in table2. 8.Add the GPIO88 PIN in the GPIO row of Table 5, and add the EBIN2 interface in Table 5. 9.Delete the used RFU PIN, and modify the Pin assignment of Figure 2 accordingly.	Tao yu Yi Zheng Chen Cheng
2021-12-29	1.02	1. Change table 61 GPIO66 not support INT 2. Module pin AH3 change PIN name to RFU, table5, table42 delete this PIN description and change figure2 of the pin assignment of the module. 3.table 5 add notice for EBI2 interface 4.Exchang table5, table49 SIM8260C module ANT1 and ANT2 ant description	Yaling Wang Yi Zheng
2022-03-02	1.03	1. Change Figure 2 pin BA25 TO ANT1, BA33 to ANT2 2. Change table 44 3G net night to 200ms ON/OFF 3. Chane Table 62 power consumption current 135uA of the Power off mode and RF max power 4. Change the definition of GNSS antenna in table5/49/50 5. Updated Figure 46 and 47 6. Updated Figure 50 7. Change PIN AH3 GPIO90 for EBI2_CS	Yaling Wang
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		SIM83X0X_Series_Hardware Design 2.Add SIM8360A, SIM8380A and SIM8280A information 3.change table 6: about ANT Pin Frequency Range 4.change Table 13 Power on timing and electronic characteristic and add note 5.change chapter 3.8 about (u)SIM socket model 6.add chapter 3.21 about mmW interface 7.add chapter 6.7 about baking conditions	Shaoxu Hou
2022-09-05	1.05	1. Changed Table about mmW recommended connector type 2. Modify Table, add SIM8380E module information 3. Modify Table, modify the main frequency of the application processor, and add the module weight information 4. Add lines of Ipeak (QTM) related information to the content of Table 5. Increase the minimum output current capability requirement of external DCDC for mmW modules 6. Add module VDD_EXT peripheral reference circuit 7. Changed the content of the PCIe switch chapter, and changed the corresponding recommended material table 8. Add PCIe interface for IPQxxxx related content 9. Change the Codec ALC5616 special attention content 10. Supplement table content of W_DISABLE pin description 11. Change module Figure 12. Increase the content that PCIe_RST needs to be pulled up 13. The ID resistance of the PM7250B interface reference circuit is changed from 100K to 200K 14. Modify the description of pin AF3(SLEEP_OUT) 15. The data transfer throughput of different modules is changed to a table representation 16. Add the antenna port definition table of SIM8380E 17. Modify the Ipeak,Ton (STATUS)value 18. Change the description of module pin D9 19. Added chip junction temperature table in thermal design chapter	Shaoxu Hou Zhongxi Xiang

Contents

Table Index

Figure Index

1 Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics, and test results of the SIM8260A module. With the help of this document，customers can quickly understand SIM8260A module.

Associated with other software application notes and user guides, customers can use SIM8260A to design and develop mobile and laptop applications easily.

1.1 Product Outline

SIM8260A is a wireless communication module focusing on 5G market; it supports multi-air access technology including 5G NR (NSA/SA), LTE-FDD, LTE-TDD, and WCDMA, can meet the 3GPP R16 NR specification, and integrates GNSS[1] system including dual bands GPS, GLONASS, Beidou, Galileo and QZSS. The module's supported radio frequency bands are shown in the following table.

Table 1: SIM8260A frequency bands

Standard	Frequency bands
SIM8260A Module	
5G NR	n2/n5/n7/n12/n14/n25/n26/n41/n48/n66/n71/n77/n78
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B48/B66/B71
LTE-TDD	B41
WCDMA	B2/B4/B5
GNSS1	GPS L1+L5 dual bands/GLONASS/BeiDou/Galileo/QZSS

NOTE

1. GNSS function is optional. Standard modules do not support L5 by default.

The data transfer throughput of the module is shown in the table below.

Table 2: SIM8260Adata transfer throughput

Standard	Data transfer
SIM8260A Module	
Sub-6G SA	2.4Gbps(DL)/1Gbps(UL)
Sub-6G NSA	3.4Gbps(DL)/600Mbps(UL)
LTE	1.6Gbps(DL)/200Mbps(UL)
HSPA+	42Mbps(DL)/5.76Mbps(UL)

With a physical dimension of 41.0mm*43.6mm*2.8mm, SIM8260A can meet almost all requirements of customer’s applications.

With the 369 LGA pins, SIM8260A owns rich interfaces, includes USB3.1, PCIe3.0/4.0, SDIO3.0, (U)SIM card, digital audio (I2S or PCM), SPI, I2C, UART, GPIOs, four antennas for 3G/4G/5G and GNSS. For more details about the antenna pins, please refer to the pin definition.

With all these interfaces, SIM8260A Series can also be utilized in the handheld terminal, laptop application and especially the 5G CPE.

1.2 Hardware Block Diagram

The block diagram of SIM8260A is shown in the following figure.

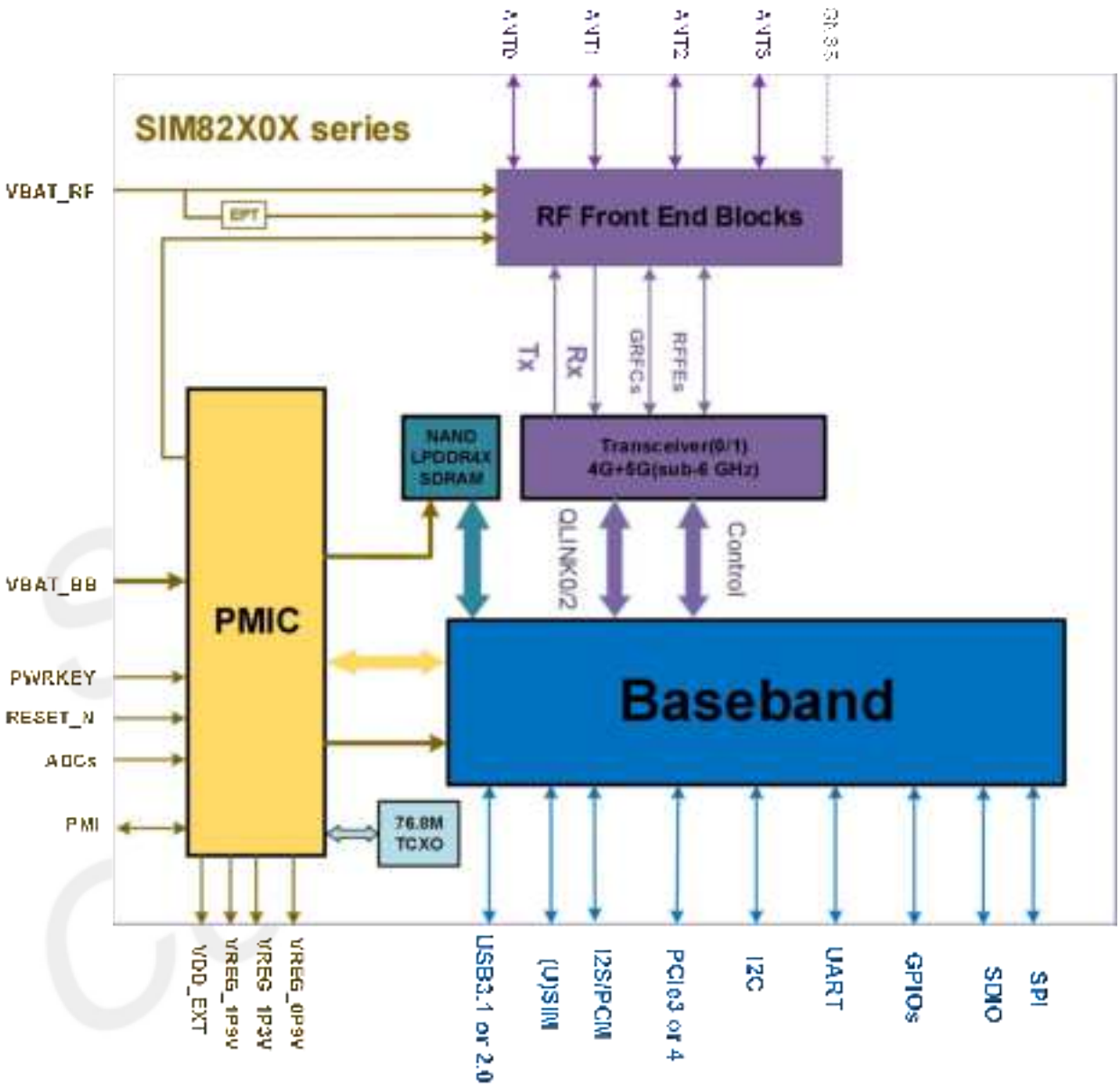

Figure 1: Module block diagram

1.3 Feature Overview

Table 3: Key features

Feature	Implementation
Application processor	Arm Cortex-A7 up to 1.8 GHz
Memory RAM	4Gb 16-bit LPDDR4X at 2.13 GHz, 8Gb optional*
Memory ROM	4Gb 8-bit NAND, 8Gb optional*
Power supply	VBAT:3.3V～4.4V Typical: 3.8V
Power consumption	Typical: 2.6 mA @sleep mode (GNSS off, VBAT=3.8V)
Transmit power	Power Class 3 for WCDMA/LTE/5G NR Power Class 2 for 5G NR(n41/n77/n78/n79)
Antenna	Five antennas for 3G/4G/5G/GNSS
GNSS (optional)	GNSS engine: GPS L1+L5/GLONASS/BeiDou/Galileo/QZSS Protocol: NMEA
SMS	MT, MO, CB, Text and PDU mode SMS storage: (U)SIM card or ME (default) Transmission of SMS alternatively over CS or PS.
(U)SIM interface	Support identity card: 1.8V/ 3.0V Include (U)SIM1 and (U)SIM2 interfaces Support Dual SIM single standby
(U)SIM application toolkit	Support SAT class 3 Support USAT
Phonebook management	Support phonebook types: DC, MC, RC, SM, ME, FD, ON, LD, EN
Digital audio interface	One I2S interface with dedicated main clock for primary digital audio, the I2S also can be configured as PCM ● MCLK frequency: 12.288MHz (default) ● WCDMA AMR-NB ● VoLTE AMR-WB ● Echo cancellation ● Noise suppression
PCIe interface	● Two lane PCIe interfaces, support PCIe Gen 3 (Gen 1/2 compatible), which up to 8Gbps per lane. ● One lane PCIe interfaces, support PCIe Gen 4, which up to 16Gbps per lane.
WLAN/BT interface	Support W82[2] interface, which support 802.11ax with 3.6Gbps, support BT5.2
PMI interface[3]	Support PM7250B interface, which support USB Type-C, QC4.0* and USB-PD3.0*
UART interface	● Default Support up to three UART ● Data rate up to 4 Mbps
I2C interface	● Default Support up to two I2C, meet I2C specification, version 5.0 ● Data rate up to 400 Kbps

SPI interface	● Only support master mode ● Data rate up to 50Mbps
SDIO interface	● Support 4bit SD card or 8bit eMMC, meet SDIO3.0 specification ● 1.8V or 3.0V dual-voltage operation for SD card ● Clock output up to 200 MHz for SD card; up to 100 MHz for eMMC
USB interface	Support one USB controller, USB3.1 Gen2 or USB2.0 USB3.1: super speed, with data rate which up to 10Gbps USB2.0: high speed interface, support USB operations at low-speed and full-speed, which refer to USB1.0 and USB1.1
Firmware upgrade	Firmware upgrade over USB interface
Physical characteristics	Size: 41x43.6x2.8mm SIM8260A weight：11.45g (typical)
Temperature range	Normal operation temperature: -30°C to +70°C (3GPP compliant) Extended operation temperature: -40°C to +85°C[3] Storage temperature: -40°C to +90°C

NOTE

1. “*” means under development,for more information, please connect the SIMCom FAE teams.
2. W82 is SIMCom WiFi-6 module.
3. When Module is within the extended operation temperature range, Module is able to establish and maintain voice, data transmission, SMS and emergency call, etc. The performance may deviate slightly from the 3GPP specifications and will meet 3GPP specifications again when the temperature returns to normal operating temperature levels. It is strongly recommended that customers take heat dissipation measures to ensure that the junction temperature of the chip can’t be exceeded (for example, the temperature of the CPU cannot exceed 105°C).

2 Package Information

2.1 Pin Assignment Overview

All functions of the SIM8260A will be provided through 369 LGA pins. The following figure is the pin assignment of the module.

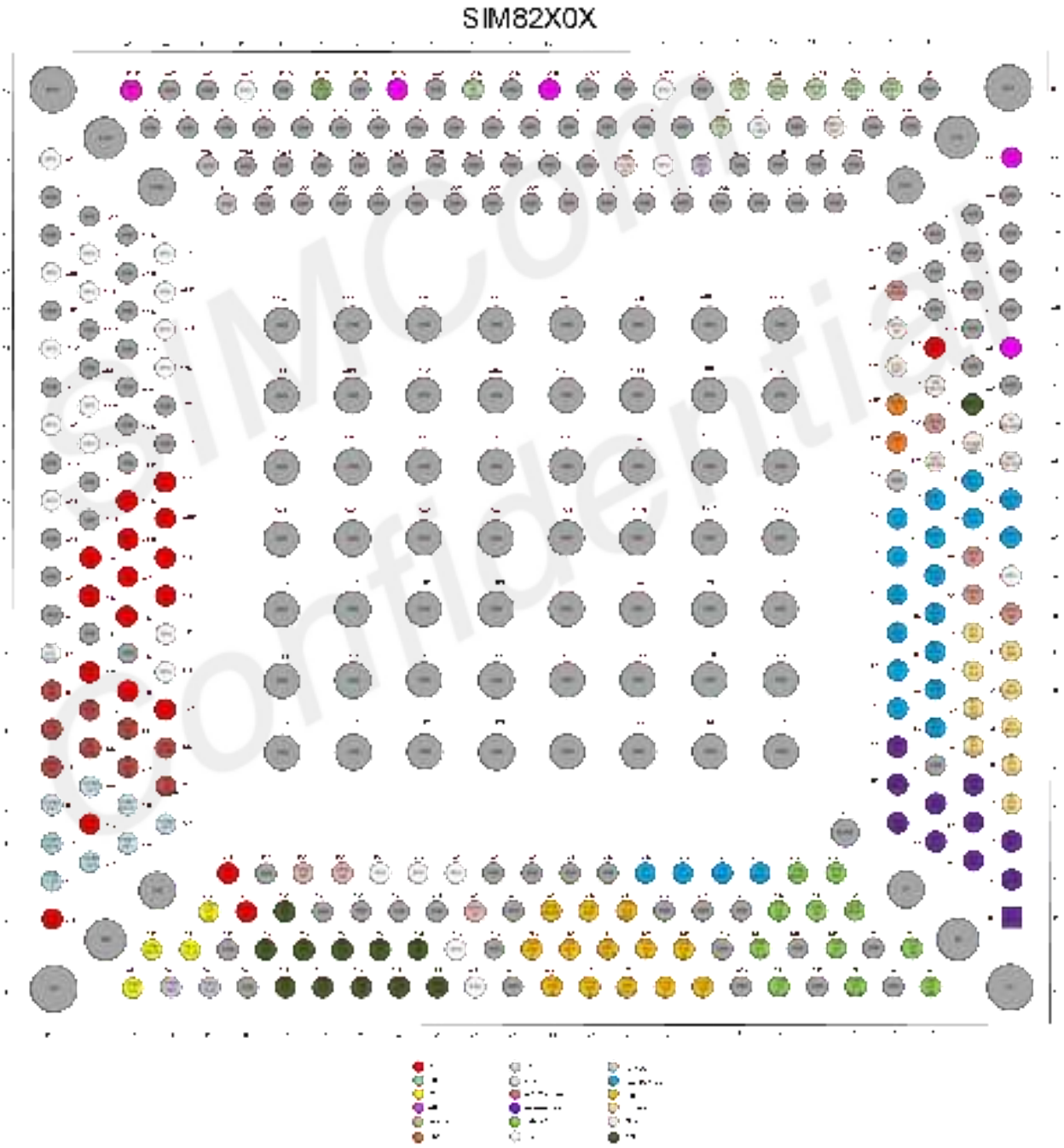

Figure 2: Pin assignment(Top View)

Table 4: Pin differences of SIM8260A

module name / M.2 pin number	SIM8260A
AR51	RFU
AG51	RFU
AL51	RFU
AC51	RFU
AM45	RFU
AT45	RFU
AK45	RFU
AP45	RFU
AT79	RFU
AH49	RFU
AF49	RFU
AP49	RFU
AW19	QTM_THERM
BA37	RFU
BA29	N79_TO_WL_TXEN
AY14	WL_TX_EN
AY1	GNSS ANT

2.2 Pin Description

Table 5: IO parameters definition

Pin type	Description
PI	Power Input
PO	Power Output
AI	Analog Input
AIO	Analog Input /Output
DIO	Bidirectional Digital Input /Output
DI	Digital Input
DO	Digital Output
PU	Pull Up
PD	Pull Down

Table 6: DC parameters definition

Voltage domain	Parameter		Min	Typ	Max
P2	VDD_P2=1.8V				
	V_{OH}	High level output	1.4V	-	-
	V_{OL}	Low level output	0V	-	0.45V
	V_{IH}	High level input	1.27V	-	2V
	V_{IL}	Low level input	0V	-	0.58V
	R_p	Pull up/down resistor	10K ohm	-	100K ohm
	VDD_P2=3.0V				
	V_{OH}	High level output	2.25V	-	3.0V
	V_{OL}	Low level output	0V	-	0.375V
	V_{IH}	High level input	1.84V	-	3.25V
	V_{IL}	Low level input	0V	-	0.75V
	R_p	Pull up/down resistor	10K ohm	-	100K ohm
P3	VDD_P3=1.8V				
	V_{OH}	High level output	1.35V	-	1.8V
	V_{OL}	Low level output	0V	-	0.45V
	V_{IH}	High level input	1.26V		2.1V
	V_{IL}	Low level input	0V	-	0.6V
	R_p	Pull up/down resistor	20K ohm	-	60K ohm
P4/P5	VDD_P4/P5=1.8V				

	V_{OH}	High level output	1.44V	-	1.8V
	V_{OL}	Low level output	0V	-	0.4V
	V_{IH}	High level input	1.26V	-	2.1V
	V_{IL}	Low level input	0V	-	0.36V
	R_p	Pull up/down resistor	10K ohm	-	100K ohm
	VDD_P4/P5=3.0V				
	V_{OH}	High level output	2.4V	-	3.0V
	V_{OL}	Low level output	0V	-	0.4V
	V_{IH}	High level input	2.1V	-	3.05V
	V_{IL}	Low level input	0V	-	0.6V
	R_p	Pull up/down resistor	10K ohm	-	100K ohm

Table 7: Pin description

Pin name	Pin no.	Electrical description		Description	Comment
Power supply					
VBAT_BB	V45, V49, U47	PI	V_{MAX}= 4.4V V_{TYP} =3.8V V_{MIN}=3 .3V	Input power supply for module's BB part	
VBAT_RF	Y49, AC47, AA47, W47, AD45, AB45, Y45	PI	V_{MAX}= 4.4V V_{TYP} =3.8V V_{MIN}=3 .3V	Input power supply for module's RF part	
VDD_EXT	AL5	PO	V_{TYP} =1.8V	Output power supply for external IO pull up circuits	
VREG_1P3	M45	PO	V_{TYP} =1.28 V	Output power supply for W82 only	
VREG_0P9	P49	PO	V_{TYP} =0.88 V	Output power supply for W82 only	
VREG_1P9	N47	PO	V_{TYP}= 1.88V	Output power supply for W82 and QTM	
L10E_3P1	C41	PO	V_{TYP}= 3.08V	Output power supply for PM7250B USB PD-PHY and USB switch	

VIO_OUT	D42	PO	V_{TYP}= 1.8V	Output power supply for PM7250B IO only	
GND	A7, B8, A11, B12, C15, A15, B16, C17, C19, D22, D24, D26, C27, A27, B28, D28, C31, C33, C35, C37, D40, A41, B42, J5, AD7, AJ1, AK3, AM3, AN1, AN5, AP3, AR1, AR5, AT3, AT7, AU1, AU5, AV3, AW1, R47, T49, U51, W51, AA51, AB49, AD49, AE47, AF45, AH45, AG47, AJ47, AL47, AN47, AR47, AU47, AV49, AW51, AV10, AV12, AV14, AV16, AV18, AV20, AV22, AV24, AV26, AV28, AV30, AV32, AV34, AV36, AV38,A V40, AV42, AW9, AW11, AW13, AW15, AW23, AW25, AW27, AW29, AW31, AW33,AW35, AW37, AW39, AW41, AW43, AY6, AY8, AY12, AY18, AY20, AY22, AY24,AY26, AY28, AY30, AY32, AY34, AY36, AY38, AY40, AY42, AY44, AY46, BA5, BA17, BA21, BA23, BA27, BA31, BA35, BA39, BA43, BA45, AM13, AM17, AM21, AM24, AM27, AM31, AM35, AM39, AH13, AH17, AH21, AH24, AH27, AH31, AH35, AH39, AE13, AE17, AE21, AE24, AE27, AE31, AE35, AE39, AA13, AA17, AA21, AA24, AA27, AA31, AA35, AA39, U13, U17, U21, U24, U27, U31, U35, U39, P13, P17, P21, P24, P27, P31, P35, P39, K13, K17, K21, K24, K27, K31, K35, K39, A1, B4, C7, A51, B48, C45, BA1, AY4, AW7, BA51, AY48, AW45, AM49, AK49, AE51, AJ51, AN51, AU51				
System control					
PWRKEY	A45	DI	1.1V	Power on/off the module, active low	Pull up to 1.2V internally without PM7250B
RESIN_N	A43	DI	P3	Reset the module, active low	Pull up to 1.8V inside the module
Status indicator					
STATUS	AJ5	DO	P3	Indicate Module is on	PMU_GPIO_13
NET_STATUS	AE1	DO	P3	Indicate network activity status of the module	PMU_GPIO_14
TDD_SYNC_PPS	AW21	DO	P3	1.It can generate pulse use for indication NSA and SA sub6 the beginning frame flag of DL-UL 2.TDD_SYNC_PPS Can be Configuration to GPS_1PPS	1.8V voltage domain. The TDD_SYNC_PPS and GPS_1PPS function can't be used at the same time. GPIO_32
USB_BOOT	D12	DI	P3	Module will be forced into USB boot mode by connect to VDD_EXT externally	GPIO_42, this pin can't be pulled up before power on
W_DISABLE	AG1	DI	P3	Flight mode control input active low	GPIO_86
SLEEP_OUT	AF3	DO	P3	Module in Sleep mode output signal to external AP active high	GPIO_97
USB interface					
USB_VBUS	C9	AI		USB VBUS detection	Not support charge
USB_HS_DP	B6	AIO		Differential USB bi-directional data plus	Required 85Ω differential impedance
USB_HS_DM	A5	AIO		Differential USB bi-directional data minus	Compliant with USB 2.0 standard specifications

USB_SS_TX_P	A13	AO		USB3.1 super-speed transmit data plus	Required 85Ω differential Impedance Compliant with USB 3.1 standard specifications
USB_SS_TX_M	B14	AO		USB3.1 super-speed transmit data minus	
USB_SS_ RX_P	B10	AI		USB3.1 super-speed receive data plus	
USB_SS_RX_M	A9	AI		USB3.1 super-speed receive data minus	
USB_ID*	C11	DI	P3	USB ID	If unused, please keep open
OTG_EN*	D10	DO	P3	USB OTG power supply DC-DC enable signal	
USB_SS_SW	C13	DO	P3	USB Type-C switch control signal, Used without PM7250B	
PM7250B interface[2]					
CHG_SYS_OK	C43	DI		When charger input is inserted, PM7250B output signal to Module. When the charging chip is not used, this pin can be connected to GND to realize the power-on function	
FAULT_N	B44	DIO		Used to send/receive the fault condition across all PMICs in the chipset	
SPMI_CLK	A47	DO		SPMI communication bus clock signal	Required 50Ω impedance
SPMI_DATA	B46	DIO		SPMI communication bus data signal	
(U)SIM interface					
(U)SIM1_VDD	B51	PO	P4	Power supply for (U)SIM1 card	1.8/3.0V voltage domain, (U)SIM interface should be protected against ESD. If unused, please keep open
(U)SIM1_DATA	E51	DIO	P4	(U)SIM1 card data signal, which has been pulled up to (U)SIM1_VDD by a 20K resistor in Module	
(U)SIM1_CLK	D49	DO	P4	(U)SIM1 clock signal	
(U)SIM1_RST	C51	DO	P4	(U)SIM1 reset signal	
(U)SIM1_DET	E47	DI	P3	(U)SIM1 card detect signal, which need pulled up to VDD_EXT by a 470K resistor externally	
(U)SIM2_VDD	F49	PO		Power supply for (U)SIM2 card	

(U)SIM2_DATA	G47	DIO	P5	(U)SIM2card data, which has been pulled up to (U)SIM2_VDD by a 20K resistor in Module	
(U)SIM2_CLK	H49	DO	P5	(U)SIM2 clock signal	
(U)SIM2_RST	G51	DO	P5	(U)SIM2 reset signal	
(U)SIM2_DET	F45	DI	P3	(U)SIM2 card detect, which need pulled up to VDD_EXT by a 470K resistor externally	
SPI interface					
SPI_CS_N	D18	DO	P3	SPI chips select	
SPI_CLK	D20	DO	P3	SPI clock	
SPI_MOSI	D14	DO	P3	Master output slaver input	
SPI_MISO	D16	DI	P3	Master input slaver output	
UART1 interface					
UART1_CTS	AA1	DI	P3	Clear to send	Default use for AT command
UART1_RTS	AC1	DO	P3	Request to send	
UART1_TXD	AB3	DO	P3	Transmit data	
UART1_RXD	AD3	DI	P3	Receive data	
UART1_DCD	W5	DO	P3	Carrier detect	If not need 7-wire UART, these signals can be used as GPIO
UART1_RI	AA5	DO	P3	Ring indicator	
UART1_DTR	AC5	DI	P3	Data terminal ready	
BT UART interface					
BT_UART_CTS	R5	DI	P3	Clear to send	Default use for BT
BT_UART_RTS	U5	DO	P3	Request to send	
BT_UART_TXD	T7	DO	P3	Transmit data	
BT_UART_RXD	V7	DI	P3	Receive data	
Debug UART interface					
DBG_UART_RXD	L5	DI	P3	Receive data	Used for debug only
DBG_UART_TXD	N5	DO	P3	Transmit data	
I2C interface[1]					
I2C1_SCL	M7	OD	P3	I2C1 clock signal	I2C1 default use for codec Pull up to VDD_EXT externally
I2C1_SDA	P7	OD	P3	I2C1 data signal	
I2C2_SCL	AB7	OD	P3	I2C2 clock signal	I2C2 default use for sensor Pull up to VDD_EXT Externally FOR EBI LCD PIN AB7 GPIO84 for EBI LCD_TE PIN Y7 GPIO85 for EBI LCD_RESET
I2C2_SDA	Y7	OD	P3	I2C2 data signal	

BT I2S interface					
BT_ I2S_DOUT	K3	DO	P3	I2S data output	Default use for W82
BT_ I2S_DIN	M3	DI	P3	I2S data input	
BT_I2S_CLK	J1	DO	P3	I2S bit clock	
BT_ I2S_WS	G1	DO	P3	I2S word select	
I2S Audio Codec interface					
I2S_DOUT/ PCM_DOUT	N1	DO	P3	I2S/PCM data output	Default is I2S interface, can be configured as PCM interface by software. If unused, please keep open
I2S_DIN/ PCM_DIN	R1	DI	P3	I2S/PCM data input	
I2S_CLK/ PCM_CLK	P3	DO	P3	I2S/PCM clock output	
I2S_WS/ PCM_SYNC	T3	DIO	P3	I2S word select/ PCM synchronous signal	
I2S_MCLK	L1	DO	P3	I2S master clock output	
CDC_RST_N	AK7	DO	P3	Module reset the external codec active low	Soft Default not supported
ADC interface					
ADC0	AH7	AI		Analog to digital converter input0	For EBI LCD_backlight_contrl
ADC1	AF7	AI		Analog to digital converter input1	
PCIe interface					
PCIe_REFCLK_P	B22	AIO		PCIe reference clock plus	Required 85Ω differential impedance
PCIe_REFCLK_M	A21	AIO		PCIe reference clock minus	
PCIe_TX0_M	B18	AO		PCIe transmit0 minus	
PCIe_TX0_P	A17	AO		PCIe transmit0 plus	
PCIe_TX1_M	B20	AO		PCIe transmit1 minus	
PCIe_TX1_P	A19	AO		PCIe transmit1 plus	
PCIe_RX0_M	A25	AI		PCIe receive0 minus	
PCIe_RX0_P	B26	AI		PCIe receive0 plus	
PCIe_RX1_M	A23	AI		PCIe receive1 minus	
PCIe_RX1_P	B24	AI		PCIe receive1 plus	
PCIe_CLKREQ	C21	DIO	P3	PCIe clock request input low	CLKREQ and WAKE need pull up to VDD_EXT externally; When there is an external level conversion chip, CLKREQ,WAKE, RST all need to be pulled up Default as RC mode
PCIe_WAKE	C25	DI	P3	PCIe wake-up input low	
PCIe_RST	C23	DO	P3	PCIe reset output low	

W82 control interface[2]					
WL_SW_CTRL	K49	DI	P3	W82 switch control	If unused, please keep open
SDX_TO_WL_CTI	M49	DO	P3	W82 GPIO	
WL_TO_SDX_CTI	L47	DI	P3	W82 GPIO	
WL_PA_MUTING	H45	DO	P3	WLAN XFEM control for PA mute	
SLEEP_CLK	J51	DO		Sleep clock output for W82 only	
BT_EN	N51	DO	P3	W82 BT enable	If unused, please PD 10k
WL_EN	K45	DO	P3	WLAN enable	
WL_LAA_RX	J47	DO	P3	WLAN XFEM control for LAA receiver	SIM8260C not support LAA, unused please PD 10k to GND
WL_LAA_AS_EN	L51	DO	P3	WLAN LAA AS enable	
COEX_UART_TXD	BA7	DO	P3	LTE&WLAN coexistence data transmit	LTE coexistence signals
COEX_UART_RXD	BA9	DI	P3	LTE&WLAN coexistence data receive	
WL_TXEN_TO_N79	BA37	DI	P3	From Module N79 to the W82	N79 and WIFI coexistence signals SIM8260E/A unused, please keep open
N79_TO_WL_TXEN	BA29	DO	P3	From the W82 to Module N79	
WL_LAA_TX_EN	R51	DO	P3	From Module to the W82	SIM8260C/E/A unused, please keep open
WL_TX_EN	AY14	DI	P3	From the W82 to Module	SIM8260C unused, please keep open
SDIO interface					
SDIO_VDD[3]	F7	PI	1.8/3.0V	Power input for internal SDIO circuit	
SDIO_DATA0	B1	DIO	P2	SDC data bit 0 or eMMC data bit 0	Required 45Ω impedance and length match<1mm Layout bus length <15mm(208MHZ) <100mm(50MHZ) SD card can support 1.8V/3.3V, but eMMC only support 1.8V
SDIO_DATA1	C1	DIO	P2	SDC data bit 1 or eMMC data bit 1	
SDIO_DATA2	D3	DIO	P2	SDC data bit 2 or eMMC data bit 2	
SDIO_DATA3	F3	DIO	P2	SDC data bit 3 or eMMC data bit 3	
SDIO_CMD	G5	DIO	P2	SDC command output	
SDIO_CLK	E5	DO	P2	SDC clock output	
SDIO_VDD_EN	H7	DO	P3	Enable the SD card power or eMMC data bit 4	
SDIO_DET	E1	DI	P3	SD card insertion detect or eMMC data bit 5	

GPIO100	H3	DIO	P3	eMMC data bit 6	
GPIO101	K7	DIO	P3	eMMC data bit 7	
RESOUT_N	AW17	DO	P3	eMMC RST_N	
EBI2 interface					
EBI2_AD_0	A33	DO	P3	EBI2 data0	
EBI2_AD_1	A39	DO	P3	EBI2 data1	Required 50Ω impedance, Standard software not supported EBI2 interface The EBI2 interface and the internal NAND of the module share the interface, there can be no pull-up or pull-down externally, and the external length is preferably less than 100mm
EBI2_AD_2	B34	DO	P3	EBI2 data2	
EBI2_AD_3	B38	DO	P3	EBI2 data3	
EBI2_AD_4	C39	DO	P3	EBI2 data4	
EBI2_AD_5	B36	DO	P3	EBI2 data5	
EBI2_AD_6	B40	DO	P3	EBI2 data6	
EBI2_AD_7	A37	DO	P3	EBI2 data7	
EBI2_WE_N	A35	DO	P3	EBI2_WE_N	
EBI2_ CLE	A31	DO	P3	EBI2_ CLE	
EBI2_RE_N	B32	DI	P3	EBI2_RE_N	
EBI2 _CS	AH3	DI	P3	EBI2_LCD_CS	
mmW interface					
IFH1	AR51	AIO		Horizontal polarization IF output signal and control signal for mmW RFIC device 1	If unused, please keep open
IFH2	AG51	AIO		Horizontal polarization IF output signal and control signal for mmW RFIC device 2	
IFH3	AL51	AIO		Horizontal polarization IF output signal and control signal for mmW RFIC device 3	
IFH4	AC51	AIO		Horizontal polarization IF output signal and control signal for mmW RFIC device 4	
IFV1	AM45	AIO		Vertical polarization IF output signal and local oscillator (LO) signal for mmW RFIC device 1	
IFV2	AT45	AIO		Vertical polarization IF output signal and local oscillator (LO) signal for mmW RFIC device 2	
IFV3	AK45	AIO		Vertical polarization IF output	

				signal and local oscillator (LO) signal for mmW RFIC device 3	
IFV4	AP45	AIO		Vertical polarization IF output signal and local oscillator (LO) signal for mmW RFIC device 4	
QTM0_PON	AT49	DO	P3	Power on/reset 0 for QTM module	
QTM1_PON	AH49	DO	P3	Power on/reset 1 for QTM module	
QTM2_PON	AF49	DO	P3	Power on/reset 2 for QTM module	
QTM3_PON	AP49	DO	P3	Power on/reset 3 for QTM module	
QTM_THERM	AW19	AI		QTM thermal detect	Only QTM547 support thermal detect If unused, please keep open
GPIO interface					
GPIO106	AY10	DIO	P3	Used for GPIO	
GPIO47	AE5	DIO	P3	Used for GPIO	
GPIO105	D38	DIO	P3	Used for GPIO	
GPIO31	C29	DIO	P3	Used for GPIO	
GPIO102	D36	DIO	P3	Used for GPIO	
GPIO107	U1	DIO	P3	Used for GPIO	
GPIO82	V3	DIO	P3	Used for GPIO	
GPIO83	Y3	DIO	P3	Used for GPIO	
GPIO88	AG5	DIO	P3	Used for GPIO	
GPIO96	AM7	DIO	P3	Used for GPIO	
PMU_GPIO6	AP7	DIO	1.8V	Used for GPIO	
Antenna control interface[4]					
RFFE0_CLK	BA11	DO	P3	Antenna tuner MIPI CLK	Required 50Ω impedance
RFFE0_DATA	BA13	DIO	P3	Antenna tuner MIPI DATA	
ANT_CTRL0	BA15	DO	P3	Antenna tuner control0	
ANT_CTRL1	AY16	DO	P3	Antenna tuner control1	
ANT interface					
GNSS ANT	AY1	AI		Receiving GNSS signals 1166MHz~1229MHz 1565MHz~1610MHz	
SIM8260A Module					
ANT0	AL1	AIO		4G/5G LB/MHB TX0/DRX, 5G N41/77/78/79	617MHz~894MHz 1710MHz~2690MHz

				TX0/DRX_MIMO	3300MHz~5000MHz
ANT1	BA25	AI		4G/5G MHB DRX_MIMO, 5G N77/78/79 DRX 4G LAA DRX	1930MHz~2690MHz 3300MHz~5925MHz
ANT2	BA33	AI		4G/5G MHB PRX_MIMO, 5G N77/78/79 PRX_MIMO, 4G LAA PRX	1930MHz~2690MHz 3300MHz~5925MHz
ANT3	BA47	AIO		4G/5G LB TX1/PRX, 5G MHB TX1/DRX, 5G N41/77/78/79 TX1/PRX	617MHz~894MHz 1710MHz~2690MHz 3300MHz~5000MHz
RFU PIN					
RFU	BA41, AY51, BA19, B30, A29, D32, D30, D34, T45, P45, W1				Reserved for future use
MARK	D9				PIN used inside the module, keep it floating externally

NOTE

1. The I2C signals need pull up to VDD_EXT by 2.2K resistors out of the module.
2. Only used to W82 and PM7250B pins don't use as other circuits.
3. If not use SDIO function, the SDIO_VDD pin should connect to VDD_EXT out of the module.
4. Please confirm with SIMCom for the detail design about Antenna control interface.
5. "*" means under development, for more information, please connect the SIMCom FAE support team.

- RFU pins should keep open.
- Recommend add ESD protect components to the interface that is touched by human hands. (e. g. SIM/SD/USB/BUTTOM/ANT)
- The GPIO MAX voltage is 2.1V, if exceeded, may cause permanent damage to the module.
- All GND pins should be connected to the customer's main PCB.
  For SIM8260A module BA37 RFU.

2.3 Mechanical Dimensions

The following figure shows the mechanical dimensions of SIM8260A.

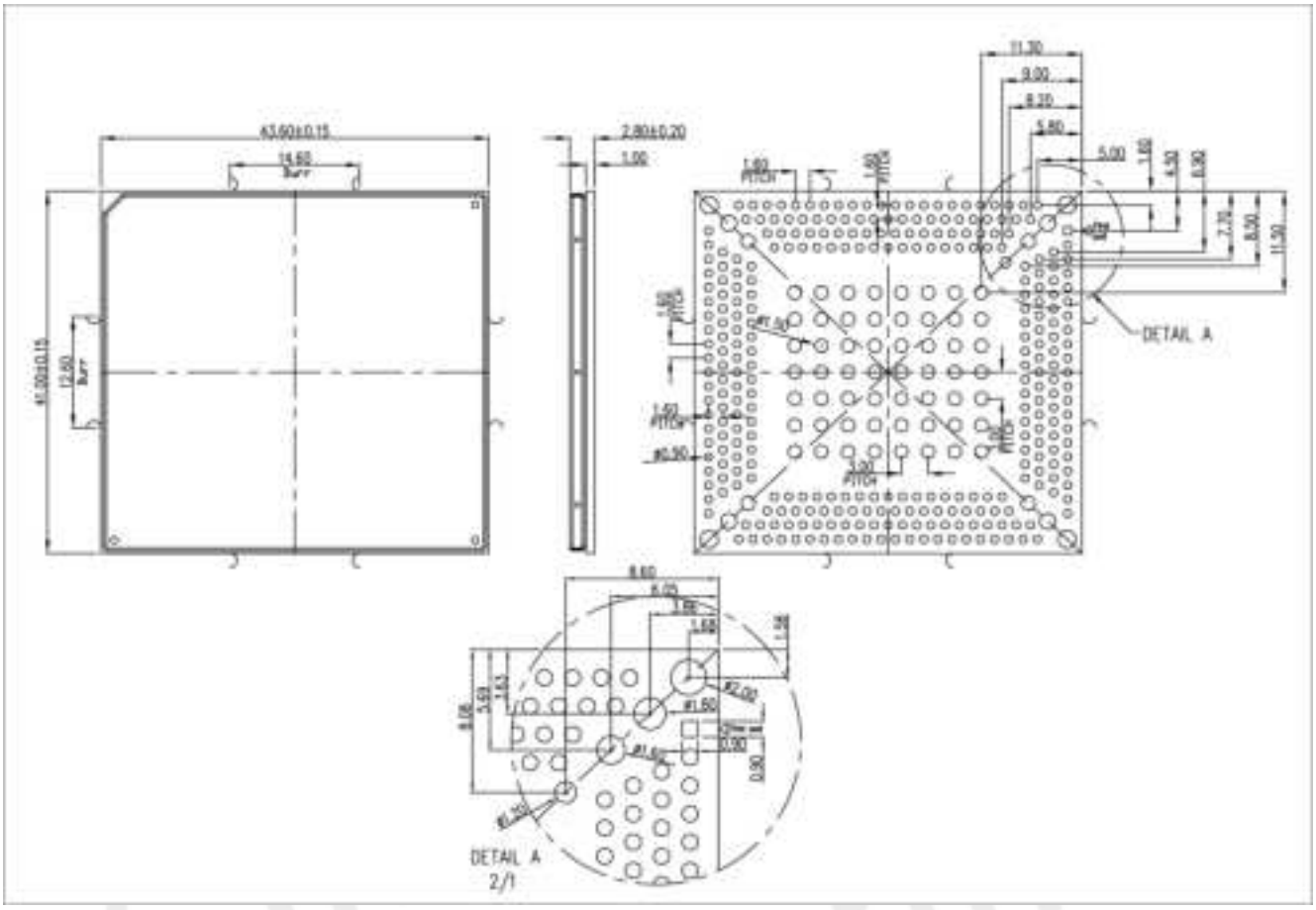

Figure 3: Dimensions of SIM8260A (unit: mm)

3 Interface Application

3.1 Power Supply

The recommended power supply for SIM8260A is 3.8V and the voltage range from 3.3V to 4.4V. It is necessary to ensure that the voltage of VABT cannot be lower than 3.3V after the maximum voltage drop. the module will be powered off automatically. The max voltage is not higher than 4.4V, otherwise the module may be permanently damaged.
The module has 3 BB power pins, 7 RF power pins and 10 power ground pins, to ensure the module works normally, all power and ground pins should be connected.

Table 8: VBAT pins electronic characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
VBAT[1]	Module power supply voltage	3.3	3.8	4.4	V
I_{peak}	Peak current	-	-	1.8	A
$I_{peak\ (QTM545)}$	Peak current at maximum power	-	-	1.0	A
$I_{peak\ (QTM547)}$	Peak current at maximum power	-	-	TBD	A
I_{sleep}	Current in sleep mode	-	4.5	-	mA
$I_{leakage}$	Current in power off mode	-	135	-	uA

NOTE

1. The VBAT include VBAT_BB and VBAT_RF pins in this document.
2.If the customer uses the charging chip PM7250B and the software with charging function, when the power supply voltage is lower than 3.3V, the module will not be powered on. If the customer wants o power on the module, the charger must be plugged in.

3.1.1 Power Supply Design Guide

When B2(20MHz) and N79(100MHz) ENDC combination are connected under the instrument, the peak current can reach to 1.8A at 3.8V power supply. In order to ensure that the VBAT voltage is no less than required 3.3V when the module at maximum power radio transmission, and considering the voltage drop and conversion efficiency, it is strongly recommended that the DC-DC or LDO output capacity should not be less than 3A.

This chapter is under development. The indicated peak power consumption data is an estimated value, not the final measured data. The data will be supplemented by subsequent versions.

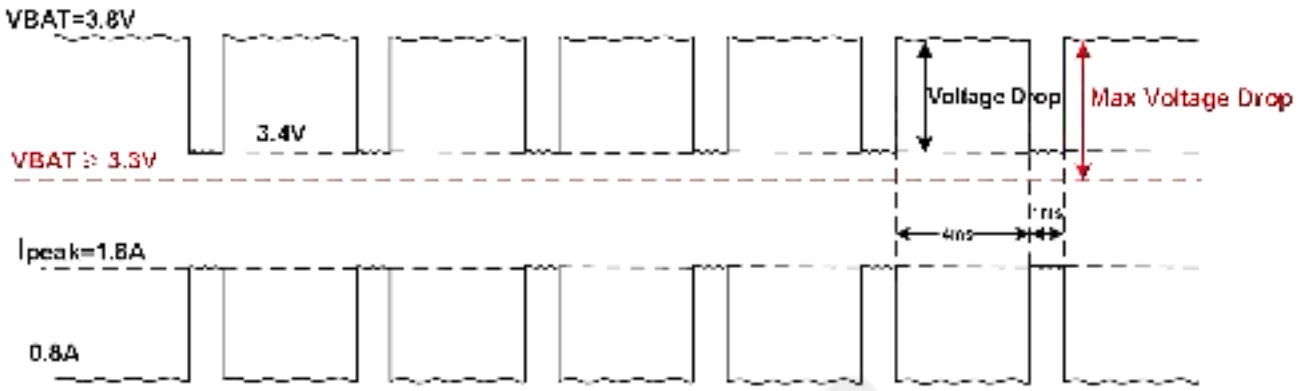

Figure 4: Power consumption at ENDC combination of B2 (20MHz) and N79 (100MHz)

NOTE

Test conditions

- The total capacitors of VBAT net are not less than 640uF.
- The peak current is only the current consumption of the module, don't include the current consumption of other devices outside the module.
- The I_{peak} and voltage drop data in Table and Figure above were tested using SIMCom EVB and connecting instrument at 3.8V power supply, the ENDC combination is B2 (20MHz) and N79 (100MHz), subcarrier spacing is 30KHz.
- The B2 (20MHz) and N79 (100MHz) ENDC combination is the max power consumption of the module.

When WLAN and Ethernet functions are added according to SIMCOM's reference design, the peak current of the entire system can reach 2.6A. For ensure the normal operation of the module and peripherals, it is strongly recommended that the DC-DC or LDO output capacity is not less than 3A.

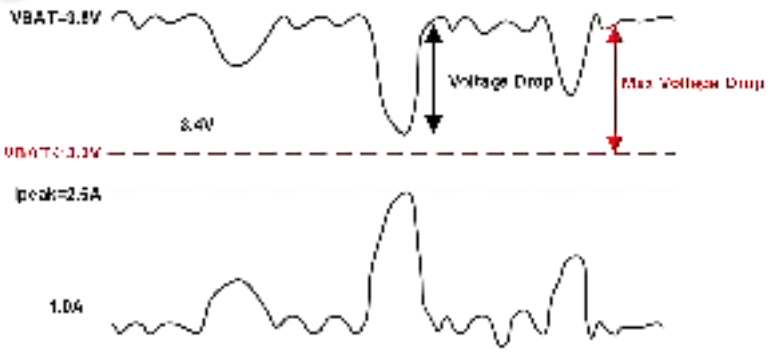

Figure 5: Power consumption of entire systeam

NOTE

Test conditions

- The above current consumption data is measured using SIMCOM EVB.
- The test current consumption data includes SIM8260A module, SIMCom WLAN module W82 and Ethernet PHY RTL8125B, to be added in subsequent versions.

To decrease the voltage dropping, make sure that the capacitors of VBAT net must not less than 640uF. The following figure shows the reference circuit of power supply for the VBAT.

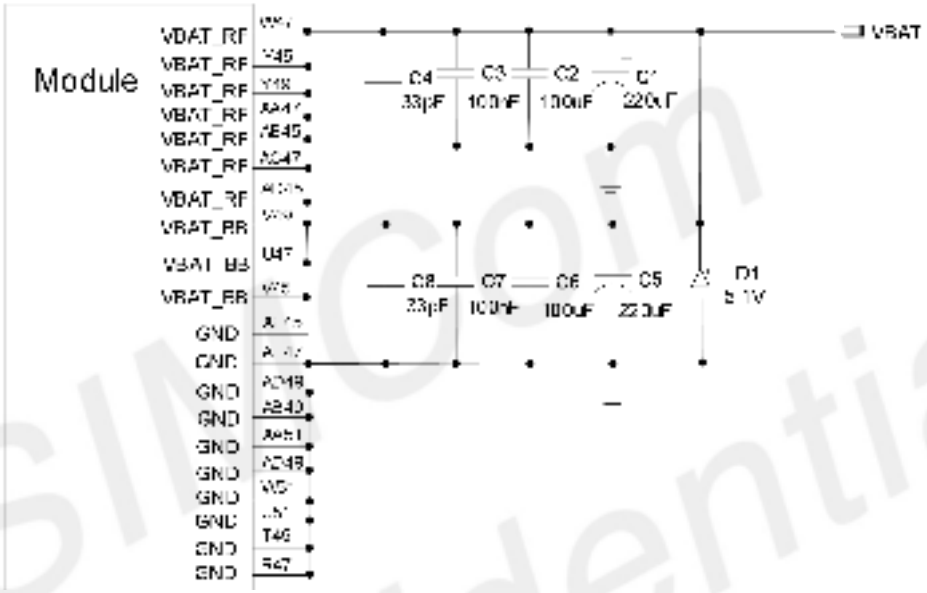

Figure 6: Power supply reference circuit

Table 9: Definition of VBAT and GND pins

Pin name	Pin no.	Electrical description	Description	Comment
VBAT_BB	V45, V49, U47	PI	V_{MAX}=4.4V V_{TYP} =3.8V V_{MIN}=3.3V	Input power supply for module's BB part
VBAT_RF	Y49, AC47, AA47, W47, AD45, AB45, Y45	PI	V_{MAX}=4.4V V_{TYP} =3.8V V_{MIN}=3.3V	Input power supply for module's RF part
GND	A7,B8,A11,B12,C15,A15,B16,C17,C19,D22,D24,D26,C27,A27,B28,D28,C31,C33,C35,C37,D40,A41,B42,J5,AD7,AJ1,AK3,AM3,AN1,AN5,AP3,AR1,AR5,AT3,AT7,AU1,AU5,AV3,AW1,R47,T49,U51,W51,AA51,AB49,AD49,AE47,AF45,AH45,AG47,AJ47,AL47,AN47,AR47,AU47,AV49,AW51,AV10,AV12,AV14,AV16,AV18,AV20,AV22,AV24,AV26,AV28,AV30,AV32,AV34,AV36,AV38,AV40,AV42,AW9,AW11,AW13,AW15,AW23,AW25,AW27,AW29,AW31,AW33,AW35,AW37,AW39,AW41,AW43,AY6,AY8,AY12,AY18,AY20,AY22,AY24,AY26,AY28,AY30,AY32,AY34,AY36,AY38,AY40,AY42,AY44,AY46,BA5,BA17,BA21,BA23,BA27,BA31,BA35,BA39,BA43,BA45,		

	AM13,AM17,AM21,AM24,AM27,AM31,AM35,AM39,AH13,AH17,AH21,AH24,AH27,AH31,AH35,AH39,AE13,AE17,AE21,AE24,AE27,AE31,AE35,AE39,AA13,AA17,AA21,AA24,AA27,AA31,AA35,AA39,U13,U17,U21,U24,U27,U31,U35,U39,P13,P17,P21,P24,P27,P31,P35,P39,K13,K17,K21,K24,K27,K31,K35,K39,A1,B4,C7,A51,B48,C45,BA1,AY4,AW7,BA51,AY48,AW45,AM49,AK49,AE51,AJ51,AN51,AU51

NOTE

- Both C1 and C5 are 220 μF tantalum capacitor (ESR=0.7Ω).
- C3, C4, C7 and C8 are multi-layer ceramic chip (MLCC) capacitors from 33pF to 1uF with low ESR in high frequency band, which can be used for EMC performance.
- D1 is used for surge protection.
- Pins AF45, AE47, AD49, AB49, AA51, AD49, W51, U51, T49 and R47 of GND are the main ground for power return.

Table 10: Recommended D1 list

Name	Manufacturer	Part number
D1	LRC	LEDZ5.1BT1G
	Prisemi	PZ5D4V2H

Power supply layout guidelines:

- Both VBAT and return path should be as short and wide as possible to minimize the voltage drop.
- The width of VBAT_BB trace should be no less than 1.5mm, and the width of VBAT_RF trace should be no less than 2mm. ESR<20mΩ
- These capacitors should be placed as closely as possible to the VBAT_BB and VBAT_RF pins.
- The VBAT trace should pass through Zener diode and capacitors, and then pass through the VBAT pins. The small value capacitors should be placed close to the VBAT pins.
- The customer's PCB design must have a solid ground plane throughout the board as the primary reference plane for most signals.

3.1.2 Recommended Power Supply Circuit

It is recommended to use a switching mode power supply or a linear regulator power supply. Make sure it can provide the current up to 3A at least.
The following figure shows the linear regulator reference circuit with 5V input and 3.8V output.

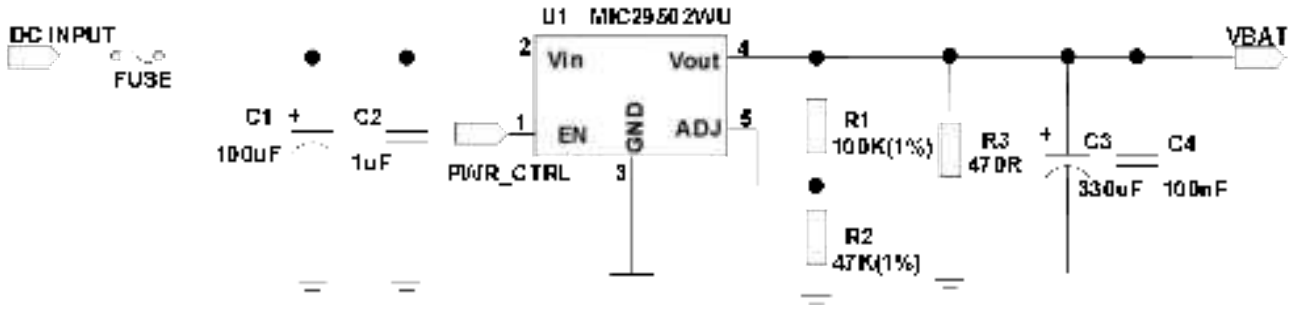

Figure 7: Linear regulator reference circuit

NOTE

- An extra minimum load of R3 is required, to ensure it work properly under light load in sleep mode and power off mode. For the details about minimum load, please refer to specification of MIC29502WU.

Table 11: Recommended power chip list

Name	Manufacturer	Model
U1	MICREL	MIC29502WU

The following figure shows the switching mode power supply reference circuit with 5~12V input and 3.8V output.

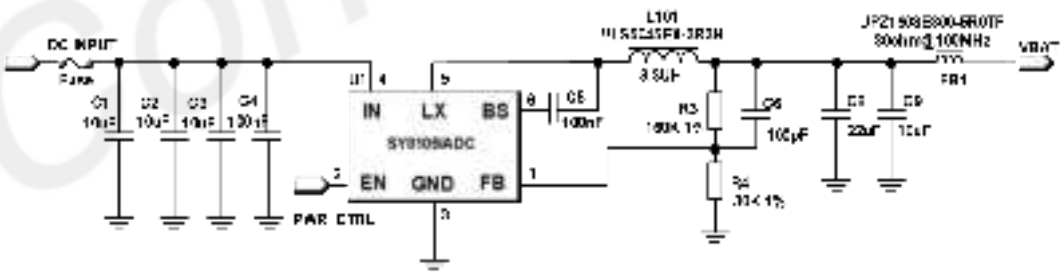

Figure 8: Switching mode power supply reference circuit

The following figure shows the switching mode power supply reference circuit with 8.8~16V input and 3.8V output.

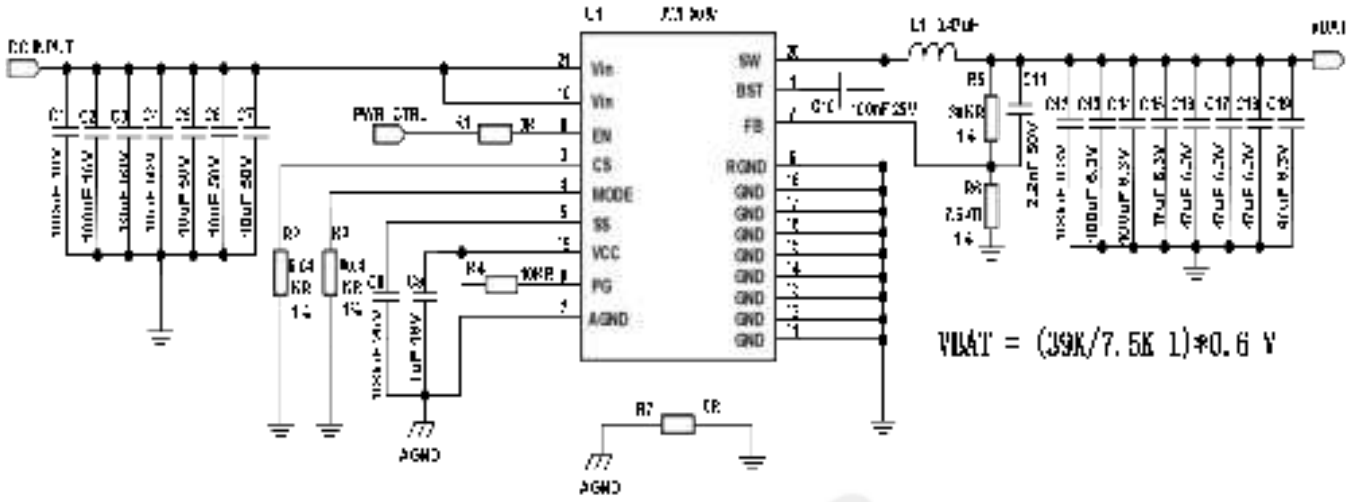

Figure 9: Switching mode power supply reference circuit for mmW

NOTE

- In order to avoid damaging the module, please do not switch off the power supply when module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
- It is suggested that customer's design should have the ability to switch off the power supply for module in abnormal state, and then switch on the power to restart the module.
- The PWR_CTRL signal recommend connect to the host and can be controlled.

Table 12: Recommended chip list

Name	Manufacturer	Model
Ferrite bead	Sunlord	UPZ1608E300-5R0TF
Power inductor	Coilcraft	XAL1010-451ME

3.1.3 Voltage Monitor

To monitor the VBAT voltage, the AT command “AT+CBC” can be used.

NOTE

- For more details about voltage monitor commands, please refer to Document [1] in the appendix.

3.2 Power On and Off Module

3.2.1 Power On

Drive the PWRKEY pin to a low level and hold it for 2 seconds, then release, the module will be powered on. This pin is already pulled up internally. The power on timing and electrical characteristics are listed in the following table, and the following figure shows the power on circuit.

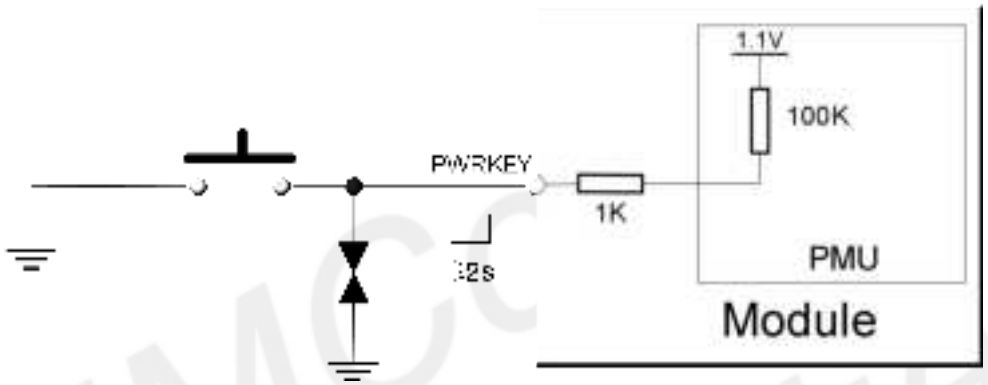

Figure 10: Power on the module use button

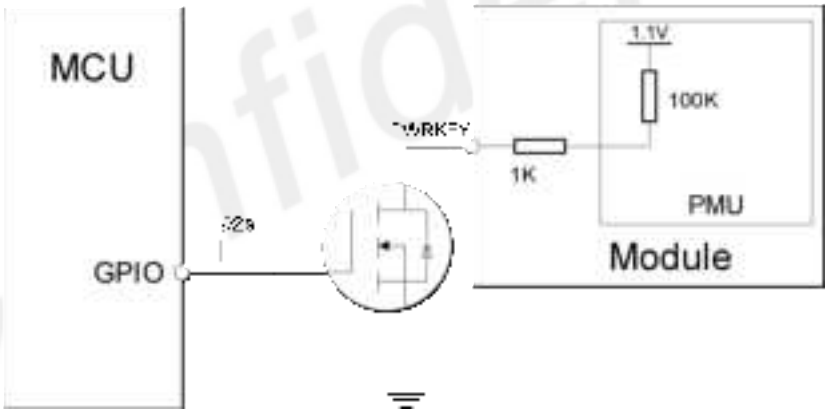

Figure 11: Power on the module use GPIO drive

Table 13: Definition of PWRKEY pin

Pin name	Pin no.	Electrical description	Description	Comment
PWRKEY	A45	DI	Power on/off the module, active low	

The power on sequence is shown in the following figure.

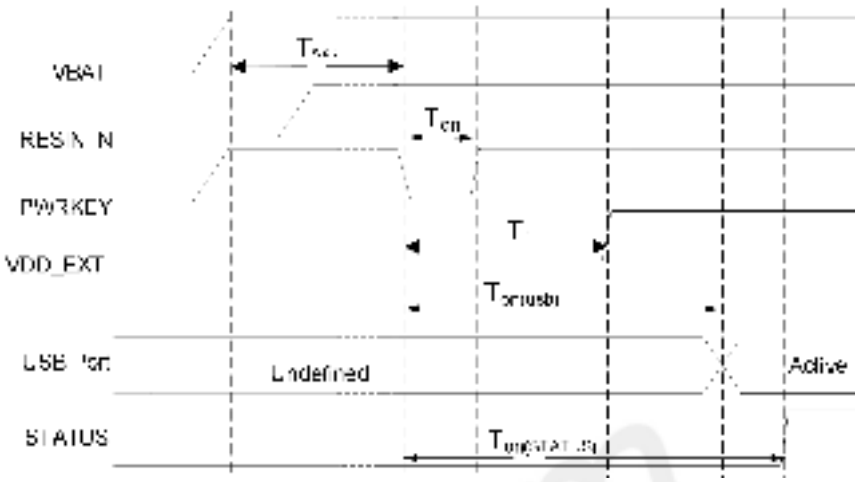

Figure 12: Power on sequence

Table 14: Power on timing and electronic characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{wait}	The waiting time from power supply available to power-on action	100	-	-	ms
T_{on}	The time of holding on PWRKEY pin to a low level	2	-	-	s
T_1	The time from power-on action to VDD_EXT ready	-	11.45	12	ms
$T_{on(usb)}$	The time from power-on action to USB port ready	-	20	-	s
$T_{on\ (STATUS)}$	The time from power-on action to STATUS ready	-	55	-	s
V_{IH}	Input high level voltage on PWRKEY pin	1.1	-	2.1	V
V_{IL}	Input low level voltage on PWRKEY pin	0	-	0.3	V

NOTE

- After enter force download mode, the PWRKEY pin need to release and don't pull low always. If not, the module will restart and then cause the download fail.
- The timing of $T_{on(usb)}$ and $T_{on\ (STATUS)}$ is related to the module software. The time here is based on the standard version test and is for reference only.

3.2.2 Power Off

The following methods can be used to power off the module.

- Method 1: Power off the module by holding the PWRKEY to a low level two second then release.
- Method 2: Power off the module by AT command "AT+CPOF".

NOTE

- If the temperature is outside the range of -30~+70°C, some warning will be reported via AT port.
- If the temperature is outside the range of -40~+85°C, module will be powered off automatically.
- For details about “AT+CPOF”, please refer to Document [1] in the appendix.

Normal power off action will make the module disconnect from the network, allow the software entered a safe state, and save key data before the module is powered off completely.

The power off sequence is shown in the following figure.

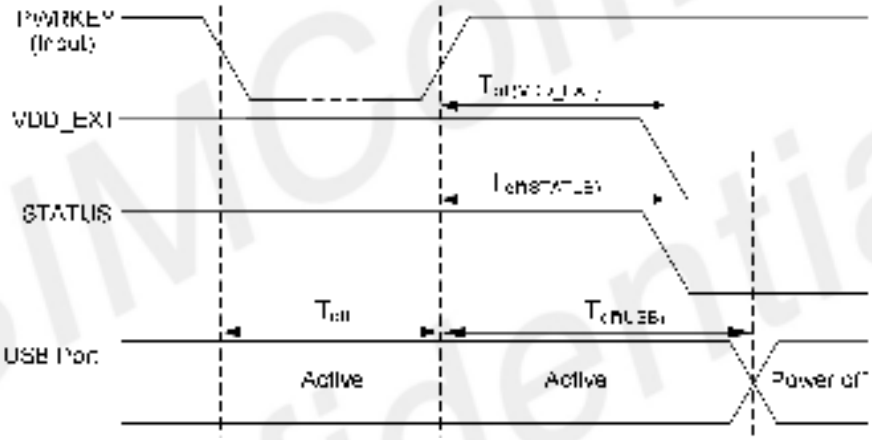

Figure 13: Power off sequence

Table 15: Power off timing and electronic characteristic

Parameter	Description	Time value			Unit
		Min.	Typ.	Max.	
T_{off}	The time of holding on PWRKEY pin to a low level	2	-	-	s
$T_{off(usb)}$	The time from power-off issue to USB port off	-	3.5	-	s
$T_{off(status)}$	The time from power-off issue to STATUS off	-	2.1	-	s

NOTE

- After pressing the PWRKEY button, you must wait for 12S to disconnect the power supply or press the PWRKEY again to turn on the module, otherwise it may damage the module or fail to turn on module.
- The timing of $T_{off(usb)}$ and $T_{off(status)}$ is related to the module software. The time here is based on the standard version test and is for reference only.

3.3 Reset Function

Module can be reset by driving the RESIN_N pin down to a low level.

The RESIN_N signal has been internally pulled up to 1.8V, so there is no need to pull it up externally. Please refer to the following figure for the recommended reference circuit.

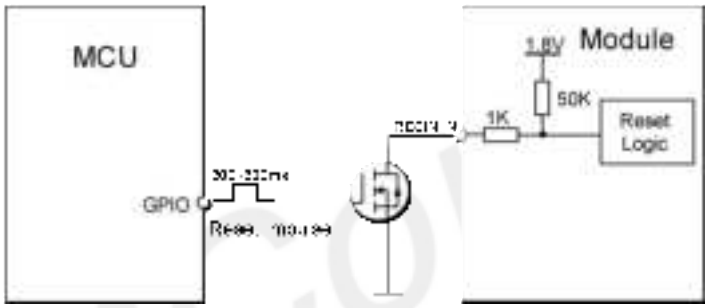

Figure 14: Reset the module use GPIO drive

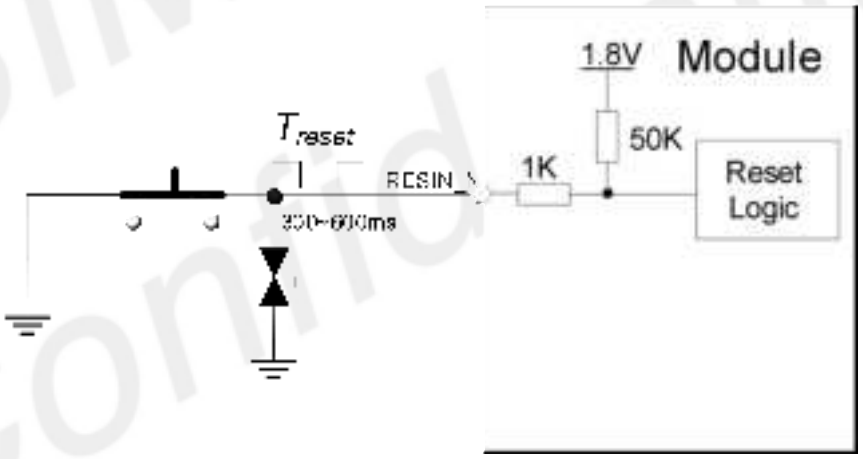

Figure 15: Reset the module use button

Table 16: Definition of RESIN_N pin

Pin name	Pin no.	Electrical description	Description	Comment
RESIN_N	A43	DI	P3	Reset the module, active low

The reset timing sequence of the module is shown in the following figure.

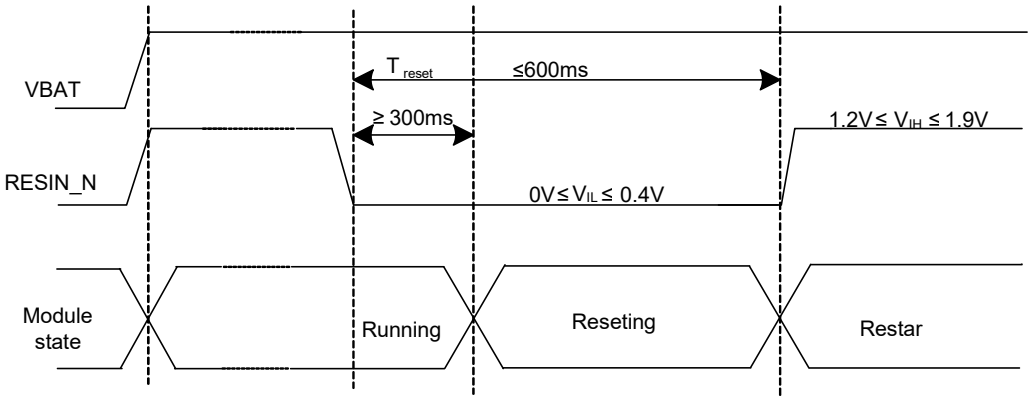

Figure 16: The reset timing sequence of the module

Table 17: RESET electronic characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
T_{reset}	The time of holding on RESIN_N pin to a low level	300	-	600	ms
V_{IH}	Input high level voltage	1.2	-	1.9	V
V_{IL}	Input low level voltage	0	-	0.4	V

NOTE

- Please ensure that there is no capacitance on RESIN_N pin.

3.4 Output Power Management

Table 18: Output power management summary

Pin name	Pin no	Typical voltage (V)	Rated current (mA)	Sleep state	Comment
VDD_EXT	AL5	1.8	50	LPM	Output power supply for external IO pull up circuits
VREG_1P3	M45	1.28	500	retention	Output power supply for W82 only
VREG_0P9	P49	0.88	1500	off	Output power supply for W82 only
VREG_1P9	N47	1.88	500	retention	Output power supply for W82 only
L10E_3P1	C41	3.08	30	off	Output power supply for PM7250B USB PD-PHY and USB switch
VIO_OUT	D42	1.8	0.2	on	Output power supply for PM7250B IO circuit only

3.4.1 VDD_EXT Reference Circuit

The following figure is the reference circuit diagram of the VDD_EXT pin periphery of the module.

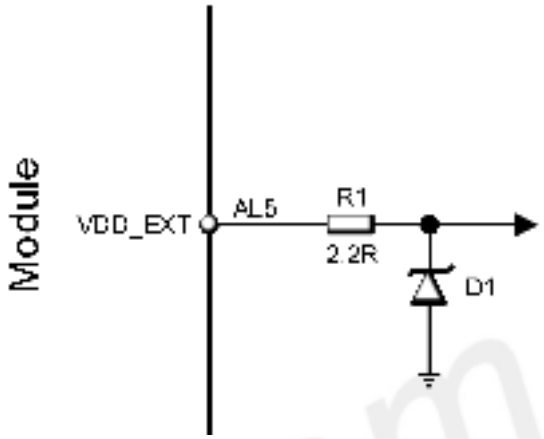

Figure 17: Module VDD_EXT peripheral reference circuit

NOTE

- It is recommended to place a TVS protection tube near the VDD_EXT pin of the module to protect the module pins. The recommended TVS models are shown in the following table.
- It is recommended to connect a 2.2R resistor in series with the VDD_EXT pin close to the module for ESD protection.

Table 19: Module VDD_EXT pin protection tube TVS recommended materials

NO.	Manufacturer	Model	Operating Voltage	package	Name
1	ON	ESD9L5.0ST5G	3.3V	SOD-923	D1
2	YAGEO	RC0402JR072R2L	-	0402	R1

3.5 USB Interface

SIM8260A has one USB controller，which complies with USB3.1 and USB2.0 specifications. The high-speed PHY and super-speed PHY share the same USB 3.1 Gen2 controller, customers can choose USB3.1 or USB2.0 for their needs. USB3.1 Gen2 data rate is up to 10Gbps.

The USB interface is used for AT command communication, data transmission, GNSS NMEA output, firmware upgrade and software debugging.

SIM8260A supports USB suspend and resume mechanism, which can save power consumption. If there is no data transmission on the USB bus, module will enter suspend mode automatically. The following figure is the USB reference circuit.

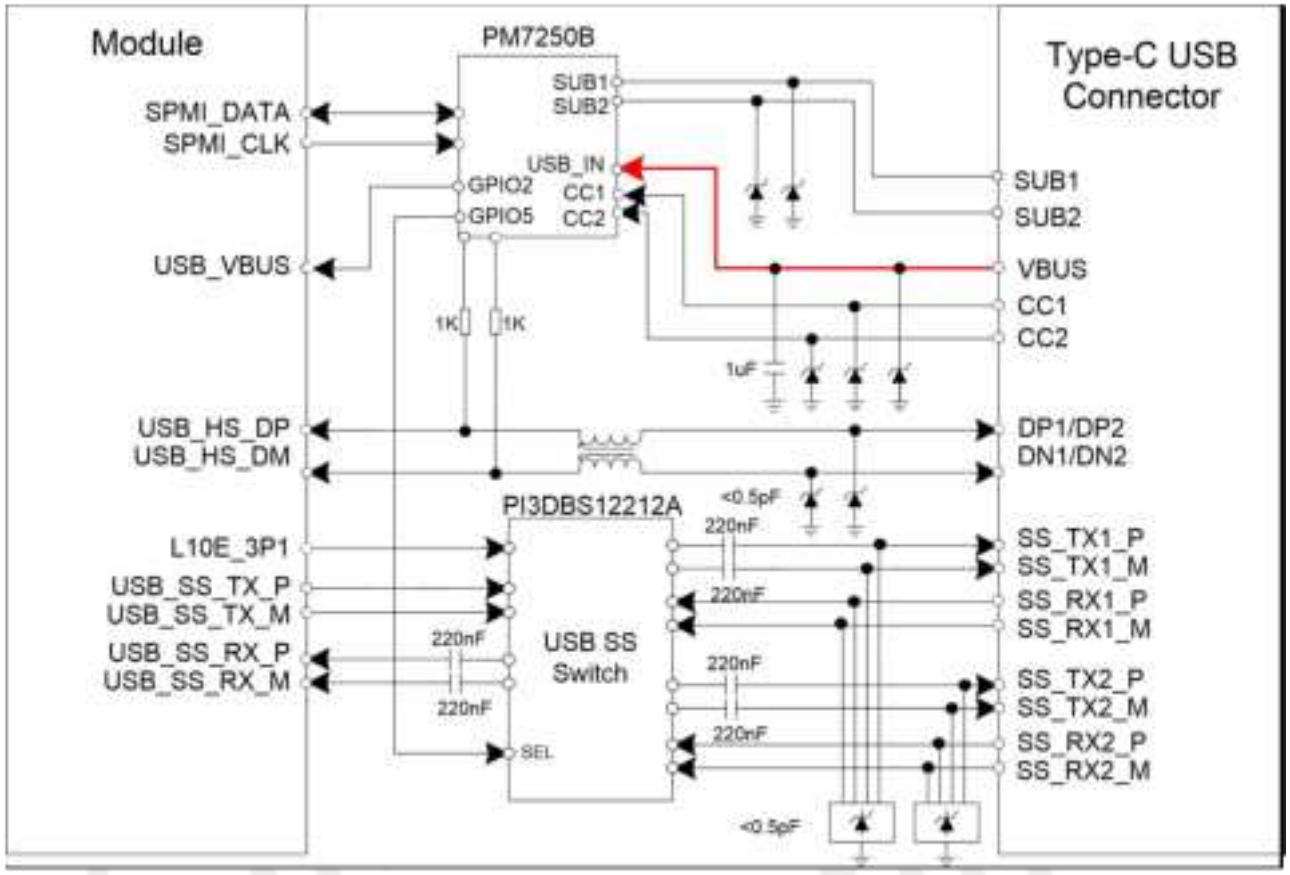

Figure 18: Type-C USB reference circuit with PM7250B

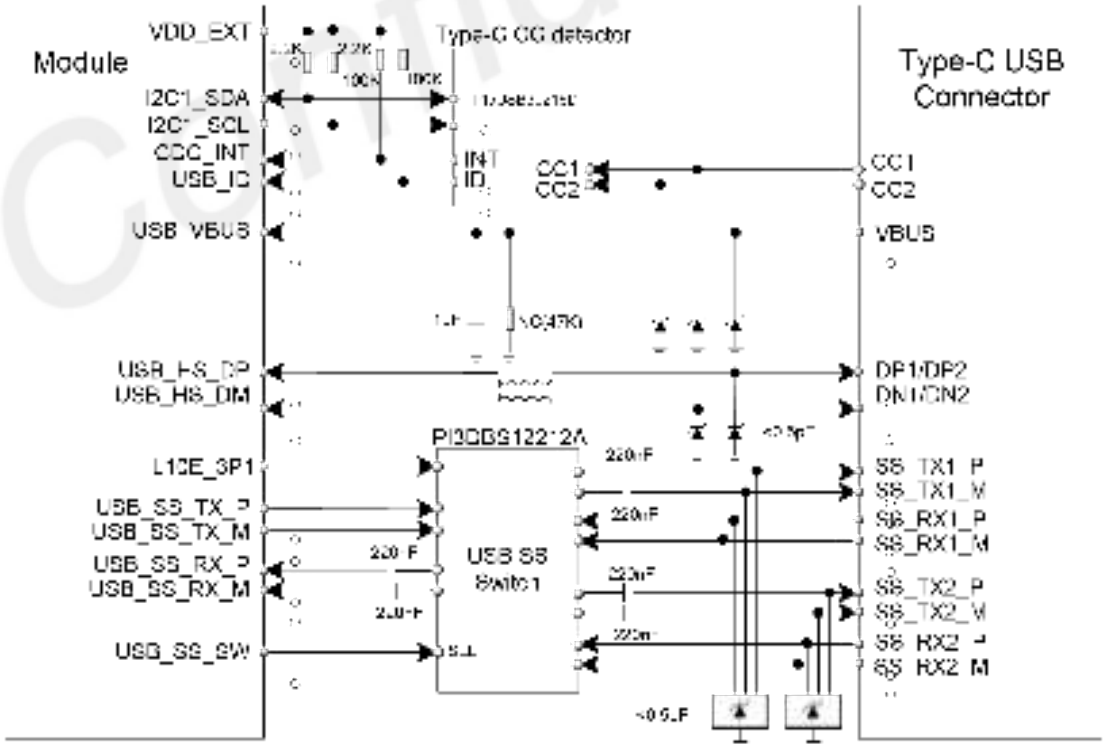

Figure 19: Type-C USB reference circuit with CC detector

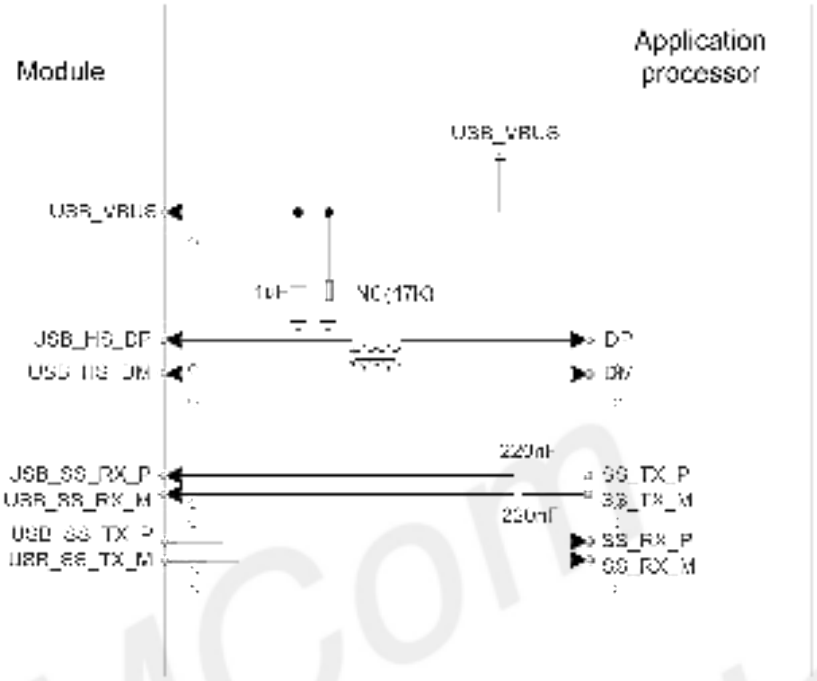

Figure 20: USB3.1 reference circuit

Table 20: Definition of USB interface

Pin name	Pin no.	Pin characteristics		Functional description	Comment
USB_VBUS	C9	AI		USB VBUS detection	Not support charge
USB_HS_DP	B6	AIO		Differential USB bi-directional data plus	Required 85Ω differential impedance Compliant with USB 2.0 standard specifications
USB_HS_DM	A5	AIO		Differential USB bi-directional data minus	
USB_SS_TX_P	A13	AO		USB3.1 super-speed transmit data plus	Required 85Ω differential Impedance Compliant with USB 3.1 standard specifications
USB_SS_TX_M	B14	AO		USB3.1 super-speed transmit data minus	
USB_SS_ RX_P	B10	AI		USB3.1 super-speed receive data plus	
USB_SS_RX_M	A9	AI		USB3.1 super-speed receive data minus	
USB_ID	C11	DI	P3	USB ID	Standard software not supported
OTG_EN	D10	DO	P3	USB OTG power supply DC-DC enable signal	

USB_SS_SW	C13	DO	P3	USB Type-C switch control signal	

Table 21: Recommended CC detector list

Name	Manufacturer	Model
CC Detector	PERICOM	PI5USB30216D

Table 22: Recommended SS USB switch list

Name	Manufacturer	Model
USB Switch	PERICOM	PI3DBS12212A

Table 23: Recommended OTG 5V DC-DC and USB interface TVS list

Name	Manufacturer	Model
OTG	AWINIC	AW3605DNR
TVS	WILL	ESD5302N-3/TR

Please refer to the reference design for the design circuit diagram of OTG.

HS USB DP/DM layout guidelines:

- Require differential trace impedance is 85±10% Ω.

- The intra-lane length mismatch of the differential signal lanes is less than 1mm.
- Gap from other signals keeps 3xline width.
- External TVS or EMI components should be placed near the USB connector.
- Trace routes away from other sensitive signals (RF, audio, and XO).
- Maximum PCB trace length cannot exceed 100mm outside of module, the shorter trace and better.

SS USB TX/RX layout guidelines:

- Require differential trace impedance is 85±10% Ω.
- The intra-lane length mismatch of the differential signal lanes is less than 500um.
- Gap from other signals keeps 4xline width.
- Gap between Rx-to-Tx keeps 4xline width.
- External TVS or EMI components should be placed near the USB connector.
- Trace routes away from other sensitive signals (RF, especially 2.4 GHz).
- Route differential pairs in the inner layers with a solid GND reference to have good impedance control and to minimize discontinuities.
- Keep isolation between the Tx pair, Rx pair, and DP/DM to avoid crosstalk.
- If core vias are used, use no more than two core vias per signal line to limit stubs.

3.6 PCIe Interface

SIM8260A support PCIe Gen3 2-lane or PCIe Gen4 1-lane interfaces, which can be used as EP or RC mode. PCIe3 data rate up to 8Gbps per lane, PCIe4 data rate up to 16Gbps per lane. The following figure is the PCIe reference circuit.

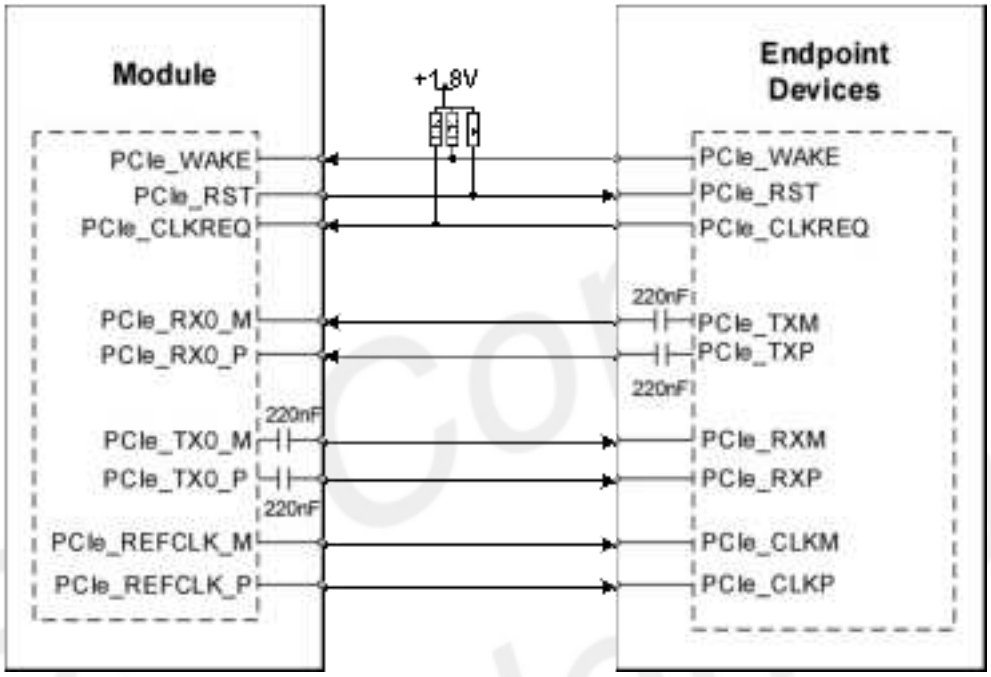

Figure 21: PCIe interface reference circuit (RC)

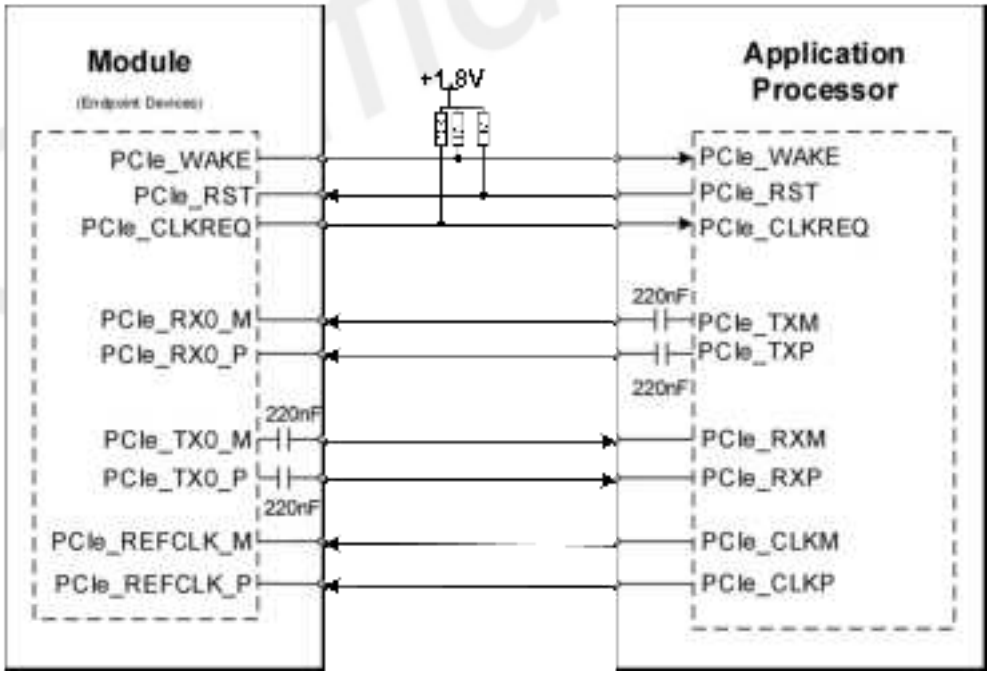

Figure 22: PCIe interface reference circuit (EP)

NOTE

- The 220nF AC capacitors should be placed near the PCIe_TX

Table 24: Definition of PCIe interface

Pin name	Pin no.	Pin characteristics		Functional description	Comment
PCIe_REFCLK_P	B22	AIO		PCIe reference clock plus	Required 85Ω differential impedance
PCIe_REFCLK_M	A21	AIO		PCIe reference clock minus	
PCIe_TX0_M	B18	AO		PCIe transmit0 minus	
PCIe_TX0_P	A17	AO		PCIe transmit0 plus	
PCIe_TX1_M	B20	AO		PCIe transmit1 minus	
PCIe_TX1_P	A19	AO		PCIe transmit1 plus	
PCIe_RX0_M	A25	AI		PCIe receive0 minus	
PCIe_RX0_P	B26	AI		PCIe receive0 plus	
PCIe_RX1_M	A23	AI		PCIe receive1 minus	
PCIe_RX1_P	B24	AI		PCIe receive1 plus	
PCIe_CLKREQ	C21	DI	P3	PCIe clock request	PCIe_CLKREQ and PCIe_WAKE need pull up to VDD_EXT externally, Default as RC mode
PCIe_WAKE	C25	DI	P3	PCIe wake-up	
PCIe_RST	C23	DO	P3	PCIe reset	

PCIe interface layout guidelines:

- All other sensitive/high-speed signals must be far away PCIe signals.
- PCIe signals must be protected be far away noisy signals (clocks, SMPS).
- Each trace needs to be adjacent to a ground plane.
- Require differential trace impedance is 85±10% Ω.
- The intra-lane length mismatch of the differential signal lanes is less than500um.
- Gap from other signals keeps 4xline width.
- Gap between Rx-to-Tx keeps 4xline width.
- Maximum PCB trace length cannot exceed 150mm outside of module, the shorter trace and better.

3.6.1 PCIe for W82

PCIe Gen3 lane0 can be connected to W82 as WLAN data interface, SIM8260As module serves as RC and W82 module serves as EP. PCIe_CLKREQ and PCIe_WAKE already be pulled up to 1.8V in W82. The details design please refer to the reference circuit document. The following figure is the PCIe

reference circuit.

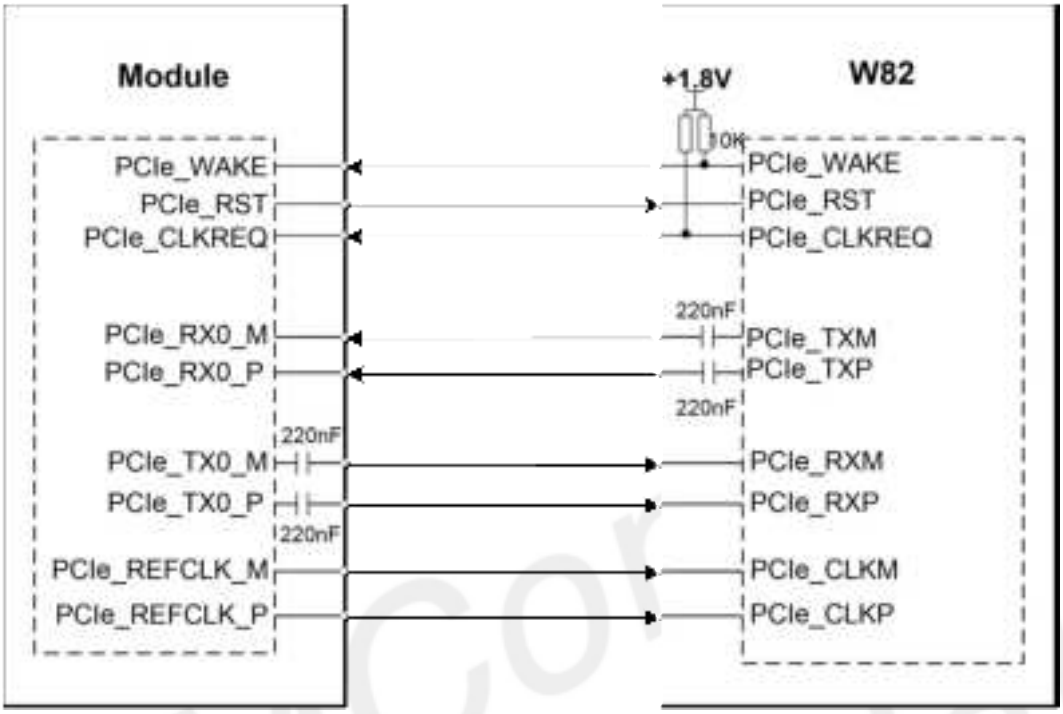

Figure 23: PCIe interface reference circuit (RC) for W82

NOTE

- The PCIe control signal voltage domain of the module and W82 are 1.8V.
- For more details about W82, please refer to Document [20] in the appendix.

Table 25: Recommended W82 list

Name	Manufacturer	Model
W82	SIMCOM	S2-10ADA

3.6.2 PCIe for RTL8125B

PCIe Gen3 lane0 can be connected to RTL8125B-TE as Ethernet data interface. SIM8260A module serves as RC and RTL8125B-TE serves as EP. Need to pull up PCIe_CLKREQ, PCIe_WAKE, PCIe_RST from module to 3.3V. The details design please refer to the reference circuit document. The following figure is the PCIe reference circuit.

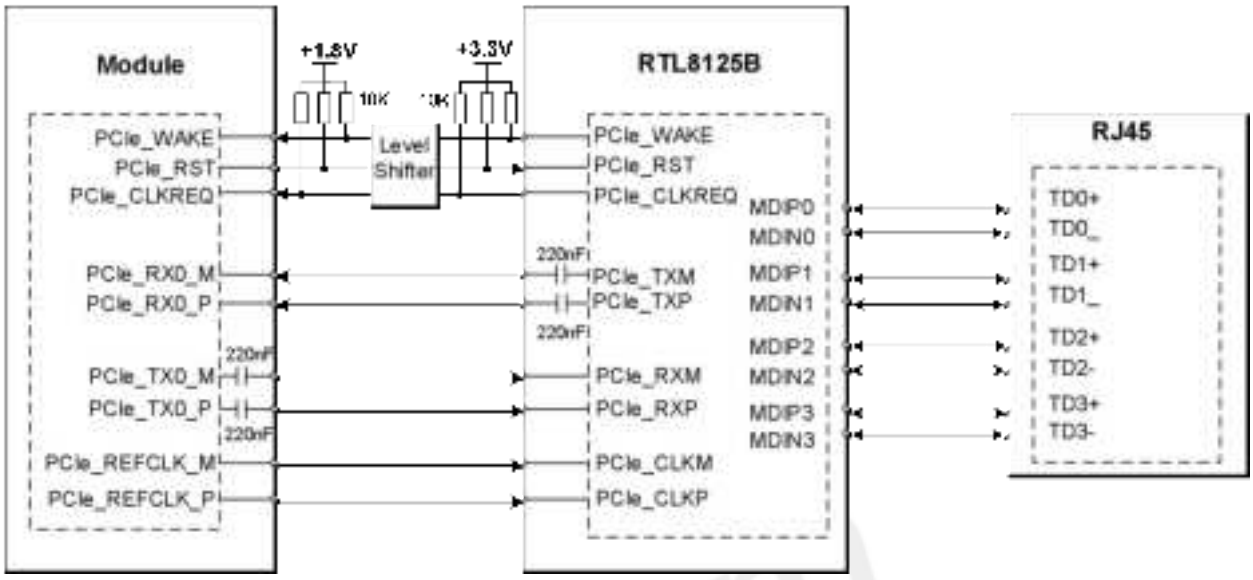

Figure 24: PCIe interface reference circuit (RC) for RTL8125B

NOTE

- The 220nF AC capacitors should be placed near the PCIe_TX
- The PCIe control signal voltage domain of the module is 1.8V, through the level shifter, the RTL8125B is 3.3V.
- For more details about RTL8125B, please refer to Document [17] in the appendix.

Table 26: Recommended RTL8125B and RJ45 list

Name	Manufacturer	Model
RTL8125B	REALTEK	RTL8125B-CG
RJ45	ZhengGu	RJ45-114B4DZ-G020

3.6.3 PCIe Switch

When PCIe switch is added, the module can use W82 and others such as AQR113* at the same time. The details design please refer to the QPS615 reference circuit document. The following figure is the PCIe reference circuit.

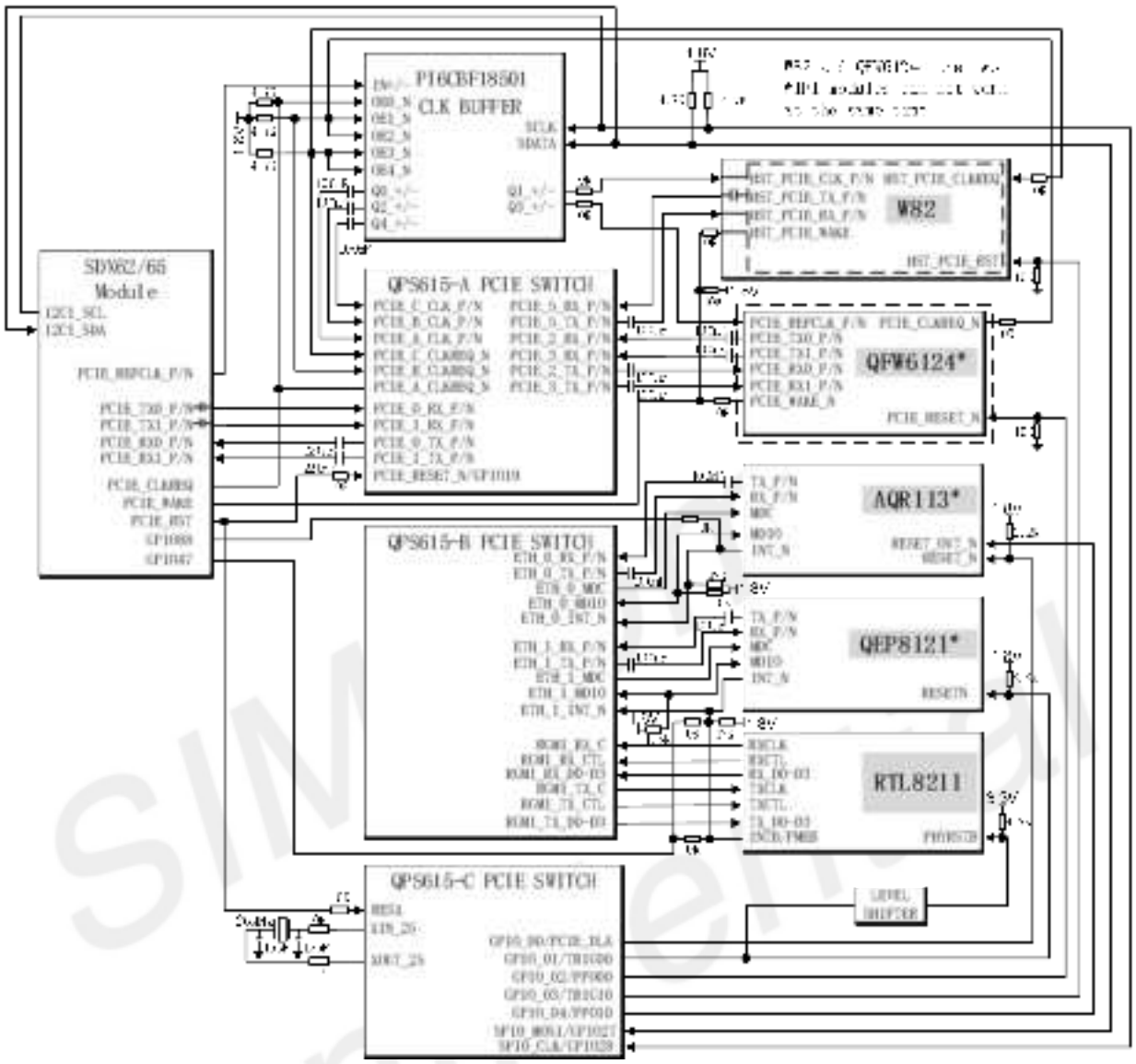

Figure 25: PCIe switch reference circuit

NOTE

- The 220nF AC capacitors should be placed near the PCIe_TX
- "*" means under development.

Table 27: Recommended PCIe SWITCH list

Name	Manufacturer	Model
PCIe Switch	Qualcomm	QPS615
PCIE clock buffer	Diodes	PI6CBF18501ZLAIEX-13R
W82 module	SIMCom	S2-10ADA

AQR113	MARVELL	AQR113C-B0-C
QEP8121	Qualcomm	QEP-8121-1-56MQFN-**-02-0
RTL8211	REALTEK	RTL8211F-CG

3.6.4 PCIe interface for Qualcomm IPQxxxx

PCIe connected to qualcomm IPQxxxx is designed to be used as CPE application, the module does EP and the qualcomm IPQxxxx does RC.

Since the PCIe_WAKE, PCIe_RST, and PCIe_CLKREQ control signals of IPQxxxx are in the voltage domain of 1.8V, on the module side, CLKREQ# and PEWAKE# need to be pulled up to 1.8V externally through 100KR. The following figure is a schematic diagram of the module connected to IPQxxxx.

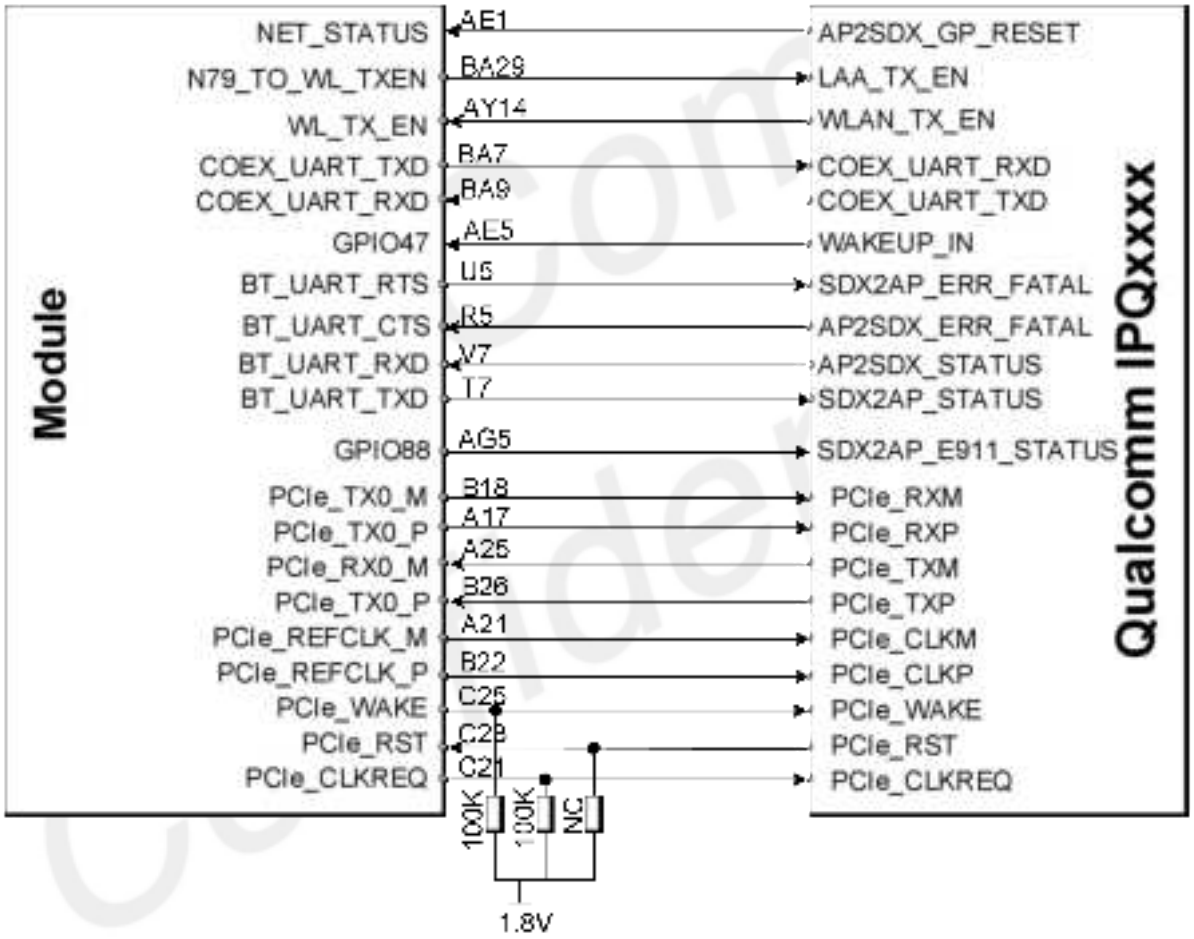

Figure 26: Schematic diagram of module connected to IPQxxxx

3.7 SDIO Interface

SIM8260A provide 8-bit SDIO interface, which meets the SDIO3.0 specifications and supports SDIO host mode. The clock output up to 200MHz for SD card, and up to 100MHz for eMMC. Support 4-bit dual-voltage 1.8V or 3.0V SD card or 8-bit 1.8V eMMC.

The SD card and the eMMC reference circuits are shown below.