Block Diagram / Circuit Descriptions

This exhibit contains descriptions of the frequency generation, modulation and transmitter circuits in accordance with FCC Rules Part 2.983(d).

The following descriptions are included:

EXHIBIT 4A – Block Diagram

EXHIBIT 4B - Means for Frequency Stabilization, 2.983 (d) 10

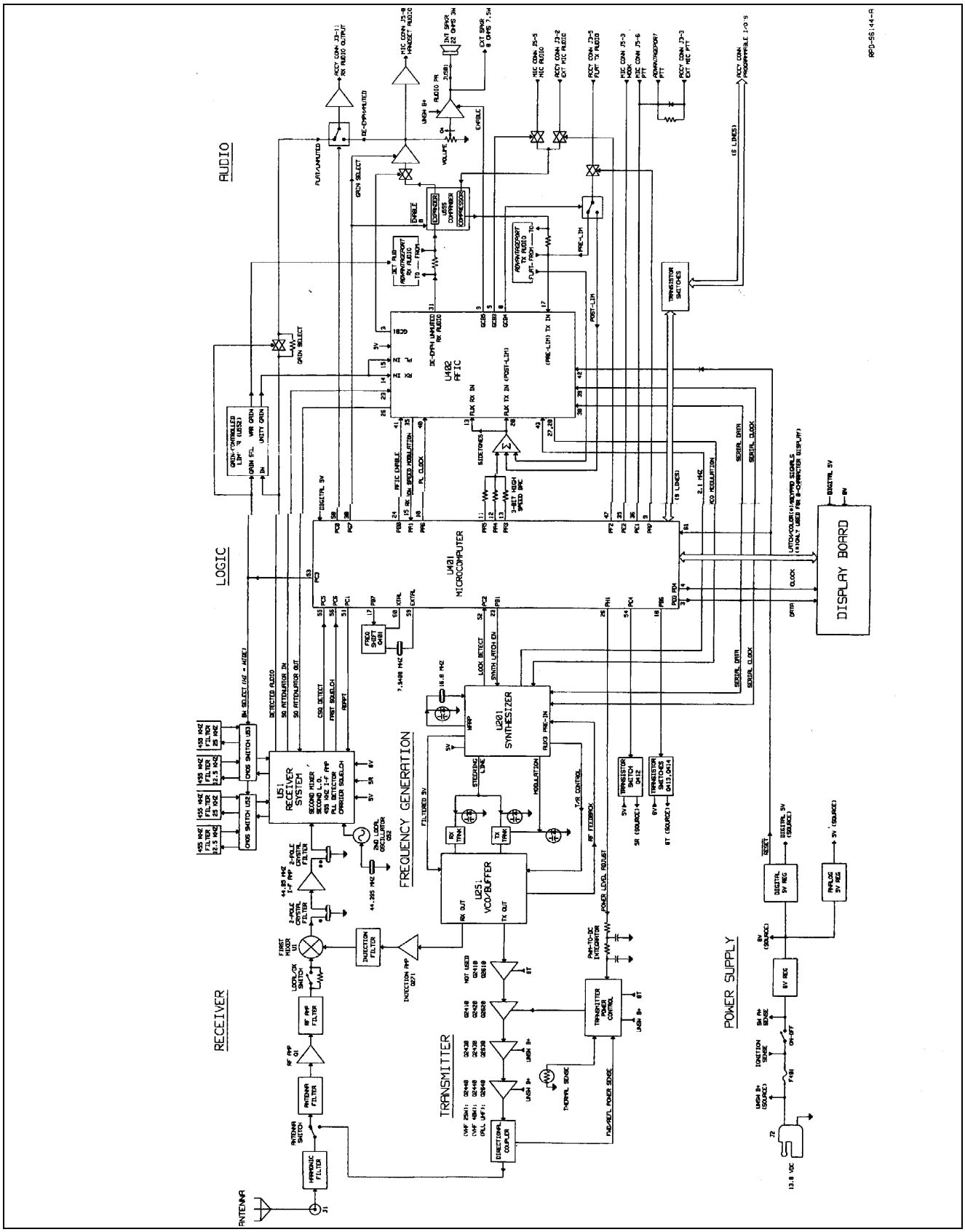
EXHIBIT 4C - Means for Limiting Modulation, 2.983 (d) 11

EXHIBIT 4D - Means for Attenuation of Higher Audio Frequencies, 2.983 (d) 11

EXHIBIT 4E - Means for Attenuation of Spurious Emissions, 2.983 (d) 11

EXHIBIT 4F - Means for Limiting Power Output, 2.983 (d) 11

EXHIBIT 4G - Modulation Techniques, 2.983 (d) 12



BLOCK DIAGRAM

EXHIBIT 4A
Sheet 2 of 8

Means For Frequency Stabiliztion

Frequency stability is maintained by a reference oscillator/programmable temperature compensation circuit located in the frequency synthesizer IC U201. The oscillator is a Colpitts design with an amplifier on the IC. The 16.8 MHz crystal, varactor and feedback capacitors are external circuitry. A control voltage applied to the varactor via the programmable compensation circuit maintains the frequency stability to within ±2.5 ppm over temperature. Frequency tuning, also from the programmable compensation circuit, has 128 steps of resolution.

Each 16.8 MHz crystal is numerically coded providing its unique characteristic over the temperature range. with this information an equally unique compensation characteristic is programmed into the compensation algorithm.

Means for Limiting Modulation

Modulation limiting is accomplished within the custom processor IC U402. The limiting action itself occurs at the rails (i.e., 5V and ground). Using an op-amp with feedback, very hard limiting is obtained. The limited modulation signal is then input through a low pass filter to an electronic attenuator within U402 in order to adjust for variations in modulation sensitivities of the frequency synthesizer.

The electronic attenuator is controlled by the radio's logic circuit. To keep the deviation constant over the RF frequency range, the microcomputer adds the proper correction factor to the attenuator.

Means for Attenuation of Higher Audio Frequencies

The output of the limiter is applied to a low-pass filter. The filter is a fifth-order switched capacitor filter with the rolloff corner located at 3000 Hz. The output of the low-pass filter is input to the electronic attenuator.

Means for Attenuation of Spurious Emissions

The final stage of the RF power amplifier circuit feeds a low-pass filter in order to attenuate harmonics of the output frequency as well as spurious outputs. The filter is a seven pole .1 dB Chebychev design using LC reactive elements.

Shielding of the transmitter RF power amplifier circuit also attenuates spurious emissions.

Means for Limiting Power Output

The transmitter line-up consists of four stages of amplification. The second stage device is power controlled by regulation of its collector voltage, via a series-pass regulator controlled by a comparator circuit.

The comparator circuit receives a reference voltage from an averaged PWM signal from the microprocessor. A directional coupler located after the RF final power amplifier provides a feedback signal proportional to the RF output power.

Included in the Power Control circuitry is a temperature sensing circuit which monitors the temperature in the vicinity of the RF final power amplifier, and limits the power out of the radio under extreme high temperature conditions. Additionally, the directional coupler provides an output voltage which is proportional to the level of RF power reflected from the antenna under mismatch conditions. This in turn is used to reduce output power under conditions of significant mismatch.

Modulation Techniques

The transmitter is capable of the following types of modulation:

1. Modulation of PL (Private Line) - Direct FM tone modulation of 67 Hz to 250.3 Hz at 15% of full system deviation.

2. Modulation of DPL (Digital Private Line) - Direct FM modulation at 134 BPS at 15% of full system deviation.

3. Modulation of DTMF tones at nominally 60% of full system deviation.

Direct FM of PL or DPL is generated by a 6-bit D/A converter contained within U402. The frequency-determining clock signal is generated by the radio microcomputer. The modulation signal is processed through a five pole switched capacitor filter. The output of the filter is input to the electronic attenuator circuit.

The microcomputer adjusts the attenuator to compensate for modulation sensitivity variations of the synthesizer, ensuring 15% of full system deviation for PL and DPL.

DTMF tones are generated by an external tone generator IC contained within the accessory DTMF microphone. The DTMF tones are routed and processed in the same manner as voice signals. A potentiometer inside the microphone allows adjustment of the DTMF tones to nominally 60% of full system deviation.