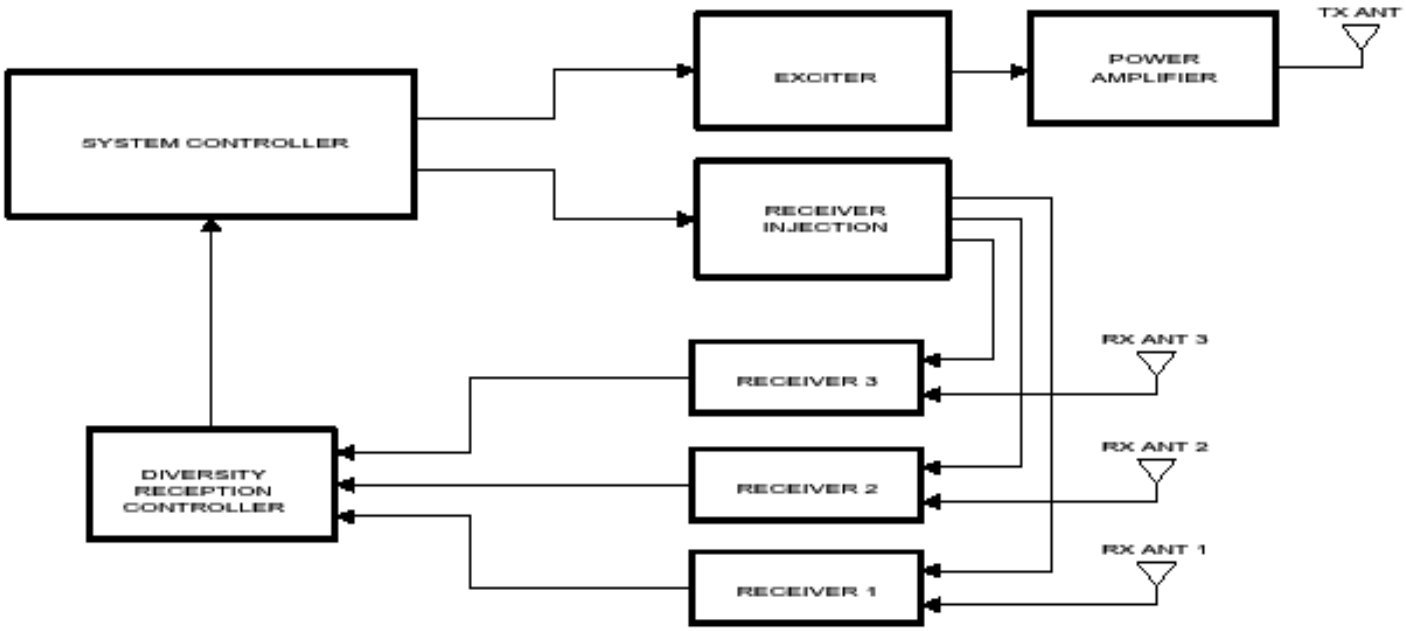
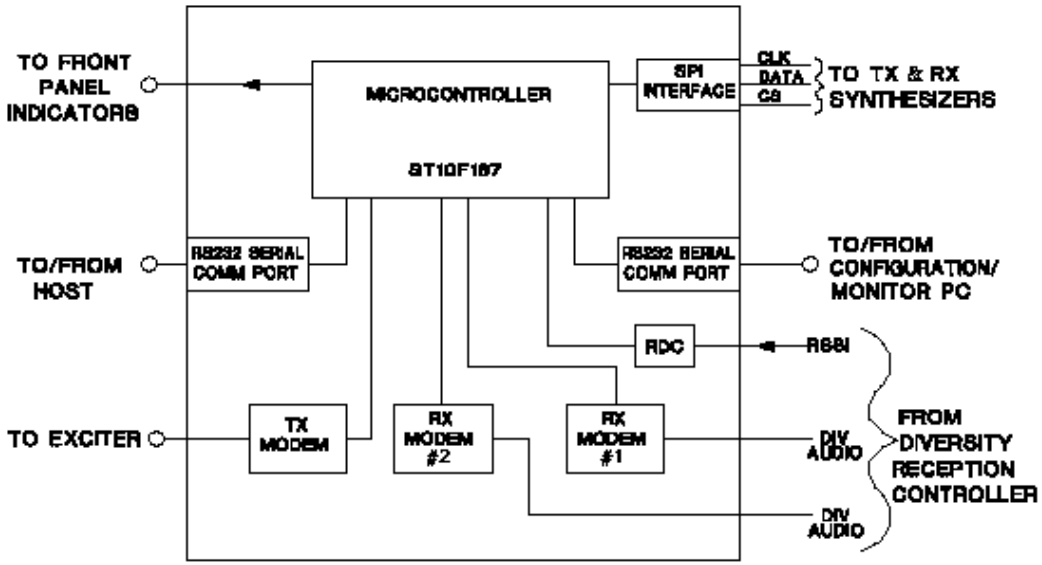
IP1B Base Station General Block Diagram



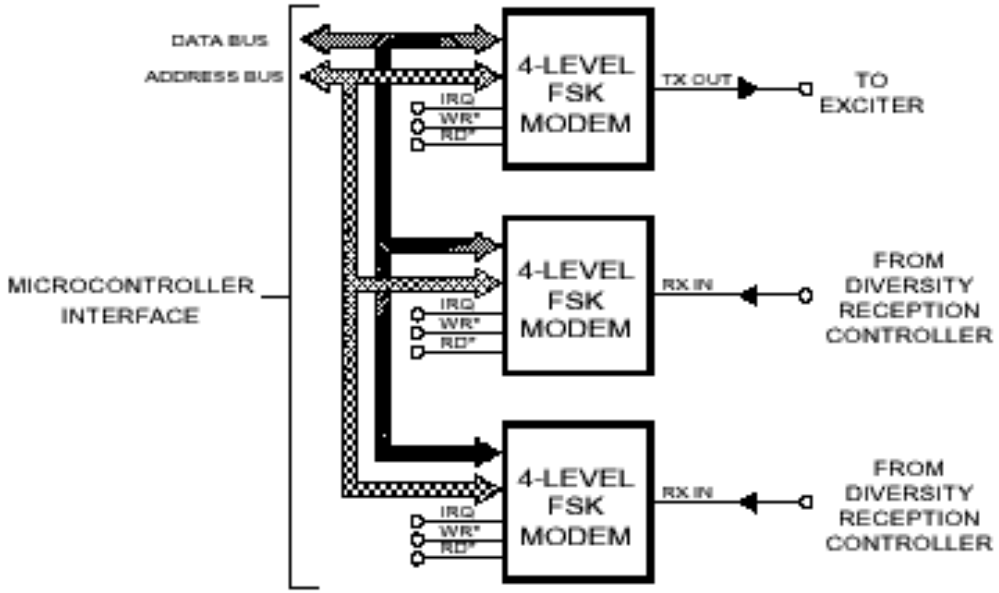
General block diagram of the IP1B, which is comprised of eight (8) PCBs (Printed Circuit Boards)

IP1B Base Station System Controller Block Diagram

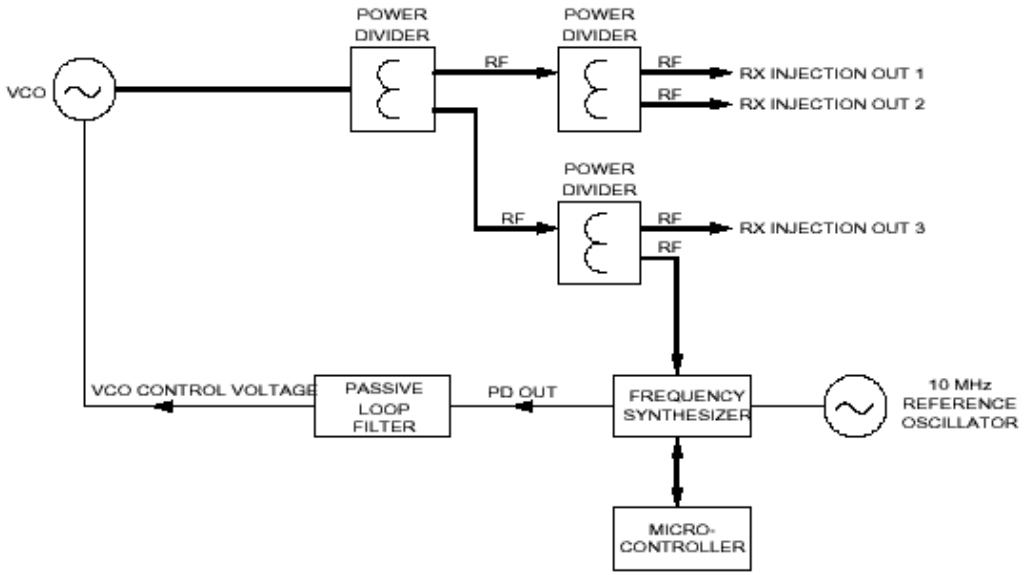


Functional block diagram of the System Controller

IP1B Base Station 4-Level FSK Modem Section

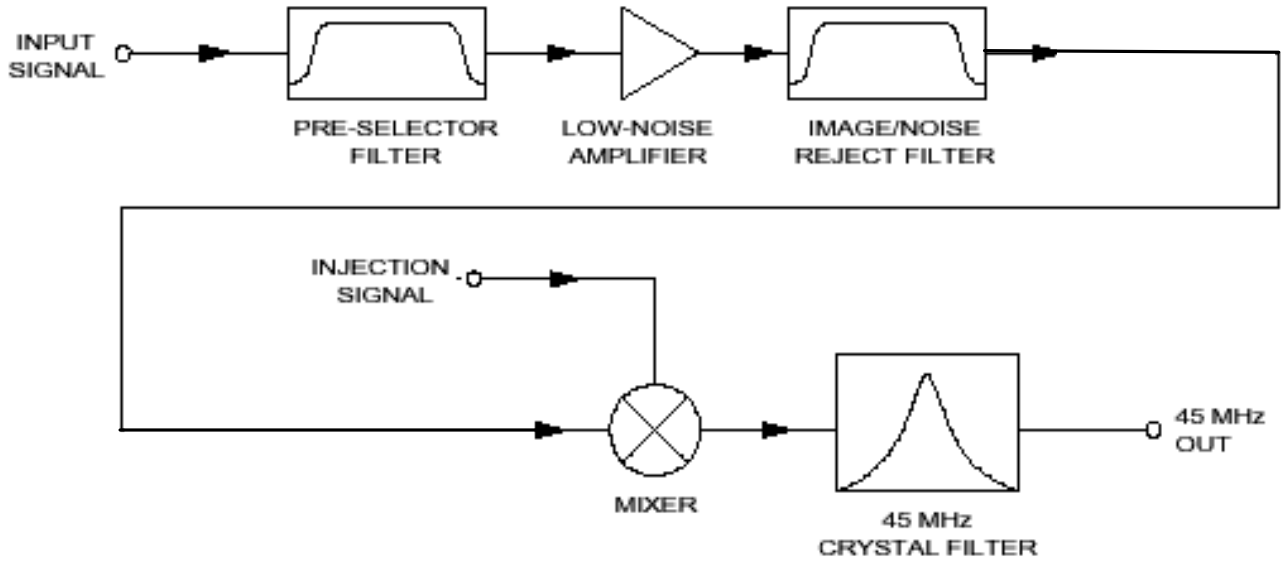


IP1B Base Station Receiver Injection

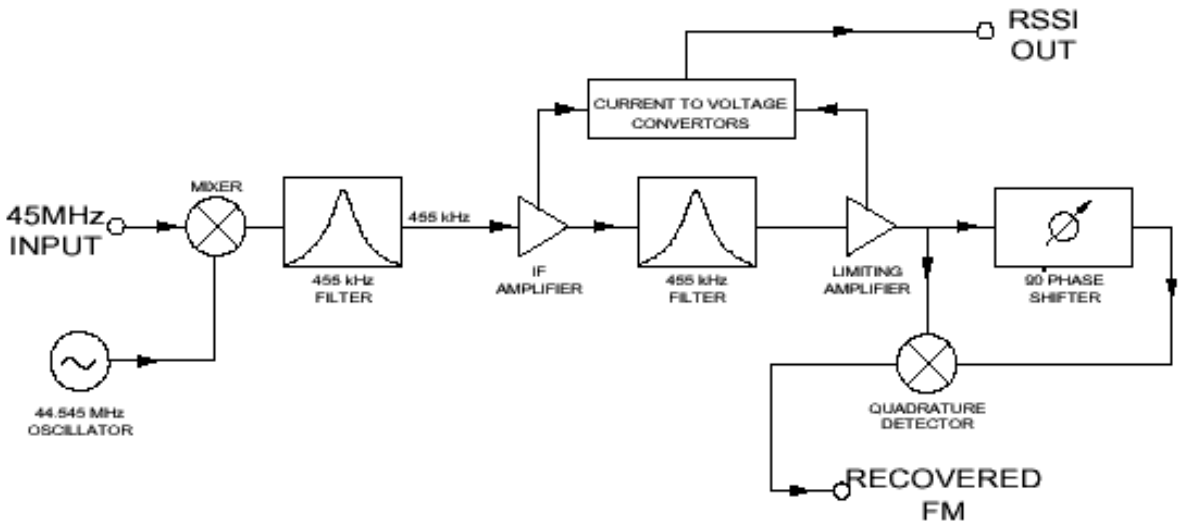


Functional block diagram of the receiver injection

IP1B Base Station VHF Front-End Section

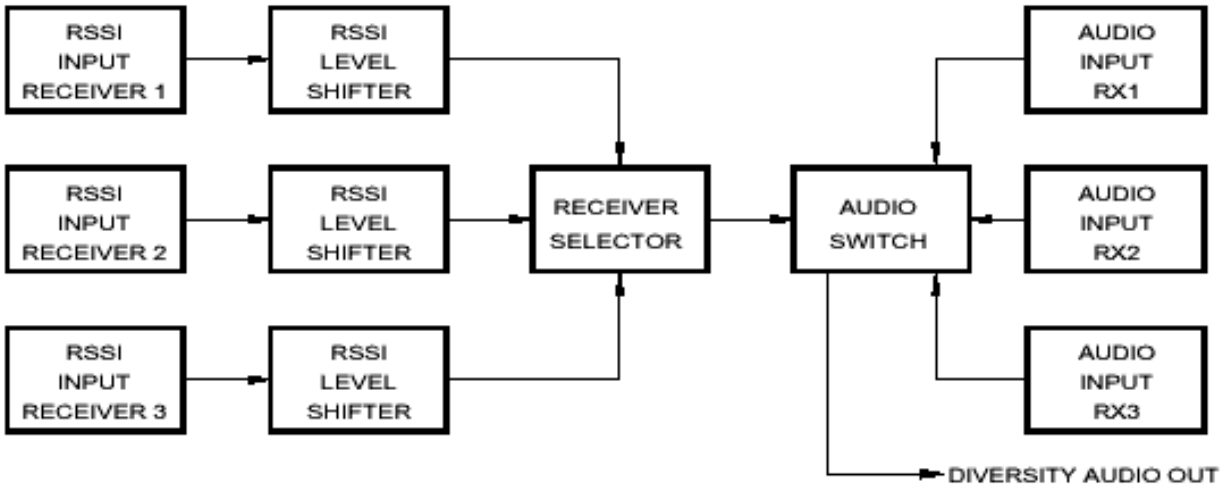


IP1B Base Station 45 MHz Receiver Section



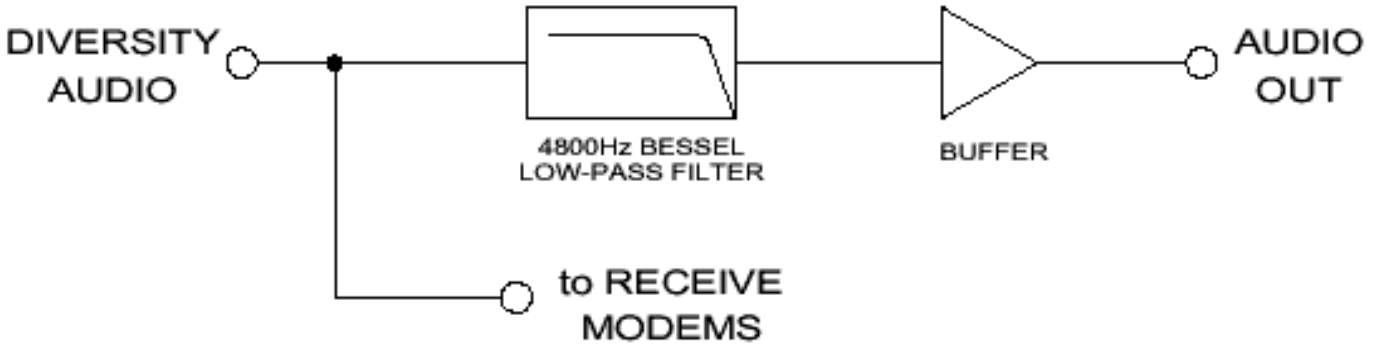
Functional block diagram of the 45 MHz Receiver

Diversity Reception Controller



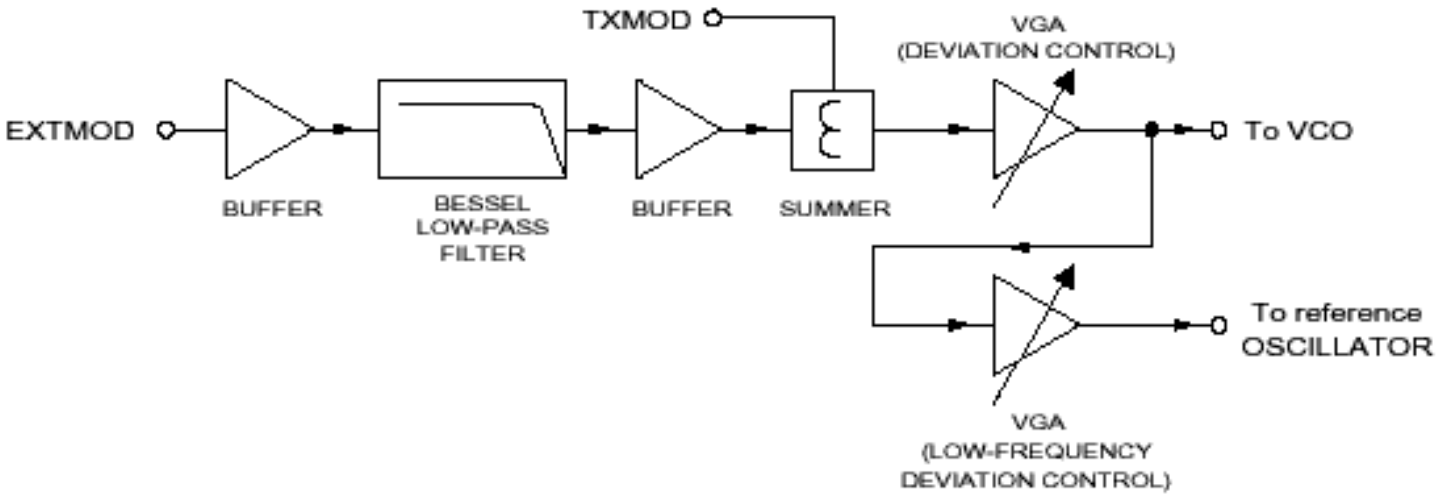
The DRC is the central processor of a patented triple-receiver DRC.

IP1B Base Station Receive Baseband Processing



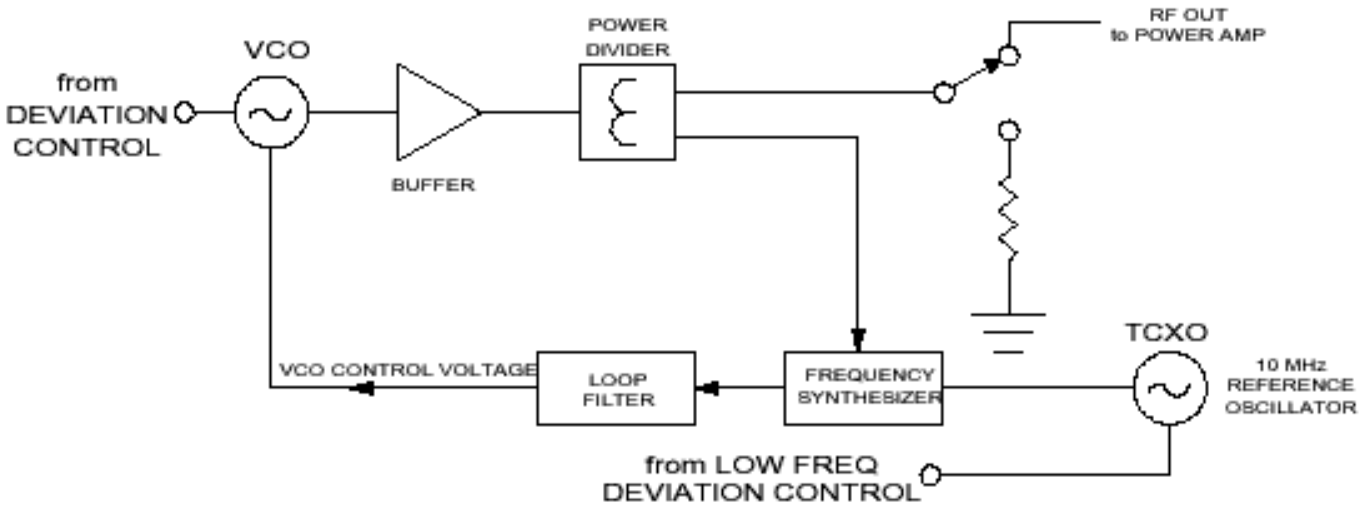
Functional diagram of the receive baseband processing section.

IP1B Base Station Exciter
Transmit Baseband Processing



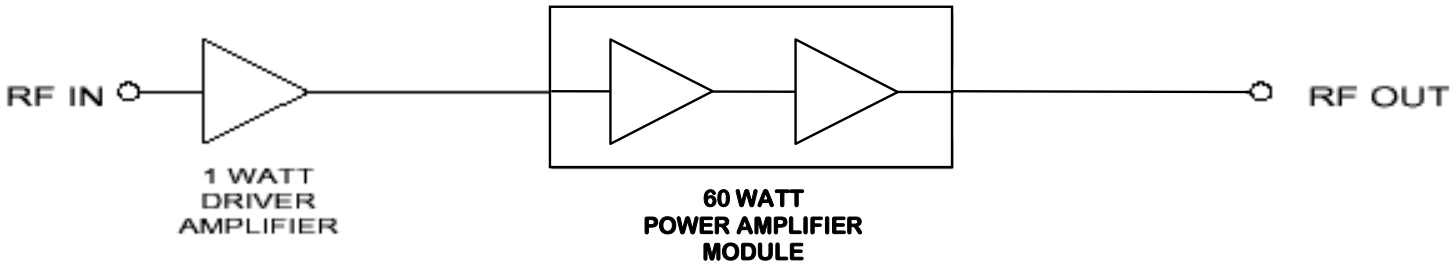
Functional diagram of the IP1B's transmit baseband processing section

IP1B Base Station Exciter
Exciter RF Section



Functional block diagram of the exciter RF section

IP1B Base Station Power Amplifier Module



Functional diagram of the power amplifier.