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EUM3005 Block Diagrams

The following are the block diagrams for the RF and digital sections of the EUM3005. The blocks shown are as follows:

Top level
RF section
Ethernet PHY
Microprocessor/MAC memory
Microprocessor/MAC
Baseband processor interface

1 Block Diagrams

1.1 Top Level Block Diagram

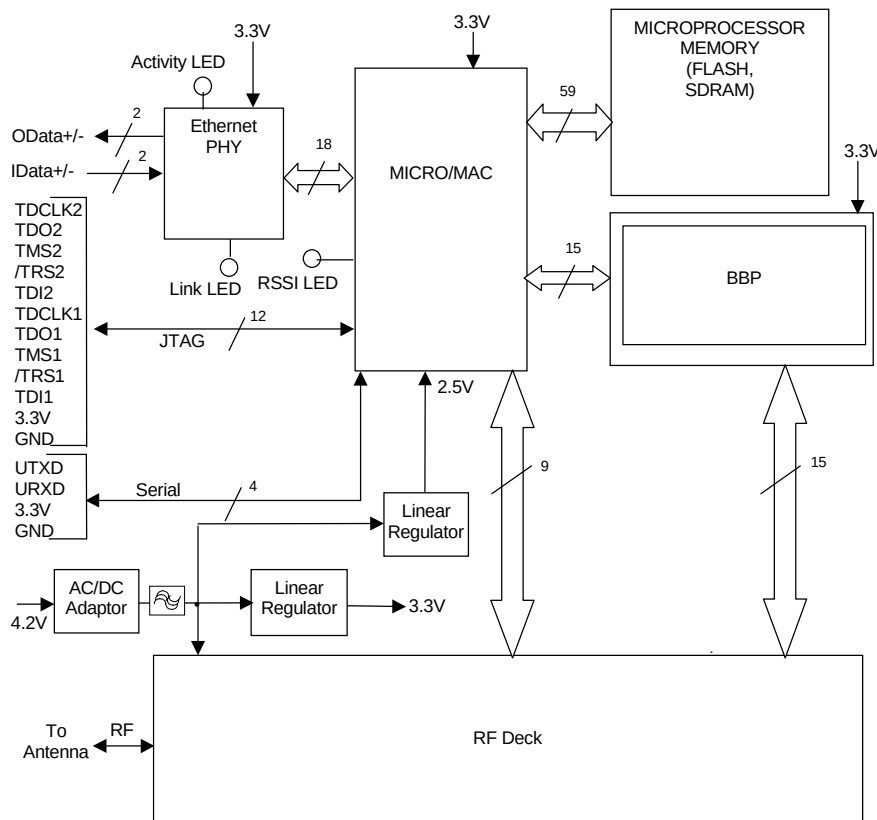


Figure 1.1 – Top Level Block Diagram

4.2V

To MICRO/MAC

M_LE_RF

PAPE

PE1

PE2

CAL_EN

RFSW

M_SD_IF_RF

M_SCLK_IF_RF

M_LE_IF

IFDET

TXI+/- 2

TXQ+/- 2

VREF

RXI+/- 2

RXQ+/- 2

TXIFAGC

RXIFAGC

44MHz

140 MHz IFLO

ANTSEL

RXRFAGC

To BBP

3.3V LO Regulator

3.3V LO

3.3V Regulator

3.3V RF

Legend

Shield wall

Logic + 2.85V reg

4.2V DC

TX Mixer

TX RF Image Filter

PA

TX RX Switch

Front End Filter

To Antenna

4.2V DC

Doubler

3.3V RF

Logic

RFSW

ANTSEL

3.3V RF

TX IF Amp

TX Pad

902-928 MHz

Buffer

RF LO 975-995 MHz

SYN

M_SD_IF_RF

M_SCLK_IF_RF

M_LE_RF

44MHz_synth

RX Pad

RX RF Image Filter

902-928 MHz

RF LNA

RX Mixer

70 MHz

3.3V LO

IF Filter

TXIF+

TXIF-

70 MHz

XFER

RXIF+

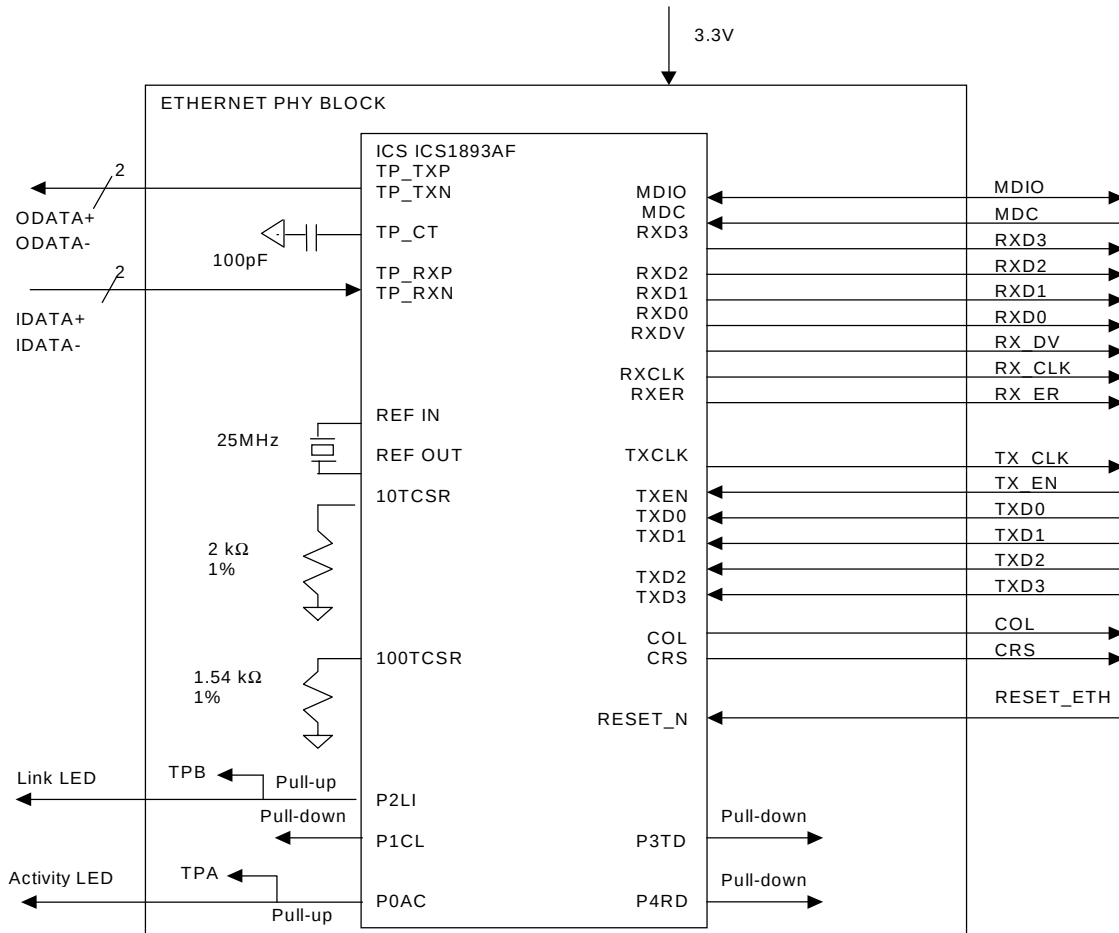
RXIF-

XFER

Figure 1.2 – RF Section Block Diagram

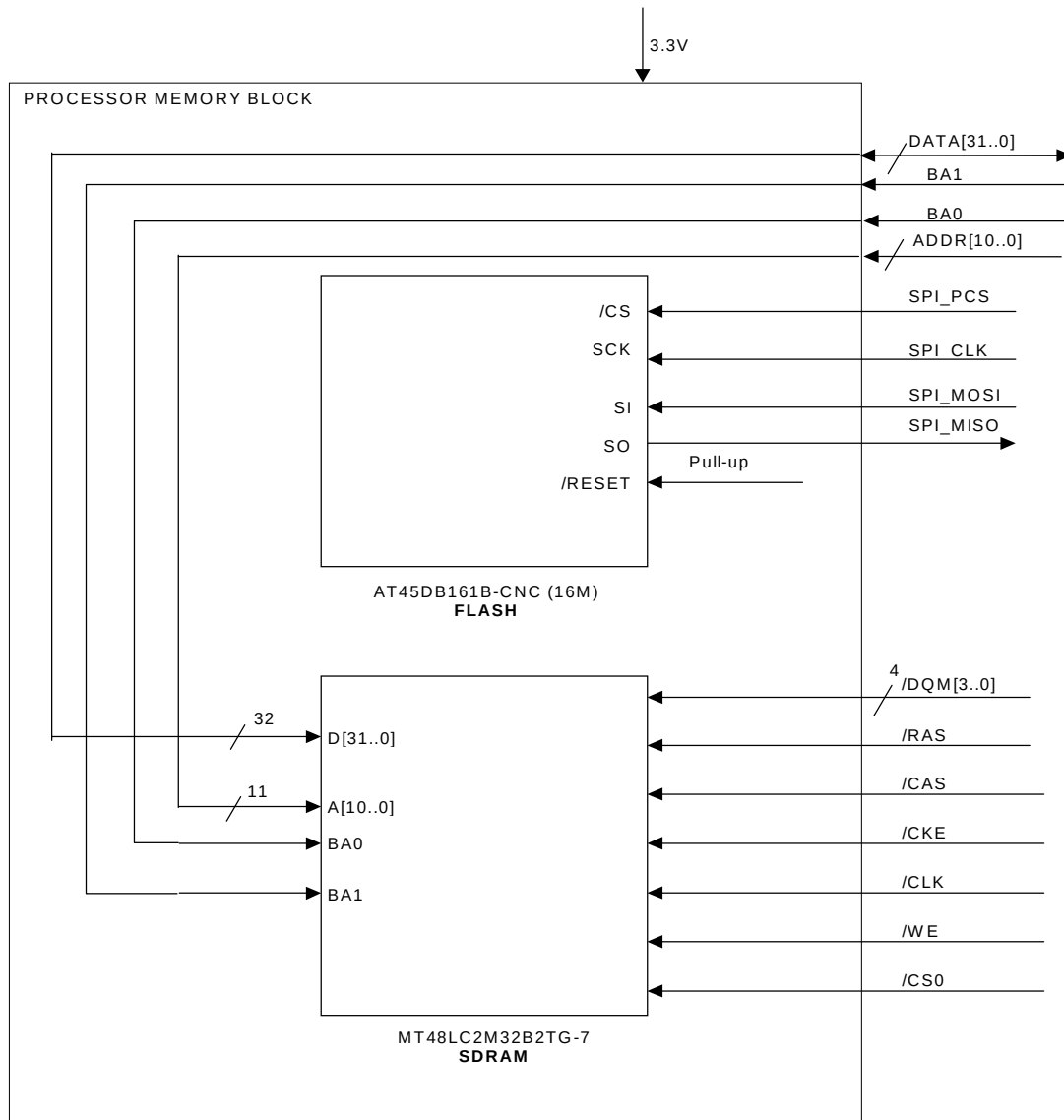
1.3 Digital Section

1.3.1 Ethernet PHY



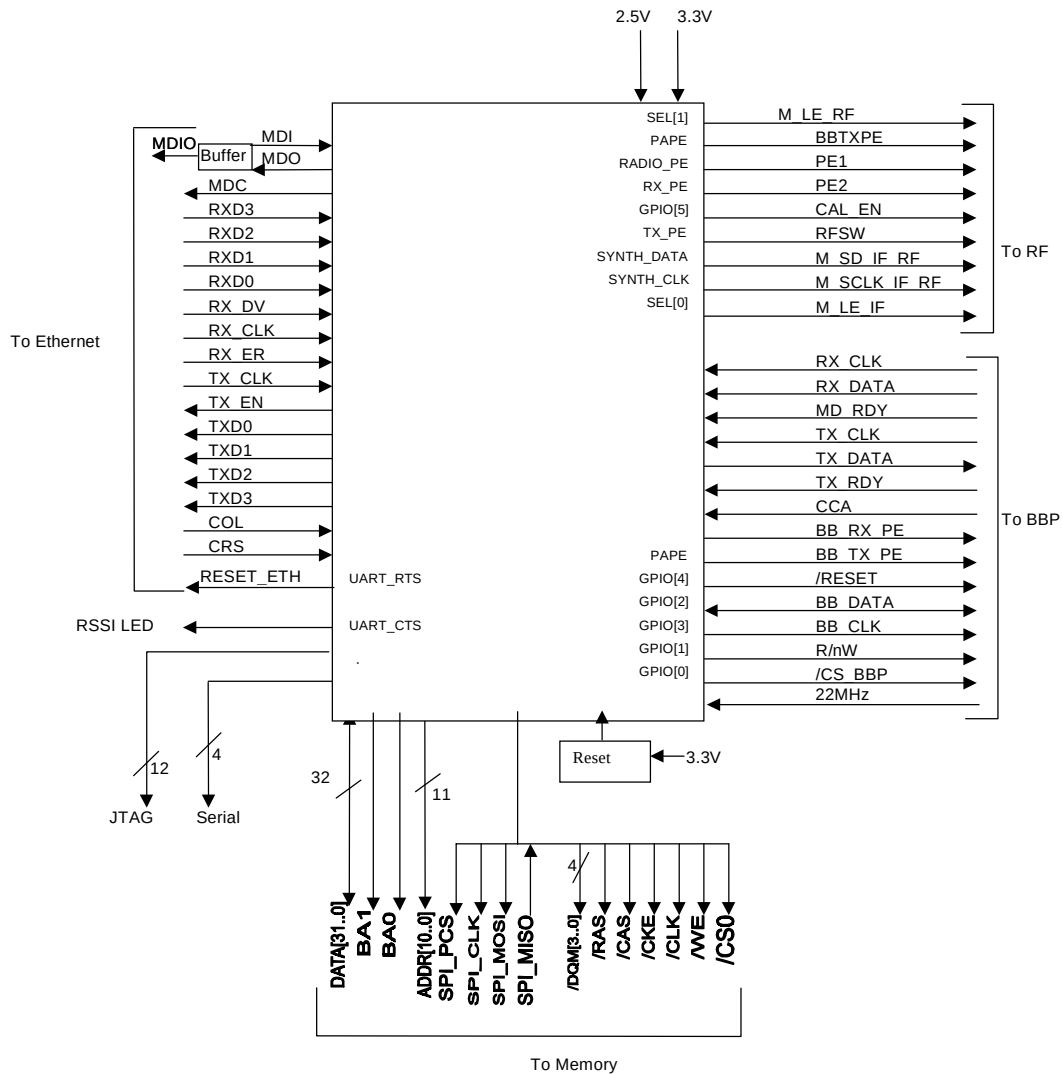
5.3.1 Ethernet PHY Block Diagram

1.3.2 Microprocessor/MAC Memory (FLASH,SDRAM)



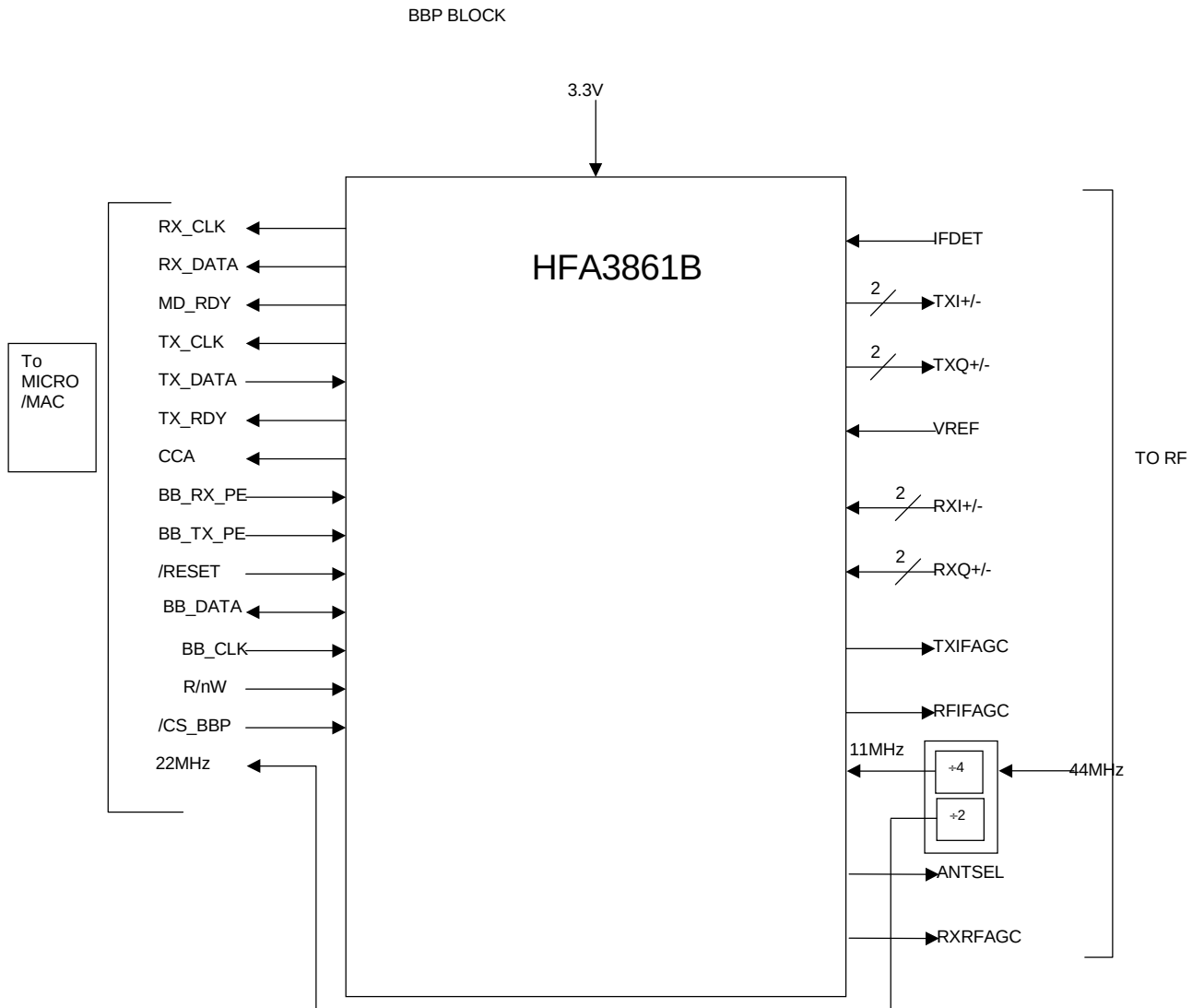
5.3.2 Microprocessor/MAC Memory Block Diagram

1.3.3 Microprocessor/MAC



5.3.3 Microprocessor/MAC Interface Block Diagram

1.3.4 BBP Interface



5.3.4 BBP Interface Block Diagram