FCC ID: ALH30643130
2.1033(c)(9) TUNING [redacted]NG PROCEDURE

No.	Item	Condition	Measuement point	Method	Equipment	Spec
0	Set up	Install a I/F jig and powersupply				
1	RD output Level(wide)	Ch4, 465.1MHz/-53dBm(0-10)	ANT SG	PC Adj.	Radio tester	80mV±3mV
		Ch4, 496.1MHz/-53dBm(0-11)				
		Ch4, 415.1MHz/-53dBm(0-12)				
		1kMOD/3kDEV	D-Sub RD terminal(10pin)			
2	RD output Level(narrow)	Ch10, 465.1MHz/-53dBm(0-10)	ANT SG	PC Adj.	Radio tester	80mV±3mV
		Ch10, 496.1MHz/-53dBm(0-11)				
		Ch10, 415.1MHz/-53dBm(0-12)				
		1kMOD/1.5kDEV	D-Sub RD terminal(10pin)			
3	RA output Level(wide)	Ch4, 465.1MHz/-53dBm(0-10)	ANT SG	PC Adj.	Radio tester	400mV±20mV
		Ch4, 496.1MHz/-53dBm(0-11)				
		Ch4, 415.1MHz/-53dBm(0-12)				
		1kMOD/3kDEV	D-Sub RA terminal(11pin)			
4	RA output Level(narrow)	Ch10, 465.1MHz/-53dBm(0-10)	ANT SG	PC Adj.	Radio tester	400mV±20mV
		Ch10, 496.1MHz/-53dBm(0-11)				
		Ch10, 415.1MHz/-53dBm(0-12)				
		1kMOD/1.5kDEV	D-Sub RA terminal(11pin)			
5	RRA output Level(wide)	Ch4, 465.1MHz/-53dBm(0-10)	ANT SG	Check	Radio tester	400mV±20mV
		Ch4, 496.1MHz/-53dBm(0-11)				
		Ch4, 415.1MHz/-53dBm(0-12)	-			
		1kMOD/3kDEV	Remort I/O terminal(1pin)			
6	RRA output Level(narrow)	Ch10, 465.1MHz/-53dBm(0-10)	ANT SG	Check	Radio tester	400mV±20mV
		Ch10, 496.1MHz/-53dBm(0-11)				
		Ch10, 415.1MHz/-53dBm(0-12)				
		1kMOD/1.5kDEV	Remort I/O terminal(1pin)			
7	Voting Tone Level(wide)	f-Center Ch4	Remove SG	PC Adj.	Radio tester	400mV±20mV
		Voting Tone:1950Hz	D-Sub RA terminal(11pin)			
8	Voting Tone Level(narrow)	f-Center Ch10	Remove SG	PC Adj.	Radio tester	400mV±20mV
		Voting Tone:1950Hz	D-Sub RA terminal(11pin)			
9	Max Dev(wide)	VCO-A(Lo) Ch1	MIC terminal 6pin	PC Adj.	MOD.ANA	4.1kHz±0.2kHz
		1kHz/50mV load			AG	
10		VCO-A(Center) Ch2			MOD.ANA	
					AG	
11		VCO-A(Hi) Ch3			MOD.ANA	
					AG	
12		VCO-B(Lo) Ch4			MOD.ANA	
					AG	
13		VCO-B(Center) Ch5			MOD.ANA	
					AG	
14		VCO-B(Hi) Ch6			MOD.ANA	
					AG	
15	Max Dev(narrow)	VCO-A(Lo) Ch7	MIC terminal 6pin	PC Adj.	MOD.ANA	1.7kHz±0.1kHz
		1kHz/50mV load			AG	
16		VCO-A(Center) Ch8			MOD.ANA	
					AG	
17		VCO-A(Hi) Ch9			MOD.ANA	
					AG	
18		VCO-B(Lo) Ch10			MOD.ANA	
					AG	
19		VCO-B(Center) Ch11			MOD.ANA	
					AG	
20		VCO-B(Hi) Ch12			MOD.ANA	
					AG	
21	Mic Dev(wide)	VCO-A(Center) Ch2	MIC terminal 6pin	Check	MOD.ANA	3±0.25kHz
		1kHz/4.5mV load			AG	
22		VCO-B(Center) Ch5			MOD.ANA	
					AG	
23	Mic Dev(narrow)	VCO-A(Center) Ch8	MIC terminal 6pin	Check	MOD.ANA	1.5±0.1kHz
		1kHz/5.5mV load			AG	
24		VCO-B(Center) Ch11			MOD.ANA	
					AG	
25	DQT balance (wide)	VCO-A(Center) Ch2	D-Sub TD terminal	PC Adj.	MOD.ANA	Make the demodulation wave square
		50Hz/0.5Vpp square wave	(8pin)		AG	
26		VCO-B(Center) Ch5			MOD.ANA	
					AG	
27	DQT balance (narrow)	VCO-A(Center) Ch8	D-Sub TD terminal	PC Adj.	MOD.ANA	Make the demodulation wave square
		50Hz/0.5Vpp square wave	(8pin)		AG	
28		VCO-B(Center) Ch11			MOD.ANA	
					AG	
29	TD Dev(wide)	VCO-A(Center) Ch2	D-Sub TD terminal	PC Adj.	MOD.ANA	0.75kHz±0.05kHz
		100Hz/0.5Vpp sine wave	(8pin)		AG	
30		VCO-B(Center) Ch5			MOD.ANA	
			-		AG	
31	TD Dev(narrow)	VCO-A(Center) Ch8	D-Sub TD terminal	PC Adj.	MOD.ANA	0.75kHz±0.05kHz
		100Hz/0.5Vpp sine wave	(8pin)		AG	
32		VCO-B(Center) Ch11			MOD.ANA	
					AG	
33	TA Dev(wide)	f-Center Ch4	D-Sub TA terminal	PC Adj.	MOD.ANA	3±0.1kHz
		1kHz/280mV sine wave	(9pin)		AG	
34	TA Dev(narrow)	f-Center Ch10	D-Sub TA terminal	PC Adj.	MOD.ANA	1.5±0.05kHz
		1kHz/280mV sine wave	(9pin)		AG	
35	TA Dev(wide)	VCO-A(Center) Ch2	D-Sub TA terminal	Check	MOD.ANA	3±0.1kHz
		1kHz/280mV load	(9pin)		AG	
36		VCO-B(Center) Ch5			MOD.ANA	
					AG	
37	TA Dev(narrow)	VCO-A(Center) Ch8	D-Sub TA terminal	Check	MOD.ANA	1.5±0.05kHz

39	RTA Dev(wide)	f-Center Ch4	Remort I/O terminal	PC Adj.	MOD.ANA	3±0.1kHz
		1kHz 280mV sine wave	(1pin)		AG	
40	RTA Dev(narrow)	f-Center Ch10	Remort I/O terminal	PC Adj.	MOD.ANA	1.5±0.05kHz
		1kHz 280mV sine wave	(1pin)		AG	
41	RTA Dev(wide)	VCO-A(Center) Ch2	Remort I/O terminal	Check	MOD.ANA	3±0.1kHz
		1kHz/280mV load	(1pin)		AG	
42		VCO-B(Center) Ch5			MOD.ANA	
					AG	
43	RTA Dev(narrow)	VCO-A(Center) Ch8	Remort I/O terminal	Check	MOD.ANA	1.5±0.05kHz
		1kHz/280mV load	(1pin)		AG	
44		VCO-B(Center) Ch11			MOD.ANA	
					AG	
45	QT Dev(wide)	f-Center Ch4	ANT Dummy	PC Adj.	MOD.ANA	0.75kHz±0.05kHz
		QT:67Hz				
46	QT Dev(narrow)	f-Center Ch10	ANT Dummy	PC Adj.	MOD.ANA	0.35kHz±0.05kHz
		QT:67Hz				
47	DQT Dev(wide)	f-Center Ch4	ANT Dummy	PC Adj.	MOD.ANA	0.75kHz±0.05kHz
		DQT:023N				
48	DQT Dev(narrow)	f-Center Ch10	ANT Dummy	PC Adj.	MOD.ANA	0.35kHz±0.05kHz
		DQT:023N				
49	QT Dev(wide)	VCO-A(Center) Ch17	ANT Dummy	Check	MOD.ANA	0.75kHz±0.05kHz
		QT:67Hz				
50		VCO-B(Center) Ch18			MOD.ANA	
51	QT Dev(narrow)	VCO-A(Center) Ch19	ANT Dummy	Check	MOD.ANA	0.35kHz±0.05kHz
		QT:67Hz				
52		VCO-B(Center) Ch20			MOD.ANA	
53	DQT Dev(wide)	VCO-A(Center) Ch21	ANT Dummy	Check	MOD.ANA	0.75kHz±0.05kHz
		DQT:023N				
54		VCO-B(Center) Ch22			MOD.ANA	
55	DQT Dev(narrow)	VCO-A(Center) Ch23	ANT Dummy	Check	MOD.ANA	0.35kHz±0.05kHz
		DQT:023N				
56		VCO-B(Center) Ch24			MOD.ANA	
57	Test Tone Dev(wide)	f-Center Ch4	ANT Dummy	PC Adj.	MOD.ANA	3±0.1kHz
		Test Tone:1kHz				
58	Test Tone Dev(narrow)	f-Center Ch10	ANT Dummy	PC Adj.	MOD.ANA	1.5±0.05kHz
		Test Tone:1kHz				
59	CW ID Dev(wide)	f-Center Ch4	ANT Dummy	PC Adj.	MOD.ANA	2±0.1kHz
		CW ID:800Hz				
60	CW ID Dev(narrow)	f-Center Ch10	ANT Dummy	PC Adj.	MOD.ANA	1±0.05kHz
		CW ID:800Hz				
61	Repeat Gain Level(wide)	f-Center Ch4	RX ANT SG	PC Adj.	Radio tester	1±0.2kHz
		1kHzDev/1kHzMod	TX ANT Dummy		MOD.ANA	
62	Repeat Gain Level(narrow)	f-Center Ch10	RX ANT SG	PC Adj.	Radio tester	1±0.2kHz
		1kHzDev/1kHzMod	TX ANT Dummy		MOD.ANA	
63	Pager Dev(wide only)	VCO-A(Center) Ch2	ANT Dummy	PC Adj.	MOD.ANA	Adj 137
					AG	
64	Pager Blance(wide only)	VCO-B(Center) Ch2	ANT Dummy	PC Adj.	MOD.ANA	Make the demodulation wave square
					AG	
65	Pager Dev(wide only)	VCO-B(Center) Ch2	PTT/D-Sub 5pin	Check	MOD.ANA	±4.5kHz shift
		1kHz/3Vpp/Square	DATA IN/D-Sub 6pin		AG	
66	TX S/N(Wide)	VCO-A(Center) Ch2	D-Sub TA terminal	Check	MOD.ANA	Less than -55dB
		No modulation	(9pin)			
67		VCO-B(Center) Ch5		Check	MOD.ANA	Less than -55dB
68	TX S/N(Narrow)	VCO-A(Center) Ch8	D-Sub TA terminal	Check	MOD.ANA	Less than -50dB
		No modulation	(9pin)			
69		VCO-B(Center) Ch11		Check	MOD.ANA	Less than -50dB
70	END	Remove I/F jig and powersupply				

TKR－840 Circuit Description

Outline

The TKR-840 is a UHF-band relay radio unit for business radio applications.
It has the following features:

- High-performance model with enhanced basic functions
- QT and DQT signalling function for waiting 16 signals at the same time
- Various remote functions that can be used by base stations
- Fine frequency steps using DDS
- Signalling encoding and AF processing with DSP

Transmitter Unit

The transmitter unit (X56-305 A/3) consists of the following circuits:(1) internal / external reference circuit. (2) transmit reference PLL circuit. (3) transmit DDS circuit. (4) transmit main PLL circuit. (5) driver circuit. (6) modulation level adjustment circuit. and (7) other circuits.

(1) The internal / external reference circuit switches between the internal +/－1.0ppm / 20MHz TCXO (X101) and the 10MHz external reference automatically. If there is no external reference input, the internal TCXO is used as the reference frequency. When an external reference (10MHz/ -10dBm or higher) is input , the external reference is automatically used as the reference frequency. The circuit 0f Q102 ,Q106,XF210,Q109,D101,D103,Q15,X101,Q205,D205,Q206,IC204,Q110,Q114,Q112,Q113,Q108,XF211,and Q115.

(2) The transmit reference PLL circuit generates the reference frequency signal (19.2MHz) for the transmit DDS and modulates the low-frequency components of QT and DQT . This circuit consists of IC201,X201,Q201,and Q202. The signal generated by the VCO is fed to buffer amplifier Q202 and unwanted harmonic components are removed with a LPF . The resulting signal goes to PLL IC (IC201). and its phase is compared with that of the reference using the comperieng frequency of 200kHz. The phase difference signal is converted to a direct current voltage by a laglead type loop filter. The capacity of D201 and D204 is varied by the direct current voltage to keep the VCO oscillator frequency 19.2MHz . The 19.2MHz oscillator signal is fed to Q241 and used as the reference frequency signal for the transmit DDS.

(3) The transmit DDS circuit produce the reference frequency signal (4.5MHz) for the DDS PLL and modulates the low-frequency components of digital pager modulation. This circuit of IC241,IC202,IC107,IC207,Q207,and Q242. The 19.2MHz signal coming from the transmit sub PLL is amplified by Q241 and fed to IC202. IC202 produces the about 4.5MHz reference frequency signal for the transmit main PLL based on 19.2MHz signal. Since the comparison frequency of the transmit main PLL is 100kHz. the PLL frequency step is 100kHz. However, fine frequency step, such as 2.5kHz and 1.25kHz, can be used because the DDS output frequency is variable. IC202 can perform binary FSK modulation. Digital pager modulation is implemented by applying low-range modulation to DDS and high-range modulation to the transmit main PLL. There is a two-stage butterworth filter (cutoff frequencty:3.2kHz) consisting of IC102 in the high-range modulation line. The IC102 shift input is delayed by IC107 and IC207 to maintain phase balance between the low and high ranges. (See the level adjustment circuit description.)

(4) The transmit main PLL circuit produces the transmit frequency signal and consists of VCO's (Q1 and Q2) and a single-chip PLL IC (IC101). When transmitting 450.000MHz to 464.995MHz for F1 destination. 480.000 to 496.995MHz for F2 destination. and 400.000 to 414.995MHz for F3 destination. the Q1 VCO oscillates. When transmitting 465.000MHz to 480.000MHz for F1 destination, 497.000 to 512.000MHz for F2 destination, and 415.000 to 430.000MHz for F3 destination, the Q1 VCO oscillates. IC101 divides the VCO oscillator signal and the transmit PLL reference signal (4.5MHz) and the phase is compared with the 100kHz comparison frequency. The phase difference signal is converted to a direct current signal with a laglead type loop filter. The direct current signal is applied to varicap D1,D3,D2,D4 to lock the VCO oscillator frequency with the desired oscillator frequency. At the same time , the direct current signal passes through the IC109 operational amplifier and buffer amplifier, and is output as a voltage (CVT) for monitoring the transmit main PLL lock voltage.

(5) The driver circuit amplifiers the transmit frequency signal to the level required for input to the final unit (X56-305 B/3). This circuit consists of high-frequency amplifier Q9,high-frequency switch D7, high-frequency amplifier Q13 ,high – frequency amplifier Q14, and switching elements Q203,Q8,Q10,Q12 and Q11. The transmit signal level input to Q13 is about 0dBm . Since it is amplified by about 15dB by Q13,and also amplified by about 8dB by Q14, the output from Q14 becomes

about 200mW. Since it is attenuated according to destination with the R257,R258, and attenuators, the output is 20dBm(about 100mW) at the CN1 drive output connector.

(6) The level adjustment circuit adjusts the modulation signal level to provide a prescribed modulation and adjusts transmission power. This circuit consists of IC105,IC3,IC100,IC102,IC203,IC208, and Q21. IC3 is an electronic volume IC. The signalling frequency change adjustment, signalling modulation balance adjustment, digital pager modulation balance adjustment, maximum sound frequency change, and the reference voltage setting for transmission power adjustment are performed according to data from the CPU using the FPU. IC105 is a modulation signal summing amplifier (A/2) and a signalling signal amplitude fine-adjustment amplifier (B/2). IC102 is a platter filter for digital pager modulation and has the same characteristic of a two-stage butterworth filter with a cutoff frequency of 3.2kHz . IC203 is a DC amplifier that amplifies the transmission power reference voltage generated by IC3. Q21 outputs 5V to the final unit as an H/L signal when the transmission power mode is "LOW" and outputs 0V when the transmission power mode is "HIGH".

(7) In addition , IC106 is an EEPROM . The transmission adjustment data adjusted for each unit is written into the EEPROM. If the unit is installed in another set, it is not necessary to adjust it again from the beginning , but only fine-adjustment is necessary for each unit. IC1,IC2,IC103,IC108 and IC110 are three-pin constant-voltage power supply IC's . Each circuit contains its own power IC to maintain isolation between circuits.

Final Unit

The final unit (X56-305 B/3) mainly amplifies transmission power to a specified level. This unit consists of the following circuits: (1) power module, (2) harmonic wave elimination circuit, (3) progressive wave power / reflected wave power detection circuit, (4) APC circuit, (5) abnormal temperature detection circuit, (6) common mode unwanted radiation prevention circuit and (7) AVR circuit.

(1) The power module IC301 is a power module M68732** for portable transceivers. The driver output of the transmit unit passes through an attenuator ,Which differs with destinations, and enters an input pin (pin 1:RFI) of power module IC301. The power

module IC301 amplifies power according to the voltage at the amplification control pin (pin 2:VGG) and output it from the output pin (pin 4:RFO).

(2) The harmonic wave elimination circuit uses a three-stage "pi" type Chebyshev type LPF consisting of L301,L302,L303,C307,C312,C315 and C316. This circuit removes harmonic wave components from the transmission power amplified by the power module and sends the resulting signal to the progressive wave power / reflective power detection circuit.

(3) The progressive wave power / reflective wave power detection circuit consists of a CM coupling type detection circuit formed by a strip line and a direct current amplifier IC303(A/2,B/2), which are used in high-power mode , and a capacity coupling double-voltage detection circuit and direct current amplifier IC302(A/2), which are used in low-power mode. The transmission power which passes through the strip line is output from CN308.

(4) The APC circuit consists of differential amplifier IC302 (B/2), direct current amplifier Q301, analog switch IC304 ,and switching transistors Q312 and Q313. The high-power / low-power detection values are switched by analog switch IC304. The power setting range in high-power mode is 1 to 5W. The power setting range in low-power mode is 100mW to about 2W.

(5) The abnormal temperature detection circuit consists of thermal switch TS301 and digital transistorQ302 . This circuit disable the transmission power amplification function and prevents temperature rise to protect the circuit when the final unit temperature rise excessively (95C or higher) and the circuits cannot be safely operated.

(6) Common mode unwanted radiation prevention circuit. The TKR-840 has a filter L304 at the power line inlet in the final unit to reduce common mode unwanted radiation from the power cable.

(7) The AVR circuit is designed to provide the power supply voltage required to operate power module IC301. This circuit consists of Q306,Q307,D312,Q310,Q305, and D317.

For continuous operation (100% duty), there are two large-current AVRs with discrete for the power module using low-heat-resistant power transistor 2SB951A to prevent concentration of heat. The 8V AVR is controlled by 8T. and a time constant is set at the beginning of output to start transmission power smoothly and prevent band spreading.

Receiver Unit

The receiver unit (X55-306) consists of the following circuits: (1) front-end circuit ,(2) narrow IF circuit, (3) wide IF circuit ,(4) receiver main PLL circuit, (5) receive sub PLL circuit, (6) receive DDS circuit, (7) base-band circuit, and (8) other circuit.

(1) The front-end circuit consists of BPF L3, high-frequency amplifier Q7 ,BPF L16, mixer DBM A1, and IF switching circuit D10. The helical BPF covers frequency range F1: 450.000 to 480.000MHz ,F2:480.000 to 512.000MHz,and F3:400.000 to 430.000MHz,and the spread for F1,F2, and F3 is 5.0MHz. The BPF L16 attenuates the unwanted out-of-band high-frequency components produced by high-frequency amplifier Q7 and unwanted components. and sends only the necessary signal to mixer DBM A1 . The mixer DBM A1 mixer the first local oscillator signal generated by the first local oscillator PLL with the receive signal coming from the helical BPF L16 to produce a first IF signal (73.05MHz). The first IF signal is fed to the narrow IF or wide IF circuit by the following D10.

(2) The narrow IF circuit operates during narrow-band reception and consists of two-pole MCF XF2, four-pole MCF XF4, IF amplifier Q25, IF amplifier Q32, FM detection IC IC7 ,ceramic filter CF1,CF3 . The unwanted components of the removed by two-pole MCF XF4 and the resulting signal is amplified by IF amplifier Q25 and Q32. The FM IC IC7 produces the second IF signal (450kHz) , ceramic filter CF1and CF3 remove unwanted components, and an IF amplifier amplifies the signal, and the quadruture detection circuit FM-detects the signal to produce a base-band signal and output it from pin 15. The base-band signal passes through analog switch IC18. inversion amplifier IC15(B/2), low-frequency amplifier IC11 (A/2 and B/2), and IC11(A/2), and goes to the YO input of multiplexer IC9 and the V2 input of electronic volume IC9. The level of the signal that enters V2 of the electronic volume IC is adjusted, the signal passes through the hysteresis circuit AF switch Q34, goes to IC7 noise filter input (pin 17) ,and high-frequency components are removed by a HPF consisting of external CRs. The signal is noise-detected and compared ,and the noise

squelch signal (N-DET) is fed to DC switch Q36. The voltage signal (RSSI) from the two second IF amplifiers in IC7 are compared with the reference voltage set by electronic volume V4 by the internal RSSI comparator .and the RSSI squelch signal (C-DET) is output from pin 20 of IC7. C-DET enter DC switch Q37 and is ANDed with the N-DET by DC switch Q38 . A squelch signal (SC) is output from connector CN6.

(3) The wide IF circuit consists of two-pole MCF XF1, four-pole MCF XF3, IF amplifier Q24, IF amplifier Q31, FM detection IC IC8 ,ceramic filter CF2,CF4 . The unwanted components of the removed by two-pole MCF XF1 and four-pole MCF XF3 and the resulting signal is amplified by IF amplifier Q24 and Q31. The FM IC IC7 produces the second IF signal (450kHz) , ceramic filter CF2 and CF4 remove unwanted components, and an IF amplifier amplifies the signal, and the quadruture detection circuit FM-detects the signal to produce a base-band signal and output it from pin 15. The base-band signal passes through analog switch IC21, inversion amplifier IC15(A/2), low-frequency amplifier IC12 (A/2), and goes to the Y1 input of multiplexer IC and the V1 input of electronic volume IC9. The level of the signal that enters V1 of the electronic volume IC is adjusted. the signal passes through the hysteresis circuit AF switch Q35, goes to IC8 noise filter input (pin 17) .and high-frequency components are removed by a HPF consisting of external CRs. The signal is noise-detected and compared ,and the noise squelch signal (N-DET) is fed to DC switch Q36. The voltage signal (RSSI) from the two second IF amplifiers in IC8 are compared with the reference voltage set by electronic volume V3 by the internal RSSI comparator ,and the RSSI squelch signal (C-DET) is output from pin 20 of IC8. C-DET enter DC switch Q37 and is ANDed with the N-DET by DC switch Q38 . and output as a squelch signal (SC) .

(4) The receiver main PLL circuit consists of VCOs (Q8,Q9) and a single-chip PLL IC IC1 ,buffer amplifier Q14 ,high-frequency amplifier Q3.Q1,Q5, and Q6. The first local oscillator is an lower heterodyne local oscillator .and the VCO oscillator frequency is F1:376.950 to 406.950MHz,F2:406.950 to 438.950MHz, F3:326.950 to 356.950MHz. In addition ,two VCOs cover two bands: The Q8 covers the lower band and the Q9 VOC covers the upper band . PLL IC compares the 4.5MHz signal from the receive DDS circuit and the VCO signal with the 100kHz comparison frequency.

(5) The receive sub PLL circuit produces a second local oscillator signal for the receiver .and consists of PLL IC IC15 . crystal oscillator X1, oscillator FET Q21 ,buffer amplifier Q23 high-frequency amplifier Q15, Q30, Q33, and emitter follower Q27. The VCO consists of a crystal oscillator circuit (Q21 and X1) and varicap D9.

(6) The receive DDS circuit varies the reference frequency of the receive main PLL to implement fine frequency steps which cannot be achieved by a single-loop PLL. This circuit comprises IC20, Q33, Q39, and CF5. The output frequency is used as the reference frequency for the receive main PLL.

(7) The base-band signal circuit consists of HPF Q26, LPF Q28,D11,and Q29. The base-band signals detected by the narrow FM and wide FM detection circuit de-emphasized by LPF Q28. The sub-audio band components of the signal are removed by HPF Q26 , and the resulting signal is switched with a squelch signal by D11 and Q29, and output as an RA signal from CN6.

(8) In addition , the receiver circuit contains an EEPROM (IC10) as in the transmitter circuit. Adjustment data for each unit and the last channel data are written into the EEPROM . IC2,IC4,IC13,and IC16 are three-pin constant voltage power supply ICs . Q17 is a ripple filter for the power supplied to the first local oscillator PLL VCO . IC3 is a shift register. Q16,Q18,Q19,Q20,and Q22 are switching transistors.

Control Circuit

The control unit (X53-388) consists of the following circuit : (1) main CPU ,(2) sub CPU,(3) DSP circuit, (4) AF PA circuit ,(5) display circuit ,(6) base-band circuit ,(7) Microphone AGC circuit, (8) RS-232C circuit , (9) power supply circuit.

(1) The main CPU (IC17) is a 16bit single-chip microcomputer containing a 128k ROM and 5k RAM. This CPU controls the sūb CPU ,the flash ROM , and the DSP , encodes high-speed and low-speed data, controls the transmitter unit. The receiver unit, the control unit, and the display circuit and transfers data to or from an external device.

(2) The sub CPU (IC18) is of the same type as the main CPU, but is programmed so that it operate as the sub CPU by connecting its pin 18 to GND (pin 18 of the main CPU is connected to Vdd). The sub CPU mainly function as an I/O expander , and controls the flash ROM , DSP, and extended I/O.

(3) The DSP circuit filters transmit / receive audio signal and decodes signalling (QT,DQT). This circuit consists of IC30,IC24,IC27,IC22,IC31,IC34, and IC25. The receive signal DET is converted from analog to digital by IC27 with a sampling frequency of 16.128kHz. The digitized audio signal is sent to DSP IC30 to process the signalling signal and audio signal. The processed digital audio signal is fed to cordec IC27 , converted from digital to analog, and the analog signal is output from pin (VoutR). Then ,the audio signal is amplified by IC34 (ICB/2), passes through the IC34 (A/2) low-pass filter ,and goes to multiplexer IC37. The transmit audio signal coming from pin 13 of IC29 is amplified by IC22 (B/2), fed to pin 6 (VinR) of cordec IC27, and converted from analog to digital at a sampling frequency of 16.128kHz . The digitized transmit audio signal is AGC-processed , pre-emphasized and filtered at 300Hz to 3kHz by DSP IC30 , and the resulting signal is fed back to cordec IC27, and converted from digital to analog, and the analog signal is output from pin 15 (VoutL). The transmit signal from VoutL is amplified by IC34 (B/2), passes through the IC34 (A/2) low-pass filter, and goes to the IC12 (A/2) summing amplifier . IC25 is a counter IC and the clock required for the cordec and DSP is generated by dividing the 16.515MHz clock signal produced by DSP IC30.

(4) The AF PA circuit is an AF amplifier for driving speakers to monitor receive audio signal. This circuit consists of IC45. The 4W audio output can be provided to external speaker by supplying power supply voltage 13.8V/4 ohms through the 15-pin test connector "SPO,SPG" on the rear panel. The output impedance of the internal speaker is adjusted to provide an audio output of about 0.2W when the internal speaker installed on this model front panel is used.

(5) The display circuit contains 7-segment LED D700,D701 (orange: see the operation manual for details of display.) D703 (green: circuit power supply), D704 (red: transmission), D705 (green: busy), two-color LED D702 (green: internal; red external reference state). LEDs in switches S700 to S705,IC700,IC701,IC702 and

IC703 to display this model channels and states. IC700 to IC703 are shift registers which convert serial data from the CPU to parallel data and light LEDs . Q706,Q707,Q708,Q709,and Q710 are switching transistors which control two-color LED D702. IC704,IC705, and IC706 are three-pin power supply ICs which produce power used for the display circuit.

(6) The base-band circuit switches between the modulation signal to the transmitter unit, demodulation signal from the receiver unit, and remote audio and adjusts their levels. This circuit consists of IC12,IC13,IC14,IC29,IC32,IC33,IC36, and IC40. Modulation inputs include local microphone input, repeat audio input (RTA), low-speed data (LSD), high-speed data (HSD), external audio input (TA) , external data input (TD), and remote modulation input (RTA), and demodulation outputs include receive audio output (RA), receive data output (RD), and remote receive audio (RRA). The multiplexer (IC14,IC29,IC37) changes signals, the electronic volume (IC33) adjusts the level , and the operational amplifier (IC12,IC13,IC32,IC36,IC42) amplifier and sums signals.

(7) The microphone AGC circuit AGC-amplifies an audio signal coming from a local microphone so that it dose not saturates. This circuit consists of IC23 , D707,D709,D700, and D701. The AGC is operated by controlling the + and −side levels of amplitude using the current obtained by positive and negative detection of the amplified audio signal.

(8) The RS-232C circuit connects the RS-232C serial port of a personal computer directly to this model to perform FPU operation. The FPU operation can also be performed by connecting a programming cable (KPG-46) to the local microphone on the front panel. But , if the D-sub connector on the rear panel is used, the programming cable is not required. The 232C driver IC (IC14) changes the TTL-232C level . The FPU (KPG-47D) has a new transmitter / receiver circuit monitor function (transmission: transmission progressive power display, transmission reflective power display, transmit main PLL lock voltage display; reception :RSSI display , receive main PLL lock voltage display). Data required for this function is also transferred through the RS-232C serial port. The firmware can only be rewritten with the local microphone on the front panel.

(9) The power supply circuit generates power to operate the CPU .DSP ,flash ROM. bi-directional buffer. and base-band circuit . this circuit consists of IC3.IC4.IC5. and IC6.