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FIBOCOM_NL952-NA_ Hardware_User_Manual

Version: 1.0.1

Date: 2020-02-28

Applicability Table

No.	Product model	Description
1	NL952-NA-00	Cat20 WWAN Module
2	NL952-NA-20	Cat12 WWAN Module

Copyright

Notice

The document is subject to update from time to time owing to the product version upgrade or other reasons. Unless otherwise specified, the document only serves as the user guide. All the statements, information and suggestions contained in the document do not constitute any explicit or implicit guarantee.

Warning

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-- Reorient or relocate the receiving antenna.

-- Increase the separation between the equipment and receiver.

-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-- Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End user must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

The portable device is designed to meet the requirements for
exposure to radio waves established by the Federal Communications
Commission (USA). These requirements set a SAR limit of 1.6 W/kg
averaged over one gram of tissue. The highest SAR value reported under
this standard during product certification for use when properly worn on the body

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

(1) this device may not cause interference,

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) l'appareil ne doit pas produire de brouillage,

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Trademark

The trademark is registered and owned by Fibocom Wireless Inc.

Versions

Version	Author	Date	Remark
V1.0.0	Lei Daijun	2020-01-02	Draft version
V1.0.1	Xu Xialin	2020-02-28	● Add NL952-NA-00 and NL952-NA-20 ● Add PCIe_BOOT_DISABLE definition

Contents

1 Foreword

1.1 Introduction

The document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of NL952-NA (hereinafter referred to as NL952). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of NL952 modules and develop products.

1.2 Reference Standard

The design of the product complies with the following standards:

- 3GPP TS 34.121-1 V8.11.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD);Part 1: Conformance specification
- 3GPP TS 34.122 V14.0.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V14.0.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI Express M.2 Specification Rev1.2

1.3 Related Documents

- RF Antenna Application Design Specification
- NL952 System Driver Integration and Application Guidance
- NL952 AT Commands Manual

2 Overview

2.1 Introduction

NL952 is a highly integrated 4G WWAN module which uses M.2 form factor interface. It supports LTE FDD/LTE TDD/WCDMA systems and can be applied to most cellular networks of mobile carrier in the world.

2.2 Specification

Specification			
Operating Band	LTE FDD: Band 2, 4, 5, 7, 12, 13, 14, 17, 25, 26, 29, 30, 66, 71		
	LTE TDD: Band 41, 46, 48		
	DL 4x4 MIMO: Band 2, 4, 7, 25, 30, 66, 41, 48		
	WCDMA/HSPA+: Band 2, 4, 5,		
	GNSS: support GPS, GLONASS, Galileo, BDS		
Data Transmission		NL952-NA-20(Cat12)	NL952-NA-00(Cat20)
	LTE FDD	600Mbps DL(Cat 12)/ 150Mbps UL	2Gbps DL(Cat20)/ 150Mbps UL
	LTE TDD	~460Mbps DL(Cat 12)/ 90Mbps UL	~1.44Gbps DL(Cat20)/ 90Mbps UL
		When LTE TDD achieves maximum DL rate, its UL rate can reach 30Mbps only	
	UMTS/ HSPA+	UMTS:384 kbps DL/384 kbps UL	
		DC-HSPA+:42 Mbps DL(Cat 24)/5.76 Mbps UL(Cat6)	
Carrier aggregation		3CA Downlink Max	6CA Downlink Max
Power Supply	DC 3.3V～4.4V, Typical 3.8V		
Temperature	Normal operating temperature: -10° C ～+55° C Extended operating temperature: -30° C ～+75° C		
	Storage temperature: -40° C～+85° C		
Physical characteristics	Interface: M.2 Key-B		
	Dimension：30 x 52 x 2.3mm		
	Weight: About 8.0 g		
Interface			
Antenna Connector	WWAN Antenna x 4		
	Support 4x4 MIMO		

Specification	
Function Interface	Dual SIM, 1.8V/3V
	PCIe 2.0 X1
	USB 2.0
	USB 3.0
	W_Disable#
	BodySar
	LED
	Tunable antenna(Reserved)
	I2S(Reserved)
Software	
Protocol Stack	IPV4/IPV6
AT commands	3GPP TS 27.007 and 27.005
Firmware update	USB/PCIe
Other feature	Multiple carrier
	Windows update

Note:

When temperature goes beyond normal operating temperature range of -10°C~+55°C, RF performance of module may be slightly off 3GPP specifications.

2.3 CA combinations

DL CA Combinations		
2CA	Inter-band	TBD
	Intra-band(non-contiguous)	TBD
	Intra-band(contiguous)	TBD
3CA	Inter-band	TBD
	2 intra-band(non-contiguous) plus inter-band	TBD
	2 intra-band(contiguous) plus inter-band	TBD
	Intra-band(non-contiguous)	TBD
	Intra-band(contiguous)	TBD
4CA	Inter-band	TBD
	2 intra-band(non-contiguous) plus inter-band	TBD
	2 intra-band(contiguous) plus inter-band	TBD
	2 intra-band(contiguous) plus 2 intra-band(contiguous)	TBD
	2 intra-band(contiguous) plus 2 intra-band(non-contiguous)	TBD
	3 intra-band(contiguous) plus inter-band	TBD
	Intra-band(non-contiguous)	TBD
	Intra-band(contiguous)	TBD
5CA	2 intra-band(contiguous) plus 2 intra-band(contiguous) plus inter-band	TBD
	2 intra-band(contiguous) plus 3 inter-band	TBD
	2 intra-band(contiguous) plus 2 intra-band(non-contiguous) plus inter-band	TBD
	3 intra-band(contiguous) plus 2 intra-band(non-contiguous)	TBD
	3 intra-band(contiguous) plus 2 inter-band	TBD
	3 intra-band(contiguous) plus 2 intra-band(non-contiguous)	TBD
	4 intra-band(contiguous) plus inter-band	TBD
	Intra-band(non-contiguous)	TBD
6CA	4 intra-band(contiguous) plus 2 inter-band	TBD

2.4 Application Block

The peripheral applications for NL952 module are shown in Figure 2-1:

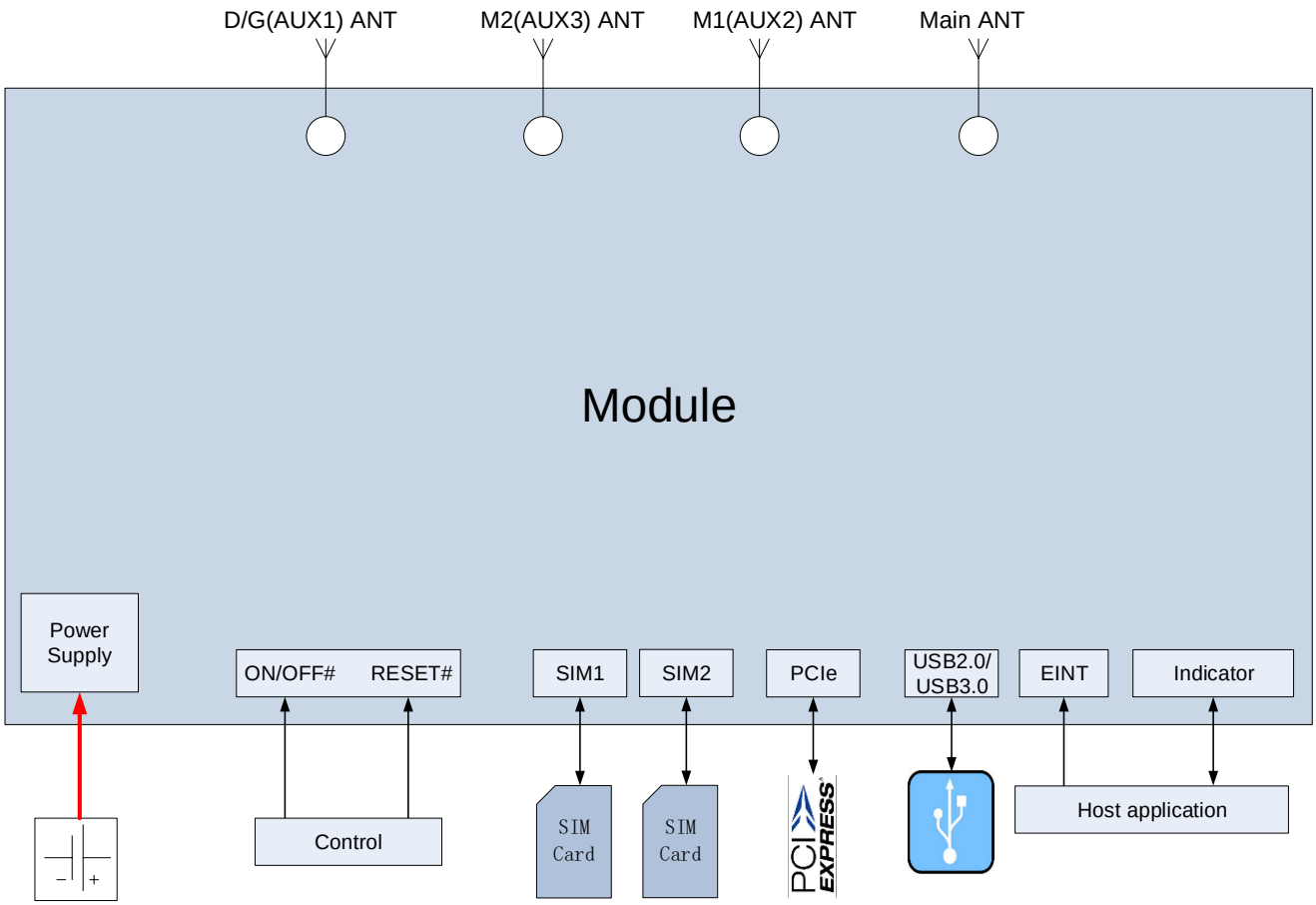

Figure2-1 Application Block

2.5 Antenna Configuration

NL952 module support four antennas and the configuration is as below table:

Antenna Connector	Function Description	Band configuration
M	Main ANT	All supported bands transmit & receive
M1	MIMO1 ANT	4x4 MIMO supported bands receive
M2	MIMO2 ANT	4x4 MIMO supported bands receive 2nd UL on inter band ULCA mode(TBD)
D/G	Diversity & GNSS ANT	All supported bands and GNSS receive

3 Application Interface

3.1 M.2 Interface

The NL952 module applies standard M.2 Key-B interface, with a total of 75 pins.

3.1.1 Pin Map

74	+3.3V	CONFIG_2	75
72	+3.3V	VIO_CFG	73
70	+3.3V	GND	71
68	ANT_CONFIG(1.8V)	CONFIG_1	69
66	SIM1_DETECT(1.8V)	RESET#(1.8V)	67
64	COEX_TXD(1.8V)	ANTCTL3(1.8V)	65
62	COEX_RXD(1.8V)	ANTCTL2(1.8V)	63
60	COEX3(1.8V)	ANTCTL1(1.8V)	61
58	RFE_RFFE_SDATA	ANTCTL0(1.8V)	59
56	RFE_RFFE_SCLK	GND	57
54	PEWAKE# (3.3/1.8V)	REFCLKP	55
52	CLKREQ# (3.3/1.8V)	REFCLKN	53
50	PERST# (3.3/1.8V)	GND	51
48	UIM2_PWR	PERp0	49
46	UIM2_RESET	PERn0	47
44	UIM2_CLK	GND	45
42	UIM2_DATA	PETp0	43
40	SIM2_DETECT(1.8V)	PETn0	41
38	PCIE_EARLY_BOOT_DISABLE	GND	39
36	UIM1_PWR	USB3.0-Rx+	37
34	UIM1_DATA	USB3.0-Rx -	35
32	UIM1_CLK	GND	33
30	UIM1_RESET	USB3.0-Tx+	31
28	I2S_WA(1.8V)	USB3.0-Tx -	29
26	W_DISABLE2#(3.3/1.8V)	GND	27
24	I2S_TX(1.8V)	DPR(3.3/1.8V)	25
22	I2S_RX(1.8V)	WOWWAN#(1.8V)	23
20	I2S_CLK(1.8V)	CONFIG_0	21
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
10	LED1#(3.3V OD)	GND	11
8	W_DISABLE1#(3.3/1.8V)	USB D-	9
6	FULL_CARD_POWER_OFF#(3.3/1.8V)	USB D+	7
4	+3.3V	GND	5
2	+3.3V	GND	3
		CONFIG_3	1

Figure 3-1 Pin Map

Note:

Pin “Notch” represents the gap of the gold fingers.

3.1.2 Pin Definition

The pin definition is as below table:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
1	CONFIG_3	O	NC	NC, NL952 M.2 module is configured as the WWAN – PCIe, USB3.0 interface type	
2	+3.3V	PI	-	Power input	Power Supply
3	GND	-	-	GND	Power Supply
4	+3.3V	PI	-	Power input	Power Supply
5	GND	-	-	GND	Power Supply
6	FULL_CARD_ POWER_OFF#	I	PU	Power enable, Module power on input, internal pull up(40KΩ)	3.3/1.8V
7	USB D+	I/O		USB Data Plus	0.3---3V
8	W_DISABLE1#	I	PD	WWAN Disable, active low	3.3/1.8V
9	USB D-	I/O		USB Data Minus	0.3---3V
10	LED1#	OD	T	System status LED, Output open drain, 3.3V	3.3V
11	GND	-	-	GND	Power Supply
12	Notch			Notch	
13	Notch			Notch	
14	Notch			Notch	
15	Notch			Notch	
16	Notch			Notch	
17	Notch			Notch	
18	Notch			Notch	
19	Notch			Notch	
20	I2S_CLK	O	PD	I2S Serial clock, Reserved	1.8V
21	CONFIG_0		NC	NC, NL952 M.2 module is configured as the WWAN – PCIe, USB3.0 interface type	
22	I2S_RX	I	PD	I2S Serial receive data, Reserved	1.8V
23	WOWWAN#	O	PD	Wake up host, Reserved	1.8V
24	I2S_TX	O	PD	I2S Serial transmit data, Reserved	1.8V
25	DPR	I	PD	Body SAR Detect, active low	3.3/1.8V

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
26	W_DISABLE2#	I	PD	GNSS disable, active low, Reserved	3.3/1.8V
27	GND	-	-	GND	Power Supply
28	I2S_WA	O	PD	I2S Word alignment/select, Reserved	1.8V
29	USB3.0_TX-	O		USB3.0 Transmit data minus	
30	UIM_RESET	O	PD	SIM reset signal	1.8V/3V
31	USB3.0_TX+	O		USB3.0 Transmit data plus	
32	UIM_CLK	O	PD	SIM clock Signal	1.8V/3V
33	GND	-	-	GND	Power Supply
34	UIM_DATA	I/O	PD	SIM data input/output	1.8V/3V
35	USB3.0_RX-	I		USB3.0 receive data minus	
36	UIM_PWR	O		SIM power supply, 1.8V/3V	1.8V/3V
37	USB3.0_RX+	I		USB3.0 receive data plus	
38	PCIe_ BOOT_DISABLE	I	PD	PCIe early boot/USB normal boot select, Reserved	1.8V
39	GND	-	-	GND	Power Supply
40	SIM2_DETECT	I	PD	SIM2 Detect, internal pull up(390KΩ), active high	1.8V
41	PETn0	O		PCIe TX Differential signals Negative	
42	UIM2_DATA	I/O	PD	SIM2 data input/output	1.8V/3V
43	PETp0	O		PCIe TX Differential signals Positive	
44	UIM2_CLK	O	PD	SIM2 clock Signal	1.8V/3V
45	GND	-	-	GND	Power Supply
46	UIM2_RESET	O	PD	SIM2 reset signal	1.8V/3V
47	PERn0	I		PCIe RX Differential signals Negative	
48	UIM2_PWR	O		SIM2 power supply, 1.8V/3V	1.8V/3V
49	PERp0	I		PCIe RX Differential signals Positive	
50	PERST#	I	PU	Asserted to reset module PCIe interface default. If module went into core dump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ)	3.3/1.8V
51	GND	-	-	GND	Power Supply

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
52	CLKREQ#	I/O	PD	Asserted by device to request a PCIe reference clock be available (active clock state) in order to transmit data. It also used by L1 PM Sub states mechanism, asserted by either host or device to initiate an L1 exit. Active low, open drain output and should add external pull up on platform	3.3/1.8V
53	REFCLKN	I		PCIe Reference Clock signal Negative	
54	PEWAKE#	O	PD	Asserted to wake up system and reactivate PCIe link from L2 to L0, it depends on system whether supports wake up functionality. Active low, open drain output and should add external pull up on platform	3.3/1.8V
55	REFCLKP	I		PCIe Reference Clock signal Positive	
56	RFFE_SCLK	O	PD	MIPI Interface Tunable ANT, RFFE clock	1.8V
57	GND			GND	Power Supply
58	RFFE_SDATA	I/O	PD	MIPI Interface Tunable ANT, RFFE data	1.8V
59	ANTCTL0	O	PD	Tunable ANT CTRL0	1.8V
60	COEX3	I/O	TBD	Wireless Coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. COEX_EXT_FTA, Reserved	1.8V
61	ANTCTL1	O	PD	Tunable ANT CTRL1	1.8V
62	COEX_RXD	I	PD	Wireless Coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. UART receive signal(WWAN module side), Reserved	1.8V
63	ANTCTL2	O	PD	Tunable ANT CTRL2	1.8V
64	COEX_TXD	O	PD	Wireless Coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. UART transmit signal(WWAN module side), Reserved	1.8V
65	ANTCTL3	O	PD	Tunable ANT CTRL3	1.8V
66	SIM1_DETECT	I	PD	SIM1 Detect, internal pull up(390KΩ), active high	1.8V
67	RESET#	I	PU	WWAN reset input, active low, internal pull up(40KΩ)	1.8V

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
68	ANT_CONFIG	I	PD	Host antenna configuration detect, internal pull up(100KΩ), Reserved	1.8V
69	CONFIG_1	O	GND	GND, NL952 M.2 module is configured as the WWAN – PCIe, USB3.0 interface type	
70	+3.3V	PI	-	Power input	Power Supply
71	GND	-	-	GND	Power Supply
72	+3.3V	PI	-	Power input	Power Supply
73	VIO_CFG	-	NC	Configuration of PCIe sideband signals power domain NC: support 1.8V/3.3V; GND: support 3.3V	
74	+3.3V	PI	-	Power input	Power Supply
75	CONFIG_2	O	NC	NC, NL952 M.2 module is configured as the WWAN – PCIe, USB3.0 interface type	

Reset Value: The initial status after module reset, not the status when working.

H: High Voltage Level

L: Low Voltage Level

PD: Pull-Down

PU: Pull-Up

T: Tristate

OD: Open Drain

PI: Power Input

PO: Power Output

Note:

The unused pins can be left floating.

3.2 Power Supply

The power interface of NL952 module as shown in the following table:

Pin	Pin Name	I/O	Pin Description	DC Parameter（V）		
				Minimum Value	Typical Value	Maximum Value
2, 4, 70, 72, 74	+3.3V	PI	Power supply input	3.3	3.8	4.4
36	UIM_PWR	PO	USIM power supply	-	1.8V/3V	-
48	UIM2_PWR	PO	USIM power supply	-	1.8V/3V	-

NL952 module uses PCIe interface, according to the PCIe specification, the PCIe Vmain should be used as the +3.3V power source, not the Vaux. The Vaux is the PCIe backup power source and it is not sufficient as the power supply. In addition, the DC/DC power supply other than PCIe ports should not be used as the external power cannot control the module status through the PCIe protocol.

3.2.1 Power Supply

The NL952 module should be powered through the +3.3V pins, and the power supply design is shown in Figure 3-2:

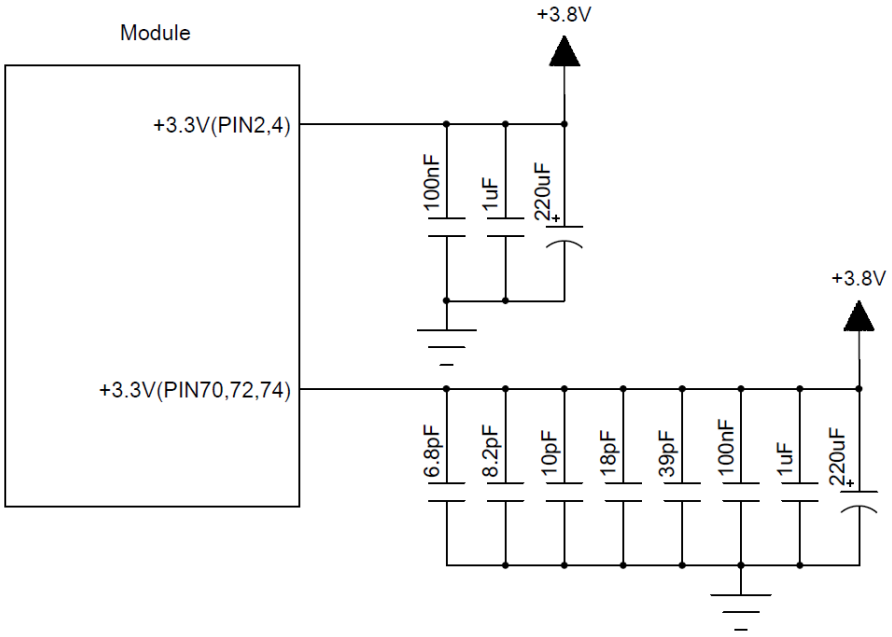

Figure 3-2 Power Supply Design

The filter capacitor design for power supply as shown in the following table:

Recommended capacitance	Application	Description
220uF x 2	Voltage-stabilizing capacitors	Reduce power fluctuations of the module in operation, requiring capacitors with low ESR. ● LDO or DC/DC power supply requires the capacitor of no less than 440uF ● The capacitor for battery power supply can be reduced to 100~200uF
1uF, 100nF	Digital signal noise	Filter out the interference generated from the clock and digital signals
39pF, 33pF	700/800, 850/900 MHz frequency band	Filter out low frequency band RF interference
18pF, 10pF, 8.2pF, 6.8pF	1500/1800, 2100/2300, 2600MHz, 3500/3600/3700MHz	Filter out medium/high frequency band RF interference

The stable power supply can ensure the normal operation of NL952 module; and the ripple of the power supply should be less than 300mV in design. Because module support 5CA download, when module operates with the maximum data transfer throughput, the peak current can reach to upper 2500mA. It requests the power source voltage should not be lower than 3.3V, otherwise module may shut down or restart. The power supply requirement is shown in Figure 3-3:

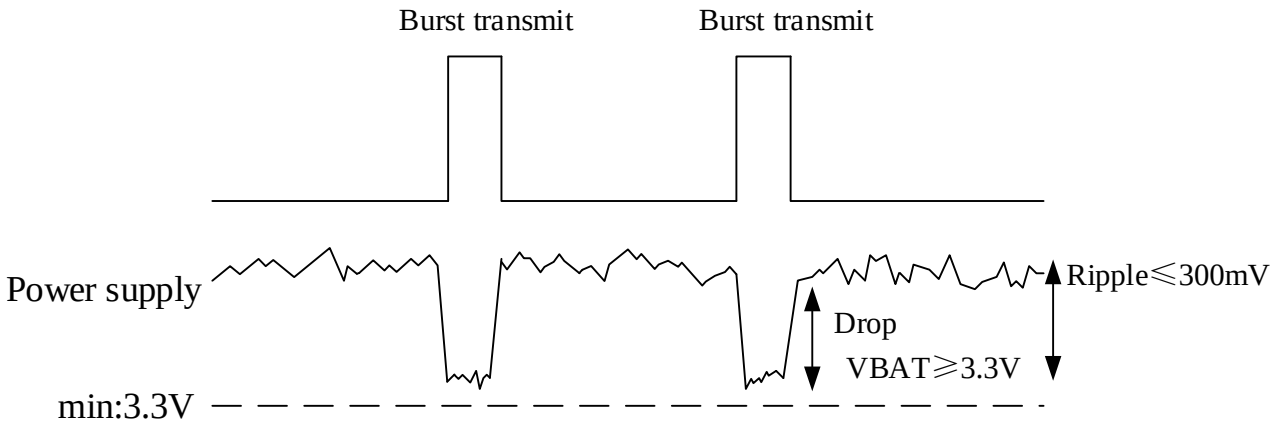

Figure 3-3 Power Supply Requirement

3.2.2 Logic level

The NL952 module 1.8V logic level definition as shown in the following table:

Parameters	Minimum	Typical	Maximum	Unit
1.8V logic level	1.71	1.8	1.89	V
V_{IH}	1.3	1.8	1.89	V
V_{IL}	-0.3	0	0.3	V

The NL952 module 3.3V logic level definition as shown in the following table:

Parameters	Minimum	Typical	Maximum	Unit
3.3V logic level	3.135	3.3	3.465	V
V_{IH}	2.3	3.3	3.465	V
V_{IL}	-0.3	0	0.3	V

3.2.3Power Consumption

In the condition of 3.3V power supply, the NL952 power consumption as shown in the following table:

Parameter	Mode	Condition	Typical Current (mA)
I_{off}	Power off	Power supply, module power off	TBD
I_{Sleep}	WCDMA	DRX=8	TBD
	LTE FDD	Paging cycle #64 frames (0.64 sec DRx cycle)	TBD
	LTE TDD	Paging cycle #64 frames (0.64 sec DRx cycle)	TBD
	Radio Off	AT+CFUN=4, Flight mode	TBD
$I_{WCDMA-RMS}$	WCDMA	WCDMA Data call Band 2 @+23.5dBm	TBD
		WCDMA Data call Band 4 @+23.5dBm	TBD
		WCDMA Data call Band 5 @+23.5dBm	TBD
$I_{LTE-RMS}$	LTE FDD	LTE FDD Data call Band 2 @+23dBm	TBD
		LTE FDD Data call Band 4 @+23dBm	TBD
		LTE FDD Data call Band 5 @+23dBm	TBD
		LTE FDD Data call Band 7 @+23dBm	TBD
		LTE FDD Data call Band 12 @+23dBm	TBD
		LTE FDD Data call Band 13 @+23dBm	TBD
		LTE FDD Data call Band 14 @+23dBm	TBD
		LTE FDD Data call Band 17 @+23dBm	TBD
		LTE FDD Data call Band 25 @+23dBm	TBD
		LTE TDD Data call Band 26 @+23dBm	TBD
		LTE TDD Data call Band 30 @+22dBm	TBD

Parameter	Mode	Condition	Typical Current (mA)
		LTE TDD Data call Band 66 @+23dBm	TBD
		LTE FDD Data call Band 71 @+23dBm	TBD
	LTE TDD	LTE TDD Data call Band 41 @+23dBm	TBD
		LTE TDD Data call Band 48 @+21.5dBm	TBD

Note：

The above data is the average value obtained by testing the sample for high/medium/low channels.

In 3CA mode, the NL952 power consumption is shown in the following table:

3CA Combination	Condition (Max data transfer)	Typical Current(mA)
TBD	Band 2 @+22dBm	TBD
	Band 4 @+22dBm	TBD
	Band 5 @+22dBm	TBD
	Band 7 @+22dBm	TBD
	Band 12 @+22dBm	TBD
	Band 13 @+22dBm	TBD
	Band 30 @+21dBm	TBD
	Band 48 @+20.5dBm	TBD
	Band 66 @+22dBm	TBD
	Band 71 @+22dBm	TBD

Note：

The data above is an average value tested on some samples at 25℃ temperature.

3.3 Control Signal

The NL952 module provides two control signals for power on/off and reset operations, the pin defined as

shown in the following table:

Pin	Pin Name	I/O	Reset Value	Functions	Level
6	FULL_CARD_POWER_OFF#	I	PU	Module power on/off input, internal pull up(40KΩ) Power on: High/Floating Power off: Low	3.3/1.8V
67	RESET#	I	PU	WWAN reset input, active low, internal pull up(40KΩ)	1.8V
50	PERST#	I	PU	Asserted to reset module PCIe interface default. If module went into core dump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ)	3.3/1.8V

Note：

RESET# and PERST# need to be controlled by independent GPIO, and not shared with other devices on the host.

3.3.1 Module Start-Up

3.3.1.1 Start-up Circuit

The FCPO#(FULL_CARD_POWER_OFF #) pin needs an external 3.3V or 1.8V pull up for booting up. AP (Application Processor) controls the module start-up. We recommend to use a reset value low or pull down port to control FCPO#, and also reserve an external pull down resistor on FCPO#. The circuit design is shown in Figure3-4:

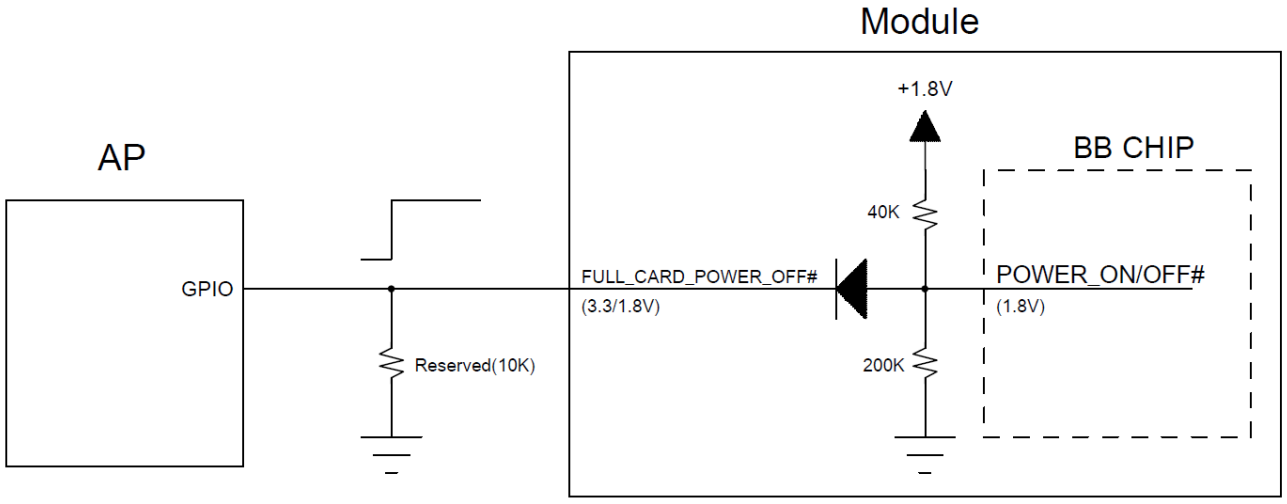

Figure 3-4 Circuit for Module Start-up Controlled by AP

3.3.1.2 Start-up Timing Sequence

When power supply is ready, the PMU of module will power on and start initialization process by pulling high FCPO# signal. After about 20s, module will complete initialization process. The start-up timing is

shown in Figure 3-5:

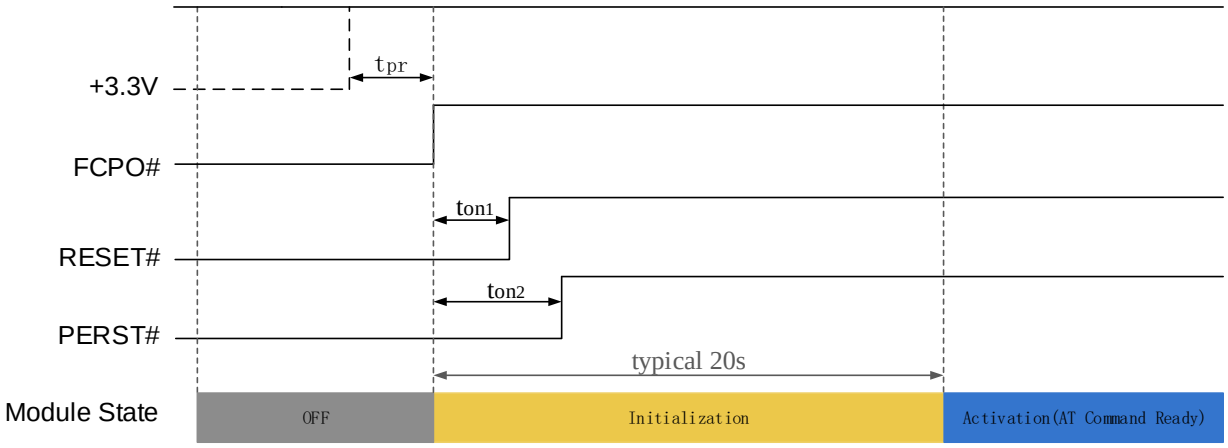

Figure 3-5 Timing Control for Start-up

Index	Min.	Recommended	Max.	Comments
t_{pr}	0ms	-	-	The delay time of power supply rising from 0V up to 3.3V.If power supply always ready, it can be ignored
t_{on1}	TBD	TBD	-	RESET# should be de-asserted after FCPO#
t_{on2}	TBD	TBD	-	The time delay of PERST# de-asserted after FCPO#, PERST# must always be the last to get de-asserted

The minimum detection time of PCIe link is about TBD after PERST# de-asserted.

Note：

When USB is used as data transfer interface, follow timing above in PERST# connecting with host, otherwise don't control PERST# in PERST# floating condition.

3.3.2 Module Shutdown

Module can be shut down by following control:

Shutdown Control	Action	Condition
Software	Sending AT+CFUN=0 command	Normal shutdown(recommend)
Hardware	Pull down FCPO# pin	Only used when a hardware exception occurs and the software control cannot be used.

Module can be shut down by sending AT+CFUN=0 command. When the module receives the software shutdown command, the module will start the finalization process (the reverse process of initialization), and it will be completed after t_{sd} time(t_{sd} is the time which AP receive OK of "AT+CFUN=0", if there is no

response, the max t_{sd} is 5s). In the finalization process, the module will save the network, SIM card and some other parameters from memory, then clear the memory and shut down PMU. The software control timing is shown in Figure 3-6:

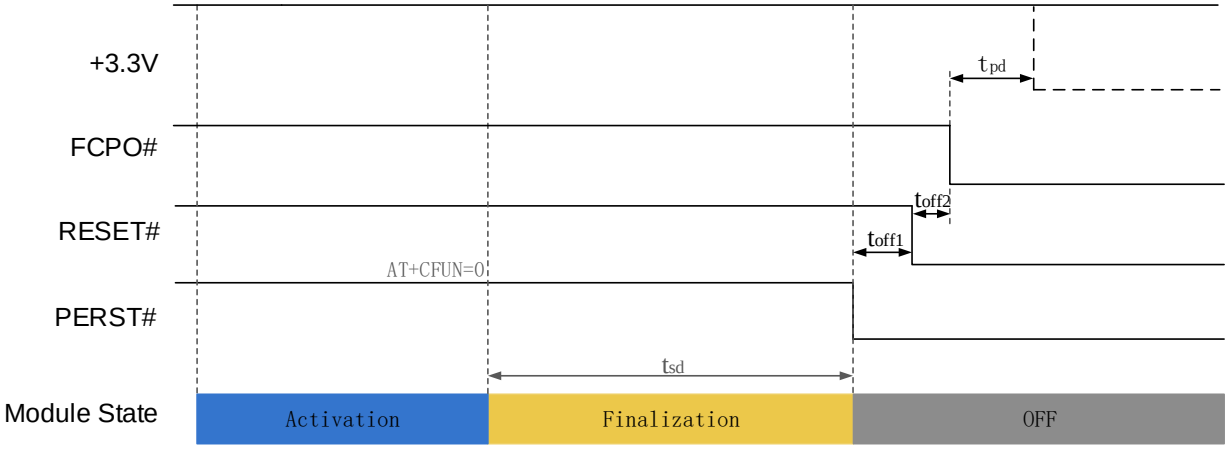

Figure 3-6 Software control power off timing

Index	Min.	Recommended	Max.	Comments
t_{off1}	TBD	TBD	-	RESET# should be asserted after PERST#
t_{off2}	TBD	TBD	-	FCPO# should be asserted after RESET#
t_{pd}	TBD	TBD	-	+3.3V power supply goes down time. If power supply is always on, it can be ignored

Note：

When USB is used as data transfer interface, follow timing above in PERST# connecting with host, otherwise don't control PERST# in PERST# floating condition.

3.3.3 Module Reset

The NL952 module can reset to its initial status by pulling down the RESET# signal for more than 2ms (10ms is recommended), and module will restart after RESET# signal is released. When customer executes RESET# function, the PMU remains its power inside the module. The recommended circuit design is shown in the Figure 3-7:

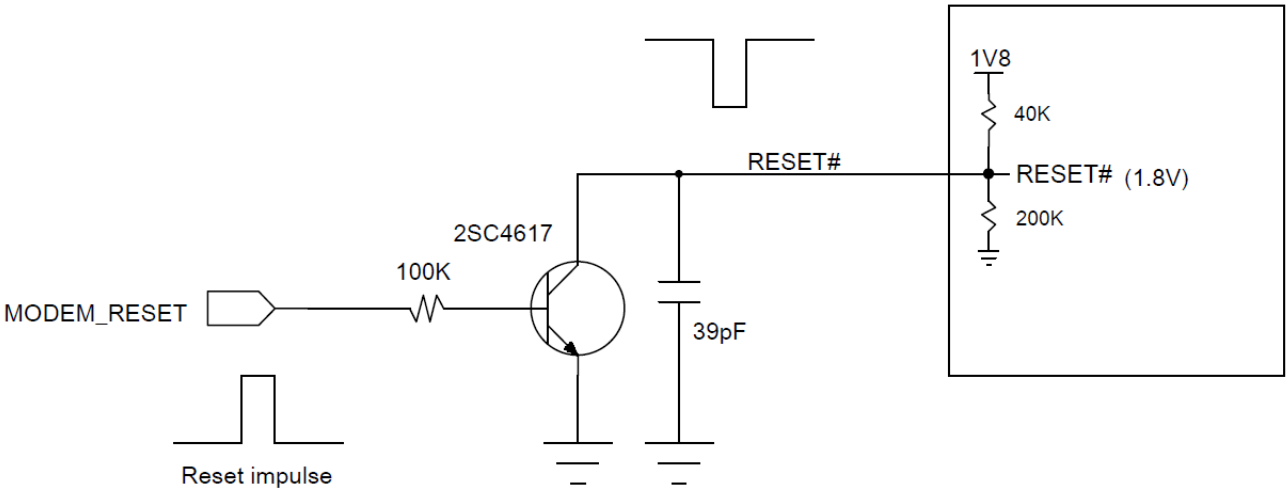

Figure 3-7 Recommended Design for Reset Circuit

There are two reset control timings as below:

- Reset timing 1st in Figure 3-8, PMU of module internal always on in reset sequence, recommend using in FW upgrade and module recovery;
- Reset timing 2nd in Figure 3-9, PMU of module internal will be off in reset sequence (including whole power off and power on sequence, t_{sd} can refer section 3.3.2), recommend using in system warm boot.

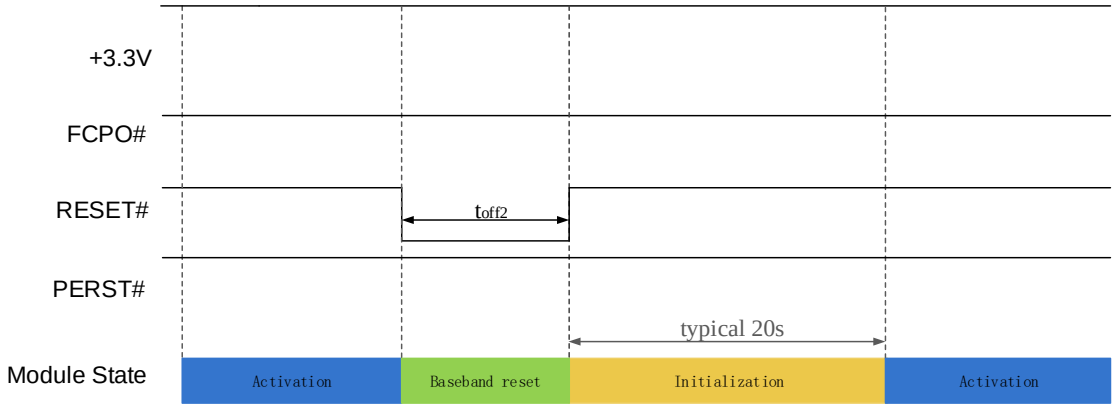

Figure 3-8 Reset control timing1st

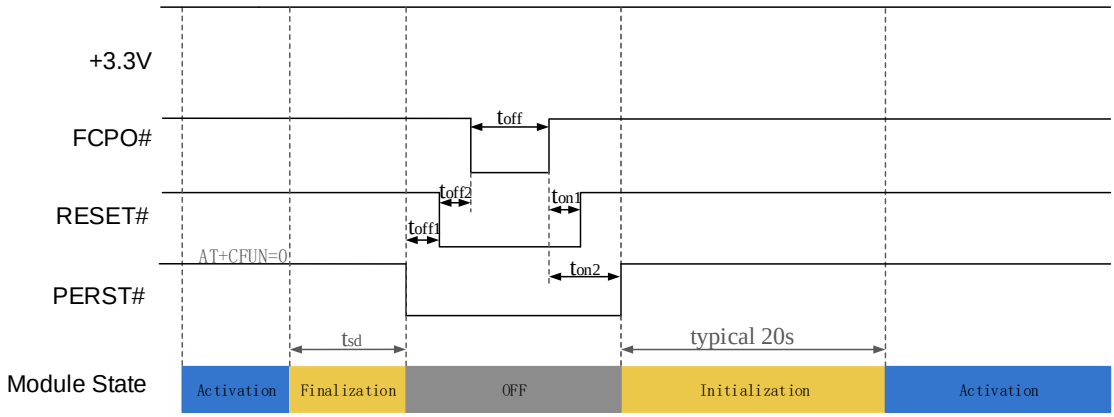

Figure 3-9 Reset control timing2nd

Index	Min.	Recommended	Max.	Comments
t_{off1}	TBD	TBD	-	RESET# should be asserted after PERST#, refer section 3.3.2
t_{off2}	TBD	TBD	-	FCPO# should be asserted after RESET#, refer section 3.3.2
t_{off}	TBD	TBD	-	Time to allow the WWAN module to fully discharge any residual voltages before the pin could be de-asserted again. This is required for both Pre-OS as well as Runtime flow
t_{on1}	TBD	TBD	-	RESET# should be de-asserted after FCPO#, refer section 3.3.1.2
t_{on2}	TBD	TBD	-	The time delay of PERST# de-asserted after FCPO#, PERST# must always be the last to get de-asserted. refer section 3.3.1.2

Note：

When USB is used as data transfer interface, follow timing above in PERST# connecting with host, otherwise don't control PERST# in PERST# floating condition.

3.3.4 PCIe Link State

3.3.4.1 D0 L1.2

Module supports PCIe goes into D0 L1.2 state in Win10 system. The D0->D0 L1.2@S0/S0ix->D0 timing is shown in figure 3-10:

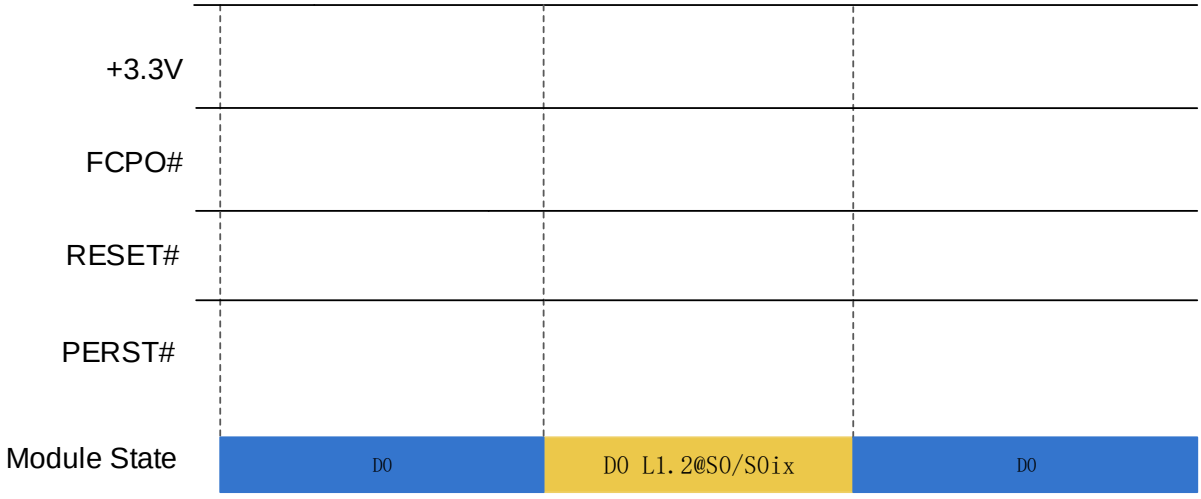

Figure 3-10 D0 L1.2 timing

Note：

When USB is used as data transfer interface in Chrome/Android/Linux OS, there is no PCIe link state. But when USB goes into suspend it also needs to follow the timing above (If PERST# is floating, don't control PERST#).

3.3.4.2 D3cold L2

Module supports PCIe goes into D3cold L2 state in Win10 system. The D0->D3cold L2@S0/S0ix ->D0 timing is shown in figure 3-11:

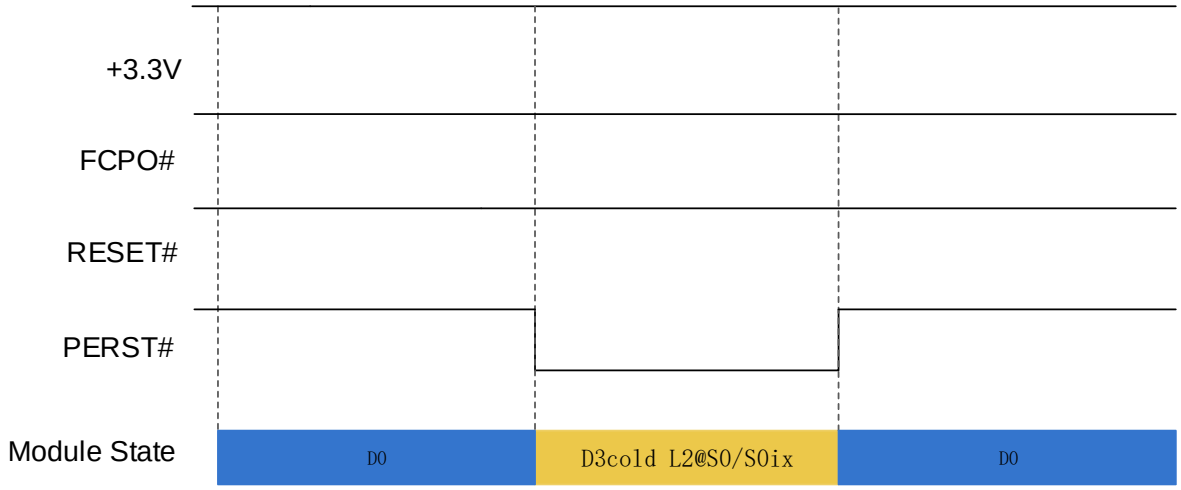

Figure 3-11 D3cold L2 timing

Note：

When USB is used as data transfer interface in Chrome/Android/Linux OS, there is no PCIe link state, so don't need to follow timing above.

3.3.5 Timing application

The recommended timing application in Win10 OS is as below table:

System status		Timing Application
S0ix (Modem standby)	D0 L1.2	Refer to section 3.3.4.1 Figure 3-10 D0 L1.2 Timing
	D3cold L2	Refer to section 3.3.4.2 Figure 3-11 D3cold L2 timing
S3,S4,S5	Power on (back to S0)	Refer to section 3.3.1.2 Figure 3-5 Timing control for start-up
	Power off (out of S0)	Refer to section 3.3.2 Figure 3-6 Software power off timing
G3 boot	Power on	Refer to section 3.3.1.2 Figure 3-5 Timing control for start-up
Warm boot		Refer to section 3.3.3 Figure 3-9 Reset timing 2nd
Modem FW upgrade / Modem recovery		Refer to section 3.3.3 Figure 3-8 Reset timing 1st

The recommended timing application in Chrome/Android/Linux OS is as below table:

System status	Timing Application
Power on	Refer to section 3.3.1.2 Figure 3-5 Timing control for start-up
Shut down	Refer to section 3.3.2 Figure 3-6 Software power off timing
Connect standby	Refer to section 3.3.4.1 Figure 3-10 D0 L1.2 Timing
Restart	Refer to section 3.3.3 Figure 3-9 Reset timing 2nd
Modem FW upgrade / Modem recovery	Refer to section 3.3.3 Figure 3-8 Reset timing 1st

3.4 IPC Interface

NL952 module supports PCIe and USB as IPC interface for data transfer. PCIe and USB interface functions are as below table:

Interface	System	Priority	Description
PCIe	Win10 OS	High	Priority: PCIe>USB. If PCIe and USB ports both connected with PC, module will initial PCIe first, then disable USB port
USB	Chrome/Linux/ Android OS	Low	It must disconnect PCIe port, only keep USB connecting. If keep PCIe and USB connecting both, it needs disable PCIe by BIOS/UEFI of PC

3.4.1 PCIe Interface

NL952 module supports PCIe Gen2, one lane for data transmission channel, it is also compatible with PCIe Gen1. PCIe interface initialized with host driver, then mapped MBIM & GNSS port in Win10 OS and RMNET & AT port in Chrome/Linux/Android OS. The MBIM and RMNET interfaces are used for data transfer, GNSS port is used for receiving GNSS data, AT port is used for AT command.

3.4.1.1 PCIe Interface Definition

Pin#	Pin Name	I/O	Reset Value	Description	Level
41	PETn0	O	-	PCIe TX Differential signals, Negative	-
43	PETP0	O	-	PCIe TX Differential signals, Positive	-
47	PERn0	I	-	PCIe RX Differential signals, Negative	-
49	PERP0	I	-	PCIe RX Differential signals, Positive	-

Pin#	Pin Name	I/O	Reset Value	Description	Level
53	REFCLKN	I	-	PCIe Reference Clock signal Negative	-
55	REFCLKP	I	-	PCIe Reference Clock signal Positive	-
50	PERST#	I	PU	Asserted to reset module PCIe interface default. If module went into coredump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ)	3.3/1.8V
52	CLKREQ#	I/O	PD	Asserted by device to request a PCIe reference clock be available (active clock state) in order to transmit data. It also used by L1 PM Sub states mechanism, asserted by either host or device to initiate an L1 exit. Active low, open drain output and should add external pull up on platform	3.3/1.8V
54	PEWAKE#	O	PD	Asserted to wake up system and reactivate PCIe link from L2 to L0, it depends on system whether supports wake up functionality. Active low, open drain output and should add external pull up on platform	3.3/1.8V

3.4.1.2 PCIe Interface Application

The reference circuit is shown in Figure 3-12:

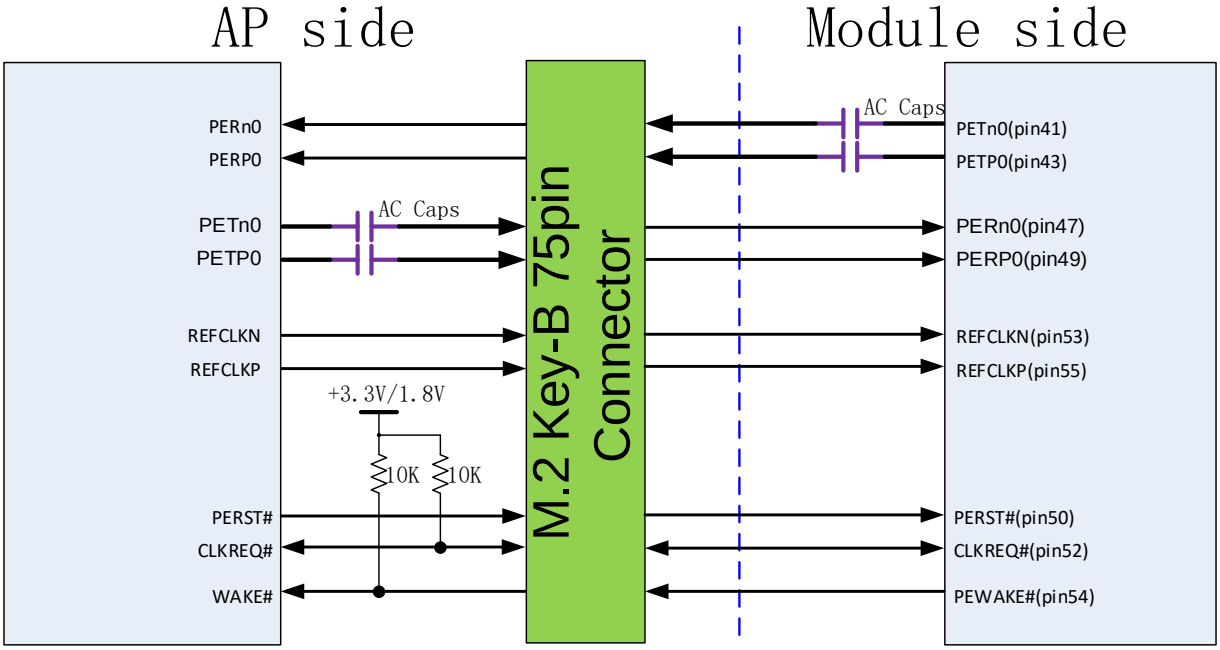

Figure 3-12 Reference Circuit for PCIe Interface

NL952 module supports PCIe Gen2 interface, including three difference pairs: transmit pair TXP/N,

receiving pair RXP/N and clock pair CLKP/N.

PCIe can achieve the maximum transmission rate of 5 GT/s, and must strictly follow the rules below in PCB Layout:

- The differential signal pair lines shall be parallel and equal in length;
- The differential signal pair lines shall be short if possible and be controlled within 15 inch(380 mm) for AP end;
- The impedance of differential signal pair lines is recommended to be 100 ohm, and can be controlled to 80～120 ohm in accordance with PCIe protocol;
- It shall avoid the discontinuous reference ground, such as segment and space;
- When the differential signal lines go through different layers, the via hole of grounding signal should be in close to that of signal, and generally, each pair of signals require 1-3 grounding signal via holes and the lines shall never cross the segment of plane;
- Try to avoid bended lines and avoid introducing common-mode noise in the system, which will influence the signal integrity and EMI of difference pair. As shown in Figure 3-13, the bending angle of all lines should be equal or greater than 135°, the spacing between difference pair lines should be larger than 20mil, and the line caused by bending should be greater than 1.5 times line width at least. When a serpentine line is used for length match with another line, the bended length of each segment shall be at least 3 times the line width (≥3W). The largest spacing between the bended part of the serpentine line and another one of the differential lines must be less than 2 times the spacing of normal differential lines (S1<2S);

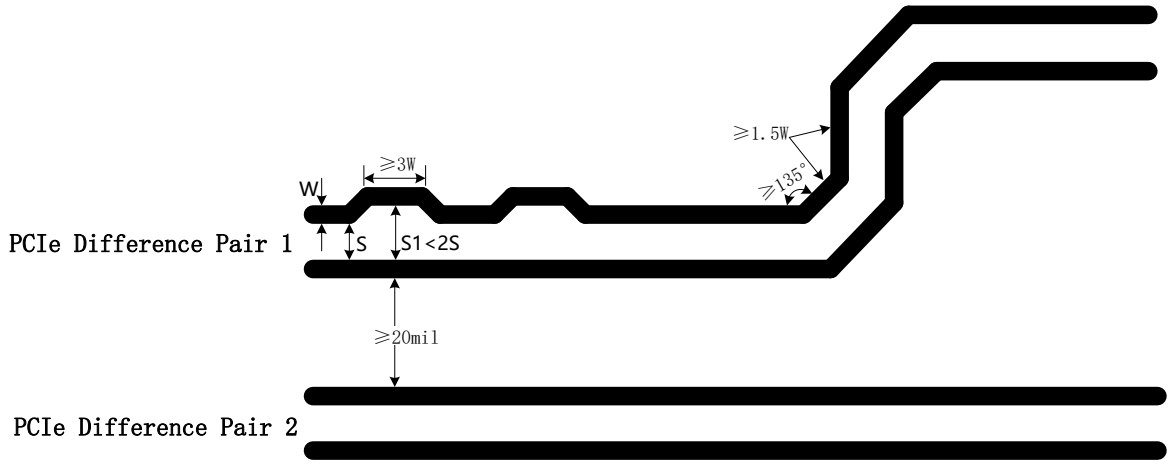

Figure 3-13 Requirement of PCIe Line

- The difference in length of two data lines in difference pair should be within 5mil, and the length match is required for all parts. When the length match is conducted for the differential lines, the designed position of correct match should be close to that of incorrect match, as shown in Figure 3-14. However, there is no specific requirements for the length match of transmit pair and receiving pair, that is, the length match is only required in the internal differential lines rather than between different difference pairs. The length match should be close to the signal pin and pass the small-angle bending design.

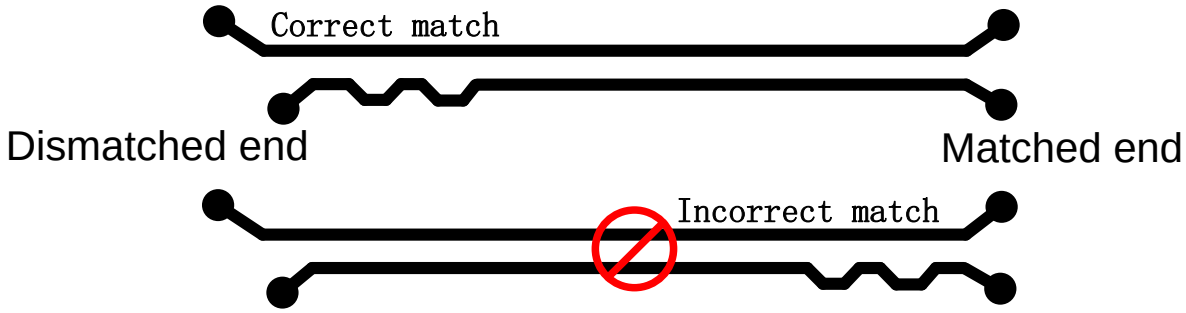

Figure 3-14 Length Match Design of PCIe Difference Pair

3.4.2 USB Interface

The NL952 module supports USB2.0 which is compatible with USB High-Speed (480 Mbit/s) and USB Full-Speed (12 Mbit/s).It supports USB3.0 using for LTE cat12 high speed data throughput at the same time. For the USB timing and electrical specification of NL952 module, please refer to Universal Serial Bus Specification 2.0" and "Universal Serial Bus Specification 3.0".

USB3.0 interface initialized with host driver, then mapped RMNET & AT port in Chrome/Linux/Android OS. The RMNET interfaces are used for data transfer, AT port is used for AT command. The port can be configured in practical application.

3.4.2.1 USB Interface Definition

Pin#	Pin Name	I/O	Description	Type
7	USB_D+	I/O	USB Data Plus	0.3---3V, USB2.0
9	USB_D-	I/O	USB Data Minus	0.3---3V, USB2.0
29	USB3.0_TX-	O	USB3.0 Transmit data minus	-
31	USB3.0_TX+	O	USB3.0 Transmit data plus	-
35	USB3.0_RX-	I	USB3.0 receive data minus	-
37	USB3.0_RX+	I	USB3.0 receive data plus	-

3.4.2.2 USB2.0 Interface Application

The reference circuit is shown in Figure 3-15:

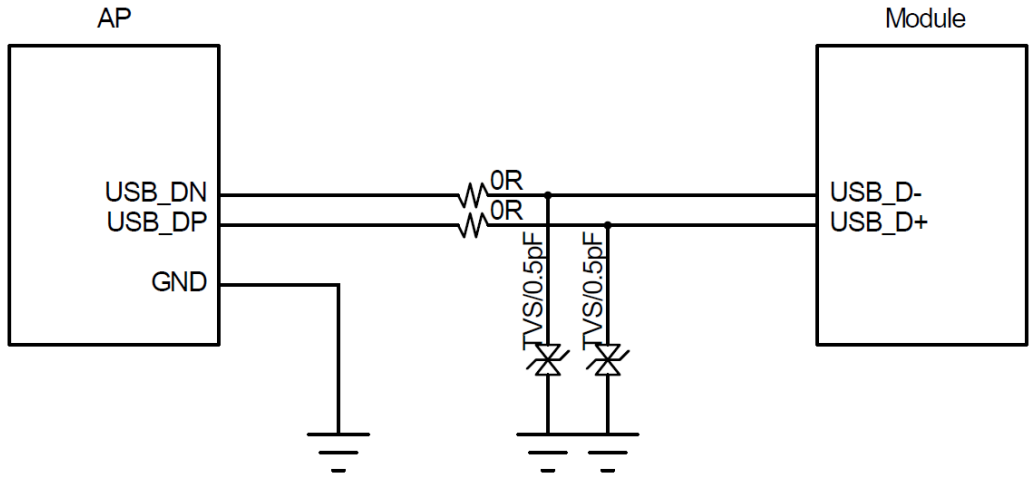

Figure 3-15 Reference Circuit for USB 2.0 Interface

Since the module supports USB 2.0 High-Speed, it is required to use TVS diodes with equivalent capacitance of 1pF or smaller ones on the USB_D-/D+ differential signal lines, it is recommended to use 0.5pF TVS diodes.

USB_D- and USB_D+ are high speed differential signal lines with the maximum transfer rate of480 Mbit/s, so the following rules shall be followed carefully in the case of PCB layout:

- USB_D- and USB_D+ signal lines should have the differential impedance of 90 ohms.
- USB_D- and USB_D+ signal lines should be parallel and have the equal length, the right angle routing should be avoided.
- USB_D- and USB_D+ signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

3.4.2.3 USB3.0 Interface Application

The reference circuit is shown in Figure 3-16:

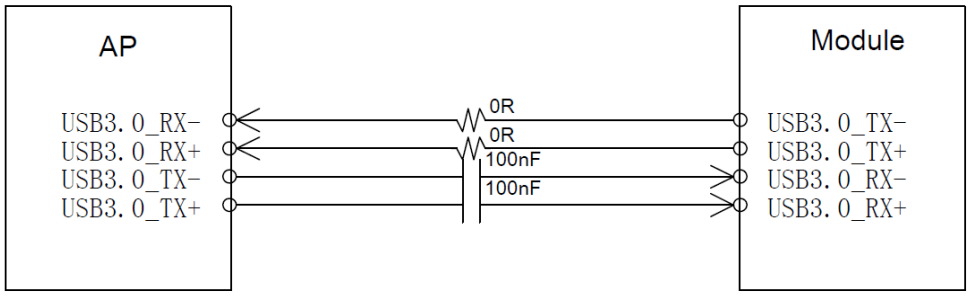

Figure 3-16 Reference Circuit for USB 3.0 Interface

USB 3.0 signals are super speed differential signal lines with the maximum transfer rate of 5Gbps.So the following rules shall be followed carefully in the case of PCB layout:

- USB3.0_TX-/USB3.0_TX+ and USB3.0_RX-/ USB3.0_RX+ are two pairs differential signal lines, the differential impedance should be controlled as 100 ohms.

- Two pairs of differential signal lines should be parallel and have the equal length, the right angle routing should be avoided.
- The two pairs differential signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

3.5 USIM Interface

The NL952 module support dual SIM card single standby, has dual built-in USIM card interface, which supports 1.8V and 3V SIM cards.

3.5.1 USIM1 Pins

The USIM1 pins description as shown in the following table:

Pin	Pin Name	I/O	Reset Value	Description	Level
36	UIM_PWR	PO	-	USIM power supply	1.8V/3V
30	UIM_RESET	O	PD	USIM reset	1.8V/3V
32	UIM_CLK	O	PD	USIM clock	1.8V/3V
34	UIM_DATA	I/O	PD	USIM data, internal pull up(4.7KΩ)	1.8V/3V
66	SIM_DETECT	I	PD	USIM card detect, internal 390K pull-up. Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached.	1.8V

3.5.2 USIM2 Pins

The USIM2 pins description as shown in the following table:

Pin	Pin Name	I/O	Reset Value	Description	Level
48	UIM2_PWR	PO	-	USIM2 power supply	1.8V/3V
46	UIM2_RESET	O	PD	USIM2 reset	1.8V/3V
44	UIM2_CLK	O	PD	USIM2 clock	1.8V/3V
42	UIM2_DATA	I/O	PD	USIM2 data, internal pull up(4.7KΩ)	1.8V/3V
40	SIM2_DETECT	I	PD	USIM2 card detect, internal 390K pull-up. Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached.	1.8V

3.5.3 USIM Interface Circuit

3.5.3.1 N.C. SIM Card Slot

The reference circuit design for N.C. (Normally Closed) SIM card slot is shown in Figure 3-17:

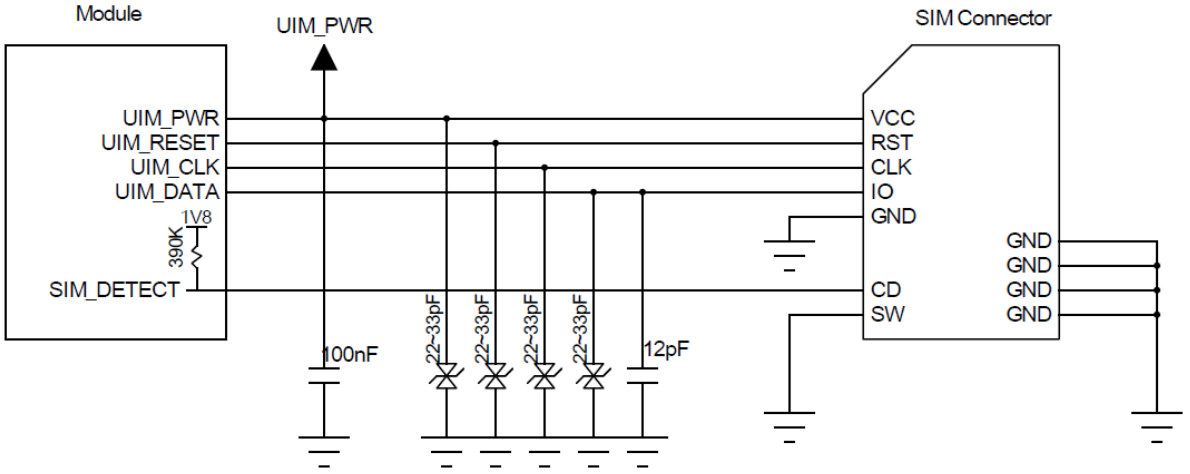

Figure 3-17 Reference Circuit for N.C. SIM Card Slot

The principles of the N.C.SIM card slot are described as follows:

- When the SIM card is detached, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin low.
- When the SIM card is inserted, it connects an open circuit between CD and SW pins, and drives the SIM_DETECT pin high.

3.5.3.2 N.O. SIM Card Slot

The reference circuit design for N.O. (Normally Open) SIM card slot is shown in Figure 3-18:

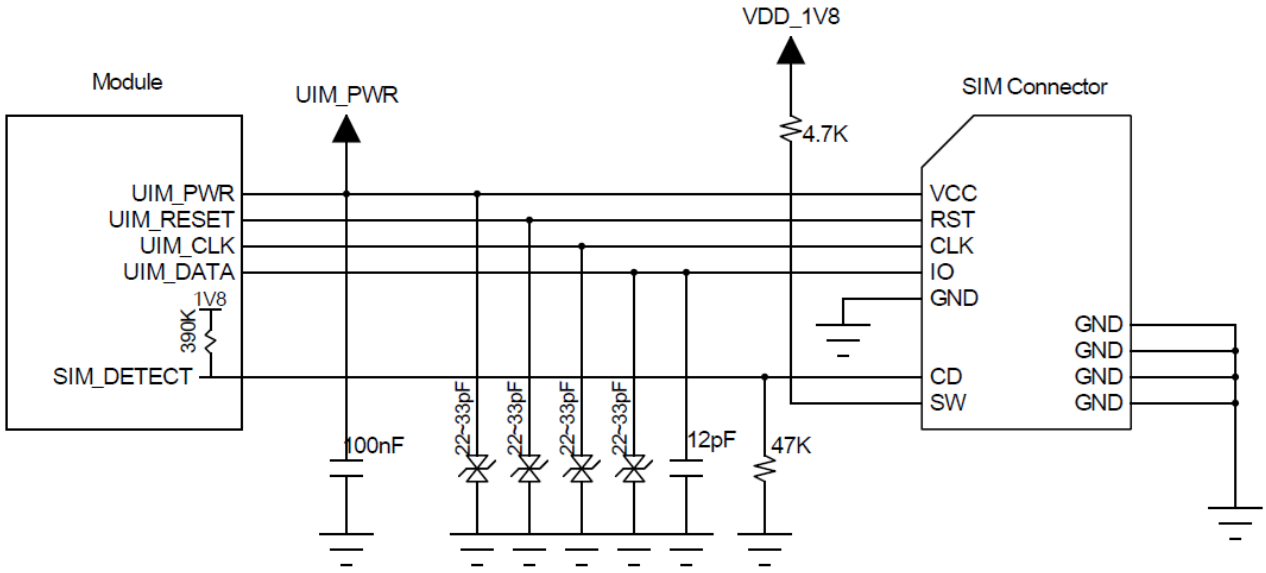

Figure 3-18 Reference Circuit for N.O. SIM Card Slot

The principles of the N.O.SIM card slot are described as follows:

- When the SIM card is detached, it connects an open circuit between CD and SW pins, and drives

the SIM_DETECT pin low.

- When the SIM card is inserted, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin high.

3.5.4 USIM Hot-Plugging

The NL952 module supports the SIM card hot-plugging function, which determines whether the SIM card is inserted or detached by detecting the SIM_DETECT pin state of the SIM card slot.

The SIM card hot-plugging function can be configured by “AT+MSMPD” command, and the description for AT command as shown in the following table:

AT Command	Hot-plugging Detection	Function Description
AT+MSMPD=1	Enable	Default value, the SIM card hot-plugging detection function is enabled. The module can detect whether the SIM card is inserted or not through the SIM_DETECT pin state.
AT+MSMPD=0	Disable	The SIM card hot-plugging detect function is disabled. The module reads the SIM card when starting up, and the SIM_DETECT status will not be detected.

Note:

By default, SIM_DETECT is active-high, which can be switched to active-low by the AT command. Please refer to the AT Commands Manual for the AT command.

3.5.5 USIM Design

The SIM card circuit design shall meet the EMC standards and ESD requirements with the improved capability to resist interference, to ensure that the SIM card can work stably. The following guidelines should be noted in case of design:

- The SIM card slot placement should near the module as close as possible, and away from the RF antenna, DC/DC power supply, clock signal lines, and other strong interference sources.
- The SIM card slot with a metal shielding housing can improve the anti-interference ability.
- The trace length between the SIM card slot and the module should not exceed 100mm, or it could reduce the signal quality.
- The UIM_CLK and UIM_DATA signal lines should be isolated by GND to avoid crosstalk interference. If it is difficult for the layout, the whole SIM signal lines should be wrapped with GND as a group at least.
- The filter capacitors and ESD devices for SIM card signals should be placed near to the SIM card slot, and the ESD devices with 22~33pF capacitance should be used.

3.6 Status Indicator

The NL952 module provides two signals to indicate the operating status of the module, and the status indicator pins as shown in the following table:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
10	LED1#	O	T	System status LED, drain output.	3.3V
23	WOWWAN#	O	PD	Module wakes up Host (AP)，Reserved	1.8V

3.6.1 LED#1 Signal

The LED#1 signal is used to indicate the operating status of the module, and the detailed description as shown in the following table:

Module Status	LED1# Signal
RF function ON	Low level (LED On)
RF function OFF	High level (LED Off)

The LED driving circuit is shown in figure 3-19:

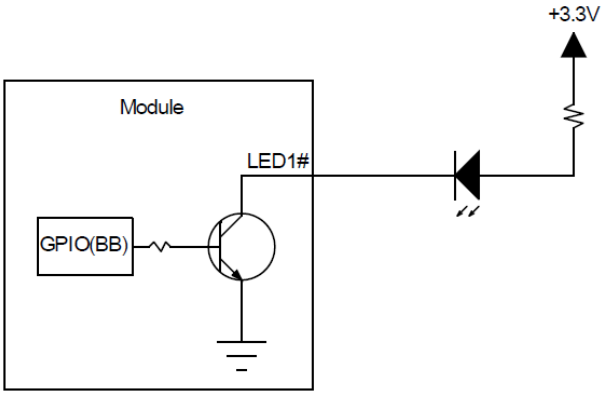

Figure 3-19 LED Driving Circuit

Note:

The resistance of LED current-limiting resistor is selected according to the driving voltage and the driving current.

3.6.2 WOWWAN#

The WOWWAN# signal is used to wake the Host (AP) when there comes the data request. The definition of WOWWAN# signal is as follows:

Operating Mode	WOWWAN# Signal
SMS or data requests	Pull low 1s then pull high (pulse signal) in default, the pulse can be configured by AT command.
Idle/Sleep	High level

The WOWWAN# timing is shown in Figure 3-20:

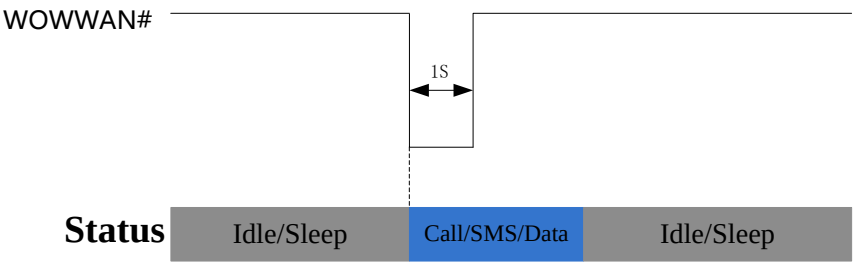

Figure 3-20 WOWWAN# Timing

Note:

WOWWAN# needs to send AT command: AT+GTWAKE=1,1 to enable this function.

3.7 Interrupt Control

The NL952 module provides four interrupt signals, and the pin definition is as follows:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
8	W_DISABLE1#	I	PD	Enable/Disable RF network	3.3/1.8V
25	DPR	I	PD	Body SAR detection	3.3/1.8V
26	W_DISABLE2#	I	PD	GNSS Disable signal Reserved	3.3/1.8V
38	PCIe_BOOT_DISABLE	I	PD	PCIe early boot/USB normal boot select	1.8V
68	ANT_CONFIG	I	PD	Host antenna configuration detection, Reserved	1.8V

3.7.1 W_DISABLE1#

The module provides a hardware pin to enable/disable WWAN RF function, and the function can also be controlled by the AT command. The module enters the Flight mode after the RF function is disabled. The definition of W_DISABLE1# signal is as below table:

W_DISABLE1# signal	Function
High/Floating	WWAN function is enabled, the module exits the Flight mode.
Low	WWAN function is disabled, the module enters Flight mode.

Note：

The function of W_DISABLE1# can be customized, please refer to the software porting guide.

3.7.2 BODYSAR

The NL952 module supports Body SAR function by detecting the DPR pin. The voltage level of DPR is high by default, and when the SAR sensor detects the closing human body, the DPR signal will be pulled down. As the result, the module then lowers down its emission power to its default threshold value, thus reducing the RF radiation on the human body. The threshold of emission power can be set by the AT Commands. The definition of DPR signal as shown in the following table:

DPR signal	Function
High/Floating	The module keeps the default emission power
Low	Lower the maximum emission power to the threshold value of the module.

3.7.3 PCIe_BOOT_DISABLE

Module provides USB/PCIe as IPC interface, the PCIe_BOOT_DISABLE signal is configured by host. If use PCIe interface as IPC interface, keep the signal Hi-Z/Floating. If use USB as IPC interface, connect it to 1.8V pull up with 4.7K ohm resistor. The definition of PCIe boot disable signal as shown in the following table:

PCIe_BOOT_DISABLE signal	Function
High	USB boot，Reserved
Hi-Z/Floating	PCIe early boot，Reserved

3.7.4 ANT_CONFIG

NL952 module can be configured to support dual antennas or 4 antennas by detecting the ANT_CONFIG pin. ANT_CONFIG is an input port which is pulled high internal in default. When ANT_CONFIG is high level, then module supports dual antennas (Main & D/G ANT). When module detects low level of ANT_CONFIG, then module will be configured to support 4 antennas. The definition of ANT_CONFIG signal is shown as below table:

ANT_CONFIG signal	Function
High/Floating	Support dual antennas(Main & D/G ANT)，Reserved
Low	Support 4 antennas，Reserved

3.8 ANT Tunable Interface (Reserved)

The module supports ANT Tunable interfaces with two different control modes, i.e. MIPI interface and 4bit GPO interface. Through cooperating with external antenna adapter switch via ANT Tunable, it can flexibly configure the bands of LTE antenna to improve the antenna’s working efficiency and save space for the

antenna.

Pin	Pin Name	I/O	Pin Description	Level
56	RFFE_SCLK	O	Tunable ANT control, MIPI Interface, RFFE clock	1.8V
58	RFFE_SDATA	I/O	Tunable ANT control, MIPI Interface, RFFE data	1.8V
59	ANTCTL0	O	Tunable ANT control, GPO interface, Bit0	1.8V
61	ANTCTL1	O	Tunable ANT control, GPO interface, bit1	1.8V
63	ANTCTL2	O	Tunable ANT control, GPO interface, Bit2	1.8V
65	ANTCTL3	O	Tunable ANT control, GPO interface, Bit3	1.8V

3.9 Configuration Interface

The NL952 module provides four configuration pins for the configuration as the WWAN-PCIe, type M.2 module:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
1	CONFIG_3	O	-	NC	
21	CONFIG_0	O	-	NC	
69	CONFIG_1	O	L	Internally connected to GND	
75	CONFIG_2	O	-	NC	

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	WWAN - PCIe Gen2	Vendor defined

Please refer to PCI Express M.2 Specification Rev1.2” for more details.

3.10 Other Interfaces

The module does not support other interfaces yet.

4 Radio Frequency

4.1 RF Interface

4.1.1RF Interface Functionality

The NL952 module supports four RF connectors used for external antenna connection. As the Figure 4-1 shows, “M” is for Main antenna, used to receive and transmit RF signals; “D/G” is for Diversity antenna, used to receive the diversity RF signals. “M1” and “M2” are used for support 4x4 MIMO data transfer.

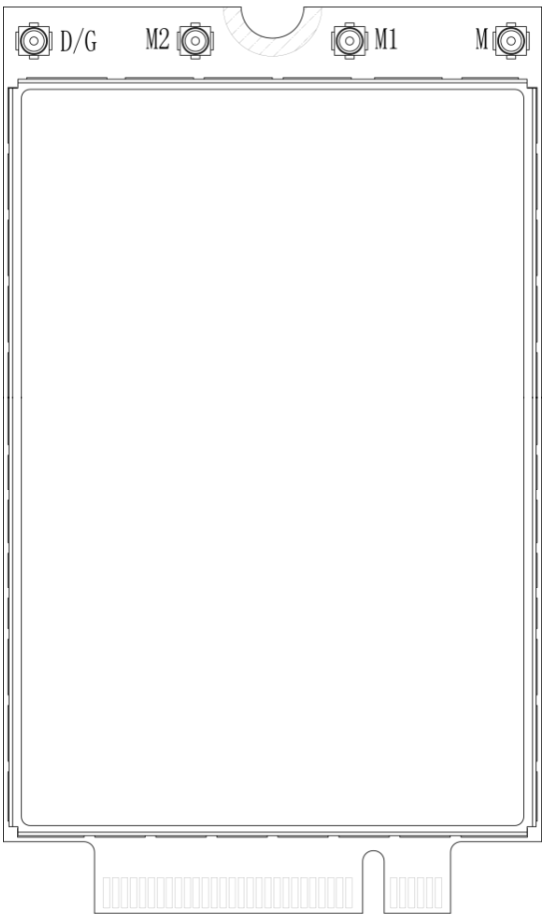

Figure 4-1 RF connectors

4.1.2 RF Connector Characteristic

Rated Condition		Environment Condition
Frequency Range	DC to 6GHz	Temperature Range
Characteristic Impedance	50Ω	－40° C to +85° C

4.1.3 RF Connector Dimension

NL952 module adopts standard M.2 module RF connectors, the model name is 818004607 from ECT Corporation, and the connector size is 2*2*0.6m. The connector dimension is shown as following picture:

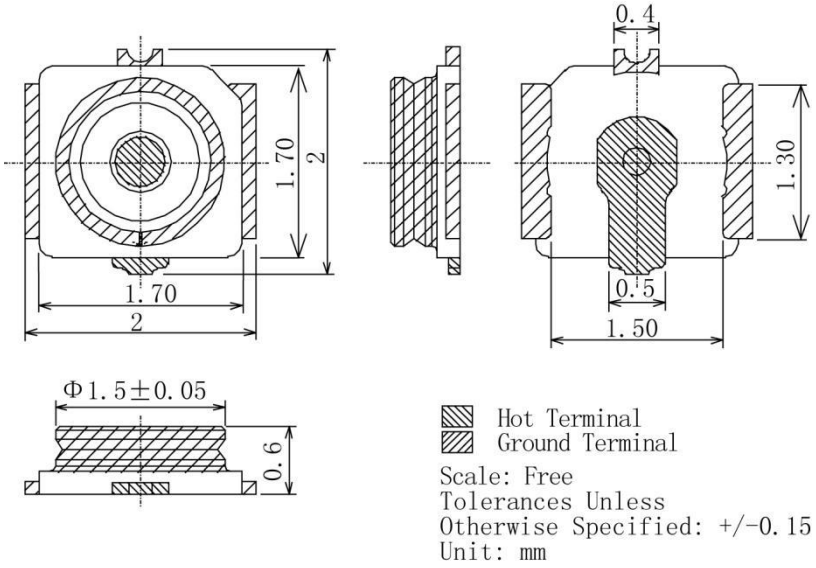

Figure 4-2 RF connector dimensions

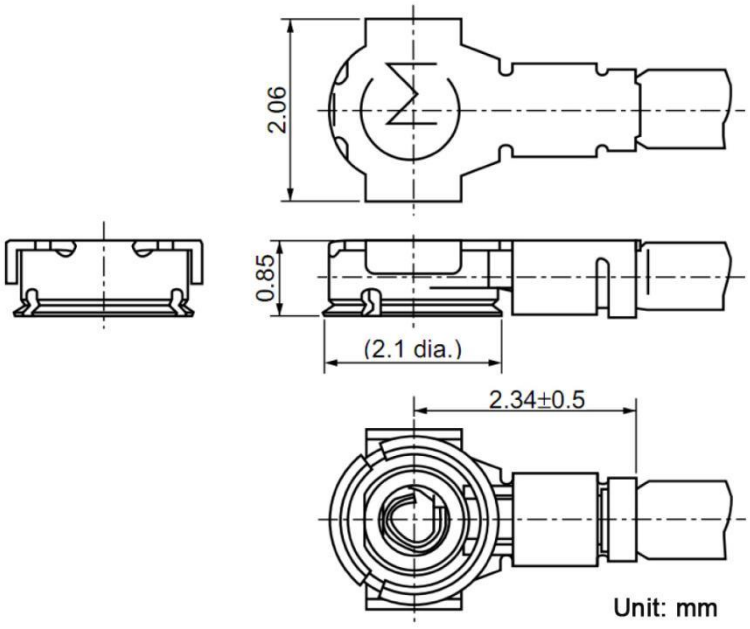

Figure 4-3 0.81mm coaxial antenna dimensions

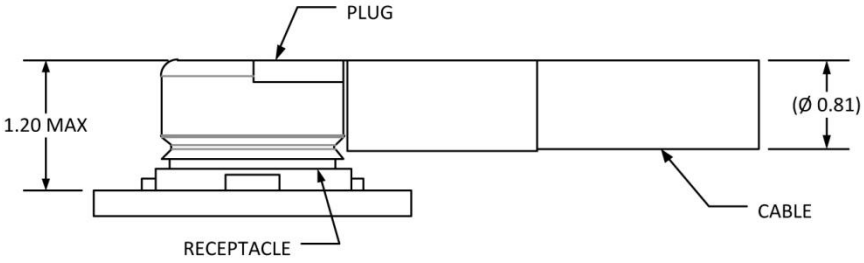

Figure 4-4 Schematic diagram of 0.81mm coaxial antenna connected to the RF connector

4.1.4 RF Connector Assembly

Mate RF connector parallel refer Figure 4-5, do not slant mate with strong force.

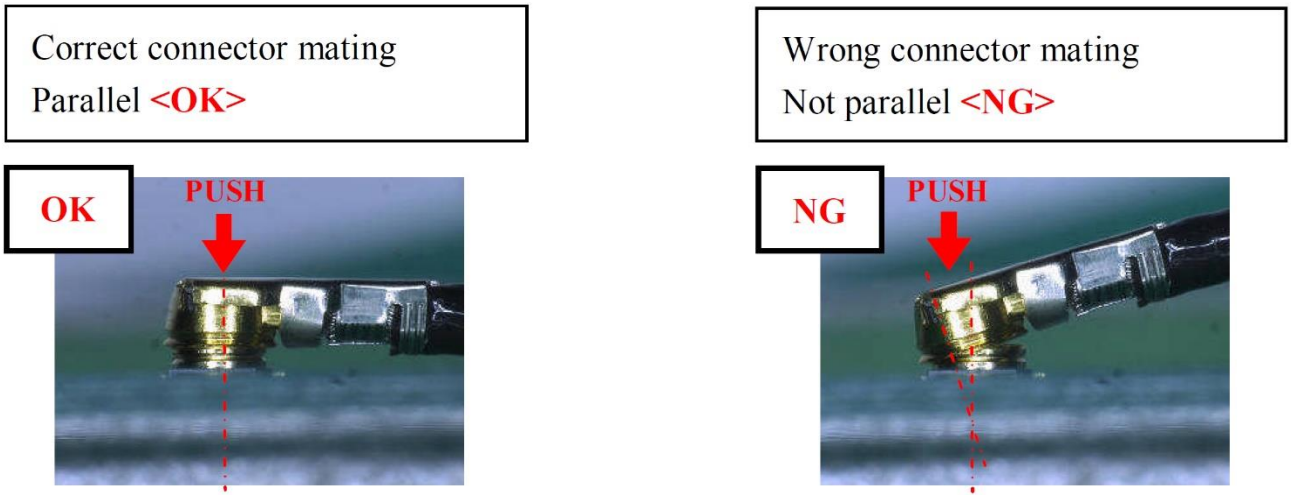

Figure 4-5 Mate RF connector

To avoid damage in RF connector unmating, it is recommended using pulling JIG as Figure 4-6, and the pulling JIG must be lifted up vertically to PCB surface (see Figure 4-7 and 4-8).

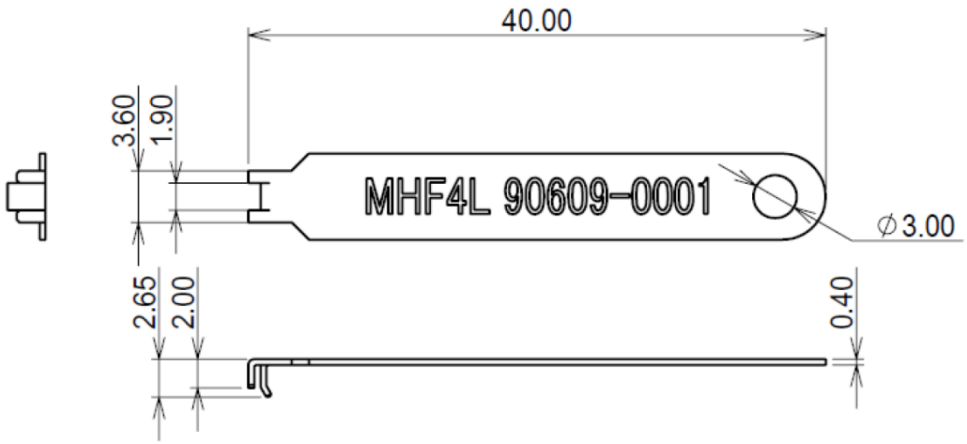

Figure 4-6 Pulling JIG

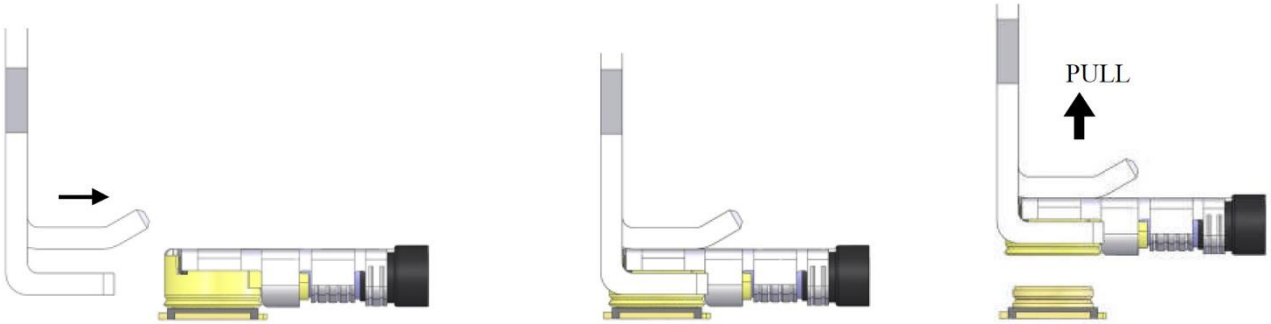

Figure 4-7 Lift up pulling JIG

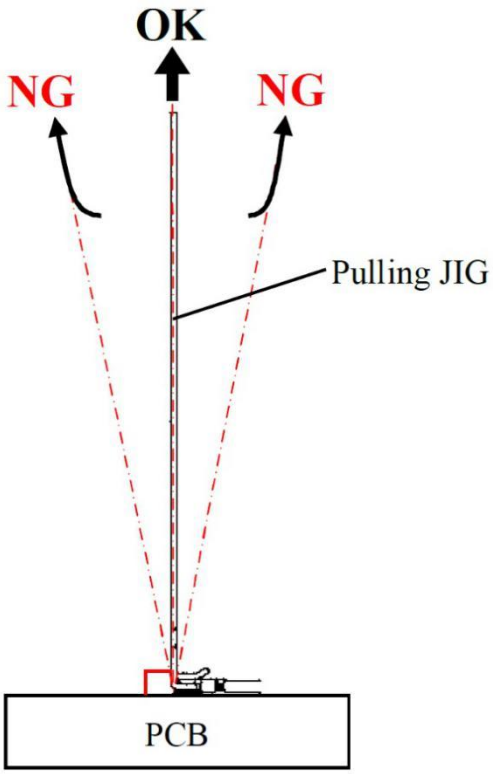

Figure 4-8 Pulling direction

4.2 Operating Band

The NL952 module operating bands of the antennas are as follows:

Operating Band	Description	Mode	Tx (MHz)	Rx (MHz)
Band 2	1900MHz	LTE FDD/WCDMA	1850 - 1910	1930 - 1990
Band 4	2100MHz	LTE FDD/WCDMA	1710 - 1755	2110 - 2155
Band 5	850MHz	LTE FDD/WCDMA	824 - 849	869 - 894
Band 7	2600Mhz	LTE FDD	2500 - 2570	2620 - 2690
Band 12	700Mhz	LTE FDD	699 - 716	729 - 746

Operating Band	Description	Mode	Tx (MHz)	Rx (MHz)
Band 13	700MHz	LTE FDD	777 - 787	746 - 756
Band 14	700MHz	LTE FDD	788 - 798	758 - 768
Band 17	700MHz	LTE FDD	704 - 716	734 - 746
Band 25	1900MHz	LTE FDD	1850 - 1915	1930 - 1995
Band 26	850MHz	LTE FDD	814 - 849	859 - 894
Band 29	700MHz	LTE FDD	N/A	717 - 728
Band 30	2300MHz	LTE FDD	2305 - 2315	2350 - 2360
Band 41	2500MHz	LTE TDD	2496 - 2690	
Band 46	5000MHz	LTE TDD	5150 - 5925	
Band 48	3600MHZ	LTE TDD	3550 – 3700	
GPS L1	-	-	/	1575.42±1.023
GLONASS G1	-	-	/	1602.5625±4
Galileo E1	-	-	/	1575.42±2.046
BDS B1	-	-	/	1561.098±2.046

4.3 Transmitting Power

The transmitting power for each band of the NL952 module as shown in the following table:

Mode	Band	3GPP Requirement(dBm)	Tx Power(dBm)	Note
WCDMA	Band 2	24+1.7/-3.7	23.5±1	-
	Band 4	24+1.7/-3.7	23.5±1	-
	Band 5	24+1.7/-3.7	23.5±1	-
LTE FDD	Band 2	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 4	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 5	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 7	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 12	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 13	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 14	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 17	23±2.7	23±1	10MHz Bandwidth, 1 RB

Mode	Band	3GPP Requirement(dBm)	Tx Power(dBm)	Note
	Band 25	23+2.7/-3.2	23±1	10MHz Bandwidth, 1 RB
	Band 26	23+2.7/-3.2	23±1	10MHz Bandwidth, 1 RB
	Band 30	23+2.7/-3.2	22±1	10MHz Bandwidth, 1 RB
	Band 66	23+2.7/-3.2	23±1	10MHz Bandwidth, 1 RB
	Band 71	23+2.7/-3.2	23±1	10MHz Bandwidth, 1 RB
LTE TDD	Band 41	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 48	23+2/-3	21.5±1	10MHz Bandwidth, 1 RB

4.4 Receiver Sensitivity

4.4.1 Dual Antenna Receiver Sensitivity

All bands support dual antenna, the receiver sensitivity for each band of NL952 module is shown in below table:

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity(dBm) Typical	Note
WCDMA	Band 2	-104.7	TBD	BER<0.1%
	Band 4	-106.7	TBD	BER<0.1%
	Band 5	-104.7	TBD	BER<0.1%
LTE FDD	Band 2	-94.3	TBD	10MHz Bandwidth
	Band 4	-96.3	TBD	10MHz Bandwidth
	Band 5	-94.3	TBD	10MHz Bandwidth
	Band 7	-94.3	TBD	10MHz Bandwidth
	Band 12	-93.3	TBD	10MHz Bandwidth
	Band 13	-93.3	TBD	10MHz Bandwidth
	Band 14	-93.3	TBD	10MHz Bandwidth
	Band 17	-93.3	TBD	10MHz Bandwidth
	Band 25	-92.8	TBD	10MHz Bandwidth
	Band 26	-93.8	TBD	10MHz Bandwidth
	Band 29*	-93.3	TBD	10MHz Bandwidth
	Band 30	-95.3	TBD	10MHz Bandwidth

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity(dBm) Typical	Note
	Band 66	-95.8	TBD	10MHz Bandwidth
	Band 71	-93.5	TBD	10MHz Bandwidth
LTE TDD	Band 41	-94.3	TBD	10MHz Bandwidth
	Band 46*	-88.5	TBD	20MHz Bandwidth
	Band 48	-95.3	TBD	10MHz Bandwidth

Note:

The above values are measured in dual antennas condition (Main+Diversity). For single main antenna (without Diversity), the sensitivity will drop about 3dBm for each band of LTE.

* B29 and B46 sensitivity test at CA-2A_29A and CA-13A_46A

4.4.2 Four Antenna Receiver Sensitivity

Some middle/high bands support four antenna, the receiver sensitivity for some middle/high bands of NL952 module is shown in below table:

Mode	Band	Middle/High Bands	3GPP Requirement (dBm)	Rx Sensitivity Typical(dBm)	Note
LTE FDD	Band 2	Middle Band	-97	TBD	10MHz Bandwidth
	Band 4	Middle Band	-99	TBD	10MHz Bandwidth
	Band 7	High Band	-97	TBD	10MHz Bandwidth
	Band 25	Middle Band	-95.5	TBD	10MHz Bandwidth
	Band 30	Middle Band	-98	TBD	10MHz Bandwidth
	Band 66	Middle Band	-98.5	TBD	10MHz Bandwidth
LTE TDD	Band 41	High Band	-97	TBD	10MHz Bandwidth
	Band 48	High Band	NA	TBD	10MHz Bandwidth

Note:

The above values are measured in four antennas condition (Main+Diversity+M1+M2). If only use dual antennas (Main+Diversity), the sensitivity will drop about 3dBm for each band of LTE.

4.5 GNSS

NL952 module supports GNSS with D/G antenna, the GNSS includes GPS/GLONASS/ Galileo/BDS. GNSS feature and performance are as below table:

Description	Condition	Test Result	
		Max	Typical
Current	Fixing	110mA@-130dBm	TBD
	Tracking	110mA@-130dBm	TBD
	Sleep	3.5mA@-130dBm	TBD
TTFF	Cold start	45s@-130dBm	TBD
	Hot Start	3s@-130dBm	TBD
Sensitivity	Tracking	-156dBm	TBD
	Acquisition	-144dBm	TBD

Note:

GNSS current is tested with RF disabled at 25℃ temperature.

4.6 Antenna Design

The NL952module provides main and diversity antenna interfaces, and the antenna design requirements as shown in the following table:

NL952 module Main antenna requirements	
Frequency range	The most proper antenna to adapt the frequencies should be used.
Bandwidth(WCDMA)	WCDMA band 2(1900) : 140 MHz WCDMA band 4(2100) : 445 MHz WCDMA band 5(850) : 70 MHz
Bandwidth(LTE)	LTE band 2(1900): 140 MHz LTE Band 4(2100): 445 MHz LTE band 5(850): 70 MHz LTE band 7(2600): 190 MHz LTE Band 12(700): 47 MHz LTE band 13(770) : 41 MHz LTE band 14(750) : 40 MHz LTE band 17(700): 42 MHz LTE band 25(1900): 145 MHz LTE band 26(850): 80 MHz LTE band 29(700): 11 MHz LTE band 30(2300): 10 MHz LTE band 41(2500): 110 MHz LTE band 46(5500): 775 MHz LTE band 48(3600): 150 MHz LTE band 66(2100): 490 MHz

NL952 module Main antenna requirements	
	LTE band 71(6500): 81 MHz
Bandwidth(GNSS)	GPS: 2 MHz GLONASS: 8 MHz Galileo: 8 MHz BDS: 4 MHz
Impedance	50 ohm
Input power	> 28 dBm average power WCDMA & LTE
Recommended standing-wave ratio (SWR)	≤ 2:1

Note:

For FCC strict EIRP requirement on B30&B48, suggest the ANT peak gain should be <1dBi@B30, <0.5dBi@B48. About the other bands, the EIRP that suggested is TBD.

5 Structure Specification

5.1 Product Appearance

The product appearance for NL952 module is shown in Figure5-1:

Figure 5-1 Module Appearance

Note: There is NL952-NA-00 module above, and the “00” will replace with “20” in NL952-NA-20 module

5.2 Dimension of Structure

The structural dimension of the NL952 module is shown in Figure 5-2:

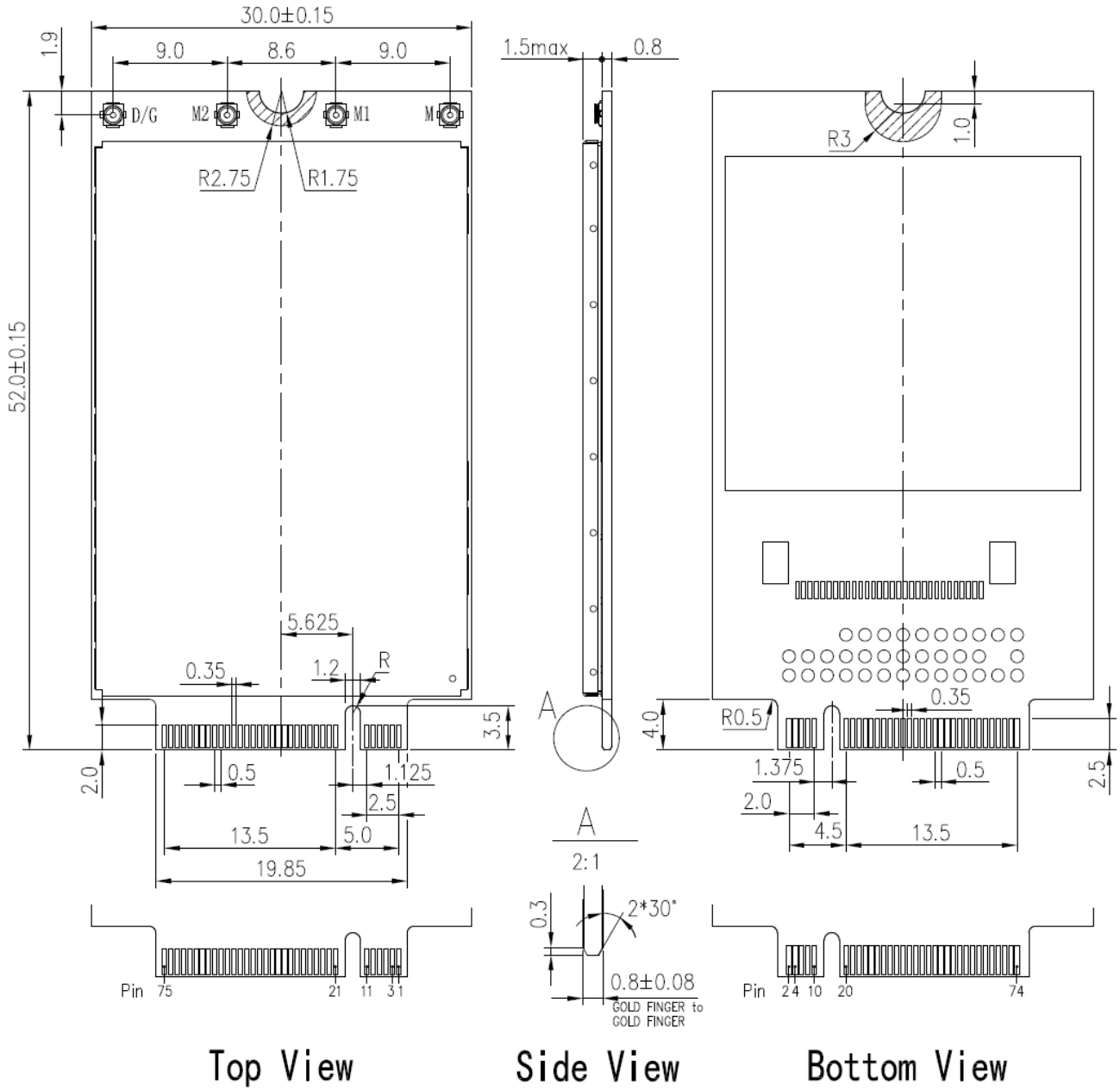

Figure 5-2 Dimension of Structure

5.3 M.2 Interface Model

The NL952 M.2 module adopts 75-pin gold finger as external interface, where 67 pins are signal pins and 8 pins are notch pins as shown in Figure 3-1. For module dimension, please refer to Figure 5-2 Dimension of Structure. Based on the M.2 interface definition, NL952 module adopts Type 3052-S3-B interface (30x52mm, the component maximum height on t top layer is 1.5mm, PCB thickness is 0.8mm, and KEY ID is B).

Module Nomenclature
Sample type 3052-S3-B

Type XX XX - XX - X - X[1]

Width (mm)
12
16
22
30

Length (mm)
16
26
30
38
42
52
60
80
110

	Component Max Ht (mm)	
	Top Max[1]	Bottom Max[1]
S1	1.2	0****
S2	1.35	0****
S3	1.5	0****
D1	1.2	1.35
D2	1.35	1.35
D3	1.5	1.35
D4	1.5	0.7
D5	1.5	1.5

Key ID	Pin	Interface
A	8-15	2x PCIe x1 / USB 2.0 / I2C / DP x4
B	12-19	PCIe x2/SATA/USB 2.0/USB 3.0/HSIC/SSIC/Audio/UIM/I2C
C	16-23	Reserved for Future Use
D	20-27	Reserved for Future Use
E	24-31	2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM
F	28-35	Future Memory Interface (FMI)
G	39-46	Generic (Not used for M.2)***
H	43-50	Reserved for Future Use
J	47-54	Reserved for Future Use
K	51-58	Reserved for Future Use
L	55-62	Reserved for Future Use
M	59-66	PCIe x4 / SATA

☒ Use ONLY when a double slot is being specified
☒☒ Label included in height dimension
☒☒☒ Key G is intended for custom use. Devices with this key will not be M.2-compliant. Use at your own risk!
☒☒☒☒ Insulating label allowed on connector-based designs

5.4 M.2 Connector

The NL952 module connects to AP via M.2 connector, it is recommended to use M.2 connector from LOTES Corporation with the model APCI0026-P001A as shown in Figure 5-3. The package of connector, please refer to the specification.

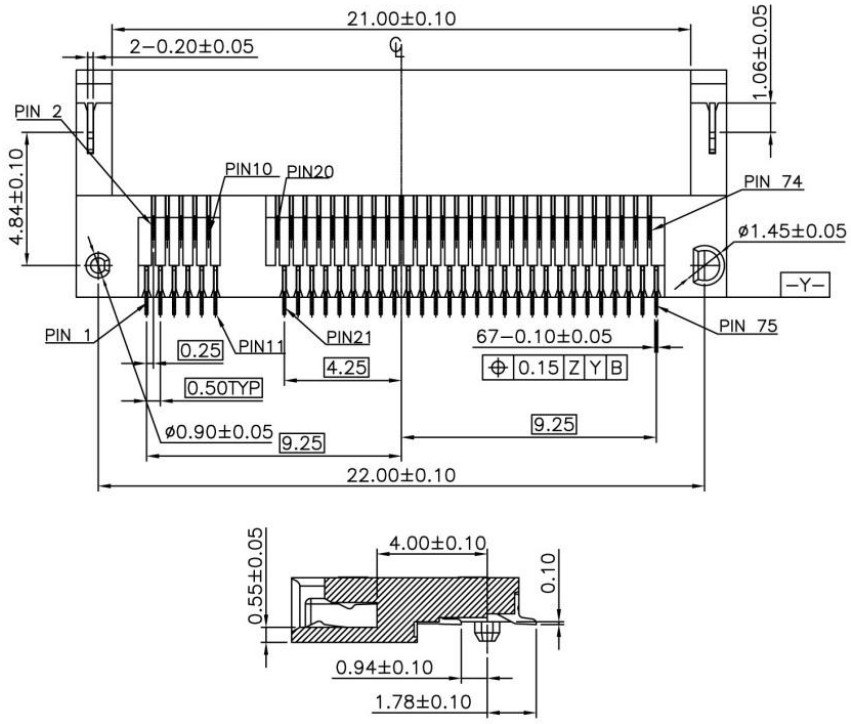

Figure 5-3 M.2 Dimension of Structure

5.5 Storage

5.5.1 Storage Life

Storage Conditions (recommended): Temperature is 23 ± 5℃, relative humidity is less than RH 60%.

Storage period: Under the recommended storage conditions, the storage life is 12 months.

5.6 Packing

The NL952 module uses the tray sealed packing, combined with the outer packing method using the hard cartoon box, so that the storage, transportation and the usage of modules can be protected to the greatest extent.

Note：

The module is a precision electronic product, and may suffer permanent damage if no correct electrostatic protection measures are taken.

5.6.1 Tray Package

The NL952 module uses tray package, 20 pcs are packed in each tray, with 5 trays including one empty tray on top in each box and 5 boxes in each case. Tray packaging process is shown in Figure 5-4:

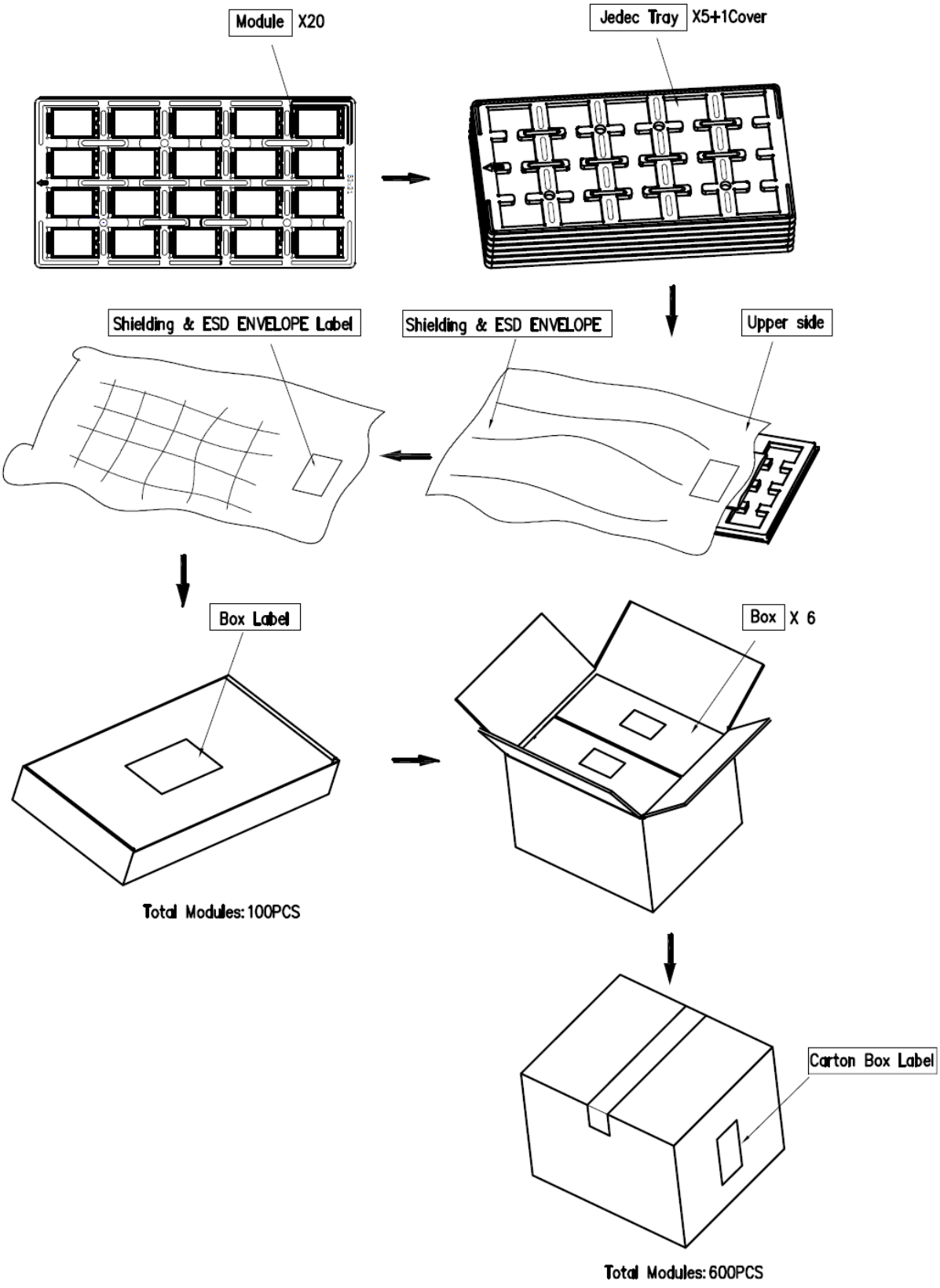

Figure 5-4 Tray Packaging Process

5.6.2 Tray size

The pallet size is 330*170*6.5mm, and is shown in Figure 5-5:

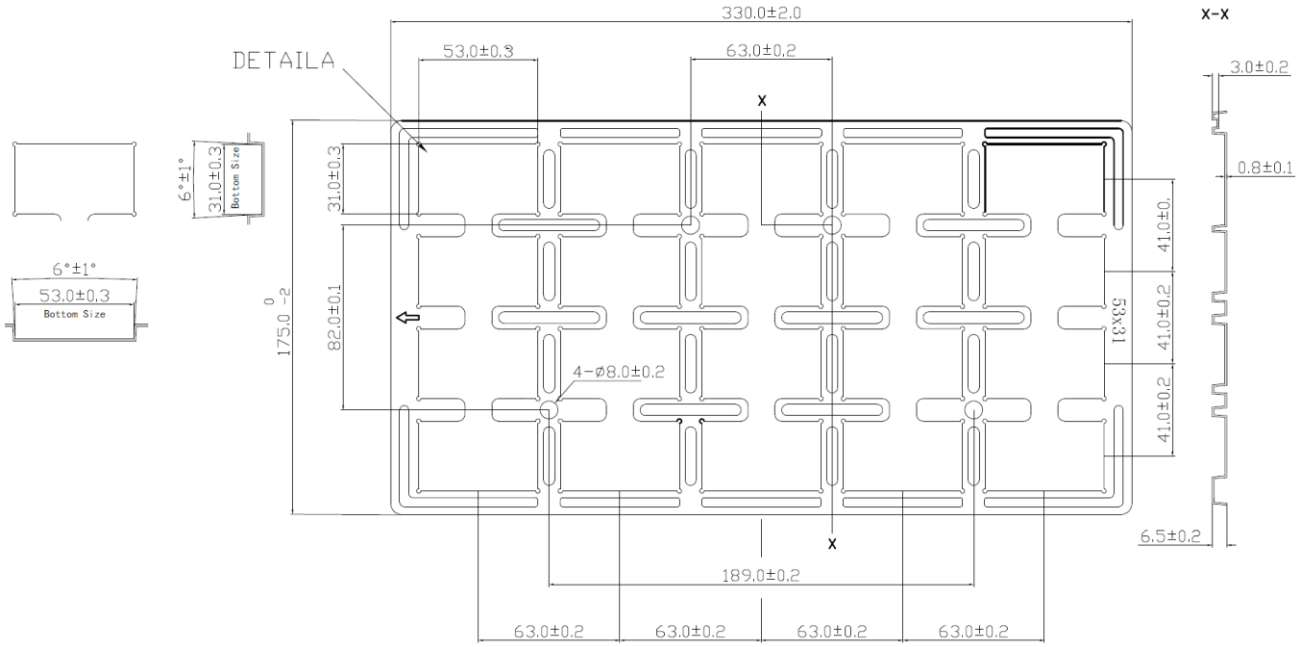

Figure 5-5 Tray Size (Unit: mm)

FCC Caution:

1 Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

2 This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the maximum antenna gain allowed as below table.

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID: ZMONL952NA”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

This device is intended only for OEM integrators under the following conditions:

The antenna must be installed such that 20 cm is maintained between the antenna and users, and the Max allowed antenna gain as following table showed:

Operating Band	Antenna Gain （dBi）
WCDMA B2	8.50
WCDMA B4	5.50
WCDMA B5	9.92
LTE B2	9.00
LTE B4	6.00
LTE B5	10.41
LTE B7	9.00
LTE B12	9.70
LTE B13	10.16
LTE B14	10.23
LTE B17	9.74
LTE B25	9.00
LTE B26	10.41
LTE B30	1.00
LTE B41	9.00
LTE B48	1.00
LTE B66	6.00
LTE B71	9.48

If the host device need fully leverage this Module’s FCC ID, the host device MUST within below ANT Gain.

Operating Band	Test Antenna Gain (dBi)
WCDMA B2	4.00
WCDMA B4	4.00
WCDMA B5	3.00

LTE B2	4.00
LTE B4	4.00
LTE B5	3.00
LTE B7	4.00
LTE B12	3.00
LTE B13	2.00
LTE B14	2.00
LTE B17	3.00
LTE B25	4.00
LTE B26	3.00
LTE B30	1.00
LTE B41	3.00
LTE B48	1.00
LTE B66	4.00
LTE B71	4.00