TM18NA Hardware Guide

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1 Preface

This document describes the TM18NA module and it's hardware and air interfaces to customer applications, and provides a quick overview of the module's hardware interface characteristics, RF characteristics, electrical characteristics, mechanical specifications, and other related information.

1.1 Safety instructions

By following the safety principles below, you can ensure personal safety and help protect the product and work environment from potential damage. Product manufacturers are required to communicate the following safety instructions to end users.

Safety on the road comes first! When you are driving, do not use handheld mobile devices, even if they have a hands-free function, and stop before making a phone call!

Please turn off your mobile devices before boarding the airplane. The wireless function of mobile devices is prohibited on board to prevent interference with the aircraft's communication system. Ignoring this reminder may lead to flight safety or even violate the law.

When in a hospital or healthcare facility, note if there are restrictions on the use of mobile devices. Radio frequency interference may cause malfunctioning of medical equipment, so it may be necessary to turn off the mobile terminal equipment.

The mobile device does not guarantee a valid connection in all circumstances, for example when the mobile device is out of credit or the (U)SIM is invalid. When you encounter these situations in an emergency, please remember to use the emergency call and ensure that your device is switched on and in an area with sufficient signal strength.

Your mobile device receives and transmits RF signals when it is turned on. RF interference occurs when in close proximity to TVs, radios, computers, or other electronic devices.

Keep the mobile terminal equipment away from flammable gases. Turn off the mobile terminal equipment when near gas stations, oil depots, chemical plants, or explosive workplaces. It is a safety hazard to operate electronic equipment in any place where there is a potential explosion hazard.

2 Product Overview

TM18NA is a LTE wireless communication module, which supports data connectivity such as LTE-FDD and LTE-TDD, WIFI SCAN and GNSS (optional) functions. The module is a SMD module in a compact package that can meet the needs of most M2M applications, such as routers, home gateways, STBs, industrial laptops, industrial PDAs, tablets, and video surveillance.

Table 1: Module Basic Information

TM18NA	
seal inside	LGA
pinout	109
sizes	17.7 mm × 15.8 mm × 2.4 mm
weights	1.2±0.1g
Wi-Fi functionality	LTE/GNSS (optional)/WIFI SCAN

2.1 Frequency bands and functions

Table 2: Wireless Network Formats

WLAN standard	TM18NA
LTE-FDD	b2/4/5/7/12/13/17/26/66
LTE-TDD	B40/B41
GNSS (optional)	GPS, GLONASS, BDS, Galileo
Wi-Fi Scan	2.4 GHz 11b (Rx)

2.2 Key features

Table 3: Key Module Characteristics

parameters	
Supply Voltage	● 3.3 to 4.3 V ● Typical: 3.8 V
Short Message Service (SMS)	● Text and PDU modes ● Send and receive peer-to-peer SMS messages ● SMS Cell Broadcast ● SMS storage: default storage to module
(U) SIM Card Interface	1.8V and 3.0V
Audio Characteristics	Supports 1 digital audio interface: PCM interface supports echo cancellation and noise suppression
Digital Audio Interface	PCM: ● 1 digital audio interface: PCM ● For audio, requires external Codec chip ● Supports master and slave modes
SPI	● Dedicated SPI all the way, only master mode supported ● 1.8V voltage domain with a maximum clock frequency of 83 MHz
I2C interface	● Triple I2C interface ● Conforms to the I2C bus protocol specification
USB interface	● USB 2.0 (Slave mode only), data transfer rate up to 480 Mbps ● For AT command sending, data transfer, software debugging, firmware upgrade ● USB Virtual Serial Port Driver: Support USB driver under Windows 7/8/8.1/10, Linux 2.6~5.14, Android 4.x~11.x and other operating systems
UART	**Main UART.** ● AT command sending and data transfer ● Baud rate defaults to 115200 bps ● Hardware flow control **Debugging the UART** ● Log output ● Baud rate of 2 Mbps **Auxiliary UART**
Matrix Keyboard	to be developed
network instruction	● NET_STATUS Indicates network operational status
AT command	● Support for commands defined in 3GPP TS 27.007 and 3GPP TS 27.005

	● Support for Toucan Enhanced AT commands
Antenna Interface	● Main Antenna Interface (ANT_MAIN) ● WIFI_SCAN Receiver Antenna Interface (ANT_WIFI_SCAN) ● GNSS (optional) Antenna interface (ANT_GNSS) ● 50 Ω characteristic impedance
firing power	● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Maximum support for Cat 1 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● LTE-FDD: Maximum downlink rate 10 Mbps, maximum uplink rate 5 Mbps ● LTE-TDD: maximum downlink rate 8.96 Mbps, maximum uplink rate 3.1 Mbps
Network Protocol Characterization	● Conforms to TCP / UDP / PPP / NTP / NITZ / FTP / HTTP / PING / CMUX / HTTPS / FTPS / SSL / FILE / MQTT / MMS / SMTP / SMTPS protocols*. ● PPP protocol-compliant PAP and CHAP authentication
temperature range	● Normal operating temperature : -35 to +75 ° C ● Extended operating temperature : -40 to +85 ° C ● Storage temperature: -40 to +90 ° C
Firmware Upgrade	Upgradeable via USB interface or DFOTA
RoHS	All devices are fully EU RoHS compliant

[1] When the module operates in this temperature range, the relevant performance of the module meets the requirements of the 3GPP standard.

[2] When the module operates within this temperature range, the module can still maintain normal working status, with voice, short message, data transmission, emergency call and other functions; there will be no recovery failure; the RF spectrum and network are basically unaffected. Only individual parameters such as output power may exceed the range of 3GPP standard. When the temperature returns to the normal working temperature range, the module's indicators still comply with the 3GPP standard.

2.3 Functional block diagrams

The following diagram shows the functional block diagram of the module and describes its main functional components:

- Power Management
- Baseband
- Memory
- RF section
- Peripheral Interface

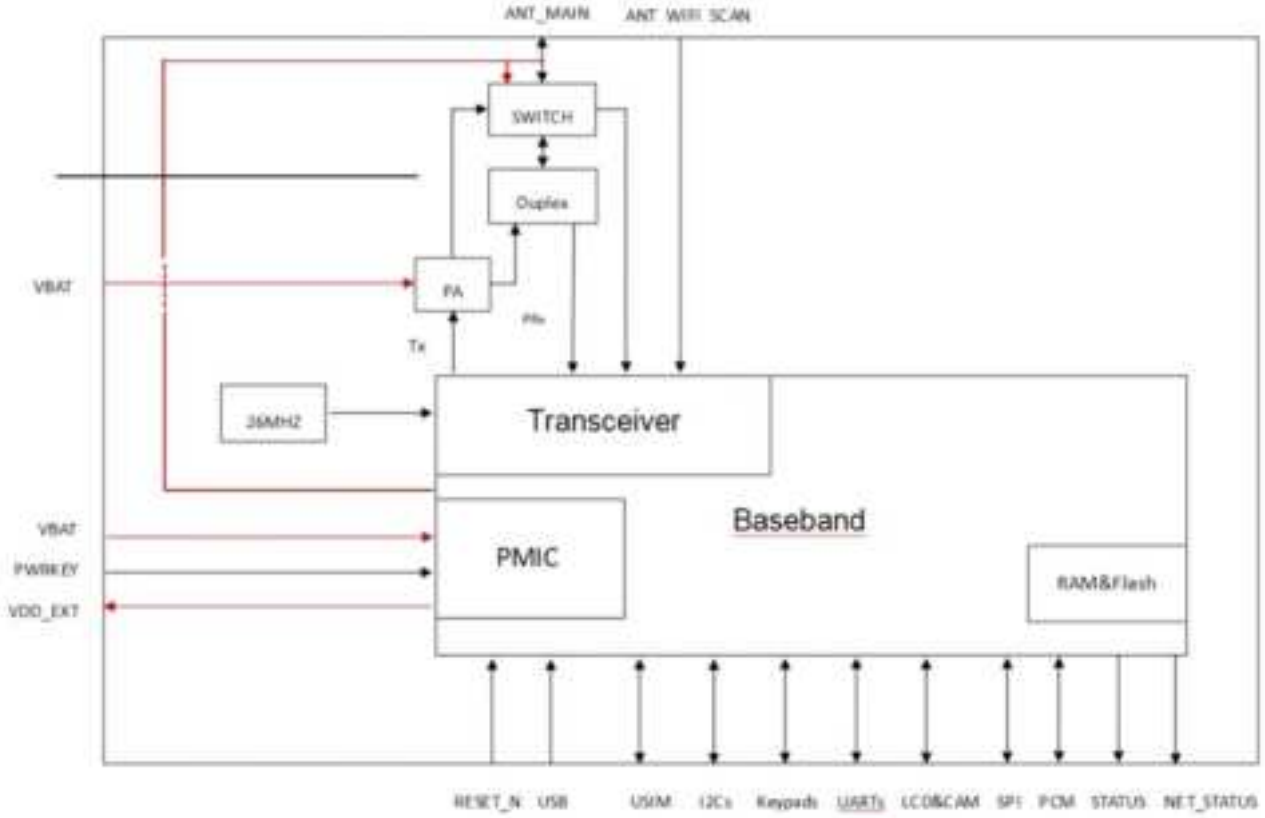

Figure 1: Functional Block Diagram

2.4. Pin Assignment Diagram

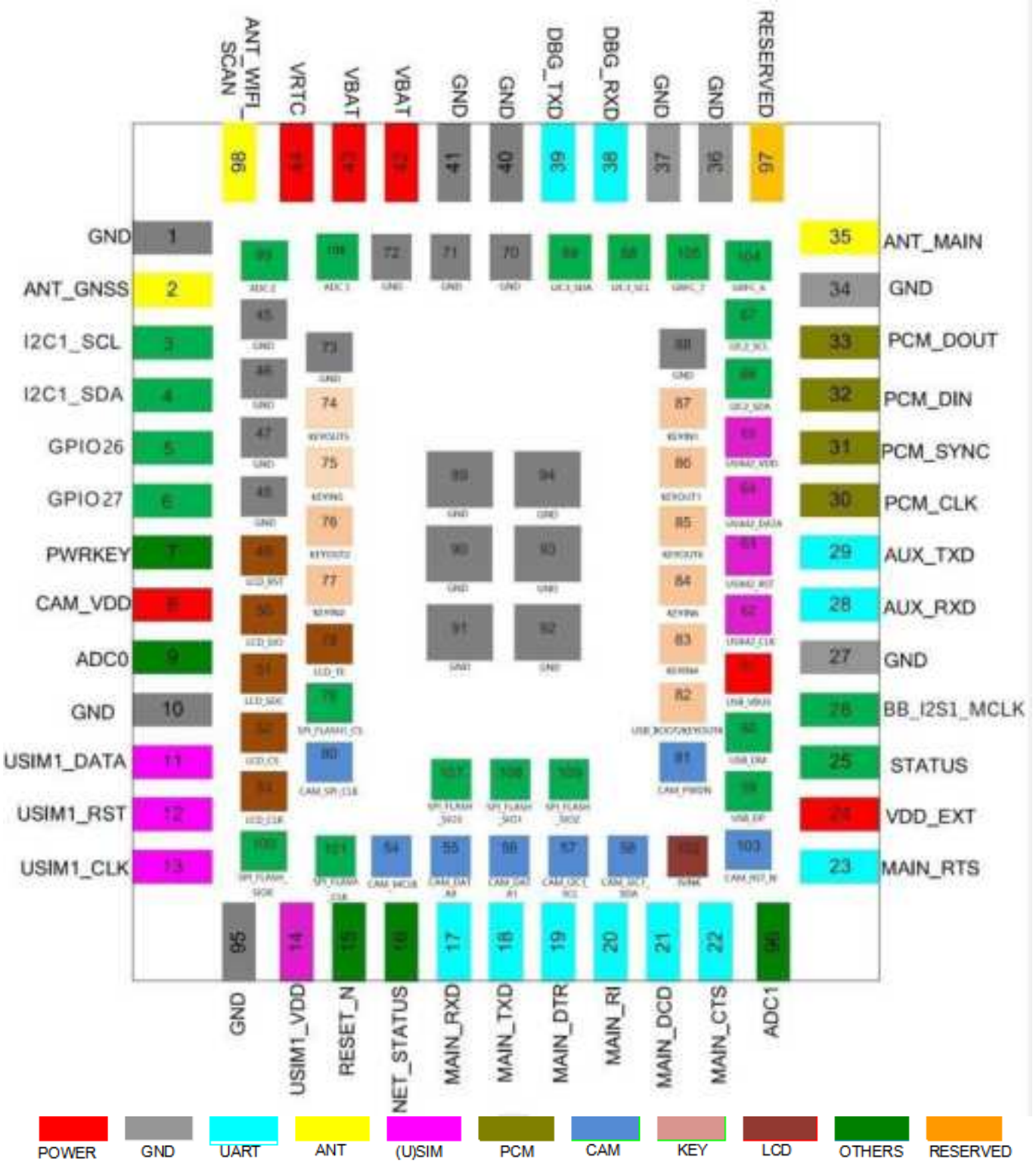

Figure 2: Pin Assignment Top View

2.5. Pin Description Table

Table 4: Parameter definitions

parameters	descriptive
AI	analog input
AIO	Analog Input/Output
AO	analog output
DI	digital input
DIO	Digital inputs/outputs
DO	digital output
OD	open drain
PD	pull down
PI	Power Input
PIO	Power input/output
PO	power output (of an electrical device etc)
PU	pull up

Table 5: Module Pin Descriptions

power supply					
pinout	pin number	I/O	descriptive	DC Characteristics	note
VBAT	42, 43	PI	Module mains power supply	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	External power supply is required to provide 2 A current-carrying capability. Additional external surge tubes are recommended.
VRTC	44		Real Time Clock Power Supply		
VDD_EXT	24	PO	1.8V supply for external circuits	Vnom = 1.8V IOmax = 50mA	Pull-ups can be provided for external GPIOs.
On/Off/Reset					

pinout	pin number	I/O	descriptive	DC Characteristics	note
PWRKEY	7	DI	Module On/Off	VILmax = 0.5 V	VBAT Voltage Domain
RESET_N	15	DI	Module reset	VILmax = 0.5 V	VBAT voltage domain, active low after power on.
Indicator Status Interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
STATUS	25	DO	Operational status indication	VOHmin = 1.35V / 2.97V VOLmax = 0.45V / 0.33V	1.8V/3.3V voltage domain. When not in use, it is suspended.
NET_STATUS	16	DO	Network Status Indication	VOHmin = 1.35V / 2.97V VOLmax = 0.45V / 0.33V	
USB interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
USB_VBUS	61	AI	USB Detection	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	Typical 5.0 V. Suspended if not in use.
USB_DP	59	AIO	USB differential data (+)		Requires 90Ω differential impedance. Compliant with USB 2.0 specification. Dangles if not used.
USB_DM	60	AIO	USB differential data (-)		
(U)SIM interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
USIM_DET	79	DI	USIM card insertion and removal detection	1.8V	If you don't use it, it hangs in the air.
USIM_VDD	14	PO	(U) Power supply for SIM card 1		
USIM_DATA	11	DIO	(U) SIM card 1 data		
USIM_CLK	13	DO	(U) SIM card 1 clock		

USIM_RST	12	DO	(U) SIM card 1 reset		
USIM2_VDD	65	PO	(U) Power supply for SIM card 2		Function development, can be used as a GPIO port
USIM2_DATA	64	DIO	U) SIM card 2 data		Function development, can be used as a GPIO port
USIM2_CLK	62	DO	(U) SIM 2 Clock		Function development, can be used as a GPIO port
USIM2_RST	63	DO	(U) SIM card 2 reset		Function development, can be used as a GPIO port

main serial port

pinout	pin number	I/O	descriptive	DC Characteristics	note
MAIN_CTS	22	DO	DTE Clear Transmit		CTS connected to DTE
MAIN_RTS	23	DI	DTE request to send	ink	RTS to DTE
MAIN_RXD	17	DO	Main serial port receive		
MAIN_DCD	21	DI	Main serial port output carrier detection		
MAIN_TXD	18	DO	Main Serial Port Transmit		
MAIN_RI	20	DO	Main serial port output ringing alert		Function development, can be used as a GPIO port
MAIN_DTR	19	DI	Main serial data terminal ready		Function development, can be used as a GPIO port

Auxiliary Serial Port

pinout	pin number	I/O	descriptive	DC Characteristics	note
AUX_RXD	28	DI	Debugging serial port reception		
AUX_TXD	29	DO	Debugging Serial Sends		

Debugging Serial Ports

pinout	pin number	I/O	descriptive	DC Characteristics	note
DBG_RXD	38	DI	Debugging serial port reception		

DBG_TXD	39	DO	Debugging Serial Sends		

I2C Interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
CAM_I2C1_SCL	57	OD	I2C Serial Clock		
CAM_I2C1_SDA	58	OD	I2C Serial Data		
I2C1_SCL	3	OD	I2C Serial Clock		
I2C1_SDA	4	OD	I2C Serial Data		Requires an external 1.8V pull-up.
I2C2_SCL	67	OD	I2C Serial Clock		If you don't use it, it hangs in the air.
I2C2_SDA	66	OD	I2C Serial Data		
I2C3_SCL	68	OD	I2C Serial Clock		
I2C3_SDA	69	OD	I2C Serial Data		

PCM					
pinout	pin number	I/O	descriptive	DC Characteristics	note
PCM_SYNC	31	DO	PCM Frame Synchronization		This pin is an output signal when the module is used as a master device.
PCM_CLK	30	DO	PCM Clock		This pin is an output signal when the module is used as a master device.
PCM_DIN	32	DI	PCM Data Input		
PCM_DOUT	33	DO	PCM Data Output		If you don't use it, it hangs in the air.
BB_I2S1_MCLK	26	DO	I2S Clock Output		

RF Antenna Interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
ANT_GNSS (optional)	2	AI	GNSS (optional) antenna interface		
ANT_MAIN	35	AIO	Primary Antenna Interface		
ANT_WIFI_SCAN	98	AI	Wi-Fi Scan Antenna connector		

GRFC Antenna Control Interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
GRFC_6	104	DO	Universal RF Control		
GRFC_7	105	DO			
LCM Interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
LCD_RST	49	DO	LCD reset		
LCD_SIO	50	DIO	LCD Data		
LCD_SDC	51	DIO	LCD register selection		
LCD_CS	52	DO	LCD Chip Selection		
LCD_CLK	53	DO	LCD Clock		
LCD_TE	78	DIO	LCD Frame Synchronization		
ISINK	102	PI	Current Sink Input Pin, Backlight Adjustment		Driven by current-flooding method, connected to the cathode of the backlight, the backlight brightness is controlled by adjusting the current level Imax=91 mA.
CAMERA Interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
CAM_MCLK	54	DO	Camera Master Clock		
CAM_DATA0	55	DIO	Camera SPI Data Bit 0		
CAM_DATA1	56	DIO	Camera SPI Data Bit 1		
CAM_SPI_CLK	80	DI	Camera SPI Clock		
CAM_PWDN	81	DO	Camera shutdown		

CAM_RST_N	103	DO	Camera reset		
CAM_VDD	8	PO	Camera Analog Power Supply		
Matrix Keyboard Interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
KEYOUT5	74	DO	Matrix key output 5		
KEYIN5	75	DI	Matrix key input 5		
KEYOUT2	76	DO	Matrix key output 2		
KEYIN2	77	DI	Matrix key input 2		
KEYIN4	83	DI	Matrix key input 4		1.8V/3.3V Voltage field, left blank if not in use.
KEYIN6	84	DI	Matrix key input 6		
KEYOUT6	85	DO	Matrix key output 6		
KEYOUT1	86	DO	Matrix key output 1		
KEYIN1	87	DI	Matrix key input 1		
SPI interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
SPI_FLASH1_CLK	101	DO	SPI Clock		Function development, can be used as a GPIO port
SPI_FLASH1_SIO0	100	DIO	SPI Data 0		Function development, can be used as a GPIO port
SPI_FLASH1_SIO1	108	DIO	SPI Data 1		Function development, can be used as a GPIO port
SPI_FLASH1_SIO2	109	DIO	SPI Data 2		Function development, can be used as a GPIO port
SPI_FLASH1_SIO3	107	DIO	SPI Data 3		Function development, can be used as a GPIO port
ADC Interface					
pinout	pin number	I/O	descriptive	DC Characteristics	note
ADC0	9	AI	General Purpose ADC Interface		
ADC1	96	AI			
ADC2	99	AI			

ADC3	106	AI			
Other interfaces					
pinout	pin number	I/O	descriptive	DC Characteristics	note
USB_BOOT / KEYOUY4	82	DI	Force the module into emergency download mode		
GPIO26	5	DIO			
GPIO27	6	DIO			
RESERVED					
97					
GND					
1, 10, 27, 34, 36, 37, 40, 41, 45~48, 70~73, 88~95					

3 Operating characteristics

3.1 Working modalities

Table 6: Operating modes

paradigm	functionality
Normal Operating Mode	The Idle software is working fine. The module is registered to the network, but there is no data interaction with the network. The Talk/Data network is connected normally. Module power consumption depends on network settings and data transfer rate.
flight mode	■ AT+CFUN=0 allows you to set the module to flight mode. ■ The RF does not work.
sleep mode	The power consumption of the module is reduced, but the module can still receive paging, SMS, phone and TCP/UDP data. Divided into PM0, PM1, and PM2 modes: ◆ AT+CSCLK=0 You can set the module to PM0 light sleep mode. ◆ AT+CSCLK=2 allows you to set the module to PM1 medium sleep mode. ◆ AT+CSCLK=5 allows you to set the module to PM2 deep sleep mode.
shutdown mode	The VBAT power supply is not disconnected and the software stops working.

3.2 Dormant mode

In sleep mode, the module minimizes power consumption.

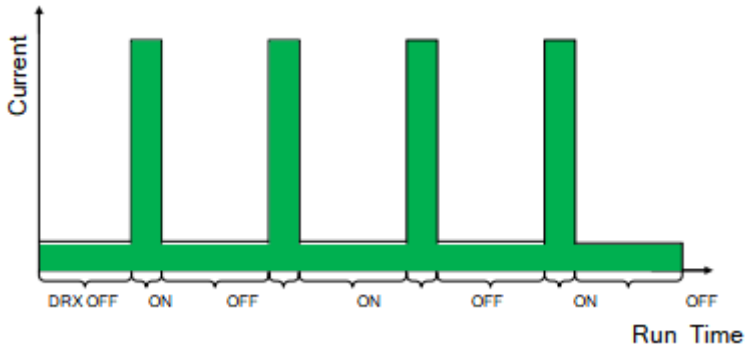

Fig 3: Schematic of module current consumption in hibernation mode

3.2.1 UART application scenarios

If the module communicates with the host computer via UART, the following two conditions must be met for the module to enter sleep mode:

- Execute AT+CSCLK=2

- Ensure that MAIN_DTR is held high or suspended

Refer to the following diagram for the connection between the module and the host computer:

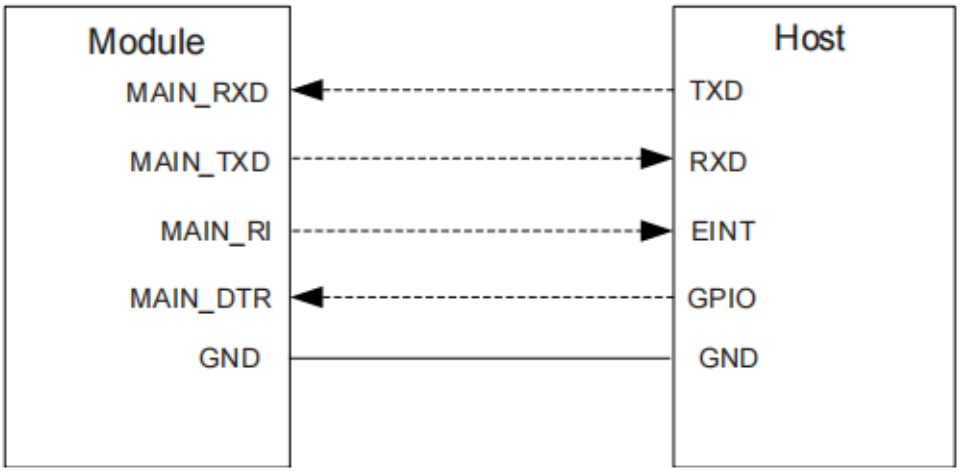

Figure 4:UART Application Connection Block Diagram in Sleep Mode

- The host pulls down the module's MAIN_DTR to wake up the module.
- The MAIN_RI pin will be actuated when the module has a URC to report.

3.3. power supply design

3.3.1. power interface

The module has a total of 2 VBAT power pins for connecting to an external power supply, where:

Table 7: Power Interface Pin Definitions

pinout	pin number	I/O	descriptive	
VBAT	42, 43	PI	Module mains power supply	External power supply is required to provide 2 A current-carrying capability. Additional external surge tubes are recommended.
VRTC	44		Real Time Clock Power Supply	
VDD_EXT	24	PO	1.8V supply for external circuits	Pull-ups can be provided for external GPIOs.

3.3.2 Power supply reference

The power supply design is critical to module performance. The current supplied to the module needs to be at least 2 A. If the voltage difference between the input voltage and the module supply voltage is small, an LDO is recommended as the power supply. If the voltage difference between the input and supply voltage is large, a switching power converter is recommended. The following figure shows the reference design of the power supply circuit.

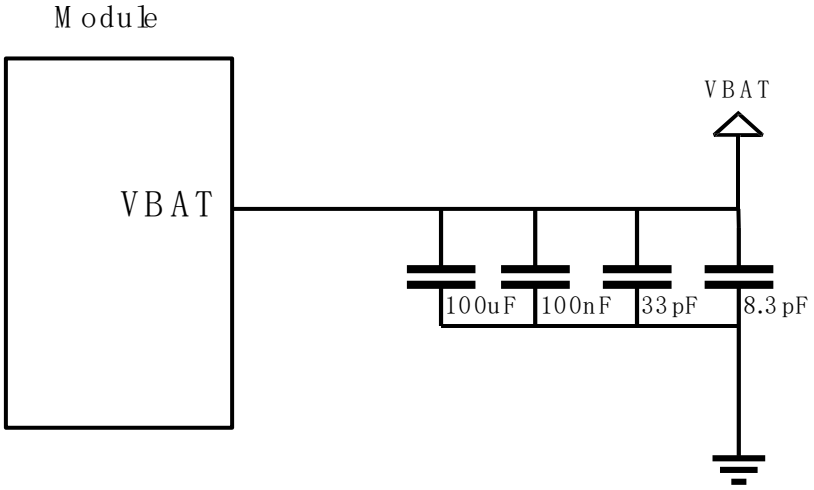

Figure 5: Power Supply Input Reference Circuit Diagram

3.3.3 Voltage stability requirements

The power supply range of the module is 3.3~4.3V and you need to make sure that the input voltage is not lower than 3.3V.

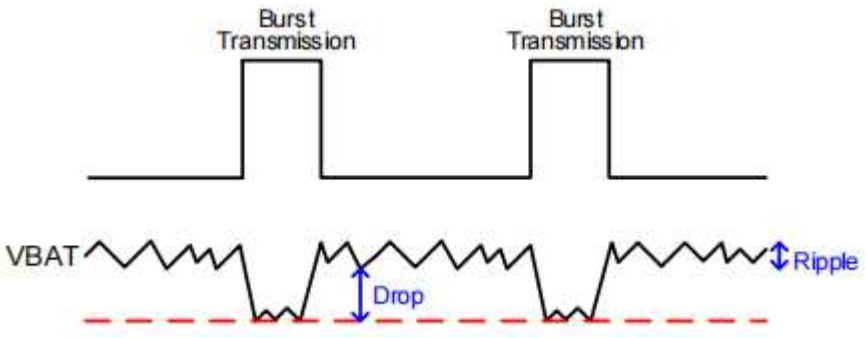

Figure 6: Burst Transfer Power Requirements

To minimize voltage dips, a 100 uF filter capacitor with low ESR (ESR = 0.7Ω) is required. It is also recommended that three chip multilayer ceramic capacitors (MLCC) with good ESR performance be reserved for VBAT_BB, and the capacitors should be placed close to the VBAT pins. The width of the VBAT_BB alignment should be no less than 1.5 mm in principle, and the longer the VBAT alignment, the wider the

line width. In order to suppress power fluctuations and shocks, to ensure the stability of the output power supply, it is necessary to add high-power TVS in the front of the power supply.

3.4.

3.4.1. PWRKEY boot up

Table 8:PWRKEY Interface Pin Definitions

pinout	pin number	I/O	descriptive	note
PWRKEY	7	DI	Module On/Off	VBAT Voltage Domain

The module can be turned on by pulling down PWRKEY for at least 2s when the module is off. It is recommended to use open-collector or open-drain driver circuit to control PWRKEY.

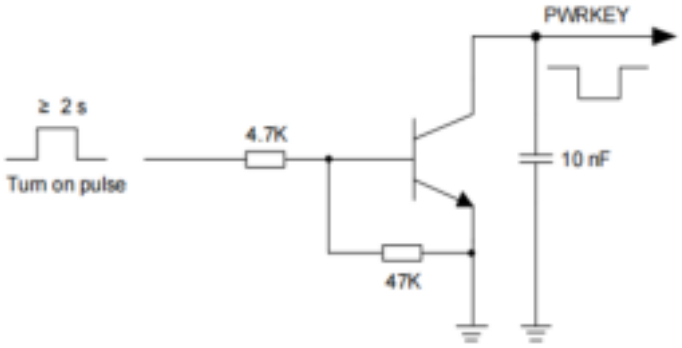

Figure7: Block diagram of open-set driver power-on reference design

The PWRKEY can also be controlled directly by a pushbutton switch. In order to prevent electrostatic shocks caused by contact, a TVS should be placed near the pushbutton for ESD protection.

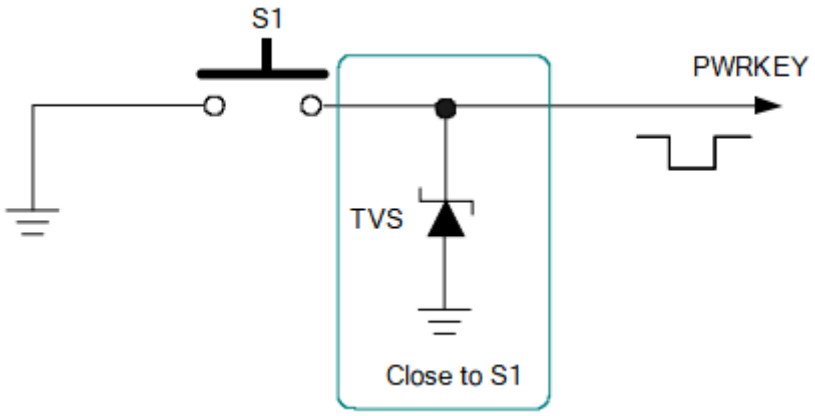

Figure8: Block Diagram of Pushbutton Power On Reference Design

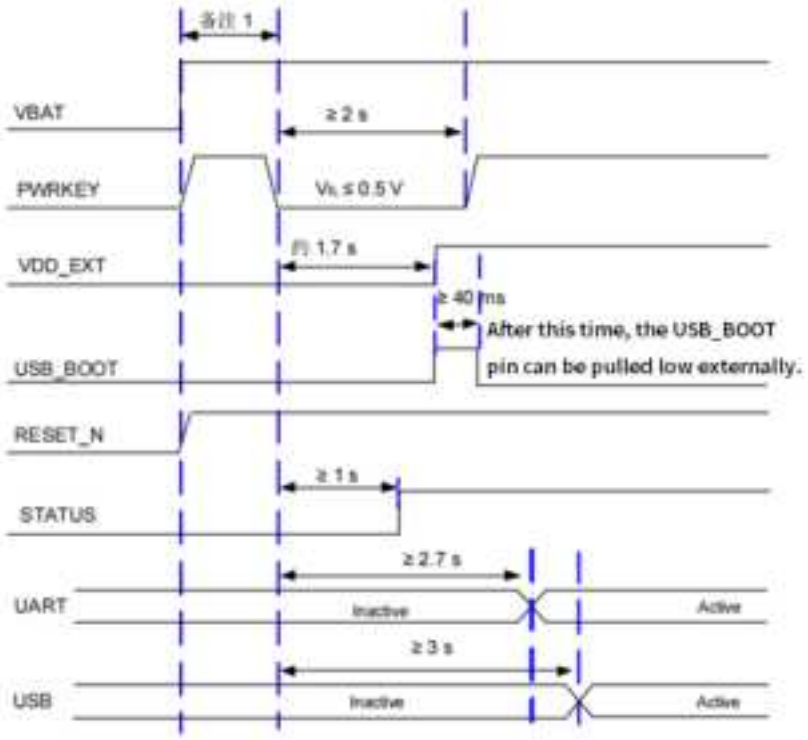

Figure 9: Power-up Timing Diagram

note

1. Before pulling down PWRKEY, make sure the VBAT voltage is stable. It is recommended to stabilize VBAT for at least 30 ms before pulling down PWRKEY.
2. If you need power-on auto power-on and do not need the power-off function, you can pull down PWRKEY directly to ground, the pull-down resistor is recommended to be 1 kΩ.

3.5 Shutdown

The module can be shut down in the following ways:

3.5.1. PWRKEY Shutdown

After pulling down PWRKEY for at least 3000 ms in the power-on state and releasing it, the module will perform the shutdown process.

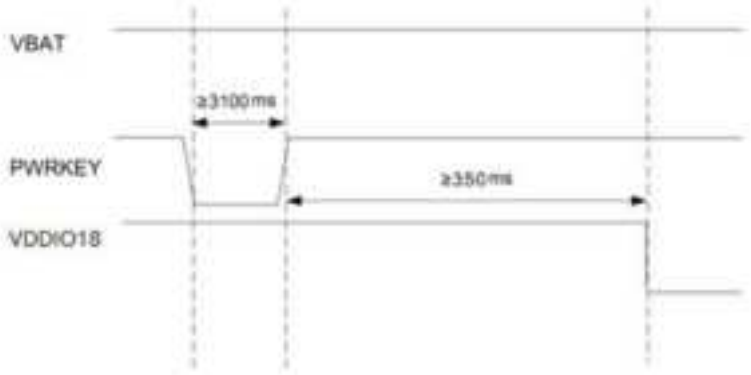

Figure 10: Shutdown Timing Diagram

3.5.2. AT Command Shutdown

Executing **AT+CPOF** shuts down the module. This operation has the same timing and

effect as pulling down PWRKEY to shut down the module.

note

1. When the module is working normally, do not disconnect the module power immediately to avoid damaging the Flash data inside the module. It is recommended to turn off the module through PWRKEY or AT command before disconnecting the power.
2. When using the AT command to turn off the power, make sure that PWRKEY remains high after the power off command is executed.

3.6 Reset

Pulling down RESET_N for 100 ms and releasing it can reset the module. the RESET_N signal is sensitive to interference, so it is recommended that the module interface alignment should be as short as possible and be ground-packed.

Table 9: Reset Pin Definitions

pinout	pin number	I/O	descriptive	note
RESET_N	15	DI	Module reset	VBAT voltage domain. Active low after power up.

The reset reference circuit is similar to the PWRKEY control circuit and can be used to control RESET_N using an open-collector or open-drain driver circuit or a pushbutton.

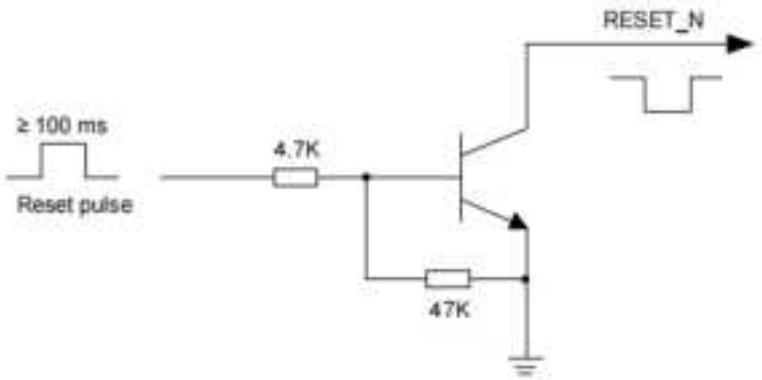

Figure 11: Open Set Driver Reset Reference Design Block Diagram

RESET_N can also be controlled using the keypad:

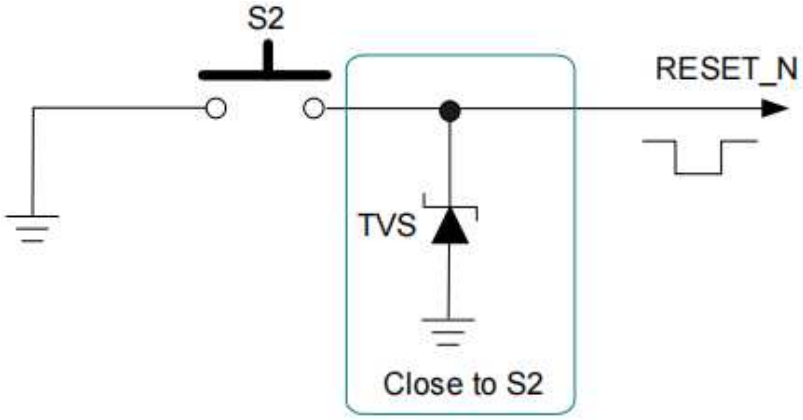

Figure 12:RESET_N Key Reset Reference Design Block Diagram

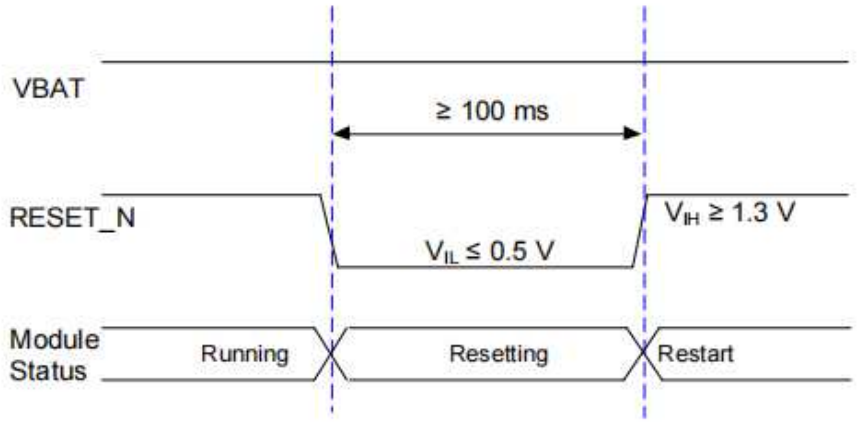

Figure 13:RESET_N Reset Timing Chart

4 Application interfaces

4.1. USB interface

The module's USB interface is compliant with the USB 2.0 specification and supports both full-speed (12 Mbps) and high-speed (480 Mbps) modes. The module only supports USB slave mode. The interface can be used for AT command transfer, data transfer, software debugging, and firmware upgrades.

Table 10: USB Interface Pin Definitions

pinout	pin number	I/O	descriptive	note
USB_VBUS	61	AI	USB Detection	Typical 5.0 V. Dormant if not in use.
USB_DP	59	AIO	USB Differential Data (+)	Requires 90Ω differential impedance. Compliant with USB 2.0 specification. Dangles if not used.
USB_DM	60	AIO	USB Differential Data (-)	

When designing, it is recommended that the USB interface be used for firmware upgrades and that a test point be reserved for debugging purposes.

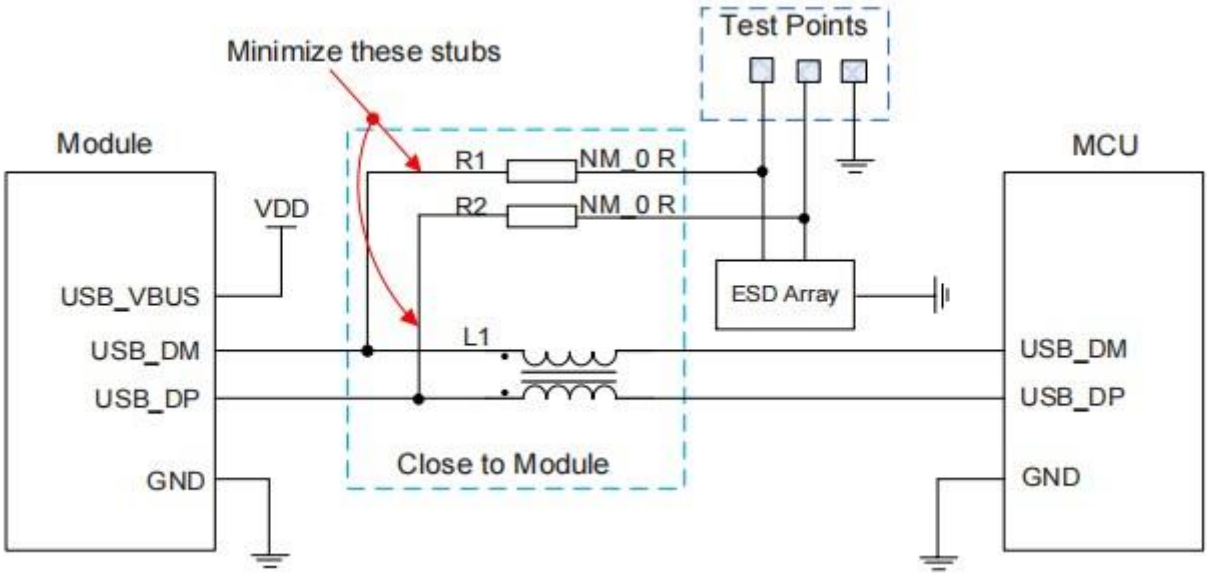

Figure 14:USB Interface Reference Circuit Diagram

It is recommended to connect a common mode inductor L1 in series between the MCU and the module to prevent the USB signal from generating EMI interference; at the same time, it is recommended to connect R1 and R2 resistors in series to the test point for debugging purposes, and the resistors will not be posted by default. In order to meet the USB data line signal integrity requirements, L1, R1 and R2 need to be placed close to the module, and R1 and R2 are placed close to each other, connecting the test point of the pile line as short as possible.

To ensure performance, the circuit design of the USB interface should follow the following principles:

- USB requirements in accordance with the 90ohm impedance differential cable design, it is recommended that the inner layer of the alignment and three-dimensional ground wrap treatment.
- USB alignment away from crystals, oscillators, magnetic devices, RF signals, etc. to avoid causing interference.
- ESD device selection on the USB data line requires special attention, its parasitic capacitance should not exceed 2pF, placed as close as possible to the USB interface.

For more information on the USB specification, visit http://www.usb.org/home.

4.2 Emergency download interface

USB_BOOT is the emergency download interface. By pulling down the USB_BOOT pin to GND before powering on the module, the module will enter the forced download mode when powering on. In this mode, the module can upgrade the firmware through the USB interface, thus saving upgrade time.

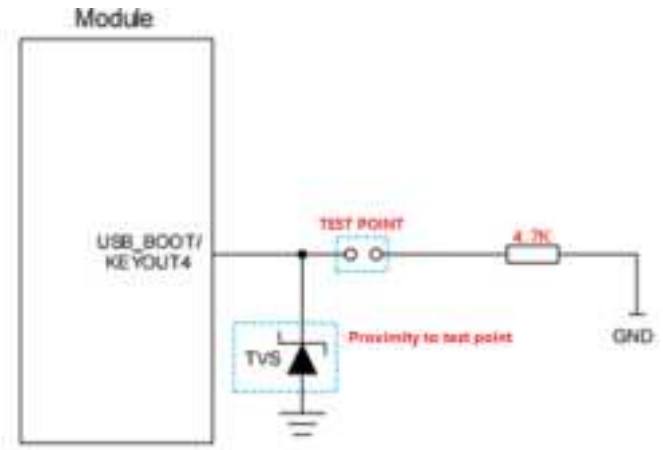

Figure 15 :USB_BOOT Reference Design Circuit Diagram

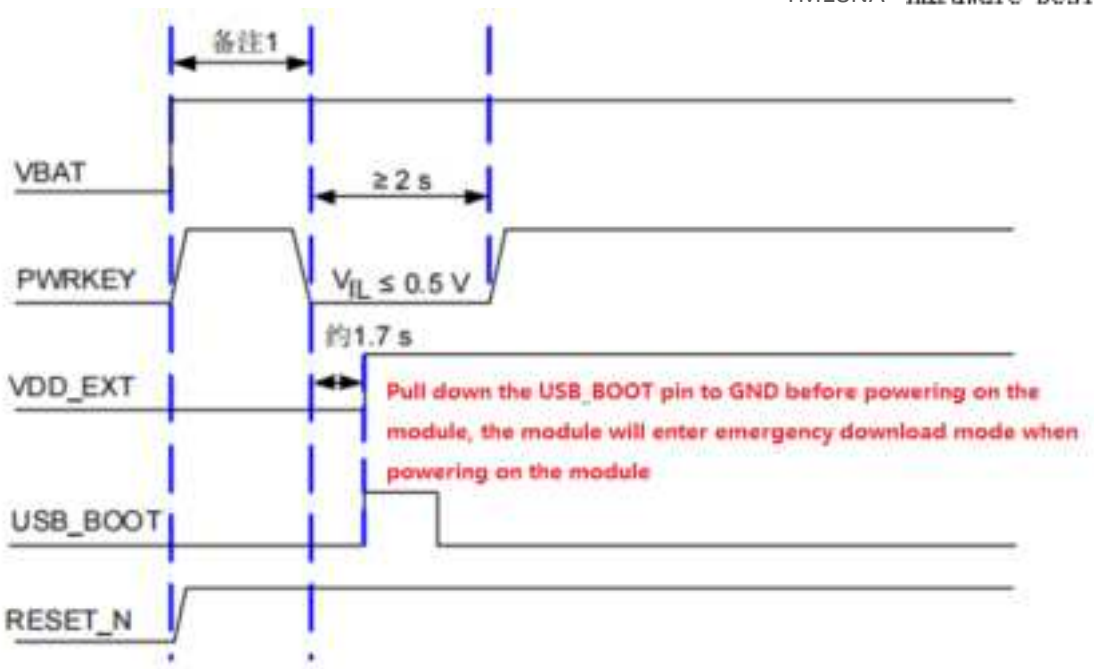

Figure 16: Timing of entering forced download mode

note

1. Before pulling down PWRKEY, make sure the VBAT voltage is stable. It is recommended to stabilize VBAT for at least 30 ms before pulling down PWRKEY.
2. When using MCU to control the module to enter the forced download mode, you need to follow the above timing diagram to control, it is not recommended to pull up the USB_BOOT to 1.8V before powering up the module VBAT. if you need to manually enter the forced download mode, please short the test points as shown in the reference circuit design diagram.

4.3. (U)SIM interface (Dual SIM)

The (U)SIM interface is *ETSI* and *IMT-2000* compliant, supports 1.8V and 3.0V (U)SIM cards, and supports dual SIM single standby.

Table 11: (U) SIM Interface Pin Definitions

pinout	pin number	I/O	descriptive	
USIM_DET	79	DI	USIM card insertion and removal detection	
USIM_VDD	14	PO	(U)SIM card 1 Power supply	
USIM_DATA	11	DIO	(U)SIM Card 1 Data	
USIM_CLK	13	DO	(U)SIM Card 1 Clock	
USIM_RST	12	DO	(U)SIM card 1 reset	

USIM2_VDD	65	PO	(U)SIM Card 2 Power Supply
USIM2_DATA	64	DIO	(U)SIM Card 2 Data
USIM2_CLK	62	DO	(U)SIM Card 2 Clock
USIM2_RST	63	DO	(U)SIM card 2 reset

The 8pin (U) SIM interface reference circuit is shown below:

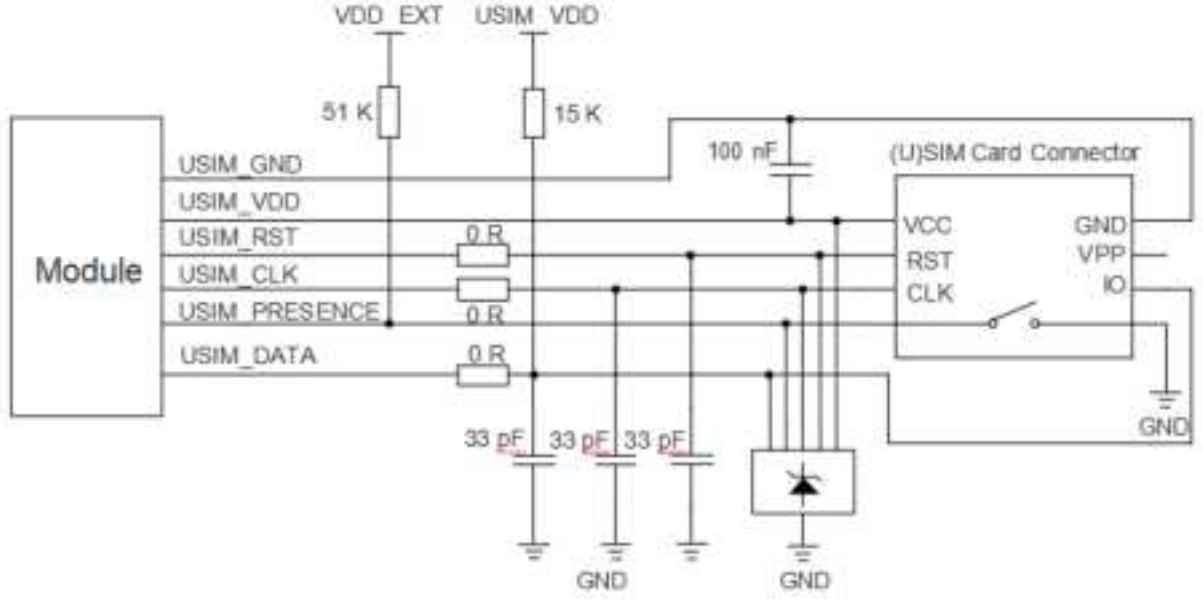

Figure 17: 8-Pin (U)SIM Interface Reference Circuit Diagram

USIM_DET may be suspended if the (U)SIM detection function is not required.

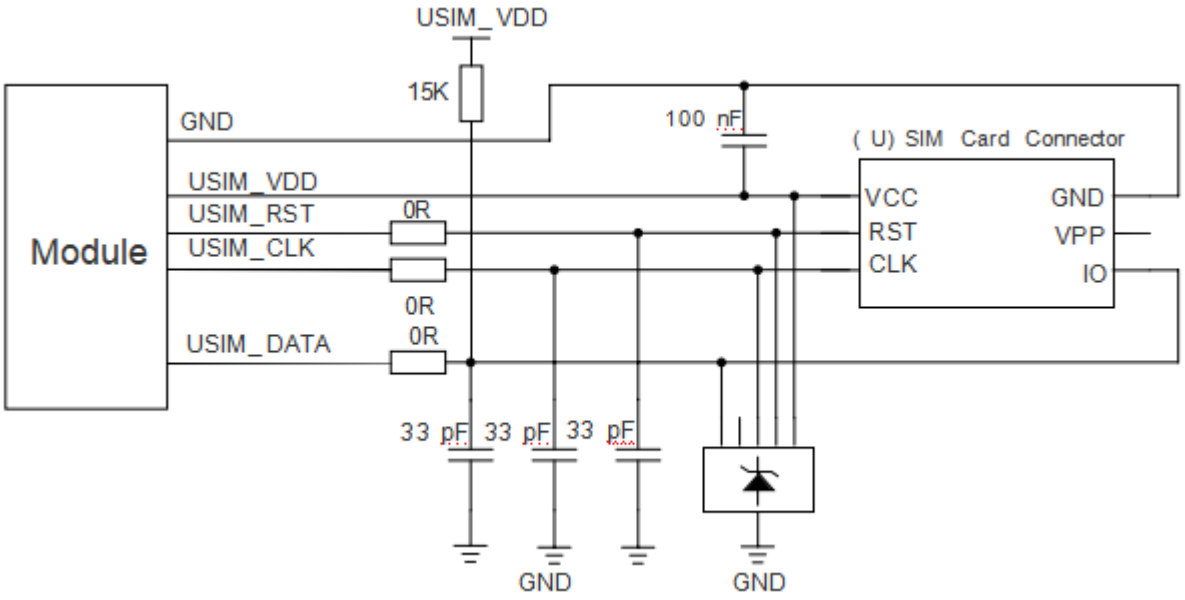

Figure 18: 6-Pin (U)SIM Interface Reference Circuit Diagram

To ensure performance, the circuit design of the (U)SIM interface should follow the following principles:

- Place the (U)SIM card holder close to the module and try to ensure that the length of the (U)SIM card signal line wiring does not exceed 200 mm.
- (U) SIM card signal wiring is routed away from the RF and VBAT power lines.
- Make sure that the bypass capacitor between USIM_VDD and GND has a capacitance of no more than 1uF and is placed as close as possible to the (U)SIM card holder.
- To prevent the USIM_CLK signal and the USIM_DATA signal from crosstalking each other, the two should not be wired too close to each other and a ground shield should be added between the two alignments.
- To ensure good ESD performance, it is recommended that a TVS array be added to the (U)SIM pins, and that the parasitic capacitance of the TVS array be selected to be no more than 15 pF. Connect a 0 ohm resistor in series between the module and the (U)SIM card to facilitate commissioning. (U)SIM card peripherals should be placed as close as possible to the (U)SIM card holder.
- The pull-up resistor on USIM_DATA is beneficial to increase the immunity of the (U)SIM card when the (U)SIM card alignment is too long, or when the interference source is relatively close. It is recommended to place the pull-up resistor close to the (U)SIM card holder.

4.4. I2C Interface

The module provides four I2C interfaces:

Table 12: I2C Interface Pin Definitions

pinout	pin number	I/O	descriptive	note
CAM_I2C1_SCL	57	OD	I2C Serial Clock	
CAM_I2C1_SDA	58	OD	I2C Serial Data	
I2C1_SCL	3	OD	I2C Serial Clock	
I2C1_SDA	4	OD	I2C Serial Data	
I2C2_SCL	67	OD	I2C Serial Clock	Requires an external 1.8V pull-up. If you don't use it, it hangs in the air.
I2C2_SDA	66	OD	I2C Serial Data	
I2C3_SCL	68	OD	I2C Serial Clock	
I2C3_SDA	69	OD	I2C Serial Data	

4.5. PCM interface

The module provides one PCM or I2S interface, supporting both master and slave modes.

Table 13: PCM Interface Pin Definitions

pinout	pin number	I/O	descriptive	note
PCM_SYNC	31	DO	PCM Frame Synchronization	This pin is an output signal when the module is used as a master device.
PCM_CLK	30	DO	PCM Clock	This pin is an output signal when the module is used as a master device.
PCM_DIN	32	DI	PCM Data Input	
PCM_DOUT	33	DO	PCM Data Output	
BB_I2S1_MCLK	26	DO	I2S Clock Output	If you don't use it, it hangs in the air.

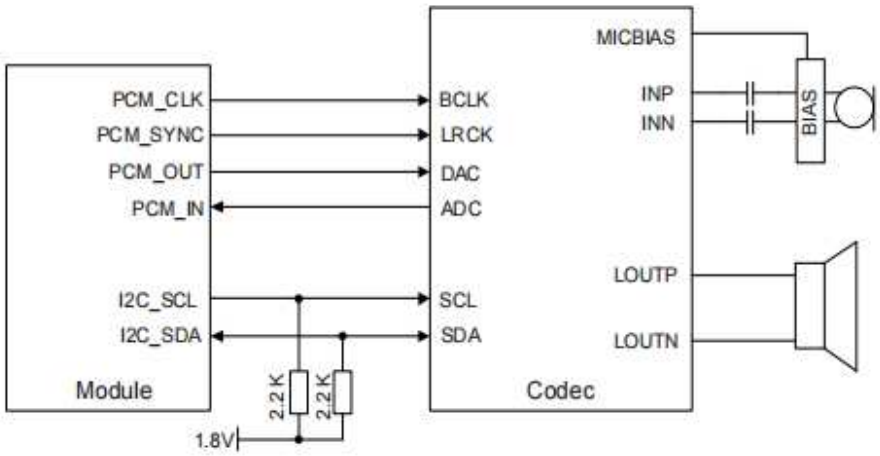

Figure 19: PCM and I2C Interface Circuit Reference Design Block Diagram

4.6 UART

The module provides three UART interfaces:

Table 14 UART Information

Interface Type	Baud rate support	Default Baud Rate	
Main UART	4800~921600 bps	115200 bps	Data Transfer and AT Command Sending
Debugging the UART	2000000 bps	2000000 bps	For partial log output
Auxiliary UART	-	-	-

Table 15: UART Pin Definitions

pinout	pin number	I/O	descriptive	note
MAIN_CTS	22	DO	DTE Clear Transmit	CTS connected to DTE
MAIN_RTS	23	DI	DTE request to send	RTS to DTE
MAIN_RXD	17	DO	Main serial port receive	
MAIN_DCD	21	DI	Main serial port output carrier detection	
MAIN_TXD	18	DO	Main Serial Port Transmit	
AUX_RXD	28	DI	UART3_RXD	
AUX_TXD	29	DO	UART3_TXD	
I2C1_SCL	3	DI	UART2_RXD	reusable
I2C1_SDA	4	DO	UART2_TXD	reusable

The UART level of the module is 1.8 V. If the external host system level is 3.3 V, a level shifter circuit will be added to the UART connection between the module and the host. The following is a reference circuit design using a level shifter chip.

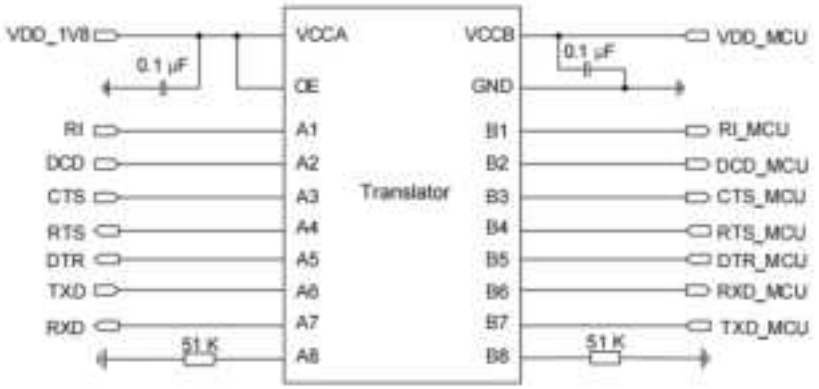

Figure 20: Level shifter reference design block diagram

Another level conversion circuit is shown below. The design of the input and output circuits in the following dotted line section can be referred to the solid line section, but the direction of connection should be noted:

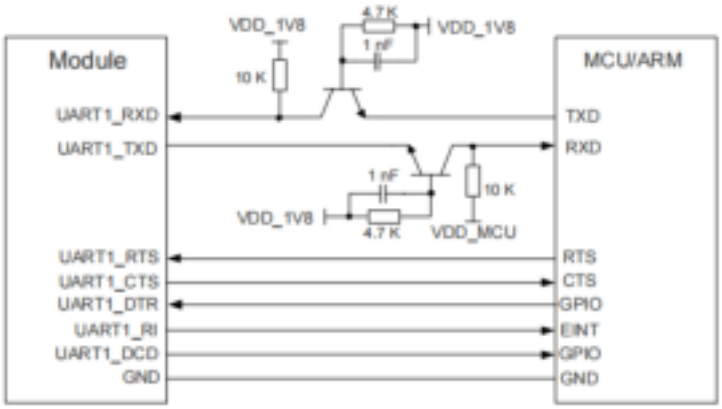

Figure 21: Triode Level Conversion Reference Design Block Diagram

note

1. Level shifting circuits are not suitable for applications with baud rates exceeding 460 kbps.
2. Please be sure to note that the serial port hardware flow control CTS and RTS pins are directly connected, and pay attention to the direction of input and output.

4.7. ADC Interface

The module provides two general-purpose analog-to-digital converter interfaces (ADC interfaces). When wiring the ADC interfaces, ground-packing is recommended to improve the accuracy of the voltage measurements on the interfaces.

Table 16: ADC Interface Pin Definitions

pinout	pin number	I/O	descriptive	note
ADC0	9	AI	General Purpose ADC Interface	
ADC1	96	AI		
ADC2	99	AI		
ADC3	106	AI		

ADCs have up to 12-bit precision.

Table 17: ADC Characteristics

parameters	minimum value	typical value	maximum values	unit (of measure)
ADC0 Voltage Range	0	-	VBAT	V
ADC1 Voltage Range	0	-	VBAT	V
ADC2 Voltage Range	0	-	VBAT	V
ADC3 Voltage Range	0	-	VBAT	V
ADC Accuracy		12		bits

note

1. The input voltage of each ADC interface pin must not exceed its respective voltage range.
2. The ADC interface cannot be directly connected to any input voltage when the module VBAT is not powered.
3. It is recommended that the ADC interface utilize a voltage divider circuit input voltage.

4.8. SPI

The module provides 1 dedicated SPI, which only supports master mode and its maximum clock frequency is 83 MHz.

Table 18: SPI Pin Definitions

pinout	pin number	I/O	descriptive	note
SPI_FLASH1_CLK	101	DO	SPI Clock	
SPI_FLASH1_CS	79	DO	SPI Chip Select	
SPI_FLASH1_SIO0	100	DIO	SPI Data 0	
SPI_FLASH1_SIO1	108	DIO	SPI Data 1	
SPI_FLASH1_SIO2	109	DIO	SPI Data 2	
SPI_FLASH1_SIO3	107	DIO	SPI Data 3	

4.9 Indicator signals

Table 19: Indicator Interface Pin Definitions

pinout	pin number	I/O	descriptive	note
STATUS	25	DO	Operational status indication	1.8V/3.3V Voltage Domain. If you don't use it, it hangs in the air.
NET_STATUS	16	DO	Network Status Indication	

4.9.1 Network status indication

As indicator pins, NET_STATUS is used to indicate the network registration status and network operation status of the module, respectively, while driving the corresponding LEDs.

Table 20: Network Status Indicator Pin Operating Status

pinout	level state	Module Network Status
NET_STATUS	Slow flash (200 ms high/1800 ms low)	search network status
	Flash (200 ms high/200 ms low)	standby mode
	Rapid flash (60 ms high/60 ms low)	data transmission mode
	high level	during a conversation

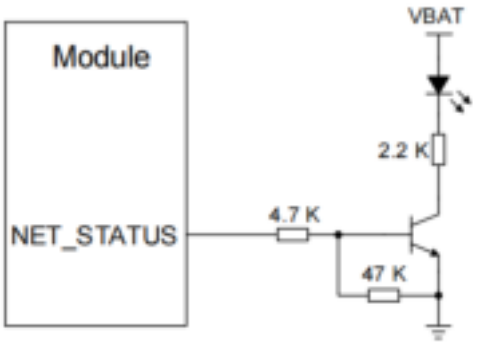

Figure 22: Network Status Indication Reference Circuit Diagram

4.9.2 STATUS

STATUS is used to indicate the working status of the module. When the module is normally powered on, STATUS will output a high level.

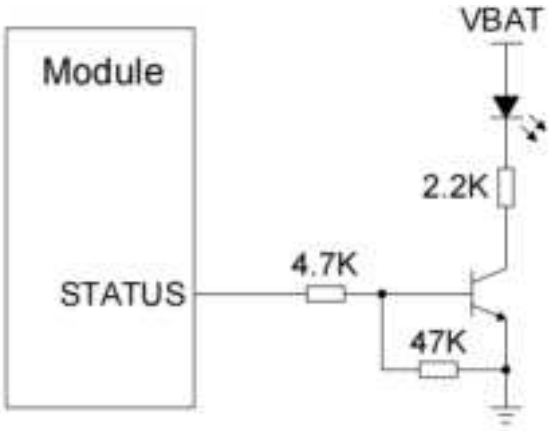

Figure 23:STATUS Reference Circuit Diagram

5 RF Characterization

5.1 Cellular networks

5.1.1 Antenna interfaces and operating frequency bands

Table 21: Cellular Network Antenna Interface Pin Definitions

pinout	pin number	I/O	descriptive	
ANT_MAIN	35	AIO	Primary Antenna Interface	50Ω characteristic impedance.

Table 22: TM18NA Operating Frequency Bands

operating frequency	Transmit (MHz)	Reception (MHz)
LTE-FDD B2	1850~1910	1930~1990
LTE-FDD B4	1710~1755	2110~2115
LTE-FDD B5	824~849	869~894
LTE-FDD B7	2500~2570	2620~2690
LTE-FDD B12	699~716	728~746
LTE-FDD B13	777~787	746~757
LTE-TDD B17	704~716	734~746
LTE-TDD B26	816~849	859~894
LTE-TDD B66	1710~ 1780	2110~2200
LTE-TDD B40	2300~2400	2300~2400
LTE-TDD B41	2496~2690	2496~2690

5.1.2 Launch power

Table 23: RF Transmit Power

(radio) band	Maximum transmit power	Transmit power min

LTE-FDD B2/4/5/7/12/13/17/26/66	23 dBm ±2 dB	< -39 dBm
LTE-TDD B40/B41	23 dBm ±2 dB	< -39 dBm

5.1.3 Receiving sensitivity

Table 24: RF Receiving Sensitivity

paradigm	(radio) band	Receiving sensitivity (LTE main antenna high power TX)	Receiving sensitivity (LTE main antenna low power TX)
LTE-FDD B2 (10 MHz)	-98.5 dBm	-98.5 dBm	LTE-FDD B2 (10 MHz)
LTE-FDD B4 (10 MHz)	-97.5 dBm	-97.5 dBm	LTE-FDD B4 (10 MHz)
LTE-FDD B5 (10 MHz)	-98.5 dBm	-99 dBm	LTE-FDD B5 (10 MHz)
LTE-FDD B7 (10 MHz)	-99dBm	-99dBm	LTE-FDD B7 (10 MHz)
LTE-FDD B12 (10 MHz)	-99dBm	-99.5dBm	LTE-FDD B12 (10 MHz)
LTE-FDD B13 (10 MHz)	-98 dBm	-99.5 dBm	LTE-FDD B13 (10 MHz)
LTE-FDD B17 (10 MHz)	-99 dBm	-99.5 dBm	LTE-FDD B17 (10 MHz)
LTE-FDD B26 (10 MHz)	-98.5 dBm	-98.5 dBm	LTE-FDD B26 (10 MHz)
LTE-FDD B66 (10 MHz)	-98.5 dBm	-98.5 dBm	LTE-FDD B66 (10 MHz)
LTE-TDD B40 (10 MHz)	-99.5 dBm	-99.5 dBm	LTE-TDD B40 (10 MHz)
LTE-TDD B41 (10 MHz)	-99 dBm	-99 dBm	LTE-TDD B41 (10 MHz)

Note: TDD high power is the same as low power, and the table shows the intermediate channel sensitivity performance for each band.

5.2. WIFI Scan

The module supports WIFI SCAN function to receive WIFI signals.

Table 25: WIFI scan antenna interface pin definitions

pinout	pin number	I/O	descriptive	note
ANT_WIFI_SCAN	98	AI	Wi-Fi Scan Antenna Interface	50 Ω characteristic impedance, not in use is suspended.

5.3. RF PCB Routing Requirements

Antennas generally default to 50 ohm standard impedance for their feed ports during the standalone design phase. At the same time, the antenna port in the chip is generally designed according to 50 ohms. Therefore, the RF alignment between the chip and the antenna on the PCB needs to consider the impedance matching problem, which is also generally 50 ohms. As long as the conditions permit, on the RF line near the antenna side of the PCB, you can consider reserving a π-matching circuit to facilitate the subsequent debugging of the impedance matching.

π-matching needs to be placed close to the antenna:

In order to minimize loss, RF alignment is as short and straight as possible to avoid impedance mismatches caused by structural mutations such as over-holes, flipped layers, and large corners. At the same time.

RF lines around the ground and the main ground should be avoided trenching, the two need to be fully electrically connected, can be appropriate to increase the density of the two sides of the metal perforations to reduce energy leakage

exposure and external signal interference. In addition, the space above the RF cable should be avoided to be covered by other devices and metal devices should not be close to the RF cable when the top layer is routed. For detailed design, please refer to the document "XINYUAN Design Guide_RF Antenna".

5.4 Antenna Design

pinout	pin number	I/	descriptive	note
ANT_MAIN	35	AI	primary antenna	50 Ω Characteristic Impedance

5.4.1 Antenna Design Guide

Users should connect antennas to TM18NA antenna pads through micro-strip line or other types of RF trace and the trace impedance must be controlled in 50Ω. Tuge recommends that the total insertion loss between the antenna pads and antennas should meet the following requirements.

Frequency	Loss
700MHz-960MHz	<0.5dB
1710MHz-2170MHz	<0.9dB
2300MHz-2650MHz	<1.2dB

To facilitate the antenna tuning and certification test, a RF connector and an antenna matching circuit should be added. The following figure is the recommended circuit

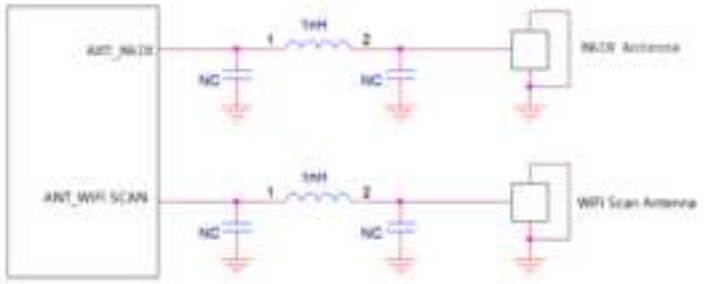

Figure 24: : Active antenna circuit

RF traces layou

- Keep the RF trace from module ant pin to antenna as short as possible.
- RF trace should be 50 Ω either on the top layer or in the inner layer.
- RF trace should be avoided right angle and sharp angle.
- Put enough GND vias around RF traces.
- RF trace should be far away from other high speed signal lines.

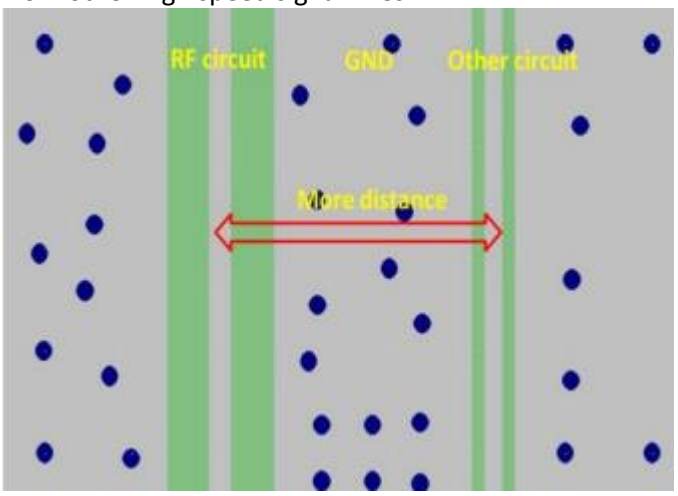

Figure 25: RF trace should be far away from other high speed signal lines

- Avoiding the paroling rout of other system antennas nearly.
- There should be some distance from The GND to the inner conductor of the SMA connector. It is better to keep out all the layers from inner to the outer conductor.
- GND pads around the ANT pad should not be hot pad to keep the GND complete.

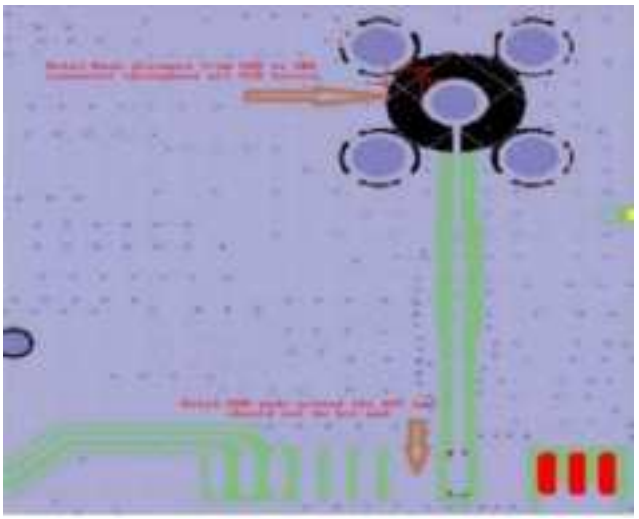

Figure 26: The distance between GND to the inner conduc

- Make sure the efficiency of LTE main ANT more than 40%
- Keep the decoupling of LTE main ANT to WiFi Scan ANT more than 15dB

The antennas that can be selected for this module are divided into two categories: PCB board-mounted antennas and external antennas. Generally speaking, due to the limitation of space, the performance of PCB board-mounted antenna is far inferior to external antenna; PCB board-mounted antenna is low cost, no need to assemble, not easy to be damaged, but the antenna efficiency is low, easy to be interfered by other devices on the PCB board; external antenna is more efficient, better directionality, far away from the interference of the motherboard, but high cost, need to be assembled, and take up space.

Since the on-board antenna can be directly connected through the RF cable, the following only introduces the common physical interfaces of external antennas, which are the following 3 types:

First of all, the most common SMA coaxial connectors, this type of connector variety, PCB board is most commonly used on the 50 ohm, straight insertion, four corners of the soldered SMA-K (female) connectors, as shown in the figure below. Note that when selecting this type of connector, you need to consider the connector pin spacing, inner and outer diameter and other dimensions are applicable to the PCB board thickness. In addition, if required, models such as 90° elbow and SMA-J (male) are available. When soldering, the SMA connector core wire is connected to the RF line on the PCB, and the coaxial outer conductor is connected to the metal ground corresponding to the RF line on the PCB.

Figure 27 Common SMA coaxial connectors

Next is the IPEX connector, shown below. This connector is soldered to the PCB board in the form of a patch, the connector's core wire on the back of the lead pin connected to the pad at the end of the RF line, the other three sides of the pin soldered to the ground around the RF line. In the welding need to pay attention to the direction, to avoid the connector core wire welded to the ground. When choosing this type of connector, the antenna end needs to be equipped with the corresponding connector and RF cable.

Figure 28 Common IPEX Connectors

Alternatively, the simplest pads can be used as the interface to the antenna by simply extending a small section of RF wire at the end and placing the pads. This approach is suitable for feeding monopole antennas (usually folded or spiral), where the feed end of the monopole antenna is soldered directly to the pad. In order to avoid the force of the soldered antenna causing the pads of the PCB board to fall off, the structural strength can be increased by means of holes at the bottom of the pads. Another way is to use the wire to connect the pad to the monopole antenna, at which time the antenna should be designed with the pad as the starting point and the wire as part of the antenna radiator.

If using the on-board antenna, it is recommended to reserve an external antenna connector in case of emergency.

5.4.2 Antenna selection

Introduction to common terms used for antennas

1. **Antenna efficiency:**

Antenna efficiency is the ratio of antenna radiated power to input power. Due to the existence of return loss, material loss, coupling loss, thermal loss, etc., the radiated power is always lower than the input power. In the design of miniaturized antennas (antenna monopole size less than a quarter wavelength), this index should be focused on . When the antenna is placed parallel to the ground, too close to the ground will greatly reduce the radiation efficiency.

2. **S11 and VSWR**:

S11 is the return loss, which is used to measure the amount of reflected energy, expressed in dB. When total reflection, the ratio of reflected energy to input energy is 1, i.e., 0 dB. Therefore, the smaller S11 is, the better, and in antenna design, S11 ≤ -10 dB is generally taken as the target.

VSWR is voltage standing wave ratio, also known as standing wave coefficient, which is the ratio of the voltage of standing wave in wave belly and wave valley. When there is no reflected wave, that

is, there is no standing wave, at this time VSWR = 1 (minimum), in antenna design, generally VSWR ≤ 2 as the goal.

The above two parameters can reflect the impedance matching situation, and the two can be converted to each other. Through the vector network analyzer can be directly measured to get these two parameters. When miniaturized antenna design is carried out in limited space, due to the larger reflection and smaller S11 value (close to 0dB), generally no longer pay attention to S11, and the change of standing wave is more intuitive.

It should be noted that all types of losses also lead to a reduction in reflected energy, so an antenna with a high standing wave must have a low radiation efficiency, but an antenna with a low standing wave does not necessarily have a high radiation efficiency.

- **polarize**

Polarization is the direction of the electric field vector of the antenna in the direction of maximum radiation, which can be divided into line polarization, elliptical polarization and circular polarization, and line polarization and circular polarization can be regarded as special elliptical polarization (two extremes). When the polarization direction of the receiving antenna is different from the polarization of the space electromagnetic wave, there will be a polarization mismatch, resulting in part of the energy not being received. When the polarizations are exactly orthogonal, such as mutually perpendicular line polarizations, left and right circular polarizations, the antenna will not be able to receive the electromagnetic wave.

Line polarization with vertical ground is recommended.

- Gain

Antenna gain generally refers to the maximum radiation direction of the gain value, usually expressed in dB (can also be used dBi and dBd, the two calculations are different), the higher the gain indicates that the energy radiation is more centralized, also indicates that the antenna in the other direction of the radiation is less. Therefore, the antenna gain is generally required to focus on when there is a directional demand.

Antenna gain is directly related to the antenna electrical size (the ratio of actual size to wavelength), and it is difficult to improve the antenna gain when the available space is limited, so it is recommended to prioritize the efficiency and standing wave index in the antenna design. When the antenna efficiency is improved, the overall antenna gain will also be improved.

- orientation **plan**

Radiation direction map reflects the antenna in the space in all directions on the distribution of radiation energy, that is, the size of the gain in all directions. For 100% efficiency, the ideal omnidirectional antenna, the gain in all directions are 0 dB. in practice, the antenna can not uniformly radiate energy, there will inevitably be a part of the direction of the gain is higher, part of the

direction of the gain is lower. At the same time, the antenna can not achieve 100% efficiency, the decline in efficiency will lead to a reduction in the overall gain.

For omni-directional antennas, a large number of gain notches should be avoided provided that the gain requirements are met.

- **disruptions**

In addition to antenna performance, other interference on the PCB board can also affect module performance. In order to ensure the high performance of the module, the interference must be well controlled. Suggestions: such as LCD, CP, FPC alignment, audio circuits, power supply part should be as far away from the antenna, and do the appropriate isolation and shielding, or path filtering.

Antenna metrics requirements

Since the performance of board-mounted antenna is closely related to PCB size, antenna headroom, antenna form and other factors, it is difficult to standardize the specific performance index, and it needs to be designed according to the demand. In the board-mounted antenna design, it is recommended to design through antenna simulation software combined with PCB structure, which can appropriately simplify the PCB model, remove unnecessary structures, improve the simulation efficiency, and determine whether the antenna form is feasible according to the simulation results.

External antenna design freedom is high, you can directly buy the finished antenna, if you do not consider the space size limitations, antenna performance indicators can refer to the following table:

Table 30: Antenna Performance Specifications

TM18NA module main antenna requirements (external antenna)	
frequency range	Coverage of all LTE Band 2, 4, 5, 7, 12, 13, 17, 26, 66, 40, 41
gain (electronics)	≥2dB
Directionality requirements	Horizontal omnidirectional
power capacity	≥ 23dBm average power
standing wave ratio (physics)	≤ 3 (in the operating band)

Commonly used external antenna forms

1、Built-in antenna

Built-in antenna generally refers to the antenna placed in the product shell, so that the product is more beautiful in appearance, but part of the product due to miniaturization requirements, the built-in antenna reserved space is small, can not meet the need for normal operation of low-frequency

antenna, the need to give up a part of the antenna performance, and the antenna's standing wave test is not convenient.

The built-in antenna is typically used with an IPEX connector or soldered directly to the PCB board.The IPEX antenna consists of a piece of coaxial wire that can be bent and a flat structure of the antenna. The antenna can be mounted with a high degree of freedom and can be affixed to the inside wall of the product casing, as shown in the figure below.

Figure 29 FPC antenna and PCB antenna

If the welding method is used, antenna forms such as folded line, spiral and PIFA can be used as shown in the figure below.

Figure 30 Folded antenna, etc.

When choosing the built-in antenna, you need to pay attention to the antenna's working band and the antenna's installation environment, and utilize the internal space of the product as much as possible to increase the distance from the PCB board ground, and it is recommended to install the antenna in the corner of the PCB board.

2、External antenna

Under normal circumstances, the external antenna is subject to the smallest space constraints, and the antenna design is simpler, which can greatly improve the antenna performance. The external antenna is usually connected by SMA connector, and if necessary, the antenna installation distance can be increased by RF cable, but the longer and thinner the cable, the greater the loss.

External antennas can be tested for standing wave by a vector network analyzer to verify whether their operating bands meet the requirements. It should be noted that when the cable loss is large, the standing wave will also be reduced, so you can not judge the antenna performance only by the standing wave.

External antennas come in a variety of shapes, the most common being columnar and flat structures, so simply choose one that meets the specifications without further ado.

6 Electrical performance and reliability

6.1 Absolute maximum ratings

Table 31: Absolute Maximum Ratings

parameters	minimum value	maximum ratings	unit (of measure)
VBAT Voltage	-0.3	6.0	V
USB_VBUS Voltage	-0.3	5.5	V
Digital Interface Voltage	-0.3	2.1	V
ADC0 Voltage	0	VBAT	V
ADC1 Voltage	0	VBAT	V
ADC_IN2 Voltage	0	VBAT	V
ADC_IN4 Voltage	0	VBAT	V
VBAT Current	0	2.0	A

6.2 Power supply ratings

Table 32: Module Power Supply Ratings

parameters	descriptive	prerequisite	minimum value	typical value	maximum values	unit (of measure)
VBAT	VBAT_BB and VBAT_RF	The actual input voltage must be within this range	3.3	3.8	4.3	V
IVBAT	Peak current (per transmitter time slot)	Under maximum transmit power level	0	0.65	0.70	A
USB_VBUS	USB Connection Detection		3.5	5.0	5.25	V

6.3 Power consumption

Table 33: LTE Power Consumption

descriptive	prerequisite	typical value	unit (of measure)
shutdown mode	Module shutdown	10	uA
PM1 Sleep Mode	AT+CFUN=0 (USB disconnected)	1.0	mA
	LTE-FDD @PF=32 (USB disconnected)	2.22	mA
	LTE-FDD @PF=64 (USB disconnected)	1.55	mA
	LTE-FDD @PF=64 (USB connection)	2.47	mA
	LTE-FDD @PF=128 (USB disconnected)	1.22	mA
	LTE-FDD @PF=256 (USB disconnected)	1.05	mA
	LTE-TDD @PF=32 (USB disconnected)	2.23	mA
	LTE-TDD @PF=64 (USB disconnected)	1.54	mA
	LTE-TDD @PF=64 (USB connection)	2.49	mA
	LTE-TDD @PF=128 (USB disconnected)	1.21	mA
	LTE-TDD @PF=256 (USB disconnected)	1.05	mA
IDLE mode	LTE-FDD @PF=64 (USB disconnected)	9.54	mA
	LTE-FDD @PF=64 (USB connection)	23.94	mA
	LTE-TDD @PF=64 (USB disconnected)	9.51	mA
	LTE-TDD @PF=64 (USB connection)	23.92	mA
LTE (intermediate channel)	LTE-FDD B2	495	mA
	LTE-FDD B4	515	mA
	LTE-FDD B5	430	mA
	LTE-FDD B7	650	mA
	LTE-FDD B12	585	mA
	LTE-FDD B13	485	mA

descriptive	prerequisite	typical value	unit (of measure)
	LTE-FDD B17	575	mA
	LTE-FDD B26	460	mA
	LTE-FDD B66	490	mA
	LTE-TDD B40	295	mA
	LTE-TDD B41	260	mA

Table 34: GNSS (Optional) Power Consumption

descriptive	prerequisite	typical value	unit (of measure)
GNSS (optional) independent positioning power consumption	Cold start, independent positioning	73	mA

6.4. Digital Logic Level Characterization

Table 35: 1.8V I/O Requirements

parameters	descriptive	minimum value	maximum values	unit (of measure)
VIH	Input High Level	0.7 x VDDIO	VDDIO + 0.3	V
VIL	Input Low Level	-0.3	0.3 × VDDIO	V
VOH	Output High Level	VDDIO - 0.5	VDDIO	V
VOL	Output Low Level	0	0.4	V

Table 36: (U) SIM Card 1.8V I/O Requirements

parameters	descriptive	minimum value	maximum values	unit (of measure)
	USIM_VDD	electricity supply	1.65	1.95

VIH	Input High Level	0.7 x USIM_VDD	USIM_VDD + 0.3	V
VIL	Input Low Level	-0.3	0.2 x USIM_VDD	V
VOH	Output High Level	0.7 x USIM_VDD	USIM_VDD	V
VOL	Output Low Level	0	0.4	V

Table 37: (U) SIM Card 3.0V I/O Requirements

parameters	descriptive	minimum value	maximum values	unit (of measure)
USIM_VDD	electricity supply	2.7	3.05	V
VIH	Input High Level	0.7 x USIM_VDD	USIM_VDD + 0.3	V
VIL	Input Low Level	-0.3	0.2 x USIM_VDD	V
VOH	Output High Level	0.7 x USIM_VDD	USIM_VDD	V
VOL	Output Low Level	0	0.4	V

6.5 Electrostatic protection

In the module application, due to the human body with static electricity, microelectronics charged friction generated by static electricity, etc., will be discharged through various ways to the module, thus causing some damage to the module, so static electricity protection should be taken seriously. In the process of research and development, production, assembly and testing, especially In the product design process, reasonable static protection measures should be taken. For example, increase anti-static protection at the interface of circuit design and at the points susceptible to damage or influence of electrostatic discharge; wear anti-static gloves in production, and so on.

Table 38: ESD performance parameters (according to IEC-61000-4-2)

test point	contact discharge	unit (of measure)
VBAT	±8	±12
Antenna Interface	±4	±8
Other interfaces	HBM mode -	

6.6 Operating and storage temperatures

Table 39: Operating and Storage Temperatures

parameters	minimum value	typical value	maximum values	unit (of measure)
Normal operating temperature range [3]	-35	+25	+75	° C
Extended operating temperature range [4]	-40	-	+85	° C
Storage temperature range	-40	-	+90	° C

[3] When the module operates within this temperature range, the relevant performance of the module meets the requirements of the 3GPP standard.

[4] When the module works within this temperature range, the module can still maintain normal working condition with functions such as voice, SMS, data transmission, emergency call, etc.; there will be no unrecoverable faults; the RF spectrum and network are basically unaffected. Only individual indexes such as output power and other parameters may exceed the range of 3GPP standard. When the temperature returns to the normal working temperature range, the module's indicators still comply with the 3GPP standard.

7 Structure and specifications

This chapter describes the mechanical dimensions of the module, all dimensions are in mm. all dimensions not labeled with tolerances have a tolerance of ±0.2 mm.

7.1 Mechanical dimensions

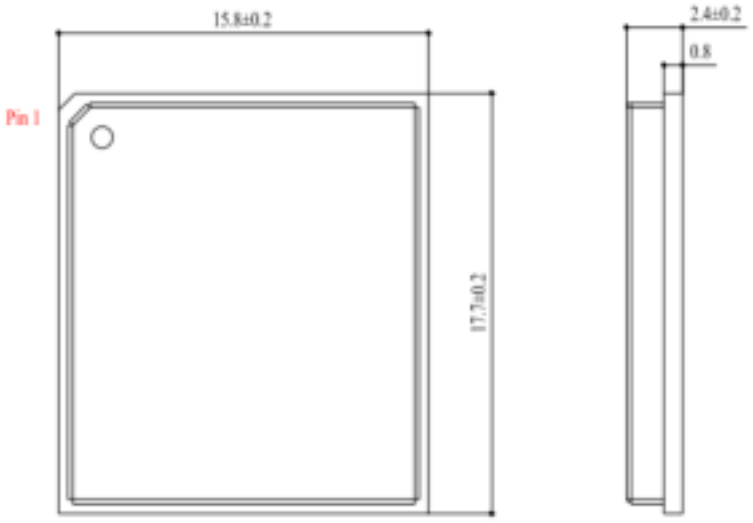

Figure 31: Dimensioned drawing in top and side view

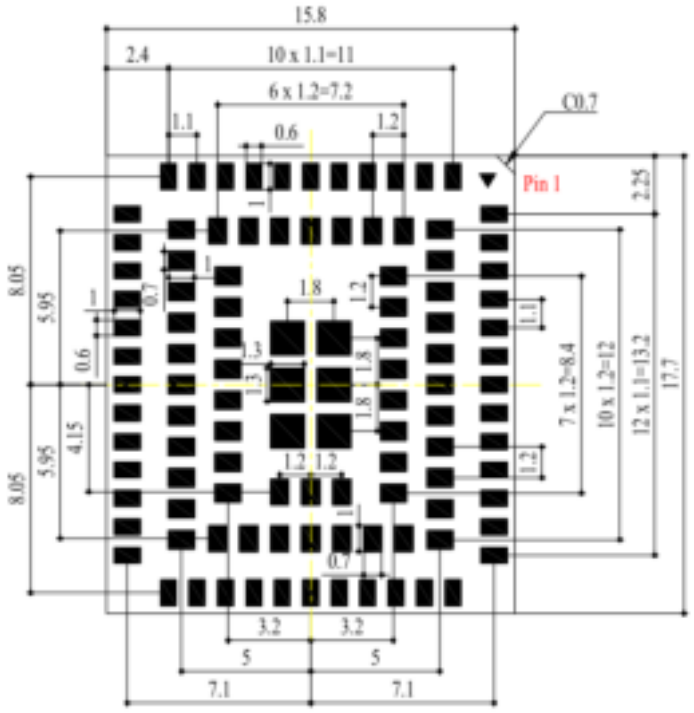

Figure 32: Bottom View Dimension Drawing

7.2 Recommended packaging

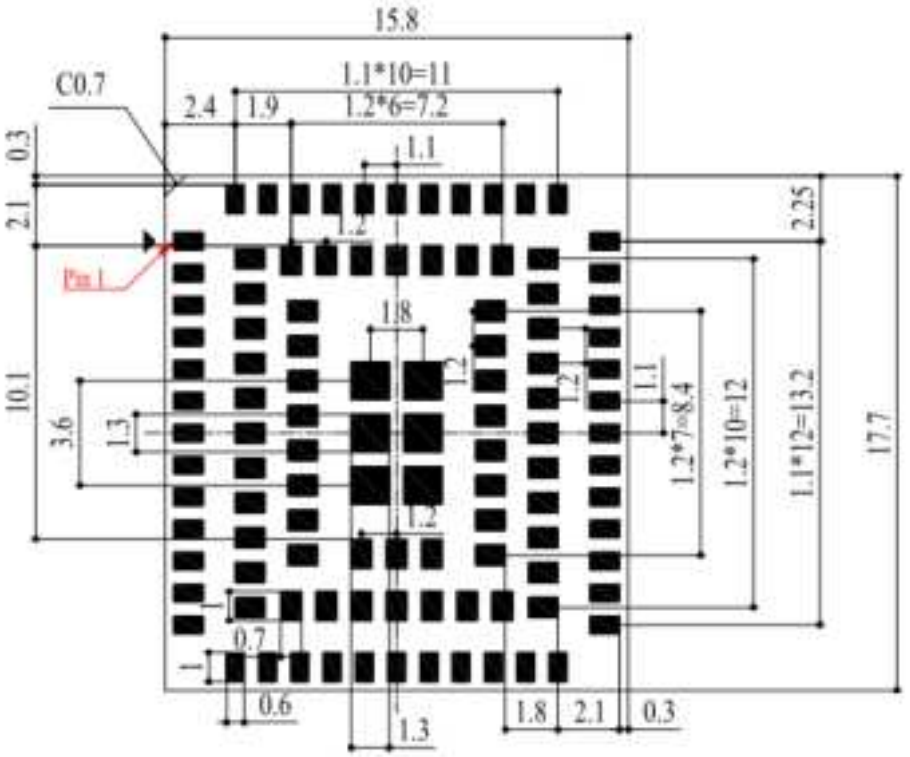

Figure 33: Recommended Package (top view)

7.3 Top and bottom views

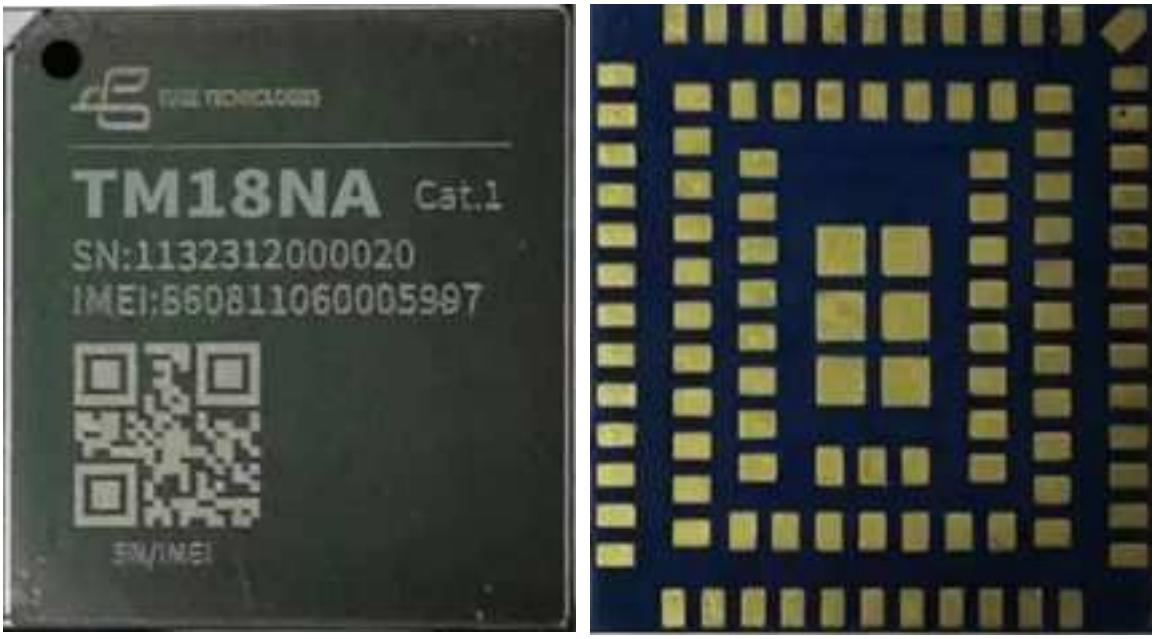

Figure 34: Bottom View of Module Top View

8 Storage, production and packaging

8.1 Storage conditions

Modules are shipped in vacuum-sealed bags. The modules have a moisture sensitivity level of 3 (MSL3) and are stored under the following conditions:

1. Recommended storage conditions: temperature 23 ±5 ° C and relative humidity 35 to 60 %.

2. Modules may be stored in vacuum-sealed bags for up to 12 months under recommended storage conditions.

3. The workshop life of the module after unpacking is 168 hours under workshop conditions at a temperature of 23 ± 5 ° C and a relative humidity of less than 60 % 5. Under these conditions, the module can be directly subjected to reflow production or other high-temperature operations. Otherwise, storage of the module in an environment with less than 10 % relative humidity (e.g., moisture-proof cabinet) is required to keep the module dry.

4. If the module is in the following conditions, it is necessary to pre-bake the module to prevent blistering, cracking, and delamination of the PCB that may occur when the module is exposed to moisture and then soldered at high temperatures:

   - Storage temperature and humidity do not meet recommended storage conditions;
   - Failure to complete production or storage of the module after unpacking in accordance with clause 3 above;
   - Vacuum package leakage, material bulk;
   - Before the module is returned for repair.

5. Baking treatment of modules:

   - Requires baking at 120 ±5 ° C for 8 hours;
   - Secondary baked modules must be soldered within 24 hours of baking, otherwise they must still be stored in the dry box.

note

1. In order to prevent and minimize the occurrence of soldering defects such as blistering and delamination caused by moisture, the module should be strictly controlled and it is not recommended to expose it to air for a long period of time after disassembling the vacuum package.
2. Before baking, the module should be taken out from the package, and the bare module should be placed on the heat-resistant appliance, so as not to damage the plastic tray or reel by high temperature; the module of the second baking should be finished soldering within 24 hours after the baking, or it should be preserved in the drying box. If only a short baking time is needed, please refer to *IPC/JEDEC J-STD-033* specification.
3. Please pay attention to ESD protection when unpacking and placing modules, for example, wear anti-static gloves.

[5] Apply only if the shop environment with low relative humidity meets *IPC/JEDEC J-STD-033* specifications; if you are not sure if the shop environment meets the conditions, or if the relative humidity is greater than 60 %, complete the patch return within 24 hours of unpacking. Do not unpack large quantities in advance.

8.2 Production welding

Print the solder paste on the stencil with a printing squeegee, so that the solder paste leaks through the stencil openings to the PCB, and the strength of the printing squeegee needs to be adjusted appropriately. In order to ensure the quality of the module printing paste, the thickness of the stencil corresponding to the pad part of the module is recommended to be 0.15~0.18 mm.

The recommended reflow temperature is 235~246 °C, and the maximum temperature should not exceed 246 °C. In order to avoid damage to the module due to repeated heat exposure, it is strongly recommended that the customer reflow the first side of the PCB board before applying the module. The recommended oven temperature profile (lead-free SMT reflow) and related parameters are shown in the chart below:

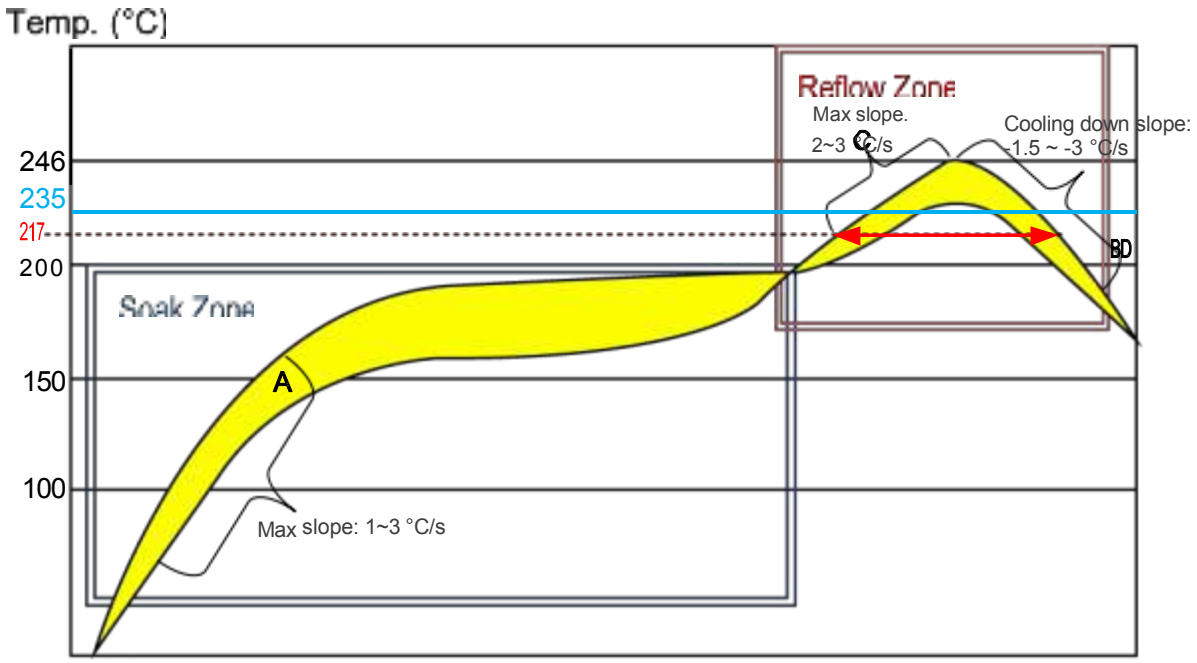

Figure 35: Recommended Reflow Temperature Profile

Table 40: Recommended Control Requirements for Furnace Temperature Testing

sports event	recommended value
Soak Zone	
Maximum temperature rise slope	1~3 ° C/s
Constant temperature time (time between A and B: during 150 to 200 ° C)	70~120 s
Reflow Zone	

Maximum temperature rise slope	2~3 ° C/s
Reflow time (D: period above 217 ° C)	40~70 s
highest temperature	235~246 ° C
Cooling down slope	-1.5 to -3 ° C/s
Number of refluxes	
Maximum number of reflows	1 time

note

1. Do not use any organic solvents (e.g., alcohol, isopropyl alcohol, acetone, trichloroethylene, etc.) to wipe the module shields during production soldering or any other process that may come into direct contact with the module; otherwise, the shields may rust.
2. The marine white copper laser engraved shield can meet: after 12 hours neutral salt spray test, the laser engraved information is clearly recognizable, and the QR code can be scanned (there may be white rust).
3. If the module is to be coated, make sure that the coating material will not react chemically with the module shield or PCB, and that the coating material will not flow into the module.
4. Do not ultrasonically clean the module as this may cause damage to the internal crystals of the module.
5. Due to the complexity of the SMT process, in case of uncertainty, please confirm with Shanghai Touge Technical Support before the start of the SMT process.

FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01r01

2.2 List of applicable FCC rules

CFR 47 FCC Part 22/24/27/90 has been investigated. It is applicable to the modular transmitter

2.3 Specific Operational Use Conditions – Antenna Placement Within the Host Platform

The module is tested for standalone mobile RF exposure use condition.

- The antenna must be installed such that 20cm is maintained between the antenna and users,
- The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.4 Limited Module Procedures

Not applicable

2.5 Trace Antenna Designs

Refer to Manual Section 5.3 on RF PCB Routing Requirements and Section 5.4 Antenna Densign.

2.6 RF Exposure Considerations

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

2.7 Antenna Type and Gain

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain(dBi)
LTE Band 2	7.01
LTE Band 4	6.00
LTE Band 5	7.41
LTE Band 7	7.01
LTE Band 12	6.69
LTE Band 13	6.15
LTE Band 17	6.73
LTE Band 26 (814 MHz - 824 MHz)	7.36
LTE Band 26 (824 MHz - 849 MHz)	7.41
LTE Band 44	7.51
LTE Band 66	7.00

2.8 End Product Labelling Compliance Information

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily removed. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: 2AU4T-TM18NA". The FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on Test Modes and Additional Testing Requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) class II permissive change re-evaluation or new FCC authorization.

Host manufacturer installed this modular with single modular approval should perform the test of radiated spurious emission and ERP/EIRP according to FCC part 22, Part 24, Part 27 and Part 90 requirement, only if the test result comply with FCC part 22, Part 24, Part 27 and Part 90 requirement, then the host can be sold legally.

2.10 Additional testing, Part 15 Subpart B Disclaimer

This transmitter modular us tested as a subsystem and its certification does not cover the FCC

Part 15 Subpart B rules requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rules requirements if applicable.
As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this modular installed.

2.11 Manual Information to The End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.
The host integrator must follow the integration instructions provided in this document and ensure that the composite system end product complies with the requirements by a technical assessment or evaluation to the rules and to KDB Publication 996369.
The host integrator installing this module into their product must ensure that the final composite product complies with the requirements by a technical assessment or evaluation to the rules, including the transmitter operation and should refer to guidance in KDB Publication 996369.

OEM/Host Manufacturer Responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and RF Exposure essential requirements of the FCC rules.

2.12 How to Make Changes – Important Note

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.