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FIBOCOM SQ808-NA Hardware Guide

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Applicability Type

NO.	Product Model	Description
1	SQ808-NA	2GB+16GB eMCP, Applicable to North America

Copyright

Notice

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Trademark

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Change History

Version	Author	Reviewer	Approver	Update Date	Description
V1.0.0	Ye Xincai Zheng Guohai	Tu Min Li Xiyi	Chen Guojiang	2020-04-27	Initial version

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Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: （1） This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
1 Reorient or relocate the receiving antenna.
2 Increase the separation between the equipment and receiver.
3 Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
4 Consult the dealer or an experienced radio/TV technician for help.

FCC Caution:
1 Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

2 This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
This device is intended only for OEM integrators under the following conditions:
1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the maximum antenna gain allowed listed in Table 1-1 Max allowed antenna gain table.
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling
This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID: ZMOSQ808NA”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Innovation, Science and Economic Development Statement

❶ This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:
   1) this device may not cause interference, and
   2) this device must accept any interference, including interference that may cause undesired operation of the device.

❶ Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
   1) l'appareil ne doit pas produire de brouillage, et
   2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

❷ This Class B digital apparatus complies with Canadian ICES-003.

❷ Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

❸ This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter, except tested built-in radios.

❸ Cet appareil et son antenne ne doivent pas être situés ou fonctionner en conjonction avec une autre antenne ou un autre émetteur, exception faites des radios intégrées qui ont été testées.

❹ The County Code Selection feature is disabled for products marketed in the US/ Canada.

❹ La fonction de sélection de l'indicatif du pays est désactivée pour les produits commercialisés aux États-Unis et au Canada.

Radiation Exposure Statement:

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

End Product Labeling:

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 21374-SQ808NA”. The grantee's IC can be used only when all ISED compliance requirements are met.

étiquette de produit final:

Ce module émetteur n 'autorise que l' installation d 'une antenne pour maintenir une distance de 20 cm entre l' antenne et l 'utilisateur.Le produit final doit être étiqueté dans la zone visible comme suit: « comprenant le IC: 21374-SQ808NA ».Le IC délivré ne peut être utilisé que si toutes les conditions de conformité de l'EED sont remplies.

Antenna Requirements：

This radio transmitter module(IC:21374-SQ808NA) requires antennas of specifications of Chapter 4 of this has been approved by Innovation, Science and Economic Development Canada document.Generally,50 ohm impedance is required and S11 is recommended less than -10 dB,the Max allowed antenna gain is as Table 1-2 Max allowed antenna gain table. Antenna types that do not meet these requirement are strictly prohibited for use with this device.

Antenne:

Ce module de radiodiffusion (IC: 21374 - sq808na) exige que les spécifications des antennes soient conformes aux prescriptions du chapitre 4 des présentes normes et a été approuvé par le Ministère canadien de l'innovation, de la

science et du développement économique.Description généraleLa recommandation S11 est inférieure à - 10 dB,Le gain d 'antenne maximum autorisé est indiqué dans le tableau ci - après.Les types d 'antennes qui ne répondent pas à ces exigences sont strictement interdits d' utilisation avec le dispositif.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the Max allowed antenna gain is as Table 1-3 Max allowed antenna gain is as following table showed:

Table 1-4 Max allowed antenna gain table

Operating Band	Antenna Gain（dBi）
GSM850	10.10
GSM1900	11.69
WCDMA BAND II	8.50
WCDMA BAND IV	5.50
WCDMA BAND V	9.92
LTE BAND 2	9.00
LTE BAND 4	6.00
LTE BAND 5	10.41
LTE BAND 7	9.00
LTE BAND 12	9.70
LTE BAND 13	10.16
LTE BAND 17	9.74
LTE BAND 25	9.00
LTE BAND 26(814~824)	10.36
LTE BAND 26(824~849)	10.41
LTE BAND 41	9.00
LTE BAND 66	6.00
BT Test Gain	2.0
2.4G WiFi Test Gain	2.0
WIFI 5G Test Gain	2.5

1 Introduction

1.1 Instruction

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of the module. With the assistance of this document and other instructions, the developers can quickly understand the hardware functions of the module and develop products.

1.2 Reference Standards

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: (U)SIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment ((U)SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module ((U)SIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module ((U)SIM) Application Toolkit (USAT)
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- IEEE 802.11n WLAN MAC and PHY, October 2009+ IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i:

- IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0+EDR/2.1/2.1+EDR/3.0/3.0+HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009

1.3 Related Document

FIBOCOM SQ808 SMT Design Guide

2 Product Overview

2.1 Product Introduction

The smart module integrates core components such as Baseband, eMCP, PMU, Transceiver, PA. It supports long distance multi-mode communication such as FDD/TDD-LTE, WCDMA, and WIFI/BT short-distance radio transmission technology, as well as GNSS wireless positioning technology. The module is embedded with Android operating system and supports various interfaces such as MIPI/USB/UART/SPI/I2C. It is the optimal solution for the core system of wireless smart products. Its corresponding network modes and frequency bands are as follows:

Table 2-1 Support bands

Mode	Band
GSM/GPRS/EDGE	GSM850 /PCS1900
WCDMA	Band 2/4/5
FDD-LTE	Band B2/B4/B5/B7/B12/B13/B17/B25/B26/B66
TDD-LTE	Band 41(2496-2690MHz)
WIFI	2412-2462 MHz, 5150-5350MHz,5470-5850MHz
BT	2402-2480 MHz
GNSS	GPS

2.2 Product Specification

The module is available in 232 LCC+LGA package that includes 148 LCC pins and 84 LGA pins. The dimension is 41mm×41mm×2.80mm. It can be embedded in various M2M applications. It is suitable for the development of smart devices such as smart POS, cash registers, robots, UAVs, smart homes, security monitoring and multimedia terminals. Its detailed performance is shown in the following table:

Table 2-2 Main performance

Performance	Description	
Power	DC 3.5~4.2V, typical voltage: 3.8V	
Application CPU	Arm Cortex-A53 microprocessor cores, 64-bit processor, Quad-core (1.3 GHz)	
Memory	2GB LPDDR3+16 GB eMMC flash	SQ808-NA
Power class	Class 4 (32.5dBm±1dB) for GSM850 Class 1 (29.5dBm±1dB) for PCS 1900 Class E2 (24dBm+4/-5dB) for GSM850 8-PSK Class E2 (23dBm+4.5/-5dB) for PCS 1900 8-PSK Class 3 (23.5dBm±1dB) for WCDMA bands Class 3 (23dBm±1dB) for LTE FDD bands Class 3 (23dBm±1dB) for LTE TDD bands	
GSM/GPRS/EDGE features	R99: CSD transmission rate: 9.6kbps, 14.4kbps GPRS: Support GPRS multi-slot class 33 Coding formats: CS-1/CS-2/CS-3 and CS-4 5 Rx time slots per frame maximum EDGE: Support EDGE multi-slot class 33 Support GMSK and 8-PSK Uplink encoding format: CS 1-4 and MCS 1-9 Downlink encoding format: CS 1-4 and MCS 1-9	
WCDMA features	Support 3GPP R8 DC-HSPA+ Support 16-QAM, 64-QAM and QPSK modulation CAT6 HSUPA: Maximum uplink rate 5.76Mbps CAT24 DC-HSPA+: Maximum downlink rate 42Mbps	
LTE features	Support FDD/TDD CAT4 Support 1.4-20M RF bandwidth Downlink support multi-user MIMO Maximum uplink rate 50Mbps, maximum downlink rate 150Mbps	

Performance	Description
WLAN features	Support 2.4G and 5G WLAN wireless communication, support 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac, the maximum rate up to 433Mbps
Bluetooth features	BT4.2 (BR/EDR+BLE)
Satellite positioning	GPS
SMS	Text and PDU modes Point-to-Point MO and MT SMS cell broadcast SMS storage: stored in the module by default
LCD interface	4 lane MIPI_DSI interfaces Support maximum HD+ 60fps (1440 * 720)
Camera interface	Two 4 lane MIPI_CSI interface, up to 2.1Gbps per lane, support 2 or 3 cameras Up to 13 MP using dual ISP
Audio interface	Audio Input: 2 analog microphone inputs Integrated internal bias Audio output: Class AB stereo headphone output Class AB differential handset output Class D differential speaker amplifier output
USB interface	USB2.0 HS interface, with data transfer rate up to 480 Mbps Support USB OTG (external 5V power supply)
(U)SIM interface	Two (U)SIM card interfaces supporting (U)SIM card: 1.8/3V adaptive Support dual (U)SIM dual standby, support hot plug (Disabled by default)
UART interface	Three UART serial interfaces, with the maximum rate up to 4Mbps One 4_line serial interface supporting RTS and CTS hardware flow control One 2_line serial interface One 2_line debug serial interface
SDC interface	Support SD3.0, 4bit SDC; SD card supports hot plug

Performance	Description
I2C interface	Multiple I2C interfaces, can be used for peripherals such as TP, Camera, and Sensor
ADC interface	Universal ADC
RTC	Support
Antenna interface	TRX antenna, DRX antenna, GNSS antenna, WIFI/BT antenna
Physical characteristics	Dimension: 41mm×41mm×2.80mm Encapsulation: 148 LCC pin + 84 LGA pin Weight: About 9.3g
Temperature range	Operating temperature: -25°C~75°C [1)] Storage temperature: -40°C~85°C
Software update	USB/OTA/SD
RoHS	RoHS Compliant

Note:

1） When the module is operating within this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

2.3 Pin Definition

2.3.1 Pin Assignment

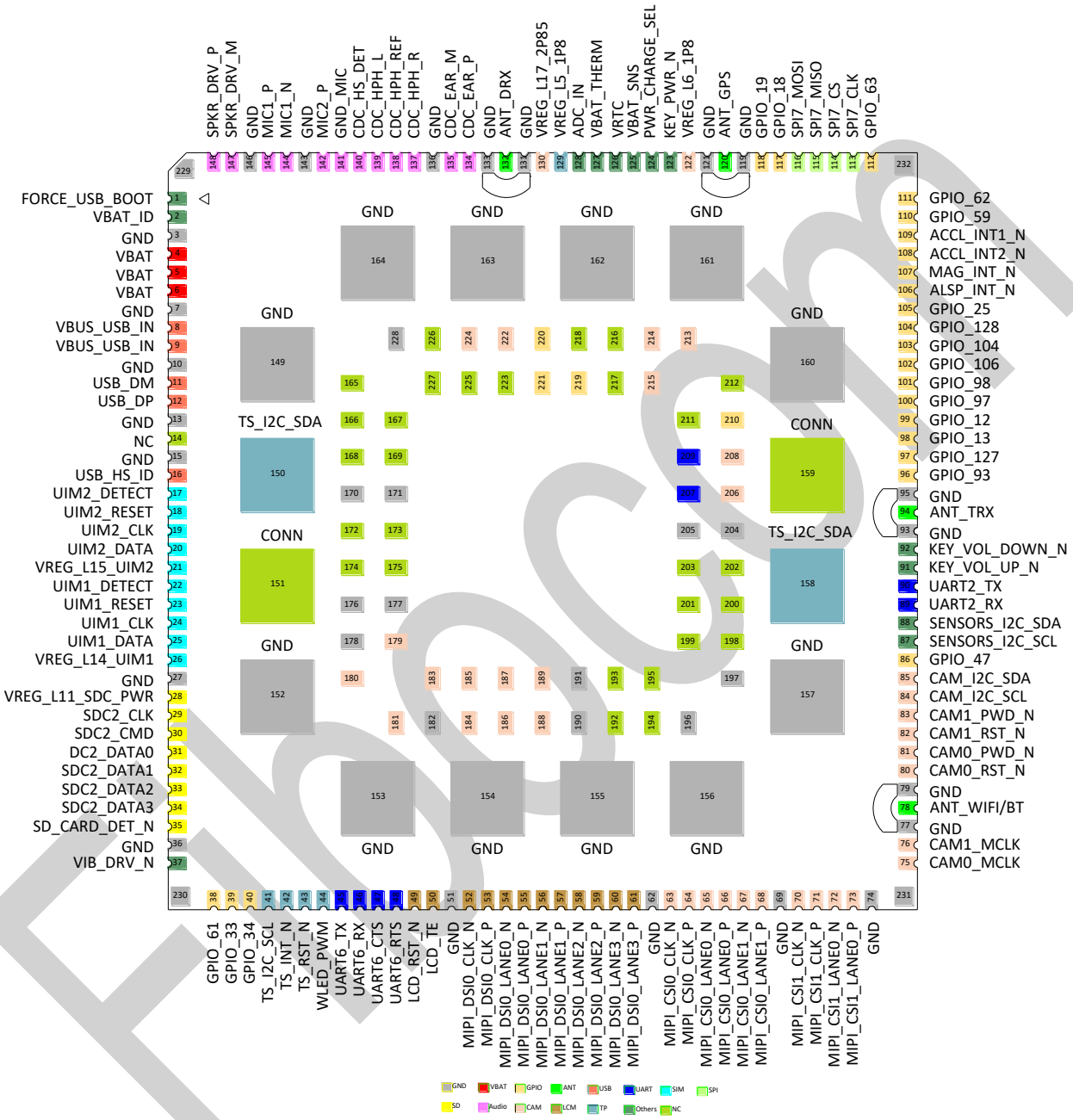

Figure 2-1 Pin assignment

Note:

"NC" indicates No Connect, the pin for this position is reserved and does not need to be connected.

2.3.2 Pin Description

Table 2-3 I/O description parameters

Symbol	Description
I/O	Input/Output
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AI	Analog Input
AO	Analog Output
OD	Open Drain

Descriptions of the module pins are presented in the following table:

Table 2-4 Pin description

Pin Name	Pin #	I/O	Pin Description	Note
Power				
VBAT	4,5,6	PI	Main power input	NA
VRTC	126	PI/PO	RTC clock power supply	NA
VREG_L5_1P8	129	PO	1.8V voltage output	NA
VREG_L6_1P8	122	PO	1.8V voltage output	NA
VREG_L10_2P8	224	PO	2.8V voltage output	NA
VREG_L11_SDC_PWR	28	PO	SD card power supply, 2.95V	NA
VREG_L14_UIM1	21	PO	(U)SIM card 1 power supply	1.8/3V adaptive
VREG_L15_UIM2	26	PO	(U)SIM card 2 power supply	1.8/3V adaptive
VREG_L16_2P8	222	PO	2.8V voltage output	NA
VREG_L17_2P85	130	PO	2.85V voltage output	NA
VIB_DRV_N	37	PO	Vibration motor driver output control	NA

Pin Name	Pin #	I/O	Pin Description	Note	
GND	3, 7, 10, 13, 15,27, 36, 51, 62, 69, 74, 77, 79, 93, 95, 119, 121, 131, 133, 136, 143, 146, 149, 152, 153, 154, 155, 156, 157, 160, 161, 162, 163, 164, 170, 171, 176, 177, 178, 182, 190, 191, 196, 197, 204, 205, 228, 229, 230, 231, 232			GND	51Pins
Battery supply interface					
VBAT_ID	2	AI	Battery ID	Connect the pin with GND through 10K resistor	
PWR_CHARGE_SEL	124	DI	Charge select	If choose external charge mode please connect this pin to GND and if choose internal charge keeps it floating	
VBAT_SNS	125	AI	Main battery voltage sense	Need sample from VBAT near Battery	
VBAT_THERM	127	AI	Battery thermistor input	Connect the pin to GND with 47K resistor	
Key					
KEY_PWR_N	123	DI	Power key	Active low	
KEY_VOL_UP_N	91	DI	Volume+	Active low, Boot configuration	
KEY_VOL_DOWN_N	92	DI	Volume-	Active low. Volume – key by default, can be configuration as reboot	
(U)SIM card interface					
VREG_L14_UIM1	26	PO	(U)SIM card 1 power supply	NA	
UIM1_DATA	25	I/O	(U)SIM card 1 data	NA	
UIM1_CLK	24	DO	(U)SIM card 1 clock	NA	

Pin Name	Pin #	I/O	Pin Description	Note
UIM1_RESET	23	DO	(U)SIM card 1 reset	NA
UIM1_DETECT	22	DI	(U)SIM card 1 plug detection	Disabled by default
VREG_L15_UIM2	21	PO	(U)SIM card 2 power supply	NA
UIM2_DATA	20	I/O	(U)SIM card 2 data	NA
UIM2_CLK	19	DO	(U)SIM card 2 clock	NA
UIM2_RESET	18	DO	(U)SIM card 2 reset signal	NA
UIM2_DETECT	17	DI	(U)SIM card 2 plug detection	Disabled by default
SD card interface				
SD_CARD_DET_N	35	DI	SD card detection	Active low by default
SDC2_DATA3	34	I/O	SD card data interface	NA
SDC2_DATA2	33	I/O	SD card data interface	NA
SDC2_DATA1	32	I/O	SD card data interface	NA
SDC2_DATA0	31	I/O	SD card data interface	NA
SDC2_CMD	30	I/O	SD card command interface	NA
SDC2_CLK	29	DO	SD card clock	NA
VREG_L11_SDC_PWR	28	PO	SD card power supply	NA
I2C interface				
SENSORS_I2C_SCL/GPIO_15	87	OD	I2C clock	Sensor use by default
SENSORS_I2C_SDA/GPIO_14	88	OD	I2C data cable	Sensor use by default
TS_I2C_SCL	41	OD	I2C clock	TP use by default
TS_I2C_SDA	150,158	OD	I2C data cable	TP use by default
CAM_I2C_SCL	84	OD	I2C clock	CAM use by only

Pin Name	Pin #	I/O	Pin Description	Note
CAM_I2C_SDA	85	OD	I2C data cable	CAM use only
CAM2_I2C_SCL	206	OD	I2C clock	CAM use only
CAM2_I2C_SDA	208	OD	I2C data cable	CAM use only
USB interface				
VBUS_USB_IN	8,9	PI	5V input	NA
USB_DP	12	AI/AO	USB HS data+	NA
USB_ DM	11	AI/AO	USB HS data-	NA
USB_HS_ID	16	DI	USB OTG detection pin	NA
UART interface				
UART2_TX	90	DO	UART2 data transmission	Debug serial TX, Boot configuration
UART2_RX	89	DI	UART2 data reception	Debug serial RX
UART6_TX	45	DO	UART6 data transmission	NA
UART6_RX	46	DI	UART6 data reception	NA
UART6_CTS	47	DI	UART6 clear to send	NA
UART6_RTS	48	DO	UART6 request to send	NA
UART5_TX	209	DO	UART5 data transmission	NA
UART5_RX	207	DI	UART5 data reception	NA
SPI interface				
SPI7_CLK	113	DO	SPI clock	Boot configuration
SPI7_CS	114	DO	SPI chip selects	NA
SPI7_MISO	115	DI	SPI Master input slave output	NA
SPI7_MOSI	116	DO	SPI Master output slave input	NA

Pin Name	Pin #	I/O	Pin Description	Note
LCD interface				
MIPI_DSI0_CLK_P	53	AO	MIPI display serial interface clock+	NA
MIPI_DSI0_CLK_N	52	AO	MIPI display serial interface clock-	NA
MIPI_DSI0_LANE0_P	55	AO	MIPI display serial interface Lane 0+	NA
MIPI_DSI0_LANE0_N	54	AO	MIPI display serial interface Lane 0-	NA
MIPI_DSI0_LANE1_P	57	AO	MIPI display serial interface Lane 1+	NA
MIPI_DSI0_LANE1_N	56	AO	MIPI display serial interface Lane 1-	NA
MIPI_DSI0_LANE2_P	59	AO	MIPI display serial interface Lane 2+	NA
MIPI_DSI0_LANE2_N	58	AO	MIPI display serial interface Lane 2-	NA
MIPI_DSI0_LANE3_P	61	AO	MIPI display serial interface Lane 3+	NA
MIPI_DSI0_LANE3_N	60	AO	MIPI display serial interface Lane 3-	NA
LCD_RST_N	49	DO	LCD reset signal	NA
WLED_PWM	44	DO	LCD backlight PWM control	NA
LCD_TE	50	DI	LCD synchronization signal	Keep floating if unused
Touch panel interface				
TS_INT_N	42	DI	LCD TP interrupt signal	NA
TS_RST_N	43	DO	LCD TP reset signal	NA
Camera interface				
MIPI_CSI0_CLK_P	64	AI	MIPI rear camera serial interface clock+	NA

Pin Name	Pin #	I/O	Pin Description	Note
MIPI_CSI0_CLK_N	63	AI	MIPI rear camera serial interface clock+	NA
MIPI_CSI0_LANE0_P	66	AI	MIPI rear camera serial interface lane 0+	NA
MIPI_CSI0_LANE0_N	65	AI	MIPI rear camera serial interface lane 0-	NA
MIPI_CSI0_LANE1_P	68	AI	MIPI rear camera serial interface lane 1+	NA
MIPI_CSI0_LANE1_N	67	AI	MIPI rear camera serial interface lane 1-	NA
MIPI_CSI0_LANE2_P	181	AI	MIPI rear camera serial interface lane 2+	NA
MIPI_CSI0_LANE2_N	183	AI	MIPI rear camera serial interface lane 2-	NA
MIPI_CSI0_LANE3_P	180	AI	MIPI rear camera serial interface lane3+	NA
MIPI_CSI0_LANE3_N	179	AI	MIPI rear camera serial interface lane 3-	NA
CAM0_MCLK	75	DO	Rear camera main clock	NA
CAM0_RST_N	80	DO	Rear camera reset signal	NA
CAM0_PWD_N	81	DO	Rear camera power down	NA
MIPI_CSI1_CLK_P	71	AI	MIPI front camera serial interface clock+	NA
MIPI_CSI1_CLK_N	70	AI	MIPI front camera serial interface clock-	NA
MIPI_CSI1_LANE0_P	73	AI	MIPI front camera serial interface lane 0+	4-Lane CSI1 can be divided to one 2-Lane camera and a 1-Lane camera
MIPI_CSI1_LANE0_N	72	AI	MIPI front camera serial interface lane 0-	
MIPI_CSI1_LANE1_P	184	AI	MIPI front camera serial interface lane 1+	

Pin Name	Pin #	I/O	Pin Description	Note
MIPI_CSI1_LANE1_N	185	AI	MIPI front camera serial interface lane 1-	
MIPI_CSI1_LANE2_P	186	AI	MIPI front camera serial interface lane 2+	
MIPI_CSI1_LANE2_N	187	AI	MIPI front camera serial interface lane 2-	
MIPI_CSI1_LANE3_P	188	AI	MIPI front camera serial interface lane3+	
MIPI_CSI1_LANE3_N	189	AI	MIPI front camera serial interface lane 3-	
CAM1_MCLK	76	DO	Front camera main clock	NA
CAM1_RST_N	82	DO	Front camera reset signal	NA
CAM1_PWD_N	83	DO	Front camera power down	NA
CAM2_MCLK	213	DO	Depth camera MCLK	NA
CAM2_RST_N	214	DO	Depth camera reset	NA
CAM2_PWD_N	215	DO	Depth camera power down	NA
Audio interface				
SPKR_DRV_P	148	AO	Speaker amp+output	NA
SPKR_DRV_N	147	AO	Speaker amp+output	NA
CDC_EAR_P	134	AO	Earpiece PA+output	NA
CDC_EAR_N	135	AO	Earpiece PA-output	NA
CDC_HPH_L	139	AO	Headphone PA left channel output	NA
CDC_HPH_REF	138	AI	Headphone PA ground sensing	NA
CDC_HPH_R	137	AO	Headphone PA right channel output	NA

Pin Name	Pin #	I/O	Pin Description	Note
CDC_HS_DET	140	AI	Headset detection	NA
MIC2_P	142	AI	Headset mic	NA
GND_MIC	141	AI	Headphone MIC GND	NA
MIC1_N	144	AI	Main mic-	NA
MIC1_P	145	AI	Main mic+	NA
Antenna interface				
ANT_TRX	94	I/O	2G/3G/4G main antenna	NA
ANT_DRX	132	AI	Diversity reception antenna	NA
ANT-WIFI/BT	78	AI/AO	WIFI/BT antenna	NA
ANT_GNSS	120	AI	GNSS antenna	NA
Interrupt interface				
ALSP_INT_N	106	DI	Ambient light sensor interrupt	NA
MAG_INT_N	107	DI	Magnetic sensor interrupt	NA
ACCL_INT2_N	108	DI	Accelerometer sensor interrupt	NA
ACCL_INT1_N	109	DI	Accelerometer sensor interrupt	NA
Other interfaces				
FORCE_USB_BOOT	1	DI	Force download	Active high 1.8V, Boot configuration
ADC_IN	128	AI	ADC detection	NA
GPIO interface				
GPIO_12	99	I/O	General Purpose Input and Output.1.8V power domain	B-PD:nppukp
GPIO_13	98	I/O		B-PD:nppukp
GPIO_18	117	I/O		B-PD:nppukp

Pin Name	Pin #	I/O	Pin Description	Note
GPIO_19	118	I/O		B-PD:nppukp
GPIO_25	105	I/O		B-PD:nppukp
GPIO_33	39	I/O		Tuner control
GPIO_34	40	I/O		B-PD:nppukp
GPIO_47	86	I/O		B-PD:nppukp
GPIO_48	219	I/O		B-PD:nppukp
GPIO_59	110	I/O		B-PD:nppukp
GPIO_61	38	I/O		B-PD:nppukp
GPIO_62	111	I/O		B-PD:nppukp
GPIO_63	112	I/O		B-PD:nppukp
GPIO_68	210	I/O		B-PD:nppukp
GPIO_93	96	I/O		B-PD:nppukp
GPIO_97	100	I/O		B-PD:nppukp
GPIO_98	101	I/O		B-PD:nppukp
GPIO_104	103	I/O		B-PD:nppukp
GPIO_106	102	I/O		B-PD:nppukp, Boot configuration
GPIO_116	220	I/O		Tuner control
GPIO_117	221	I/O		Tuner control
GPIO_127	97	I/O		B-PD:nppukp
GPIO_128	104	I/O		B-PD:nppukp
NC Interface				
NC	14, 151, 159, 165, 166, 167, 168, 169, 172, 173, 174, 175, 192, 193, 194, 195,		NC	Keep floating

Pin Name	Pin #	I/O	Pin Description	Note
	198, 199, 200, 201, 202, 203, 211, 212, 216, 217, 223, 225, 226, 227			

Note:

The pin with “Boot configuration” remark cannot be pulled-up externally.

3 Application Interface

3.1 Power Supply

The module provides 3 VBAT pins for connecting to external power supply source. The input range of power is 3.5V~4.2V and the recommended value is 3.8V. The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. In extreme cases, the peak current of the module can reach 3A and if the power supply capacity is insufficient that VBAT transient voltage drop below 3V, the module may be powered off or restarted. The VBAT voltage drop is shown as the following figure:

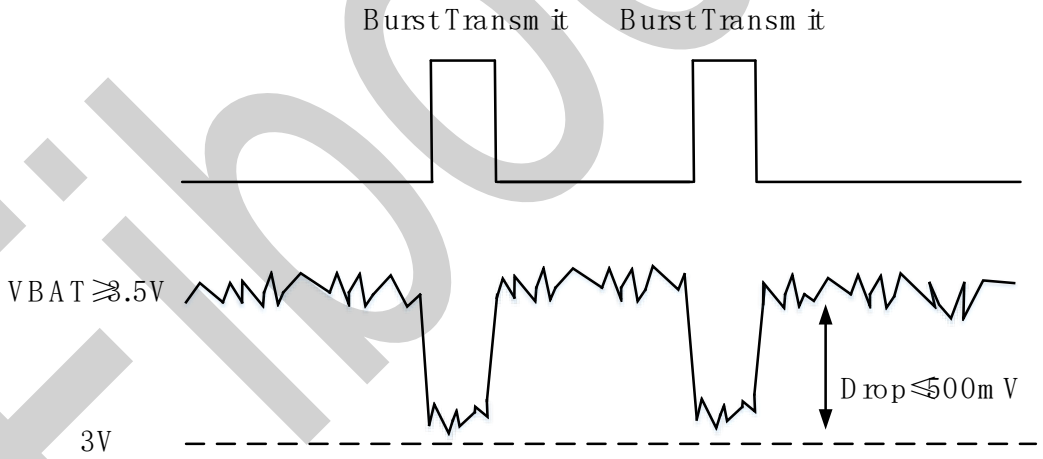

Figure 3-1 VBAT voltage drop

3.1.1 Power Input

External power source supplies the module by VBAT pins. To ensure the power transient voltage is no less than 3V, it is recommended to connect two 220μF tantalum capacitors with low ESR and decoupling capacitors of 1uF, 100nF, 39pF and 33pF in parallel to the VBAT input of the module. Besides the PCB trace of VBAT should as short and wide as possible (wider than 3mm) and the ground plane of the power section should be flat. That can reduce the equivalent impedance of the VBAT trace and ensure at maximum transmit power, significant voltage drop will not occur at high currents.

Table 3-1 Power supply

Parameter	Minimum Value	Recommended Value	Maximum Value	Unit
VBAT (DC)	3.5	3.8	4.2	V

The reference design of power supply is shown as the following figure:

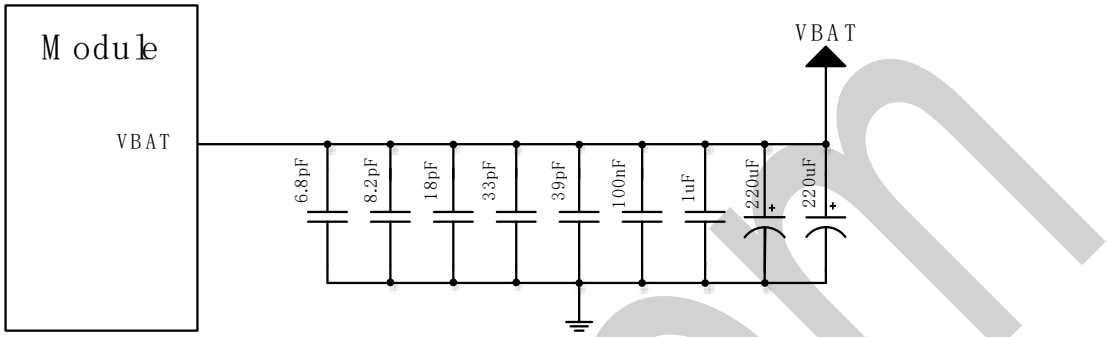

Figure 3-2 Power supply reference design

Table 3-2 Power supply decoupling capacitor design

Recommended Capacitor	Application	Description
220uF x 2	Voltage stabilizing capacitor	To reduce power fluctuations during module operation, it is required to adopt low ESR capacitor. LDO or DCDC power requires not less than 440uF capacitor. Battery power can be properly reduced to 100 ~ 220uF capacitor.
1uF,100nF	Low frequency filter capacitors	Filter clock and digital signal interference.
39pF, 33pF, 18pF, 8.2pF, 6.8pF	Decoupling capacitors	Filter high frequency interference.

3.1.2 VRTC

VRTC is the power supply of the internal RTC clock of the module. When powered on VBAT pin, the VRTC pin will output voltage. When cut off power supply of VBAT and want keep real time clock it needs to be powered by the external power (coin cell for example). The VRTC parameters are as follows:

Table 3-3 VRTC parameter

Parameter	Minimum	Typical	Maximum	Unit
VRTC output voltage	2.5	3.1	3.2	V
VRTC input voltage (clock works well)	2.0	3.0	3.25	V
VRTC input current (clock works well)	-	6	-	uA

The reference design of VRTC pin powered by external power source is shown as the following figure:

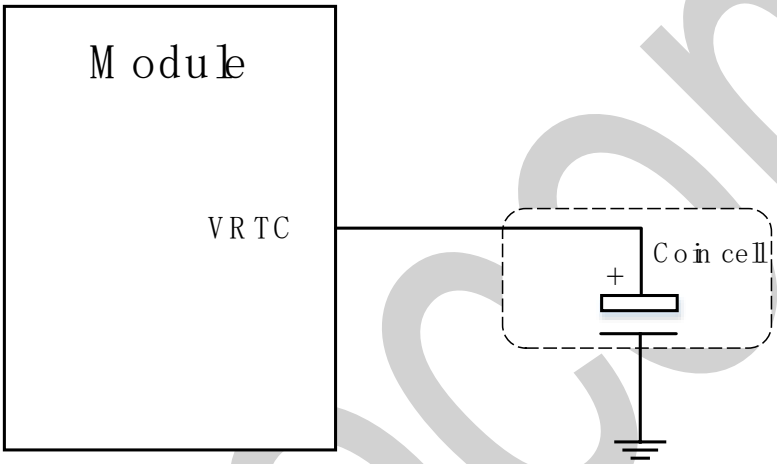

Figure 3-3 VRTC reference design

3.1.3 Power Output

The module provides multiple power outputs for peripheral circuits. It is recommended to connect 33pF and 10pF capacitors in parallel with every power to avoid high frequency interference effectively.

Table 3-4 Power output

Pin Name	Programmable Range (V)	Default Voltage (V)	Drive Current (mA)
VREG_L5_1P8	1.75~3.337	1.8	200
VREG_L6_1P8	1.75~3.337	1.8	150
VREG_L10_2P8	1.75~3.3375	2.8	150
VREG_L11_SDC_PWR	1.75~3.3375	2.95	600
VREG_L14_UIM1	1.75~3.3375	1.8/3	55
VREG_L15_UIM2	1.75~3.3375	1.8/3	55
VREG_L16_2P8	1.750~3.3375	2.8	55
VREG_L17_2P85	1.75~3.3375	2.85	450

3.2 Control Signal

3.2.1 Power On/Off

The module provides one-way power on/off control signal to module's power on/off, restart and sleep/wake up. Its pin definition is shown as follow table：

Table 3-5 Power on/off signal

Pin Name	Pin #	I/O	Description	Note
KEY_PWR_N	123	DI	Active low, can be used to power on/off, restart, sleep/wakeup the module	NA

3.2.1.1 Power On

After module's VBAT pin is powered, pull down KEY_PWR_N pin for 2~8s can trigger module power on. The button control and OC drive power on reference design is shown as follows:

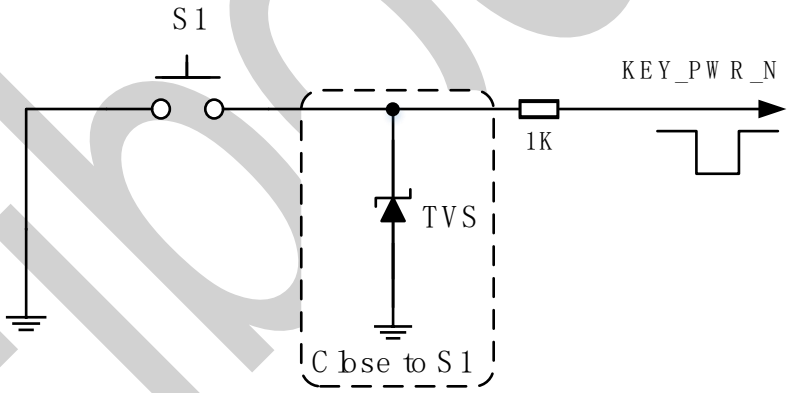

Figure 3-4 Button power on reference design

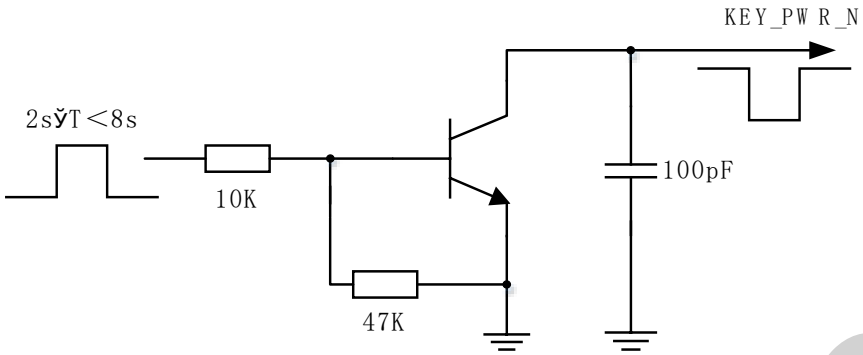

Figure 3-5 OC drive power on reference design

The power on timing is shown as follows:

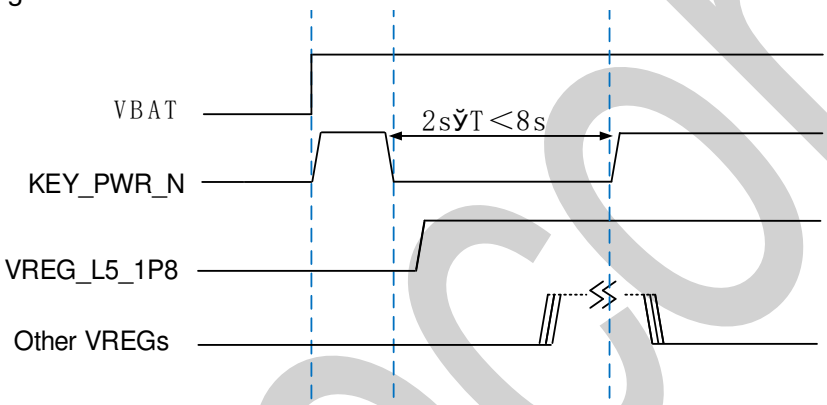

Figure 3-6 Power on timing

3.2.1.2 Power Off

Normal power off: when module in operating mode, pull down KEY_PWR_N 500mS and then release it, user interface will display selection box (select power off or restart).

Force power off: pull down KEY_PWR_N pin for 8~15s module will be forced power off. The power off timing is shown as follows:

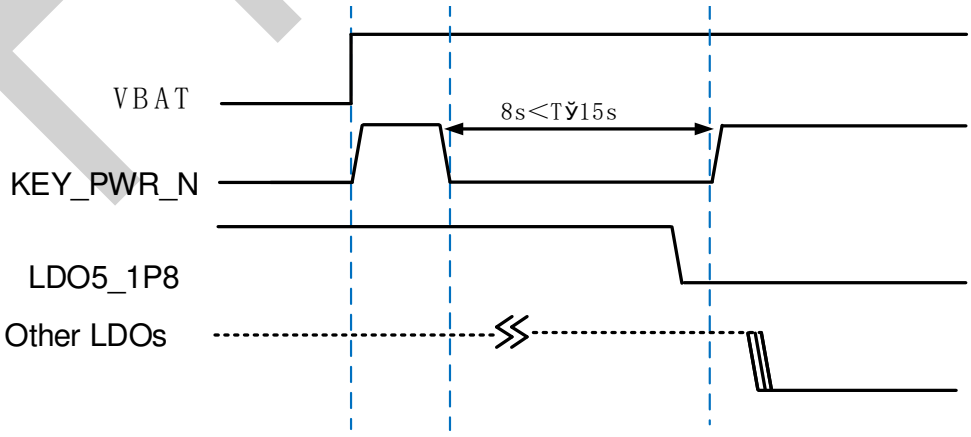

Figure 3-7 Power off timing

Note：

When the system is abnormal or shutdown, can use force power off method to power off the module, please use normal method generally, otherwise may cause data loss and other anomalies.

3.2.1.3 Sleep/Wake up

When module in standby mode, pull down KEY_PWR_N 100mS and then release it, module will enter sleep mode. When module in sleep mode, pull down KEY_PWR_N 100mS and then release it, module can be waked up.

3.2.2 Volume Control

KEY_VOL_DOWN_N and KEY_VOL_UP_N are the volume down and volume up keypads; its circuit design can refer to the power on keypad circuit.

3.3 USB

The module supports one USB 2.0 interface; USB2.0 supports HS (480Mbps) modes and compatible USB1.1 FS (12Mbps). USB supports OTG function and HUB expansion interface; Its pin definition is shown in the following table:

Table 3-6 USB2.0 pin definition

Pin Name	Pin #	I/O	Description	Note
VBUS_USB_IN	8, 9	PI	5V input	NA
USB_DP	12	AI/AO	USB HS data+	NA
USB_ DM	11	AI/AO	USB HS data-	NA
USB_HS_ID	16	DI	USB OTG detection	NA

The reference design of USB2.0 is show as follow figure:

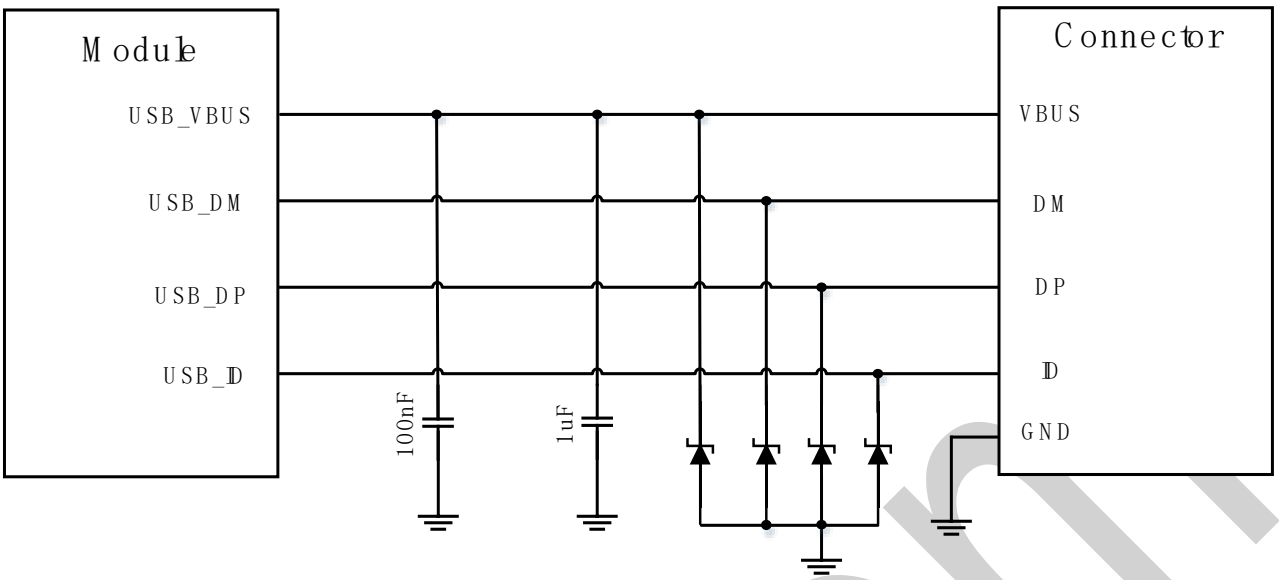

Figure 3-8 USB2.0 reference design

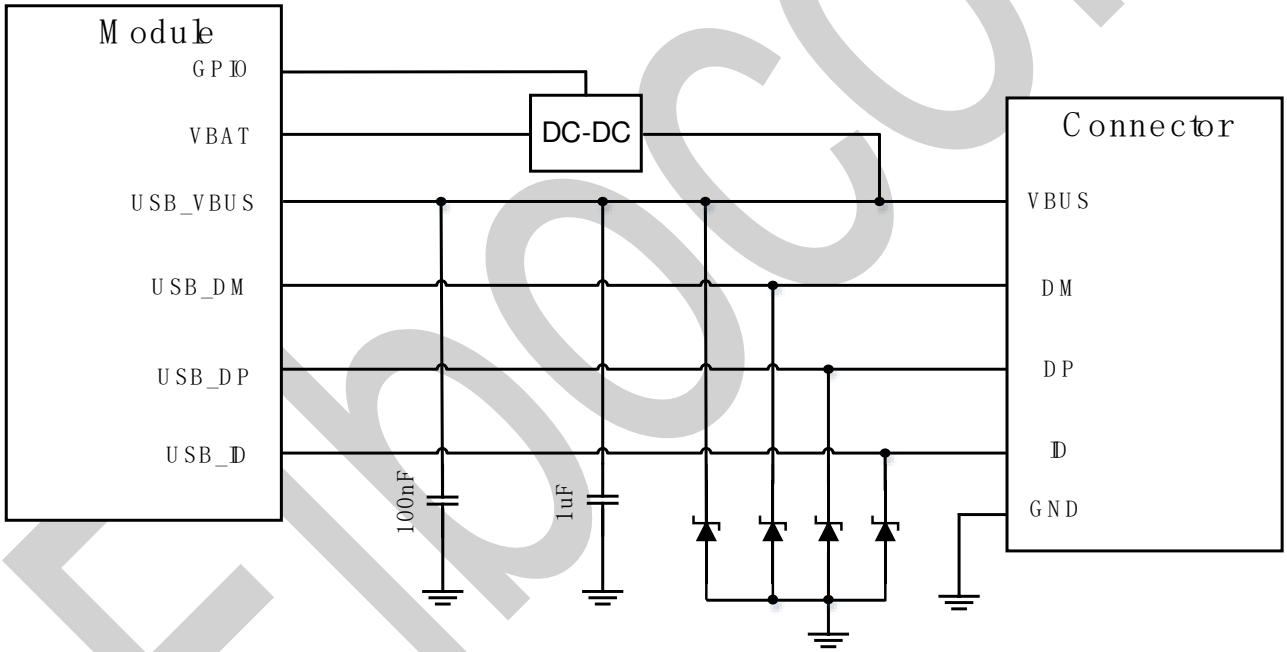

Figure 3-9 USB2.0 reference design (with OTG function)

Note:

1) Please chose junction capacitor less than 1pF for ESD protection device of USB_DP/DM.

2) USB_DP and USB_DM are high-speed differential signal. The highest transmission rate is 480Mbps. Please pay attention to the following requirements in PCB layout:

- USB_DP and USB_DM signal cables are required to be parallel and equal in length (differential cable length controlled within 2mm), while the right-angle route shall be avoided, and differential 90ohms impedance shall be controlled.

- USB2.0 differential signal cable is laid on the signal layer nearest to the ground, with well grounded.

3) Pease choose Boost DC-DC that satisfy output is 5V when support OTG function.

3.4 UART

The module defines three UART ports，all are 1.8V voltage domain. Its pin definition is shown as the following table:

Table 3-7 UART Interface pin definition

Pin Name	Pin #	I/O	Description	Note
UART2_TX	90	DO	UART2 data transmit	Debug serial port
UART2_RX	89	DI	UART2 data receive	
UART6_TX	45	DO	UART6 data transmit	NA
UART6_RX	46	DI	UART6 data receive	NA
UART6_CTS	47	DI	UART6 clear to send	NA
UART6_RTS	48	DO	UART6 request to send	NA
UART5_TX	209	DO	UART5 data transmit	NA
UART5_RX	207	DI	UART5 data receive	NA

All series ports are 1.8V voltage domain, if the peripheral is other voltage domain, please add level shift. level shift reference design is shown as follow figure:

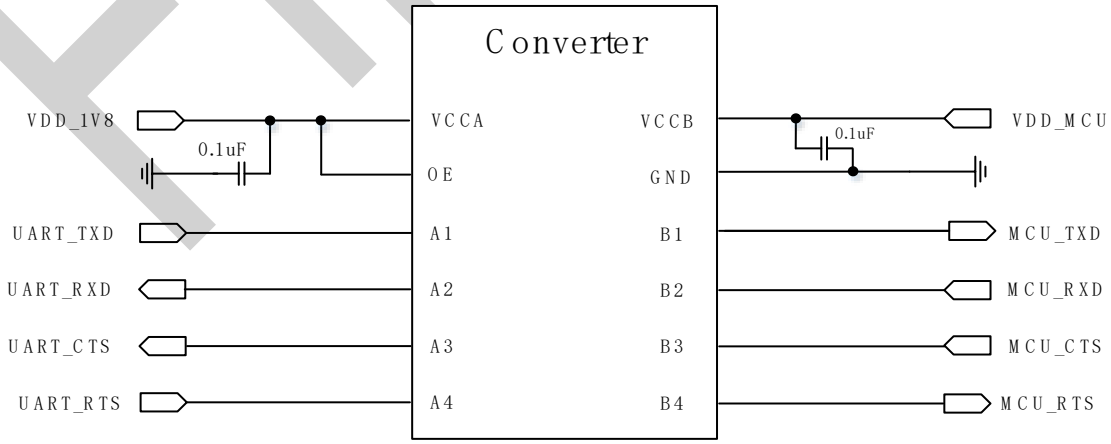

Figure 3-10 Level shift reference design

3.5 SPI

The module provide one master only SPI interface, the pin definition is as follows:

Table 3-8 SPI pin definition

Pin Name		Pin #	I/O	Description	Note
SPI7_CLK		113	DO	SPI clock	NA
SPI7_CS		114	DO	SPI chip select	NA
SPI7_MISO		115	DI	SPI Master input slave output	NA
SPI7_MOSI		116	DO	SPI Master output slave input	NA

3.6 (U)SIM

The module supports two (U)SIM cards, dual-SIM dual-standby single-active and both support hot plug (Disabled by default).

Table 3-9 (U)SIM pin definition

Pin Name	Pin #	I/O	Description	Note
UIM1_DATA	25	I/O	(U)SIM 1 data signal	NA
UIM1_CLK	24	DO	(U)SIM 1 clock signal	NA
UIM1_RESET	23	DO	(U)SIM 1 reset signal	NA
UIM1_DETECT	22	DI	(U)SIM 1 plug detect	Disabled by default
UIM2_DATA	20	I/O	(U)SIM 2 data	NA
UIM2_CLK	19	DO	(U)SIM 2 clock	NA
UIM2_RESET	18	DO	(U)SIM 2 reset	NA
UIM2_DETECT	17	DI	(U)SIM 2 plug detect	Disabled by default
VREG_L14_UIM1	26	PO	(U)SIM 1 power supply	NA
VREG_L15_UIM2	21	PO	(U)SIM 2 power supply	NA

(U)SIM reference design is shown as follow figure:

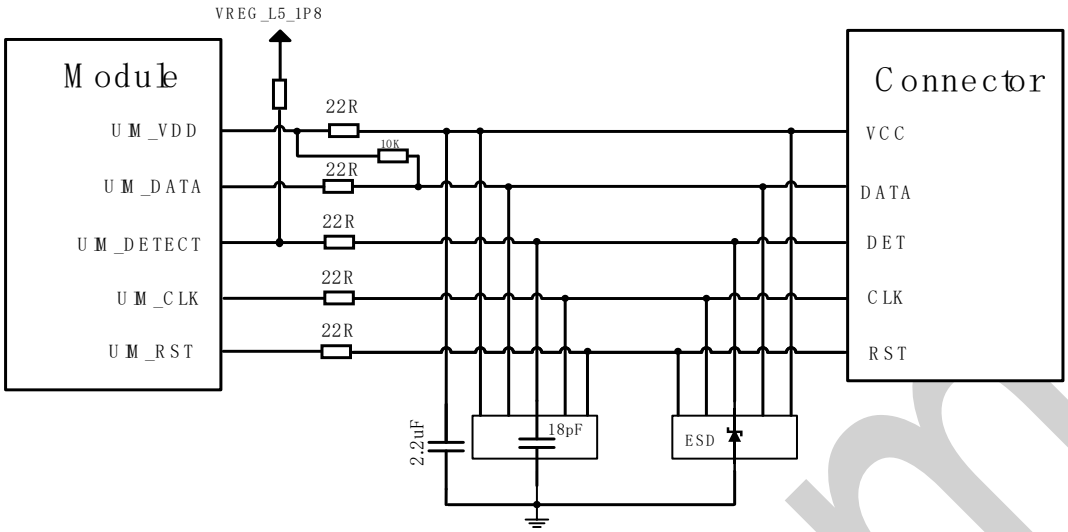

Figure 3-11 (U)SIM reference design

(U)SIM card design notice:

1) The length from the (U)SIM card holder to module should less than 100mm.

2) The layout and routing of the (U)SIM card must be kept away from EMI interference sources such as RF antenna and digital switch power.

3) The decoupling capacitors of the (U)SIM card signal and the ESD device should be placed close to the card holder.

3.7 SDC

The module supports one SDC interface. The pin definition is as follows:

Table 3-10 SDC pin definition

Pin Name	Pin #	I/O	Description	Note
SDC2_DATA3	34	I/O	SD card data interface	NA
SDC2_DATA2	33	I/O	SD card data interface	NA
SDC2_DATA1	32	I/O	SD card data interface	NA
SDC2_DATA0	31	I/O	SD card data interface	NA
SDC2_CLK	29	DO	SD card clock	NA
SDC2_CMD	30	I/O	SD card command	NA
SD_CARD_DET_N	35	DI	SD card detection	NA
VREG_L11_SDC_PWR	28	PO	SD power supply	NA

SDC interface reference design is shown as the following figure:

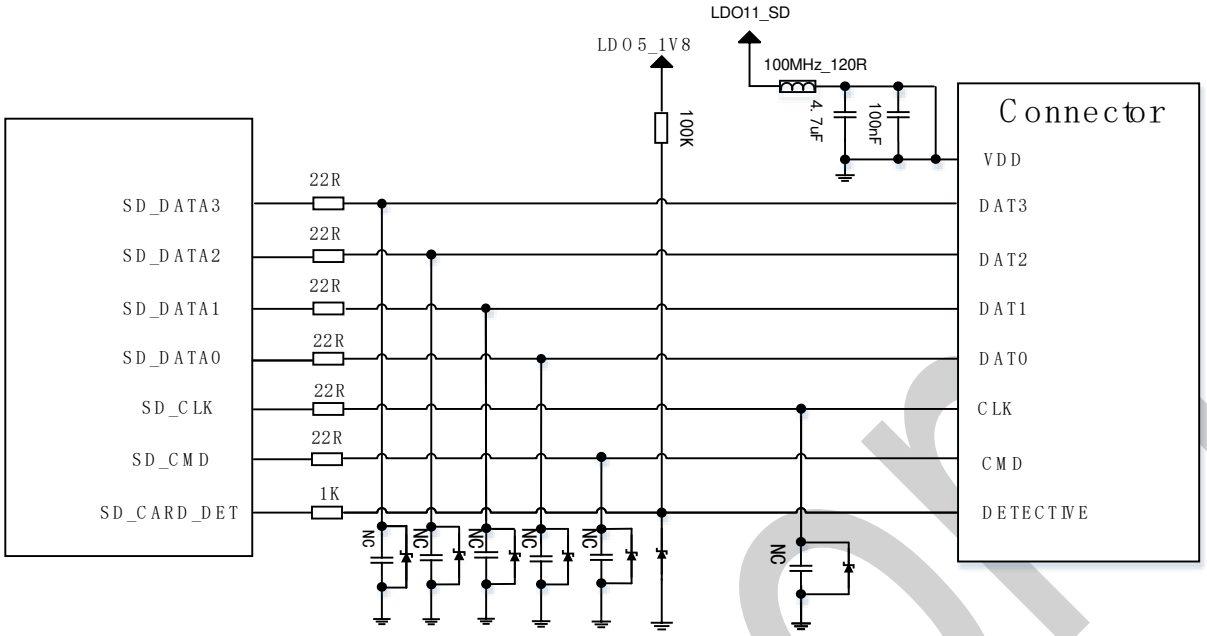

Figure 3-12 SDC reference design

SDC design notice:

1) VREG_L11_SDC_PWR is the SD card peripheral driving power and can provide about 600mA current. Pay attention to controlling the width of trace;

2) Pull up SD_DET with VREG_L5_1P8;

3) SDC is a high-speed digital signal cable, needs to be shielded, and match length on pcb layout.

3.8 GPIO

The module has rich GPIOs resource and the interface level is 1.8V. The pin definition is as follows:

Table 3-11 GPIO list

Pin Name	Pin #	I/O	Description
GPIO_12	99	B-PD:nppukp	YES
GPIO_13	98	B-PD:nppukp	YES
GPIO_18	117	B-PD:nppukp	NO
GPIO_19	118	B-PD:nppukp	NO
GPIO_25	105	B-PD:nppukp	YES
GPIO_33	39	B-PD:nppukp	NO
GPIO_34	40	B-PD:nppukp	YES

Pin Name	Pin #	I/O	Description
GPIO_47	86	B-PD:nppukp	NO
GPIO_48	219	B-PD:nppukp	YES
GPIO_59	110	B-PD:nppukp	YES
GPIO_61	38	B-PD:nppukp	YES
GPIO_62	111	B-PD:nppukp	YES
GPIO_63	112	B-PD:nppukp	YES
GPIO_68	210	B-PD:nppukp	NO
GPIO_93	96	B-PD:nppukp	NO
GPIO_97	100	B-PD:nppukp	YES
GPIO_98	101	B-PD:nppukp	NO
GPIO_104	103	B-PD:nppukp	NO
GPIO_106	102	B-PD:nppukp	NO
GPIO_116	220	B-PD:nppukp	NO
GPIO_117	221	B-PD:nppukp	NO

Note：

B: Bidirectional digital with CMOS input

NP: nppukp = default no-pull with programmable options following the colon (:)

PD: nppukp = default pulldown with programmable options following the colon (:)

PU: nppdkp = default pullup with programmable options following the colon (:)

KP: nppdpu = default keeper with programmable options following the colon (:)

3.9 I²C

The module provides 4 I2C interfaces for TP, camera, sensor, etc. The 4 I2C interfaces are all open-drain outputs, when in use, please pull up to 1.8V power domain with pull-up resistors. The pin definition is shown as the following table:

Table 3-12 I2C pin definition

Pin Name	Pin #	I/O	Description	Note
I2C8_SCL	87	OD	Sensor I2C clock	NA
I2C8_SDA	88	OD	Sensor I2C data	NA

Pin Name	Pin #	I/O	Description	Note
TS_I2C_SCL	41	OD	Main touch panel I2C clock	NA
TS_I2C_SDA	150,158	OD	Main touch panel I2C data	NA
CAM_I2C_SCL	84	OD	Camera I2C clock	CAM use only
CAM_I2C_SDA	85	OD	Camera I2C data	CAM use only
CAM2_I2C_SCL	206	OD	Camera I2C clock	CAM use only
CAM2_I2C_SDA	208	OD	Camera I2C data	CAM use only

Note:

When I2C has more than one peripheral, please ensure the uniqueness of every peripheral address. And do not use multiple devices which are strong real time ones.

3.10 ADC

The module provides one ADC interfaces and its maximum resolution is 15 bits, its pin definition is shown as the following table:

Table 3-13 ADC pin definition

Pin Name	Pin #	I/O	Description	Note
ADC	128	AI	ADC detection pin	Detection voltage range is 0.1V~1.7V(Default) or 0.3V~VBAT

3.11 Battery Power Supply Interface

Table 3-14 Battery interface pin definition

Pin Name	Pin #	I/O	Description	Note
VBAT_ID	2	AI	Battery ID	Connect the pin with GND through 100K resistor
PWR_CHARGE_SEL	124	DI	Charge route select	If choose external charge mode please connect this pin to GND and if choose internal charge keeps it floating

Pin Name	Pin #	I/O	Description	Note
VBAT_SNS	125	AI	Main battery voltage sense	Sampling from VBAT
VBAT_THERM	127	AI	Battery thermistor	Connect the pin with GND through 47K resistor

3.12 Vibration Motor Driver Interface

Table 3-15 Motor driver interface definition

Pin Name	Pin #	I/O	Description	Note
VIB_DRV_N	37	PO	Vibration motor driver	Connect with Vibration motor-

3.13 LCM

The video output of the module support single-screen display; its screen interface is based on MIPI_DSI standard and supports 4 sets of high-speed differential data transmit. Each set support 2.1Gbps speed maximum and supports 720P HD+ maximally.

Table 3-16 LCM pin definition

Pin Name	Pin #	I/O	Description	Note
VREG_L6_1P8	122	PO	LCD IO voltage	For reference, can use external power supply instead
VREG_L17_2P85	130	PO	LCD analog power VDD	
MIPI_DSI0_CLK_P	53	AO	MIPI display serial interface clock+	*NA*
MIPI_DSI0_CLK_N	52	AO	MIPI display serial interface clock-	NA
MIPI_DSI0_LANE0_P	55	AO	MIPI display serial interface Lane0+	*NA*
MIPI_DSI0_LANE0_N	54	AO	MIPI display serial interface Lane0-	*NA*
MIPI_DSI0_LANE1_P	57	AO	MIPI display serial interface Lane 1+	*NA*
MIPI_DSI0_LANE1_N	56	AO	MIPI display serial interface Lane 1-	*NA*
MIPI_DSI0_LANE2_P	59	AO	MIPI display serial interface Lane 2+	NA
MIPI_DSI0_LANE2_N	58	AO	MIPI display serial interface Lane 2-	NA
MIPI_DSI0_LANE3_P	61	AO	MIPI display serial interface Lane 3+	NA

Pin Name	Pin #	I/O	Description	Note
MIPI_DSI0_LANE3_N	60	AO	MIPI display serial interface Lane 3-	NA
LCD_RST_N	49	DO	Main LCD reset	NA
PWM	44	DO	LCD backlight PWM control	NA
LCD_TE	50	DI	LCD tearing effect	NA

The reference design of LCD interface circuit is shown as follows:

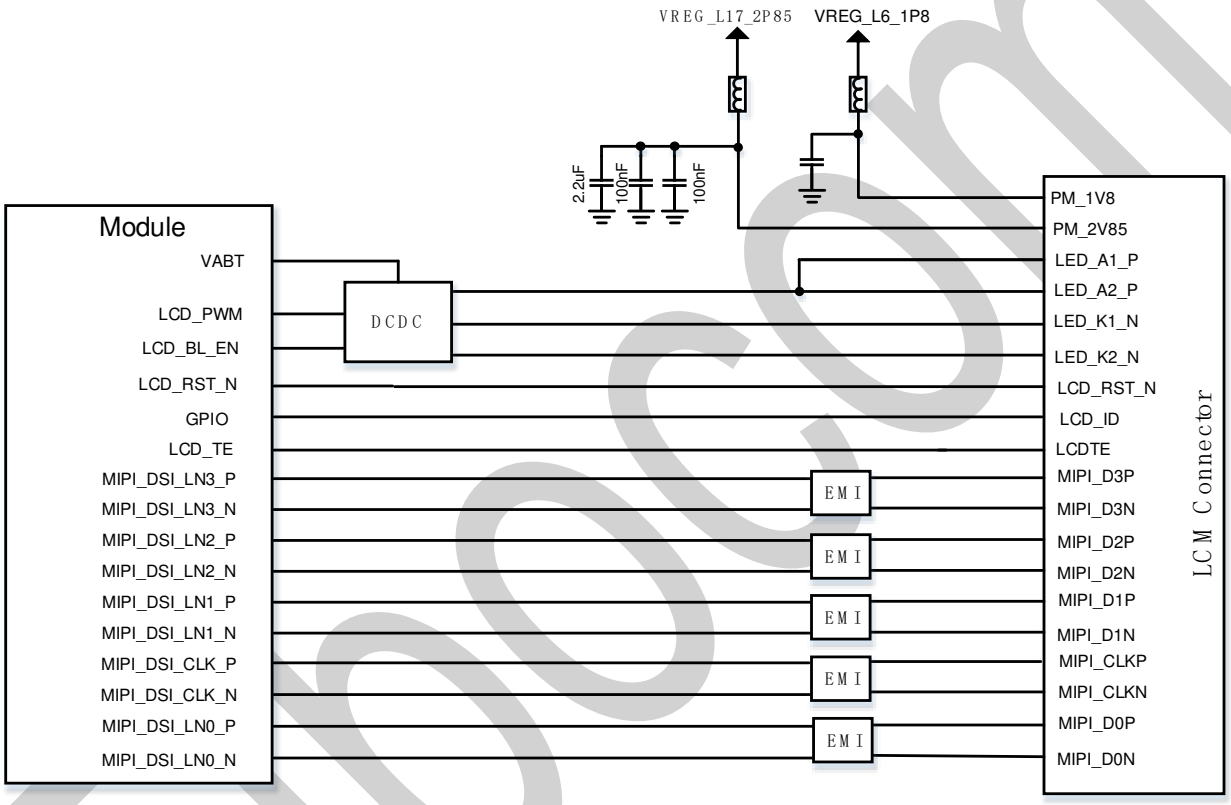

Figure 3-13 LCM reference design

LCM design notice:

1) MIPI is a high-speed signal. It is recommended to connect the common mode inductor in series near the LCD connector to reduce the electromagnetic interference of the circuit;

2) MIPI routing is recommended to be in the inner layer, with three-dimensional grounding;

3) The MIPI signal needs to be controlled with a differential impedance of 100ohms tolerance ±10%;

4) The total length of the trace must not exceed 300mm;

5) The intra lane match of MIPI signal must be controlled within 0.67mm;

6) The inter lane match of MIPI signal must be controlled within 1.3mm;

7) EMI Filters can be unused, the whole routing stray capacitance should be under 1pF;

8) It is recommended that the space of intra lane should be 1.5 times trace width and the differential

cable should keep 3 times trace width from other cables.

3.14 TP

The module provides one I2C interface can be used to connect the touch panel and it provides power, interrupt, reset pins. The pin definition of the module is shown in the following table:

Table 3-17 TP pin definition

Pin Name	Pin #	I/O	Description	Note
TS_INT_N	42	DI	LCD TP interrupt signal	NA
TS_RST_N	43	DO	LCD TP reset signal	NA
VREG_L6_1P8	122	PO	LCD TP IO voltage output	NA
VREG_L17_2P85	130	PO	LCD TP VDD voltage output	NA
TS_I2C_SCL	41	OD	LCD TP I2C clock	NA
TS_I2C_SDA	150,158	OD	LCD TP I2C data	NA

TP reference design circuit is shown as follows:

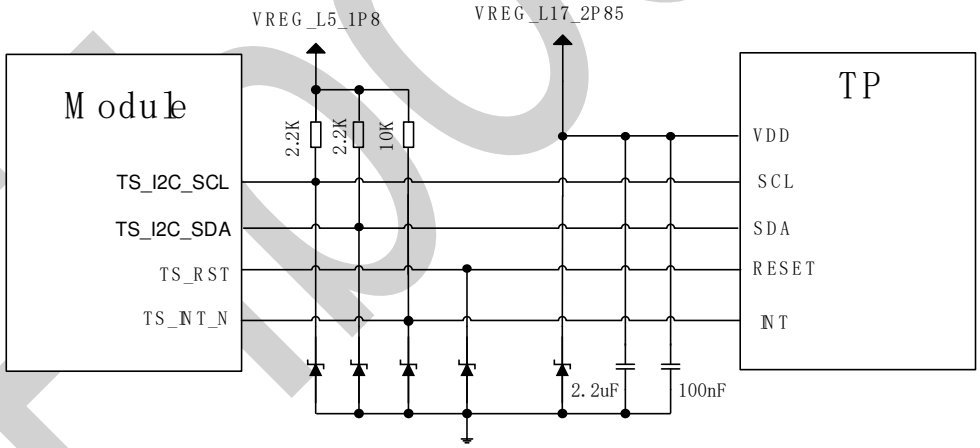

Figure 3-14 TP reference design

3.15 Camera

The camera interface is based on the MIPI_CSI standard and can support two (4 lane+4 lane) or three (4 lane+2 lane+1 lane) cameras (three cameras by default), maximum 13MP. The pin definition of camera interface is shown as the following figure:

Table 3-18 Camera interface pin definition

Pin Name	Pin #	I/O	4 lane+4 lane	4 lane+2 lane+1 lane
VREG_L6_1P8	122	PO	DOVDD power supply	DOVDD power supply
VREG_L16_2P8	222	PO	AVDD supply	AVDD power supply
VREG_L10_2P85	224	PO	Camera focus motor drive AFVDD power supply	Camera focus motor drive AFVDD power supply
MIPI_CSI0_CLK_P	64	AO	MIPI rear camera serial interface clock+	MIPI rear camera serial interface clock+
MIPI_CSI0_CLK_N	63	AO	MIPI rear camera serial interface clock+	MIPI rear camera serial interface clock+
MIPI_CSI0_LANE0_P	66	AI	MIPI rear camera serial interface lane 0+	MIPI rear camera serial interface lane 0+
MIPI_CSI0_LANE0_N	65	AI	MIPI rear camera serial interface lane 0-	MIPI rear camera serial interface lane 0-
MIPI_CSI0_LANE1_P	68	AI	MIPI rear camera serial interface lane 1+	MIPI rear camera serial interface lane 1+
MIPI_CSI0_LANE1_N	67	AI	MIPI rear camera serial interface lane 1-	MIPI rear camera serial interface lane 1-
MIPI_CSI0_LANE2_P	181	AI	MIPI rear camera serial interface lane 2+	MIPI rear camera serial interface lane 2+
MIPI_CSI0_LANE2_N	183	AI	MIPI rear camera serial interface lane 2-	MIPI rear camera serial interface lane 2-
MIPI_CSI0_LANE3_P	180	AI	MIPI rear camera serial interface lane3+	MIPI rear camera serial interface lane3+
MIPI_CSI0_LANE3_N	179	AI	MIPI rear camera serial interface lane 3-	MIPI rear camera serial interface lane 3-
CAM0_MCLK	75	DO	Rear camera master clock	Rear camera master clock
CAM0_RST_N	80	DO	Rear camera reset	Rear camera reset
CAM0_PWD_N	81	DO	Rear camera power down	Rear camera power down
CAM_I2C_SCL	84	OD	Camera I2C clock	Camera I2C clock
CAM_I2C_SDA	85	OD	Camera I2C data	Camera I2C data
MIPI_CSI1_CLK_P	71	AO	MIPI front camera serial interface clock+	MIPI front camera serial interface clock+
MIPI_CSI1_CLK_N	70	AO	MIPI front camera serial interface lane 0-	MIPI front camera serial interface lane 0-
MIPI_CSI1_LANE0_P	73	AI	MIPI front camera serial interface lane 0+	MIPI front camera serial interface lane 0+

Pin Name	Pin #	I/O	4 lane+4 lane	4 lane+2 lane+1 lane
MIPI_CSI1_LANE0_N	72	AI	MIPI front camera serial interface lane 0-	MIPI front camera serial interface lane 0-
MIPI_CSI1_LANE1_P	184	AI	MIPI front camera serial interface lane 1+	MIPI front camera serial interface lane 1+
MIPI_CSI1_LANE1_N	185	AI	MIPI front camera serial interface lane 1-	MIPI front camera serial interface lane 1-
MIPI_CSI1_LANE2_P	186	AI	MIPI front camera serial interface lane 2+	MIPI depth camera serial interface Lane 0+
MIPI_CSI1_LANE2_N	187	AI	MIPI front camera serial interface lane 2-	MIPI depth camera serial interface Lane 0-
MIPI_CSI1_LANE3_P	188	AI	MIPI front camera serial interface lane3+	MIPI depth camera serial interface clock+
MIPI_CSI1_LANE3_N	189	AI	MIPI front camera serial interface lane 3-	MIPI depth camera serial interface clock-
CAM1_MCLK	76	DO	Front camera main clock	Front camera master clock
CAM1_RST_N	82	DO	Front camera reset	Front camera reset
CAM1_PWD_N	83	DO	Front camera power down	Front camera power down
CAM2_I2C_SCL	206	OD	NC	Depth camera I2C clock
CAM2_I2C_SDA	208	OD	NC	Depth camera I2C data
CAM2_MCLK	213	DO	NC	Depth camera master clock
CAM2_RST_N	214	DO	NC	Depth camera reset
CAM2_PWD_N	215	DO	NC	Depth camera power down

3.15.1 Rear Camera

Reference design of rear camera is shown as follows:

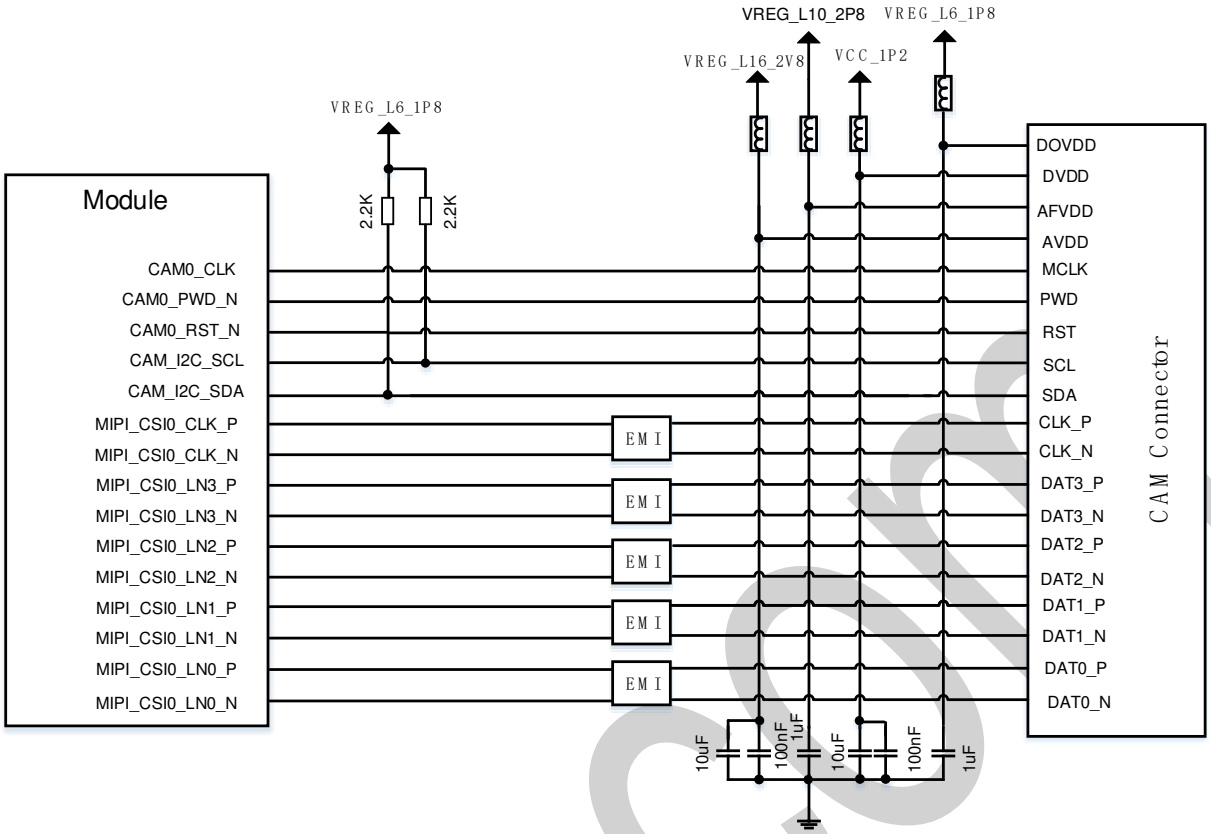

Figure 3-15 Rear camera reference design

Note:

An extra power supply for DVDD is needed.

3.15.2 Front Camera

Reference design of 4 lane front camera is shown as follows:

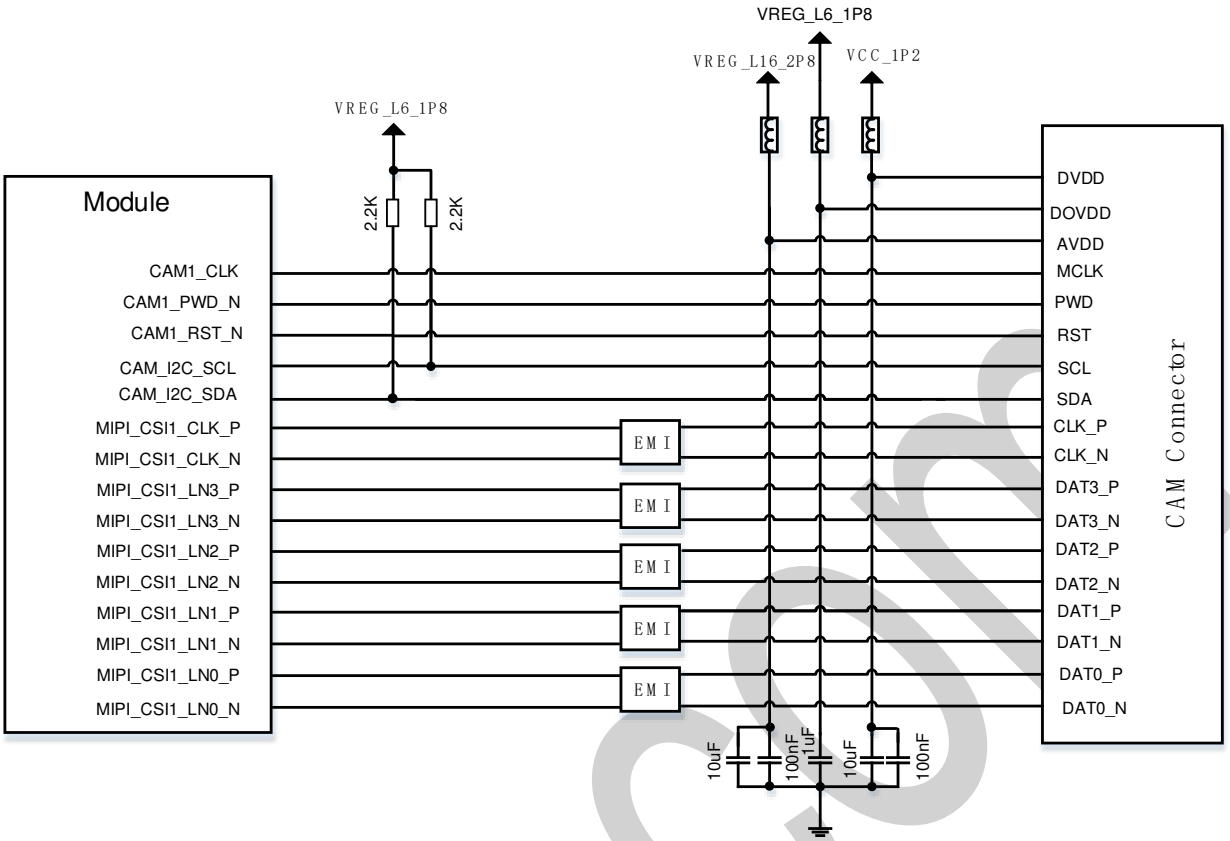

Figure 3-16 4 lane front camera reference design

Reference design of 2-Lane front camera is shown as follows:

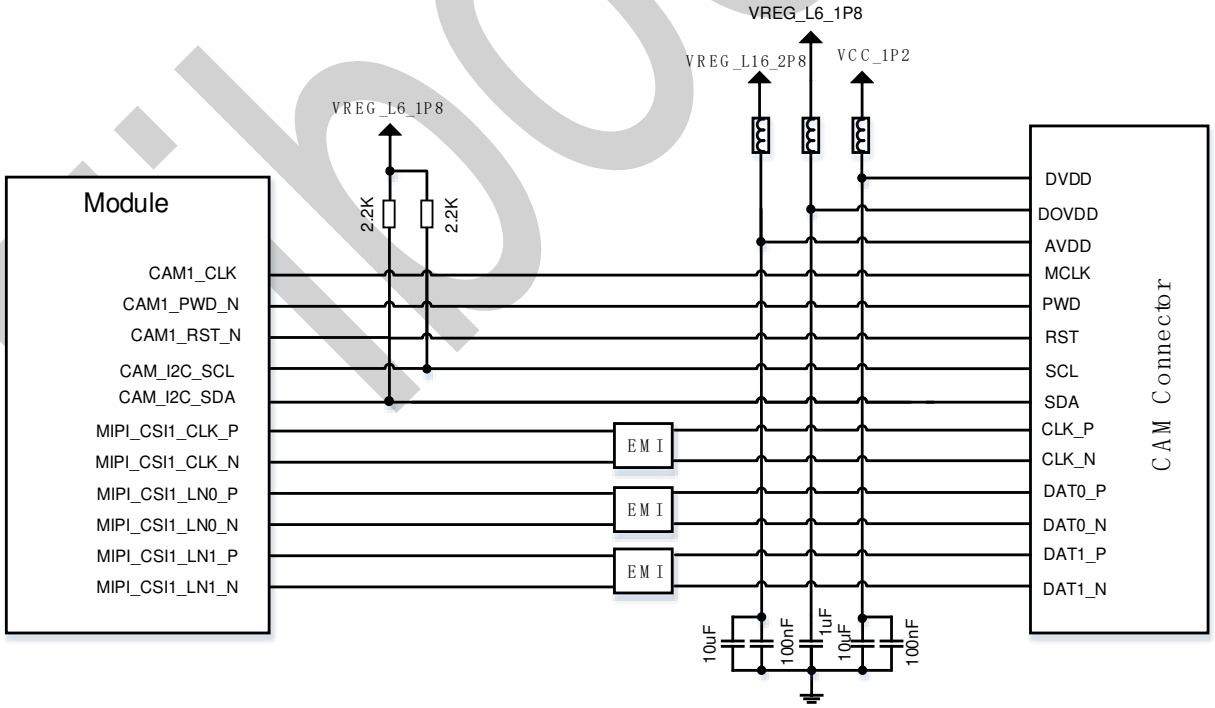

Figure 3-17 2 lane front camera reference design

Note:

An extra power supply for DVDD is needed.

3.15.3 Depth Camera

Pin definition of depth camera is shown as follows:

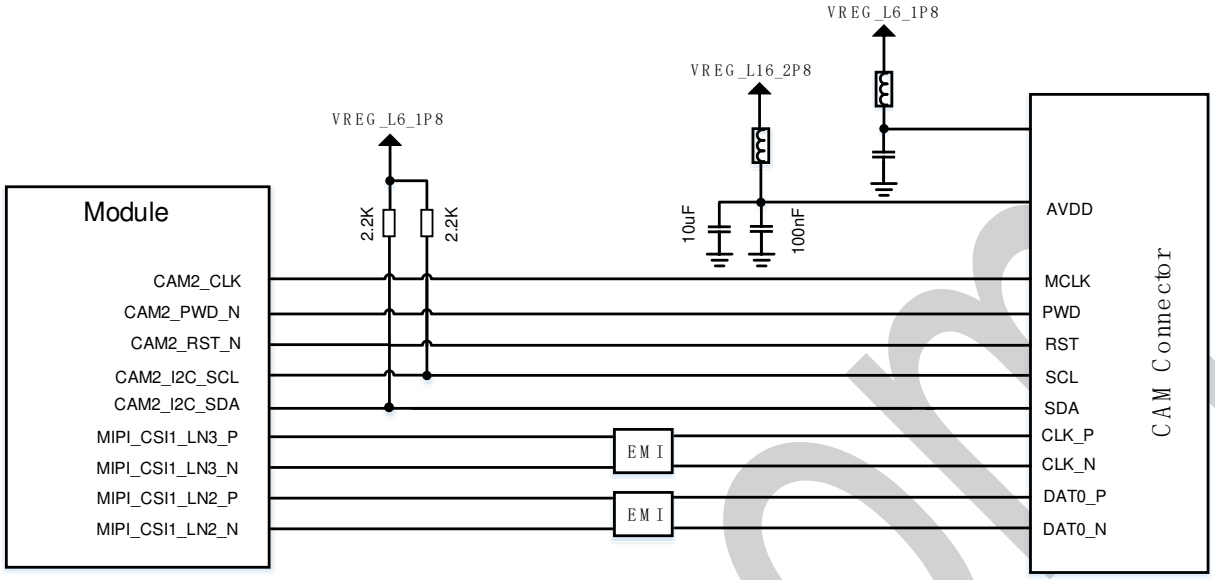

Figure 3-18 Depth camera reference design

3.15.4 Design Notice

MIPI_CSI is a high-speed signal which has relatively high requirement for routing and must be prioritized when PCB layout.

1) MIPI is a high-speed signal. It is recommended to connect the common mode inductor in series near the camera connector to reduce the electromagnetic interference of the circuit;

2) MIPI routing is recommended to be in the inner layer, with three-dimensional grounding;

3) The MIPI signal need to be controlled with a differential impedance of 90ohms and an error of ±10%;

4) The total length of the trace does not exceed 300mm;

5) The intra lane match of MIPI signal must be controlled within 0.67mm;

6) The inter lane match of MIPI signal must be controlled within 1.3mm;

7) It is recommended that the space of intra lane should be 1.5 times trace width and the differential cable should keep 3 times trace width from other cable;

8) CAM_CLK is a high-speed clock signal and requires three-dimensional grounding;

9) The CAM AVDD power supply routing should be away from interference sources, otherwise it is easy to bring interference of power noise;

10)CAM AVDD power supply suggest to add LDO with high PSRR ability;

11) If the front and rear cameras share the I2C, it need to confirm that the I2C addresses of the two cameras do not conflict.

3.16 Sensor

The module supports I2C to communicate with sensors, such as accelerometer sensor, ambient light sensor and magnetic sensor etc.

Table 3-19 Sensor interface pin definition

Pin Name	Pin #	I/O	Description	Note
SENSORS_I2C_SCL	87	OD	I2C clock	NA
SENSORS_I2C_SDA	88	OD	I2C data	NA
ALSP_INT_N	106	DI	Ambient light sensor interrupt	NA
MAG_INT_N	107	DI	Magnetic sensor interrupt	NA
ACCL_INT2_N	108	DI	Accelerometer sensor interrupt	NA
ACCL_INT1_N	109	DI	Accelerometer sensor interrupt	NA

3.17 Audio

The module supports analog audio, and have 2 input 3 output. Pin definition is shown as follows:

Table 3-20 Audio interface pin definition

Pin Name	Pin #	I/O	Description	Note
SPKR_DRV_P	148	AO	Speaker amp+ output	Power consumption 1200mW with 8ohms load
SPKR_DRV_N	147	AO	Speaker amp- output	
CDC_EAR_P	134	AO	Earpiece PA+ output	Power consumption 100mW with 32ohms loads
CDC_EAR_N	135	AO	Earpiece PA- output	
CDC_HPH_L	139	AO	Headphone PA left channel output	NA
CDC_HPH_REF	138	AI	Headphone PA ground sensing	NA
CDC_HPH_R	137	AO	Headphone PA right channel output	NA
CDC_HS_DET	140	AI	Headset detection	NA
MIC2_P	142	AI	Headset mic	NA
GND_MIC	141	AI	Headphone MIC GND	NA
MIC1_N	144	AI	Main mic-	NA
MIC1_P	145	AI	Main mic+	NA

Design notice:

1) The module has MIC bias circuit internally, and no external addition is required;

2) The SPK is configured as class D amplifier output, cannot connect with amplifier externally, it is recommended to connect 8ohms speakers. Note that the route width must meet the power rating requirements; If an external audio amplifier is required, please use the output of headphone as the input of external audio amplifier;

3) The reference ground of the headphone has already grounded in the module. The external circuit is recommended not to be grounded and resistor can be reserved;

4) It is recommended to use earpiece with 32ohms impendence;

5) Reduce noise and improve audio quality, the following approaches are recommended:

- Keep audio PCB routing away from the antenna and high-frequency digital signal;
- Reserve LC filter circuit in audio circuit to reduce EMI;
- Audio routing needs to be masked.

3.17.1 Microphone Circuit Design

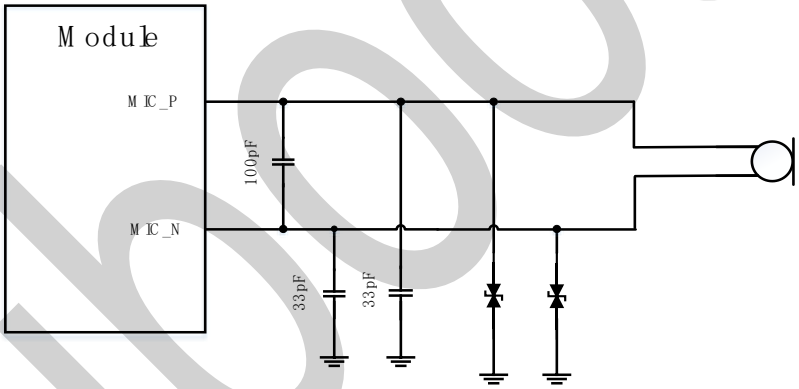

Figure 3-19 Microphone reference design

3.17.2 Earpiece Circuit Design

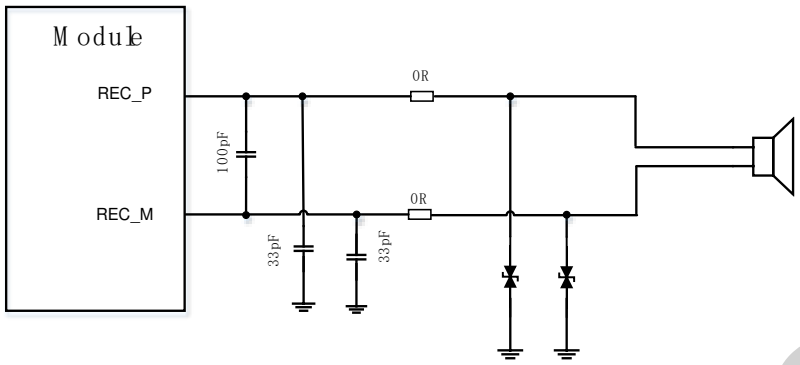

Figure 3-20 Earpiece reference design

3.17.3 Headphone Circuit Design

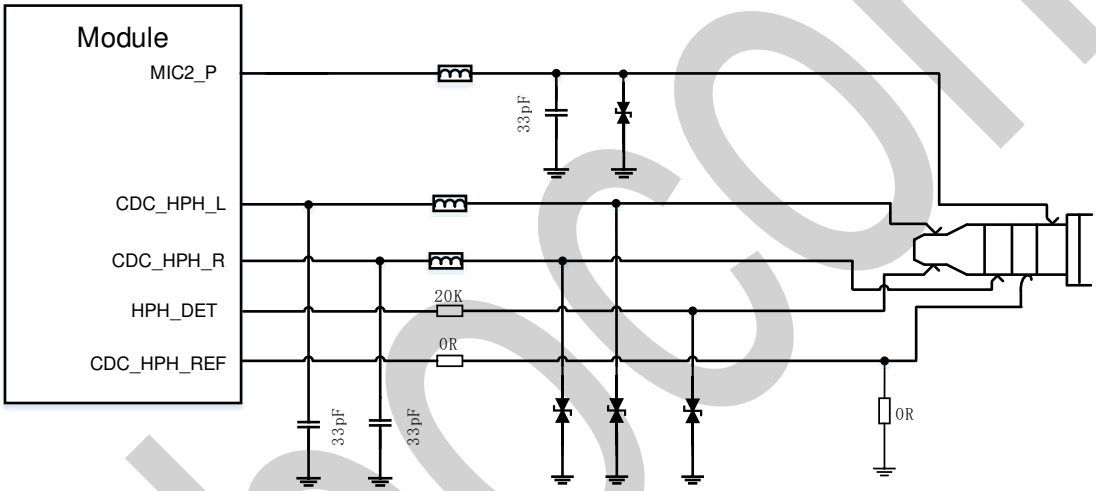

Figure 3-21 Headphone circuit design

Note:

Recommendation TVS for headphone to prevent system level issue, please choose bidirectional device.

3.17.4 Speaker Circuit Design

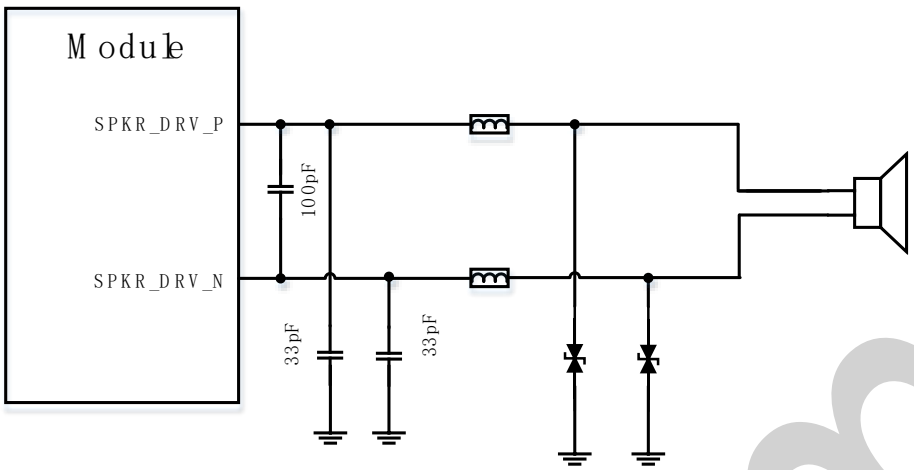

Figure 3-22 Speaker circuit design

3.18 Force Download Interface

The module provides FORCE_USB_BOOT pin as an emergency download interface. Connect the FORCE_USB_BOOT with VREG_L5_1P8 pin when power on, the module can enter the emergency download mode which is used for the final processing mode when the product fails to power on or run normally. To facilitate the subsequent software upgrade and product debugging, please reserve this pin. Reference design is shown as the following figure:

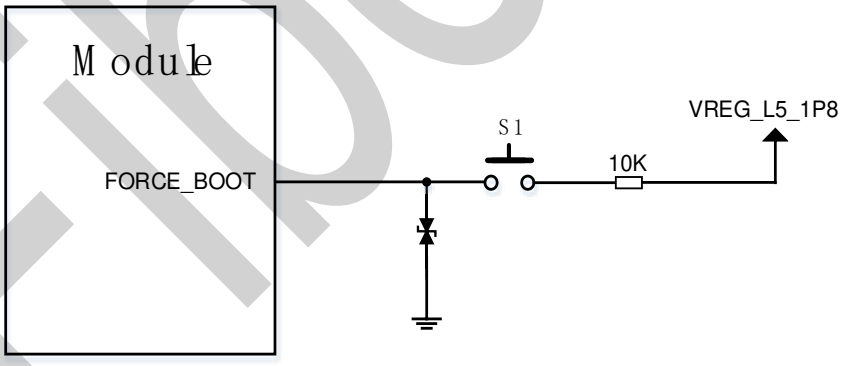

Figure 3-23 Force download reference design

4 Antenna Interface

The module supports 2G/3G/4G main antenna/diversity reception antenna, WIFI/BT antenna and GNSS antenna.

4.1 TRX/DRX Antenna

The module provides two 2G/3G/4G antenna interfaces. The ANT_TRX is used to receive and transmit RF signal, the ANT_DRX is used for diversity reception.

Table 4-1 TRX/DRX antenna interface definition

Pin Name	Pin #	I/O	Description	Note
ANT_TRX	94	AI/AO	2G/3G/4G antenna	NA
ANT_DRX	132	AI	Diversity reception antenna	NA

4.1.1 Operating Band

Table 4-2 Module operating band

Mode	Band	Tx (MHz)	Rx (MHz)
GSM	850	824~849	869~894
	1900	1850~1910	1930~1990
WCDMA	Band 2	1850~1910	1930~1990
	Band 4	1710~1755	2110~2155
	Band 5	824~849	869~894
LTE FDD	Band 2	1850~1910	1930~1990
	Band 4	1710~1755	2110~2155
	Band 5	824~849	869~894
	Band 7	2500~2570	2620~2690
	Band 12	698~716	728~746

Mode	Band	Tx (MHz)	Rx (MHz)
	Band 13	777~787	746~756
	Band 17	704~716	734~746
	Band 25	1850~1915	1930~1995
	Band 26	814~849	859~894
	Band 66	1710~1780	2110~2180
LTE TDD	Band 41	2496~2690	2496~2690

4.1.2 Circuit Reference Design

When use the module, it is necessary to connect the antenna pin with the RF connector or antenna feed point on the main board via an RF trace. Microstrip trace is recommended for RF trace, with insertion loss within 0.2dB and impedance at 50ohms. A π-type circuit is reserved between the module and the antenna connector (or feed point) for antenna debugging. Two parallel components are directly connected across the RF trace and should not pull out a branch, as the figure shows:

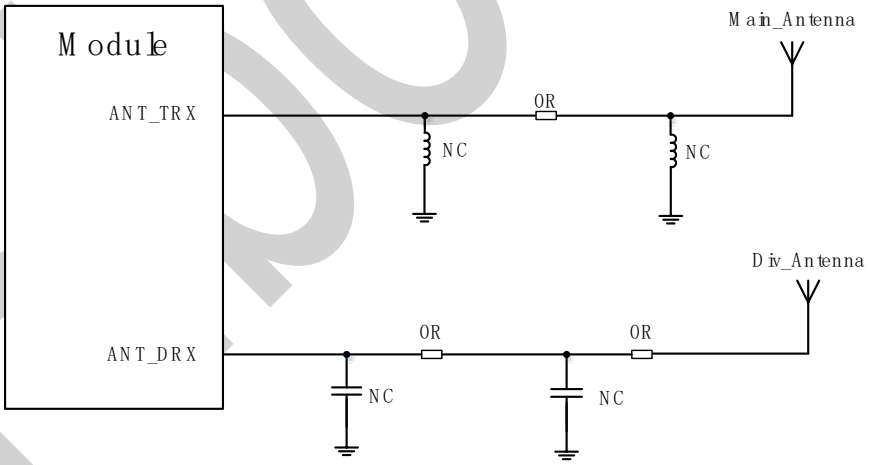

Figure 4-1 TRX/DRX antenna reference design

4.2 WIFI/BT Antenna

Microstrip trace is recommended for the WIFI/BT RF route, with insertion loss within 0.2dB and impedance at 50ohms.

Table 4-3 WIFI/BT antenna interface definition

Pin Name	Pin #	I/O	Description	Note
ANT-WIFI/BT	78	AI/AO	WIFI/BT antenna	NA

4.2.1 Operating Frequency

Table 4-4 WIFI/BT operating frequency

Mode	Frequency	Unit
WIFI	2412-2462	MHz
	5150-5350	MHz
	5470~5850	MHz
BT4.2	2402~2480	MHz

4.2.2 WIFI/BT Antenna Reference Design

WIFI/BT antenna reference design is shown as follows：

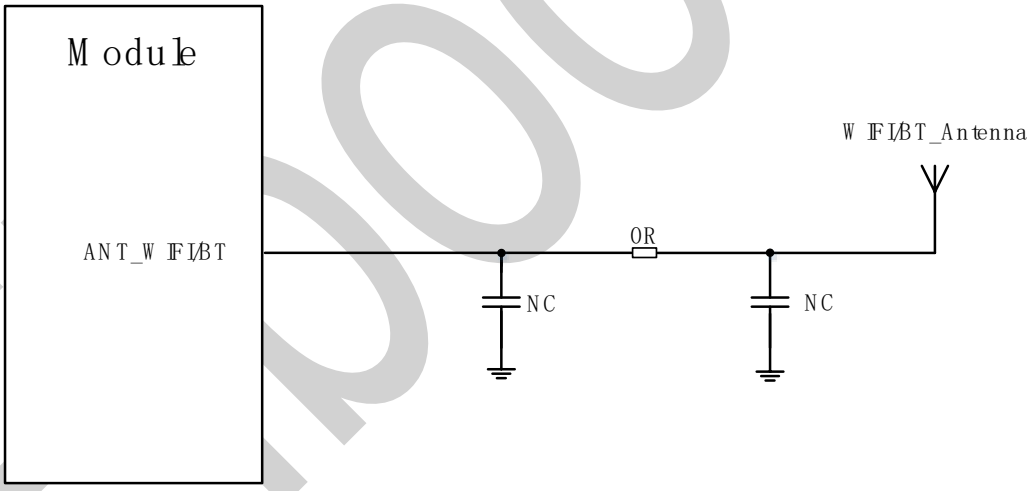

Figure 4-2 WIFI/BT antenna reference design

4.3 GNSS Antenna

GNSS supports GPS.

Table 4-5 GNSS antenna interface definition

Pin Name	Pin #	I/O	Description	Note
ANT_GNSS	120	AI	GNSS antenna	NA

4.3.1 Operating Frequency

Table 4-6 GNSS operating frequency

Mode	Frequency	Unit
GPS	1575.42±1.023	MHz

4.3.2 GNSS Antenna Reference Design

The module has a built-in LNA. The passive antenna is used in the design of the device.

Microstrip trace is recommended for the GNSS RF route, with insertion loss within 0.2dB and impedance at 50ohms.

The GNSS antenna reference design is shown as follows:

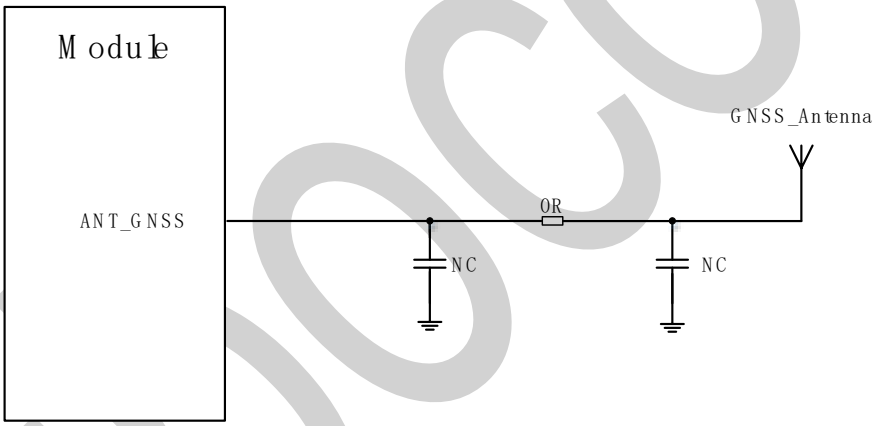

Figure 4-3-1 GNSS passive antenna reference circuit

The active antenna reference circuit is shown in the following figure:

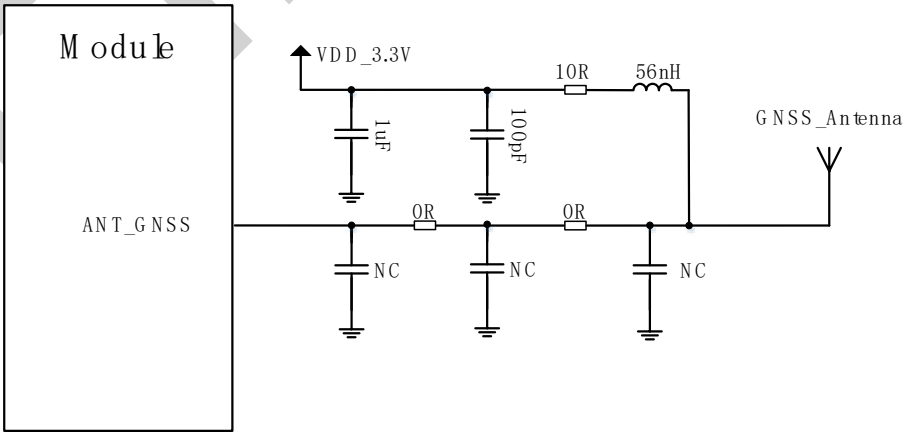

Figure 28-2 GNSS active antenna connection diagram

The power of the active antenna is fed from the antenna's signal line through a 56nH inductor. Common active antennas supply power from 3.3V to 5.0V. The active antenna itself consumes very little power, but requires a stable and clean power supply. It is recommended that a high-performance LDO be used to power the antenna. The active antenna gain requirement is <17db. If the gain is> 17db, the reserved π-type matching needs to be used to increase the attenuation network.

4.4 Antenna Requirement

The module provides four antenna interfaces: main, diversity, WIFI/BT and GNSS. The antenna requirements are as follows:

Table 4-7 Antenna requirements

Module Antenna Requirements	
Standard	**Antenna requirements**
GSM/WCDMA /LTE	VSWR: ≤ 2 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB (0.6-1GHz) Insertion loss: < 1.5dB(1.4-2.2GHz) Insertion loss: < 2dB (2.3-2.7GHz)
WIFI/BT	VSWR: ≤ 2 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB
GNSS	Frequency range: 1559MHz~1607MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical) gain: 2 dBi

5 RF PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal traces should be within 50ohms. In general, the impedance of the RF signal trace is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually in two ways: microstrip trace and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip trace and coplanar waveguide when the impedance cable is at 50ohms.

- Microstrip trace entirety structure

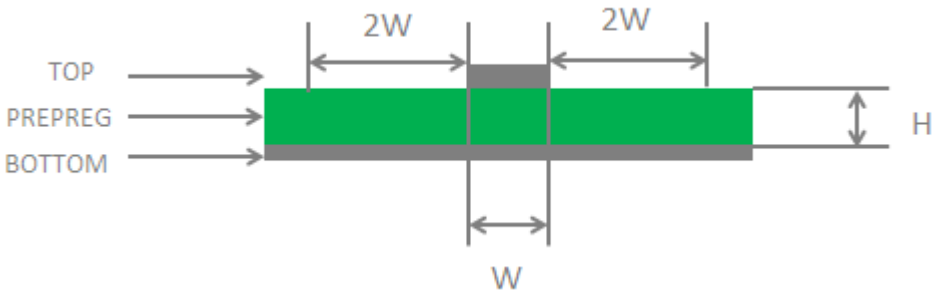

Figure 5-1 Two-layer PCB microstrip cable structure

- Coplanar waveguide entirety structure

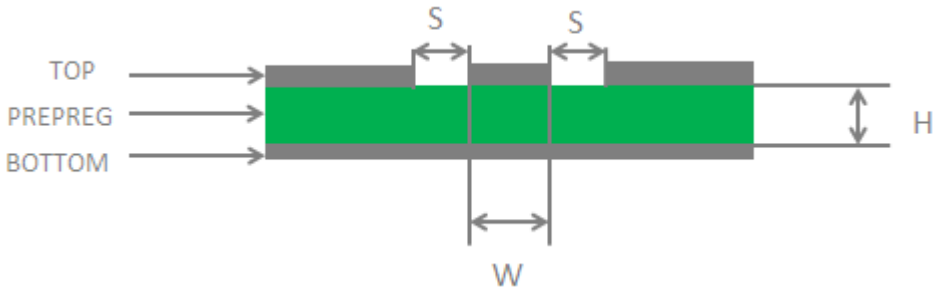

Figure 5-2 Two-layer PCB coplanar waveguide structure

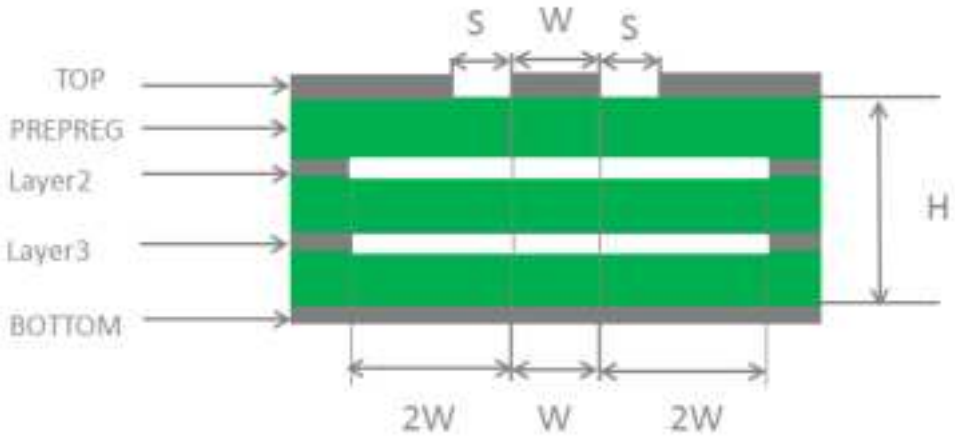

Figure 5-3 Four-layer PCB coplanar waveguide structure (reference ground layer3)

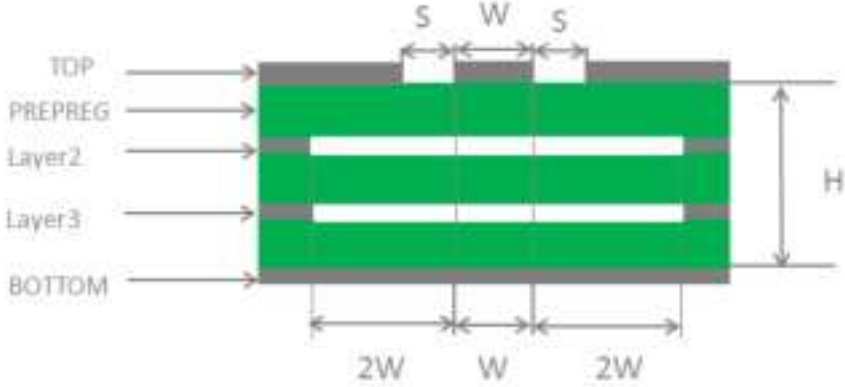

Figure 5-4 Four-layer PCB coplanar waveguide structure (reference ground layer4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

- The impedance simulation tool should be used to accurately control the RF signal cable at 50ohms impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135 degree.
- Attention should be paid to the establishment of the component package and the signal pin should be kept at a certain distance from the ground.
- The reference ground plane of the RF signal trace should be entirety; adding a certain amount of ground holes around the signal and the reference ground can help improve the RF performance; the distance between the ground hole and the signal trace should be at least 2 times the trace width (2*W).

6 WIFI and Bluetooth

6.1 WIFI Overview

The module supports 2.4G and 5G WLAN wireless communications and 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac standards, with a maximum speed up to 433Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40 (If you need to open 2.4G WIFI 40M, you need to configure the ini file, it is not recommended to use)
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 WIFI Performance

Test condition：3.8V power supply, environment temperature 25°C

Table 6-1 WIFI transmit power

Frequency	Mode	Date Rate	Bandwidth(MHz)	TX Power(dBm)
2.4G	802.11b	1Mbps	20	17.0±3
		11Mbps	20	17.0±3
	802.11g	6Mbps	20	16.0±3
		54Mbps	20	13.0±3
	802.11n	MCS0	20	15.0±3
		MCS7	20	12.0±3
		MCS0	40	15.0±3
		MCS7	40	12.0±3

Frequency	Mode	Date Rate	Bandwidth(MHz)	TX Power(dBm)
5G	802.11a	6Mbs	20	19.0±3
		54Mbps	20	16.0±3
	802.11n	MCS0	20	18.0±3
		MCS7	20	15.0±3
		MCS0	40	17.0±3
		MCS7	40	14.0±3
	802.11ac	MCS0	20	17.0±3
		MCS8	20	14.0±3
		MCS0	40	16.0±3
		MCS9	40	13.0±3
		MCS0	80	15.0±3
		MCS9	80	12.0±3

Table 6-2 WIFI RX sensitivity

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity(dBm) 2)
2.4G	802.11b	1Mbps	20	-92.0
		11Mbps	20	-88.0
	802.11g	6Mbps	20	-89.0
		54Mbps	20	-72.0
	802.11n	MCS0	20	-85.0
		MCS7	20	-70.0
		MCS0	40	-82.0
		MCS7	40	-67.0
5G	802.11a	6Mbps	20	-89.0

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity(dBm) 2)
		54Mbps	20	-72.0
	802.11n	MCS0	20	-86.0
		MCS7	20	-70.0
		MCS0	40	-83.0
		MCS7	40	-67.0
	802.11ac	MCS0	20	-88.0
		MCS8	20	-66.0
		MCS0	40	-85.0
		MCS9	40	-61.0
		MCS0	80	-82.0
		MCS9	80	-55.0

Note:

2) The sensitivity here is a typical value

6.3 Bluetooth Overview

The module supports BT4.2 (BR/EDR+BLE) standards. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK.BR/EDR. Channel bandwidth is 1MHz and can accommodate 79 channels. The BLE channel bandwidth is 2MHz and can accommodate 40 channels. Its main features are as follows:

- BT 4.2+BR/EDR+BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 6-3 BT rate and version information

Version	Date Rate	Throughput	Note
BT1.2	1Mbit/s	> 80Kbit/s	NA

Version	Date Rate	Throughput	Note
BT2.0+EDR	3Mbit/s	> 80Kbit/s	NA
BT3.0+HS	24Mbit/s	Refer to 3.0+HS	NA
BT4.2 LE	24Mbit/s	Refer to 4.2 LE	NA

6.4 Bluetooth Performance

Table 6-4 BT performance index

Type	DH-5	2-DH5	3-DH5	Unit
Transmitter	10±2.5	9±2.5	8±2.5	dBm
Sensitivity	-88	-88	-84	dBm

7 GNSS

7.1 Overview

The smart module supports multiple positioning systems including GPS. The module is embedded with LNA which can effectively improve the sensitivity of GNSS.

7.2 GNSS Performance

Test condition：3.8V power supply, environment temperature 25°C.

Table 7-1 GNSS positioning performance

Parameter	Description	Type Result	Unit
Sensitivity	Acquisition	-145	dBm
	Tracking	-156	dBm
C/N	-130dBm	39	dB-Hz
TTFF	Cold Start	44	s
	Warm Start	40	s
	Hot Start	2.5	s
CEP	Static accuracy(95%@-130dBm)	5	m

8 Electrical, Reliability and RF Performance

8.1 Recommended Parameters

Table 8-1 Recommended Parameters

Parameter	Min	Normal	Max	Unit
VBAT	3.5	3.8	4.2	V
USB_VBUS	4.75	5	5.25	V
VRTC	2.0	3.0	3.25	V
Operating Temperature	-25	25	75	℃
Storage Temperature	-40	25	85	℃

8.2 Power Consumption

Test condition：3.8V power supply, environment temperature 25°C

Table 8-2 Power consumption

Parameter	Description	Condition	Typical	Unit
I_{off}	Power Off	Power Off	15	uA
I_{sleep}	GSM	MFRMS=5	3.6	mA
	WCDMA	DRX=8	3.6	
	TDD LTE	DPC (Default Paging Cycle) =#256	3.6	
	FDD LTE	DPC (Default Paging Cycle) =#256	3.9	
	Radio Off	AT+CFUN=4 Flight Mode	2.6	
$I_{GSM-RMS}$	GSM voice RMS Current	GSM850@ PCL=5	260	mA
		GSM850@ PCL=19	104	
		PCS1900@ PCL=0	205	
		PCS1900@ PCL=15	99	
$I_{GSM-MAX}$	GSM voice	PCS1900@ PCL=0	1550	mA
$I_{GPRS-RMS}$	GPRS data RMS Current	GSM850@Gamma=3（1UL/1DL）	252	mA
		GSM850@Gamma=3（4UL/1DL）	530	
		PCS1900@Gamma=3（1UL/1DL）	196	
		PCS1900@Gamma=3（4UL/1DL）	478	

$I_{EGPRS-RMS}$	EGPRS data RMS Current	GSM850@Gamma=6（1UL/1DL）	170	mA
		GSM850@Gamma=6（4UL/1DL）	478	
		PCS1900@Gamma=5（1UL/1DL）	188	
		PCS1900@Gamma=5（4UL/1DL）	466	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band2@ max power	625	mA
		Band4@ max power	570	
		Band5@ max power	595	
$I_{LTE-RMS}$	FDD data RMS Current	Band2@max power(10MHz,1RB)	650	mA
		Band4@max power(10MHz,1RB)	660	
		Band5@max power(10MHz,1RB)	695	
		Band7@max power(10MHz,1RB)	755	
		Band12@max power(10MHz,1RB)	630	
		Band13@max power(10MHz,1RB)	660	
		Band17@max power(10MHz,1RB)	630	
		Band25@max power(10MHz,1RB)	640	
		Band26@max power(10MHz,1RB)	640	
		Band66@max power(10MHz,1RB)	650	
	TDD data RMS Current	Band41@max power(10MHz,1RB)	425	

Note:

NV947 need be changed to 0 when using white card to test sleep current.

8.3 RF Transmit Power

The transmit power of each band of the module is shown in the following table:

Test condition：3.8V power supply, environment temperature 25°C, LTE 10M 12RB

Table 8-3 RF transmit power

Mode	Band	Max Power(dBm)	Min Power(dBm)
GSM	850（GMSK）	32.5±1	5±5
	1900（GMSK）	29.5±1	0±5

Mode	Band	Max Power(dBm)	Min Power(dBm)
GSM	850（8PSK）	24+4/-5	5±5
	1900（8PSK）	23+4.5/-5	0±5
WCDMA	Band 2	23.5±1	< -49
	Band 4	23.5±1	< -49
	Band 5	23.5±1	< -49
LTE FDD	Band 2	23±1	< -39
	Band 4	23±1	< -39
	Band 5	23±1	< -39
	Band 7	23±1	< -39
	Band 12	23±1	< -39
	Band 13	23±1	< -39
	Band 17	23±1	< -39
	Band 25	23±1	< -39
	Band 26	23±1	< -39
	Band 66	23±1	<-39
LTE TDD	Band 41	23±1	<-39

8.4 RF Receiver Sensitivity[3)]

The sensitivity of each frequency band of the module is shown in the following table:

Test condition：3.8V power supply, environment temperature 25°C. LTE sensitivity test bandwidth 10M, RB configuration reference 3gpp.

Table 8-4 RF receiver sensitivity

Mode	Band	Main	DIV	Main+DIV	3GPP Requirement	Unit
GSM	850	-109	-109	-111	-102	dBm
	1900	-107.5	-108	-110.5	-102	dBm
WCDMA	Band II	-109	-110.5	-112.5	-104.7	dBm
	Band IV	-109	-110	-112	-106.7	dBm
	Band V	-110	-110.5	-113	-104.7	dBm
LTE-FDD (10M)	Band 2	-98	-98.5	-101	-94.3	dBm
	Band 4	-96.5	-98	-99	-96.3	dBm
	Band 5	-98	-98	-101	-94.3	dBm
	Band 7	-96.5	-96	-100.5	-94.3	dBm
	Band 12	-97.5	-98.5	-100.5	-93.3	dBm
	Band 13	-97.5	-98.5	-100.5	-93.3	dBm
	Band 17	-97.5	-98.5	-100.5	-93.3	dBm
	Band 25	-98	-98	-101	-92.8	dBm
	Band 26	-97.5	-98	-100.5	-93.8	dBm
	Band 66	-96.5	-98	-99.5	-96.3	dBm
LTE-TDD (10M)	Band 41	-95	-95.5	-98.5	-94.3	dBm

Note：

3) The sensitivity here is a typical value

8.5 Electrostatic Protection

In the application of the module, due to static electricity generated by human body and charged friction between micro-electronics, etc. discharging to the module through various channels that may cause damage, so ESD protection should be taken seriously attention. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added at the designed circuit interface and the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production. ESD performance parameters shown as the following table (Temperature: 25°C, Humidity: 45%~65%)

Table 8-5 ESD performance

Test Point	Contact Discharge	Air Discharge	Unit

VBAT, GND	±5	±10	KV
Antenna interface	±4	±8	KV
Other interface	±0.5	±1	KV

9 Structural Specification

9.1 Product Appearance

The module product appearance is shown in the figure:

Figure 9-1 Module product appearance

9.2 Structural Dimension

The structural dimension of the module is shown in the following figure:

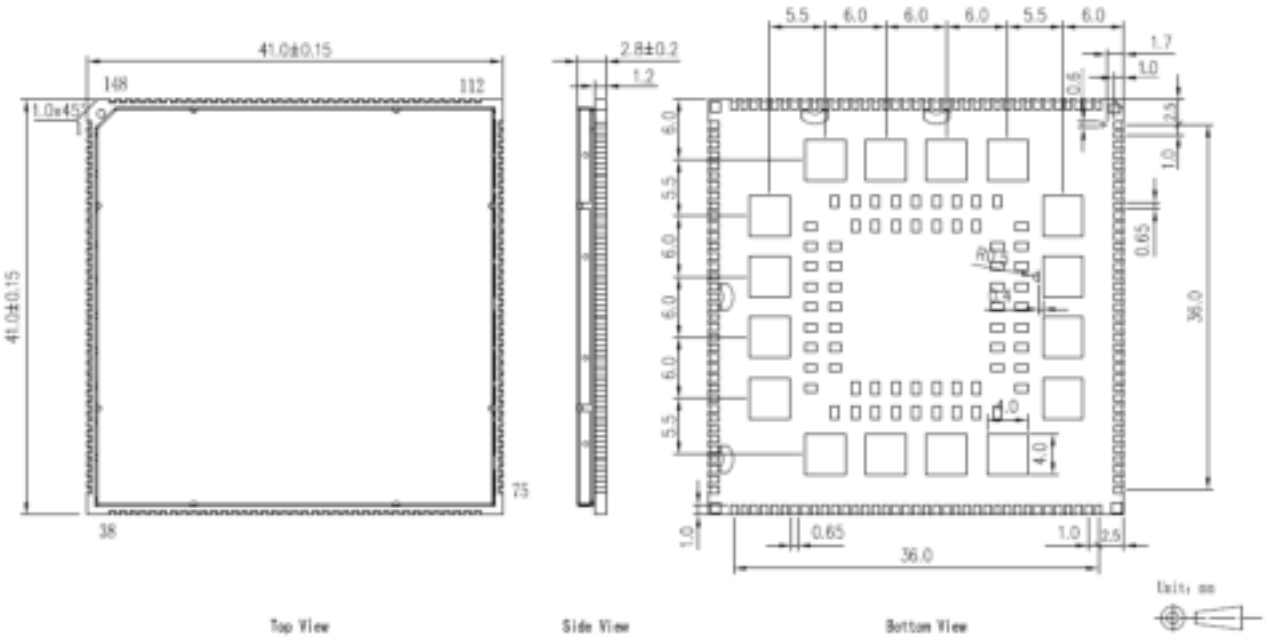

Figure 9-2 Structural dimension

9.3 PCB Soldering Pad and Stencil Design

PCB soldering pad and stencil design please refer to *FIBOCOM SQ808 SMT Design Guide.*

10 Production and Storage

10.1 SMT

SMT production process parameters and related requirements please refer to *FIBOCOM SQ808 SMT Design Guide*.

10.2 Carrier and Storage

Carrier and storage please refer to *FIBOCOM SQ808 SMT Design Guide*.

11 Appendixes

A. Terms and Acronyms

Table 11-1 Terms and acronyms

Term	Definition
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly PolarizedRMS
RMS	Root Mean Square

Term	Definition
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
DVDD	Digital voltage for cameras

B. GPRS Encoding Scheme

Table 11-2 GPRS encoding scheme

Encoding Method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

C. GPRS Multislot

In the GPRS standard, 29 types of GPRS multislot modes are defined and can be used by mobile stations. The multislot class defines the maximum rate of uplink and downlink. The expression is 3+1 or 2+2, the first number represents the number of downlink timeslots and the second number represents the number of uplink timeslots. Active timeslot represents the total number of timeslots that the GPRS device can use for both uplink and downlink communications.

Table 11-3 Multilevel multislot allocation

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
33	5	4	6

D. EDGE Modulation and Encoding Method

Table 11-4 EDGE modulation and encoding method

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.6kbps	35.2kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps