

GX1255S Circuit Description

Reception and transmission are switched by “RX-CNTL” and “TX-CNTL” lines from the CNTL Unit. The receiver uses double-conversion superheterodyne circuitry, with a 21.4 MHz 1st IF and 450 kHz 2nd IF. The 1st local is produced by a PLL synthesizer, yielding the 21.4 MHz 1st IF. The 2nd local uses a 21.850 MHz crystal oscillator, yielding the 450 kHz 2nd IF. The 2nd mixer and other circuits use a custom IC to convert and amplify the 2nd IF and detect FM to obtain demodulated signals. During transmit, the PLL synthesizer oscillates at the desired frequency directly, for amplification to obtain RF power output. During transmit, voice modulation is applied to this synthesizer. Transceiver functions, such as TX/RX control, PLL synthesizer settings, and channel programming, are controlled using the MPU.

Receiver

Incoming RF signals from the antenna connector are delivered to the RF Unit, and pass through a low-pass filter (LPF) consisting of coils and capacitors, and antenna switching diodes **D1003** and **D1004** (both **XB15A308**) for delivery to the receiver front end.

Signals within the frequency range of the transceiver are then passed through a bandpass filter consisting of T1001 and T1002 before RF amplification by **Q1014** (**2SC5006**).

The amplified RF is then bandpass filtered again by T1003, T1004, and T1005, to ensure pure in-band input to 1st mixer **Q1018** (**3SK320**).

Buffered output from the VCO Unit is amplified by **Q1016** (**2SC5006**) and bandpass filtered by L2012, C1072, and C1078, to provide a pure 1st local signal between 134.65 and 140.625 MHz for delivery to the 1st mixer.

The 21.4 MHz 1st mixer product then passes through dual monolithic crystal filter XF2001 (± 6.5 kHz BW), and is amplified by **Q1022** (**2SC4400-3**) and delivered to the input of the FM IF subsystem IC **Q1024** (**TA31136FN**). This IC contains the 2nd mixer, 2nd local oscillator, limiter amplifier, FM detector, noise amplifier, and squelch gates.

The 2nd local in the IF-IC is produced from crystal **X1001** (21.850 MHz), and the 1st IF is converted to 450 KHz by the 2nd mixer and stripped of unwanted components by ceramic filter **CF1001**.

After passing through a limiter amplifier, the signal is demodulated by the FM detector. Demodulated receive audio from the IF-IC is amplified by **Q1025** (**2SC4154E**), then the signal is through the AF Mute switch **Q1027** (**TC4S66F**).

After volume adjustment by the AF power amplifier **Q1031** (**TDA2003**), the audio signal is passed to the external Speaker terminal in the accessory cable and 16 Ω internal loudspeaker.

PLL Synthesizer

The 1st LO maintains stability from the PLL synthesizer by using a 21.850 MHz reference signal from crystal **X1001**. PLL synthesizer IC **Q1017 (LV2105V)** consists of a prescaler, reference counter, swallow counter, programmable counter, a serial data input port to set these counters based on the external data, a phase comparator, and a charge pump.

The PLL-IC divides the 21.850 MHz reference signal by 874 using the reference counter (25 kHz comparison frequency). The VCO output is divided by the prescaler, swallow counter and programmable counter. These two signals are compared by the phase comparator and applied to the charge pump.

A voltage proportional to their phase difference is delivered to the low-pass filter circuit, then fed back to the VCO as a voltage with phase error, controlling and stabilizing the oscillating frequency. This synthesizer also operates as a modulator during transmit.

The VCO is comprised of **Q1020 (2SK210GR)** and **D1011/1012**, (both **1SV230**); it oscillates at 21.4 MHz during receive, and at the fundamental frequency during transmit, with direct frequency-modulation using varactor diode **D1009 (1SV214)**. The VCO output passes through buffer amplifier **Q1019 (2SC5374)**, and is amplified by **Q1016 (2SC5374)** to obtain stable output. The VCO DC supply is regulated by **Q1015 (2SC4154E)**. Synthesizer output is fed to the 1st mixer by diode switch **D1007 (DAN235U)** during receive, and to drive amplifiers **Q1013 (2SC5227-4)**, **Q1011 (2SC3357)**, and **Q1001** for transmit.

The reference oscillator feeds the PLL synthesizer.

Transmitter

Voice audio from the microphone is delivered via the **MIC** connector to the RF Unit. After passing through amplifier **Q1028 (NJM2902M)**, a pre-emphasis network, limiter (IDC: instantaneous deviation control), and LPF **Q1028 (NJM2902M)**, the audio is adjusted for optimum deviation level and delivered to the next stage.

Voice or DSC(Digital Selective Calling) encode signal inputs from the LPF **Q1028** is 8 FM-modulated in the VCO of the synthesizer. Synthesizer output, after passing through diode switch **D1006 (DAN235U)**, is amplified by driver **Q1013 (2SC5227)**, **Q1011 (2SC3357)**, and RF power amplifier **Q1001 (RA35H1516M)** to obtain full RF output.

The RF energy then passes through antenna switch **D1003** and a low-pass filter circuit and finally to the antenna connector.

RF output power from the final amplifier is sampled by C1006 and C1011 and is rectified by **D1002 (1SS321)**. The resulting DC is fed through Automatic Power Controllers **Q1004 (2SA1602A)**, **Q1008 (2SC4154E)** and **Q1012 (2SA1602A)** to transmitter RF power amplifier **Q1001**, thus providing positive control of the power output.

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency, modulated directly in the transmit VCO. Additional harmonic suppression is provided by a low-pass filter consisting of coils and capacitors, resulting in more than 70 dB of harmonic suppression prior to delivery of the RF energy to the antenna.

DSC Encoder/ Decoder

Encoder

The DCS (Digital Selective Calling) encode signal which D/A converted in the 8-bit MPU IC **Q2003** is fed through the low-pass filter **Q1028** on the RF Unit to the VCO.

Decoder

The receiving DCS code is demodulated by the FM IC **Q1024**, then fed through the low-pass filter **Q1026 (2SC4154E)** to the DCS Decoder IC **Q1032 (NJM2211M)** which the receiving DCS code is decoded. The decoded DCS signal delivered to the 8-bit MPU IC **Q2003**

1050 Hz Weather Alert Decoder

1050Hz Weather Alert signals are demodulated on the CNTL Unit, and are applied to low-pass filter **Q1026 (2SC4154E)**, and pass thorough the limiter comparator **Q1028 (NJM2902M)**.

MPU

Operation is controlled by 8-bit MPU IC **Q2003 (M37560M)**. The system clock uses a 9.8304 MHz crystal for a time base. IC **Q2004 (PST597CN)** resets the MPU when the power is on, and monitors the voltage of the regulated 5V power supply line.

EEPROM

The EE-PROM retains TX and RX data for all memory channels , prescaler dividing, IF frequency, local oscillator injection side, and reference oscillator data.