FSC-BT956B

v4.2 & BR/EDR Bluetooth Module Datasheet

Version 2.1

Revision History

Version	Data	Notes	
2.0	2020/12/14	Initial Version	Fish
2.1	2021/03/02	Modify the error description and add the module picture	Fish

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1. INTRODUCTION

Overview

The FSC-BT956B is a high performance, highly integrated multi-media system-on-chip solution with Bluetooth connectivity, which specialized in music and audio applications.

Integrating all essential electronic components, including baseband, bluetooth transceiver, power management onto a single system on chip, it offers best in class bill of material, space requirement and cost/feature ratio for bluetooth music and audio application.

Built with Feasycom standard firmware by default, custo mized firmware is available too.

The FSC-BT956B is an appropriate product for designers who want to add wireless capability to their products.

Features

- Bluetooth v4.2, supports BR/EDR
- UART programming and data interface (baudrate can up to 921600bps)
- Audio interfaces: PCM/I2S, analog stereo line in
- I2C Master /PWM control interfaces
- Postage stamp sized form factor
- Various serial interfaces: USB 1.1 FS, UART, I2C Master and SPI Master, SD Card Interface, IR receiver
- Support analog key
- Support A2DP 1.3.1 and AVRCP1.6.1
- Dual channel 24 bits voice ADC and 24 bits stereo DAC, supports sample rate of 8, 11.025, 12, 16, 22.05, 32, 44.1, 48 and 96 KHz
- Support MP3/SBC/WMA/ACC decoder
- Support audio playback from SD/USB card
- Support two Line in or two analog/ digital MIC or one analog MIC + one digital MIC.
- Support mix of Line in and MIC input with wide range of programmable analog gain settings
- Internal 32K OSC for standby, shutoff and sleep state
- Integrated Battery charger
- Low power consumption in both active and sleep mode, 12mA when playing music
- Support External Antenna
- RoHS compliant

Application

- Bluetooth speakers
- Bluetooth music box
- Bluetooth headset or headphone

Module picture as below showing

Figure 1: FSC-BT956B Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth Version	Bluetooth v4.2 specification compliant, supports BR/EDR
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+8 dBm (Maximum)
	Receive Sensitivity	-85 dBm@0.1%BER (Typical)
	Modulation	π/4 DQPSK , 8DPSK
	Raw Data Rates (Air)	3 Mbps(Classic BT - BR/EDR)
Host Interface and Peripherals	UART Interface	TX, RX, Supports Automatic Flow Control (CTS and RTS lines).
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		5, 6, 7, 8 data bit character
	GPIO	14 (maximum – configurable) lines
		O/P drive strength (10 mA)
		Pull-up resistor (33 KΩ) control
		Read pin-level
	I2C Interface	1 (configurable from GPIO total). Up to 400 kbps
	Audio CODEC	Embedded 24-bit stereo DAC and one channel 24 bits ADC
		MIC/LINE-In-THDN: -82 dB, Dynamic
		Range SNR: 93 dB (A-Weighted)
		Headphone Output-THD:-85dB
		Output Voltage:598mV rms
		Sample Rate: 8, 11.025, 12, 16, 22.05, 32, 44.1 , 48 and 96 KHz
	SD/TF/MMC	SD/TF Card Specification Version 2.0
		SDIO Version 1.10
		MMC specification Version 3.1
	PWM	Up to 4 PWM output
		16-bit resolution
		8-bit prescaler and clock divider
		Supports PWM interrupts
		supports input capture function
Profiles	Classic Bluetooth	SPP (Serial Port Profile) - Up to 600 Kbps
	Bluetooth Low Energy	No Support
Maximum Connections	Classic Bluetooth	1 Clients(TBD)
	Bluetooth Low Energy	No Support
FW upgrade		Debug
		Via UART/SD Card/I2C(TBD)
Supply Voltage	Supply	2.4V ~ 4.35V
Power Consumption		Max Peak Current(TX Power @ +8dBm TX): 86mA

		Low power consumption in both active and sleep mode, 12mA when playing music
Physical	Dimensions	13mm X 26.9mm X 2.4mm; Pad Pitch 1.5mm
Environmental	Operating	-20°C to +65°C
	Storage	-40°C to +90°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class-2 Machine Model: Class-B

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

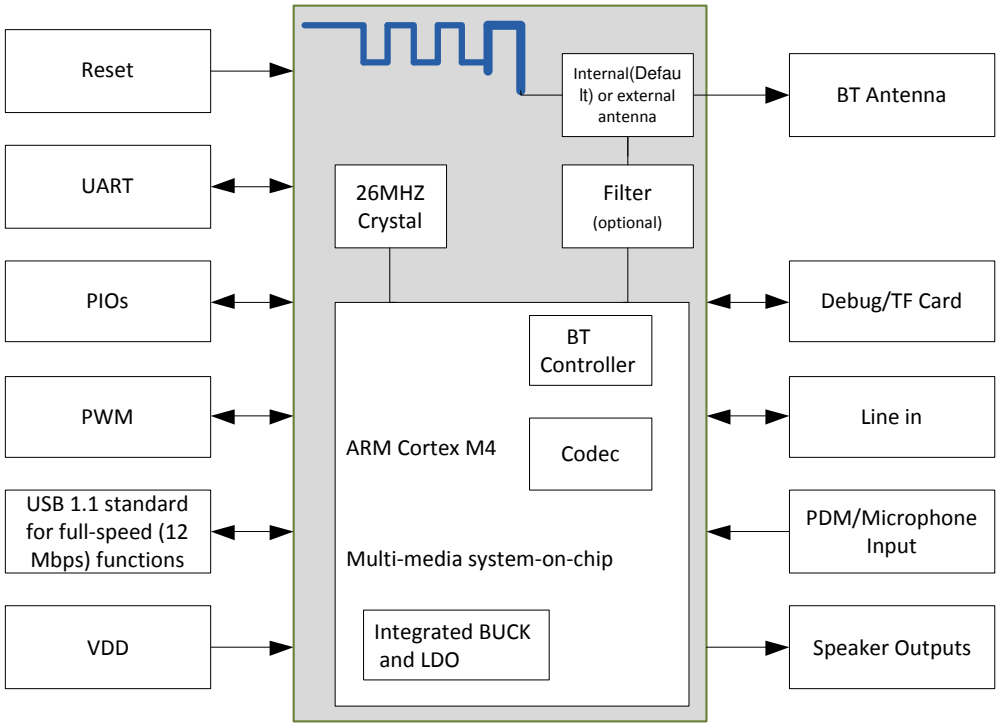


Figure 2: Block Diagram

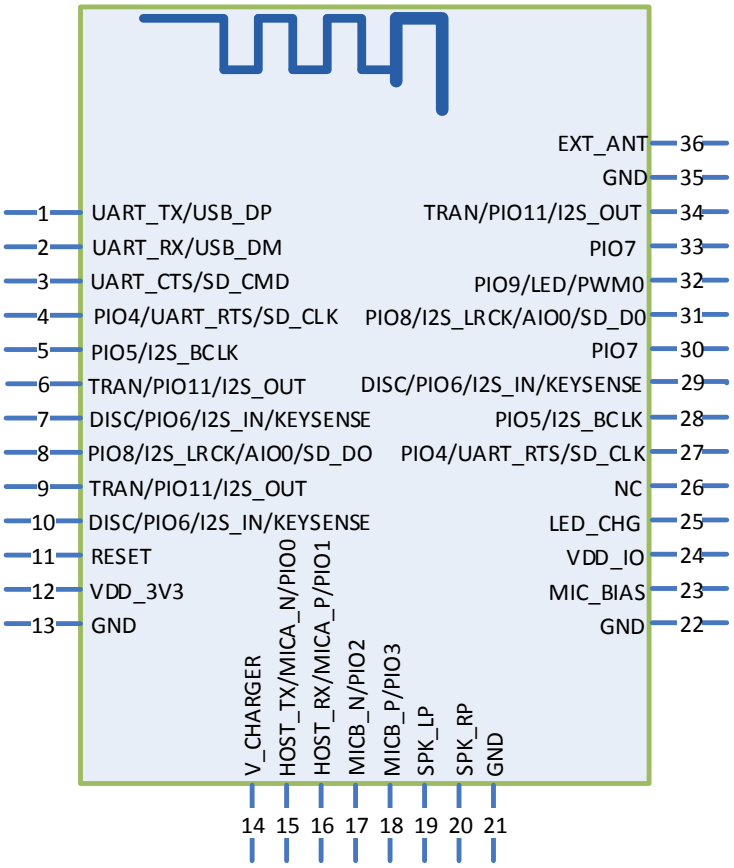


Figure 3: FSC-BT956B PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX/USB_DP	I/O	UART Data output Alternative Function: USB_DP.	Note 1,2
2	UART_RX/USB_DM	I/O	UART Data input Alternative Function: USB_DM.	Note 1,2
3	UART_CTS/SD_CMD	I/O	UART Clear to Send (active low) Alternative Function: Programmable input/output line Alternative Function: **SD_CMD**	Note 1
4,27	PIO4/UART_RTS/SD_CLK	I/O	UART Request to Send (active low) Alternative Function: Programmable input/output line Alternative Function: **SD_CLK**	Note 1
5,28	PIO5/I2S_BCLK	I/O	Programmable input/output line Alternative Function: I2S BCLK	Note 1
6,9,34	Tran/PIO11/I2S_OUT	I/O	Host MCU change UART transmission mode. (Default) Alternative Function: Programmable input/output line Alternative Function: I2S DATA OUT	Note 1,3
7,10,29	Disc/PIO6/I2S_IN/KEYSENSE	I/O	Host MCU disconnect bluetooth. (Default) Alternative Function: Programmable input/output line	Note 1,4,8

			Alternative Function: I2S DATA IN Alternative Function: ADC Keysense.	
8,31	PIO8/I2S_LRCK/AIO0/SD_D0	A,I/O	Programmable input/output line Alternative Function: I2S_LRCK. Alternative Function: Analogue programmable I/O line. Alternative Function: **SD_DATA**	Note 1
11	RESET	I	External reset input: Active LOW. Set this pin low reset to initial state	
12	VDD_3V3	Vdd	Power supply voltage 3.3V	
13	GND	Vss	Power Ground	
14	V_CHARGER	PWR	Charger power supply (5V)	Note 11
15	HOST_TX/MICA_N/PIO0	A,I/O	Programmable input/output line Alternative Function: MIC_AN Alternative Function: **Debugging through the TX line** Alternative Function: **PDM2 data**	Note 1,6,13
16	HOST_RX/MICA_P/PIO1	A,I/O	Programmable input/output line Alternative Function: MIC_AP Alternative Function: **Debugging through the RX line** Alternative Function: **PDM2 clock**	Note 1,6,13
17	MICB_N/PIO2	A,I/O	Programmable input/output line Alternative Function: MIC_BN. Alternative Function: **PDM1 data**	Note 1, 13
18	MICB_P/PIO3	A,I/O	Programmable input/output line Alternative Function: I2S MCLK. Alternative Function: MIC_BP. Alternative Function: **PDM1 clock**	Note 1, 13
19	SPK_LP	A,O	DAC right output positive	
20	SPK_RP	A,O	DAC left output positive	
21	GND	Vss	Power Ground	
22	GND	Vss	Power Ground	
23	MIC_BIAS	O	Microphone bias voltage	
24	VDD_IO	PWR, O	Power of digital IO **(For power supply to the SD card)**	Note 7
25	LED_CHG	O	LED output for charger	Note 10
26	NC			
30,33	PIO7	I/O	Programmable input/output line Alternative Function: BT Status(Default) ***Connected: High ; Not connected: low***	Note 1,8
32	PIO9/LED/PWM0	I/O	Programmable input/output line Alternative Function: LED(Default) Alternative Function: PWM.	Note 9
35	GND	Vss	Power Ground	
36	EXT_ANT	O	RF signal output .	Note 12

Module Pin Notes:	
Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	Full-speed USB interface for communicating with other devices, such as PC or USB card.
Note 3	When bluetooth connection established, H = instruction mode L = throughput mode
Note 4	When bluetooth connection established, a rising edge of the PIN will cause disconnection with remote device.
Note 5	
Note 6	The Debug UART is specially designed for communicating debug information with a PC host.
Note 7	Internal power outlet, the power supply to the SD card, external circuit need to connect a cap(1uF~4.7uF) in series.
Note 8	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 9	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 10	When the charging function is enabled, H = charging L = fully charged or not connected
Note 11	Charging power input (5V)
Note 12	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.
Note 13	Digital MIC interface that converts analog signals to digital signals.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Audio Interfaces

4.2.1 ADC&DAC(Internal CODEC)

The audio codec has one channel voice ADC and audio DAC, which supports mono voice input and stereo audio output. It also has flexible mixing and loopback paths to support variable scenario requirements, such as side tone, etc.

- Dual channel 24 bits ADC and 24 bits stereo DAC
- Support dual digital MIC
- Stereo input for voice and audio band, input resistance is typically 4KΩ.
- Integrated mic bias which don't need external load capacitor with configurable output voltage
- Stereo outputs are supported, could drive 16Ω/32Ω headphone, or act as line-out.
- Support sample rate of 8, 11.025, 12, 16, 22.05, 32, 44.1 , 48 and 96 KHz.

- Configurable gain for audio input and output path, gains control is implemented in both digital and analog.
- Flexible audio/voice path mixing/loopback.

4.2.2 Microphone Input & line IN

Check the Application Schematic for the microphone input & line IN design.
If need to use Microphone & Line IN simultaneously, please refer to the **Analog Characteristics** introduction.

4.2.3 SPEAKER

Check the Application Schematic for the microphone input & line IN design.
Please refer to the **Analog Characteristics** introduction.

4.3 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Debug Reset, Watchdog time-out reset (WDT), Global soft reset.

- POR
  Entire SoC is reset after power supply ramping from 0v to VDD.
- External Pin Reset
  Entire SoC is reset except PMU.
- Warm Reset
  - ✓ Global soft reset
    DBB can be reset by set soft reset register in system control register map.
  - ✓ Watch Dog Reset
    DBB will be reset when watch dog timer expired.
  - ✓ Debug Reset
    DBB will be reset through debug host set its internal register

4.4 General Purpose Digital IO

There are 14 general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED drives or interrupt signals to host controller, etc. Do not connect them if not use.

The I/O type of each I/O pins can be configured by software individually as Input or Push-pull output mode. After the chip is reset, the I/O mode of all pins is input mode with no pull-up and pull-down enable. Each I/O pin has an individual pull-up and pull-down resistor which is about 40 kΩ ~ 50 kΩ for VDD and Vss.

- Two I/O modes: a: Push-Pull Output mode b: Input only with high impendence mode
- CMOS/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge setting
- I/O pin has individual internal pull-up resistor and pull-down resistor
- Enabling the pin interrupt function will also enable the wake-up function

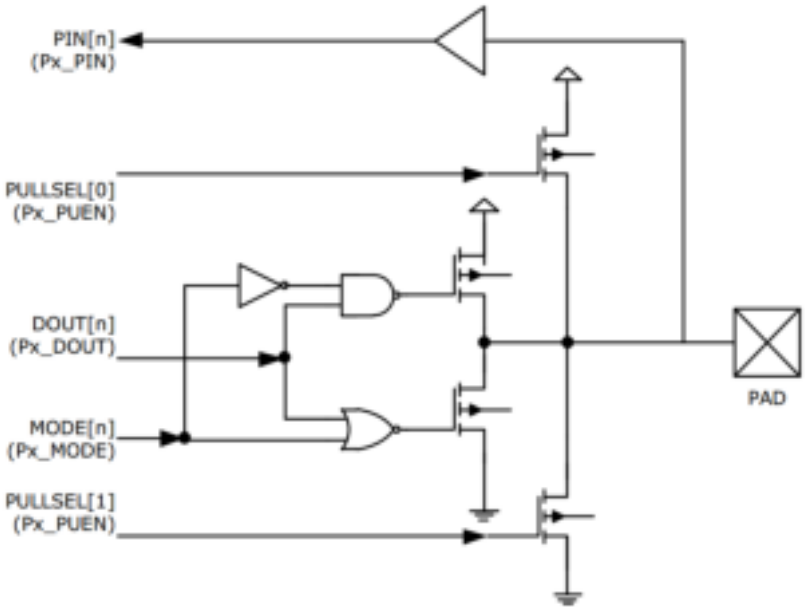


Figure 4: I/O Pin Block Diagram

4.5 RF Interface

For This Module, the default mode for antenna is external antenna.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 2.1; 1 Mbps to 3 Mbps over the air data rate.
- TX output power of +8dBm.
- Receiver to achieve maximum sensitivity -85dBm @ 0.1% BER.

4.6 Serial Interfaces

4.6.1 UART

FSC-BT956B provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	921600bps(≤1%Error)
Flow control		Supports Automatic Flow Control (CTS and RTS lines)
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

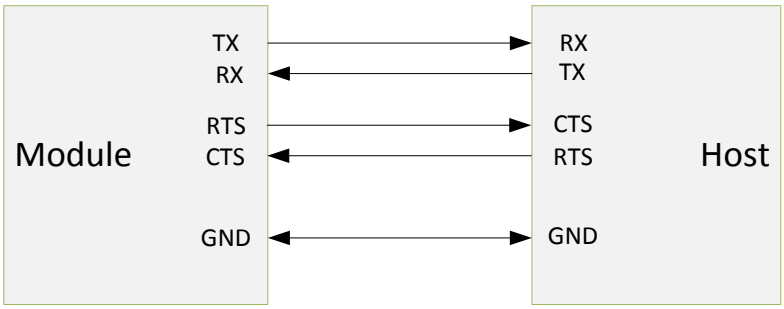


Figure 5: UART Connection

4.6.2 I2C Interface

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

FSC-BT956B has I2C master which supports 100Kbps and 400Kbps.

- Compatible with Philips I2C standard
- Multi Master Operation
- Software programmable clock frequency
- Clock stretching and wait state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Supports 7 and 10bit addressing mode
- Operates from a wide range of input clock frequencies

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I2C Bus Timing.

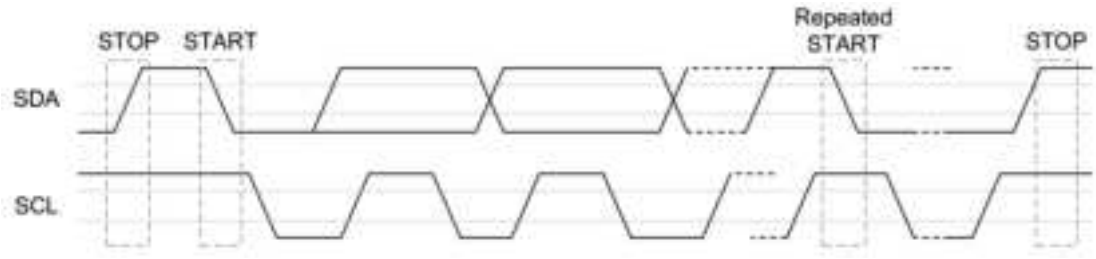


Figure 6: I2C Bus Timing

The device on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. The I2C H/W interfaces to the I2C bus via two pins: SDA and SCL. Pull up resistor is needed for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins function to I2C in advance.

4.6.3 USB Device Controller

FSC-BT956B has a full-speed USB interface for communicating with other devices, such as PC or USB card. Bothe USB PHY and Link layer is integrated. It supports both host and device. USB role detection is included to support USB Type A.

- Operates either as the host/peripheral in point-to-point communications with another USB function or as a function controller for a USB peripheral
- Complies with the USB 1.1 standard for high-speed (12 Mbps) functions
- Supports point-to-point communications with one high-, full- or low-speed device
- Supports Control, Interrupt, Bulk and Isochronous transfer
- 4 Endpoint with FIFOs
  - ✓ One Bi-directional Control Endpoint (EP0)
  - ✓ Four soft configurable Bi-directional Endpoints

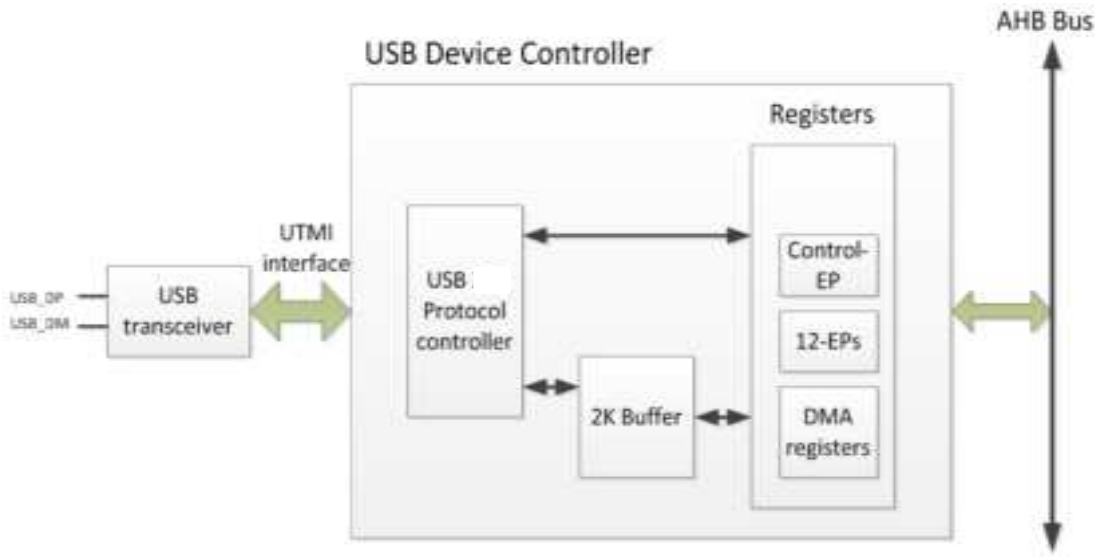


Figure 7: USB Device Controller Block Diagram

4.7 PWM Generator and Capture Timer (PWM)

The PWM module generates 4 independent PWM outputs, utilizing 3 specialized modulation schemes. All PWM outputs can be configured to PWL, PWT and LGP mode.

- Pulse Width Tone (PWT)
  - Generates square wave output capable of driving piezo electric speaker
  - Variable frequency between 349Hz and 5276Hz with 12 half-tone frequencies per octave
  - Volume control
- Light Pulse Generation (LPG)
  - Adjustable PWM frequency is from 0.01Hz ~ 6.5MHz
  - Adjustable on-time/off-time is from 0.77us to 50s.
  - Customized output mode for square wave
- Pulse Width Light (PWL)
  - Pseudo random bit sequence with output on-time proportional to a programmed threshold value
  - Minimizes flicker

4.8 SD/TF/MMC Controller

This module connects inner bus and outer SD/TF or MMC card. It receives the inner command and data, transfers it to outer SD/TF or MMC card, and transfer response or data back.

- SD/TF Card Specification Version 2.0
- SDIO Version 1.10
- MMC specification Version 3.1
- Hot insertion and removal of media cards will be considered by GPIO module

4.9 Calendar

The calendar module provides date and time information. It works on the 32.768 KHz oscillator with independent power supply. In addition to provide timing data, alarm interrupt is generated and it is also used to power-up the baseband core by sending wakeup signal.

- Independent power supply.
- Counters for second, minute, hour, day, month, year and day of week.
- Maxim day of each month stored in module, leap year supported.
- Alarm generate, wakeup triggered by alarm. Alarm IRQ.
- Periodical IRQ for certain intervals

4.10 IR Receiver

The IR receiver module performs serial-to-parallel conversion on received data from a peripheral device. It supports NEC, RC-5 and Philips 9012 mode.

- Support 3 IR modes, NEC, RC-5 and Philips 9012
- Store data code and user code
- Support data code and user code verify
- Enable interrupt when data received
- Configurable frame time, bit time, high-time and low-time

4.11 SPI Master

This module is a master interface for a synchronous serial link, it can be configured to be compatible with Motorola SPI or to comply with some various synchronous serial protocols.

- Multiple chip selects and selectable data input.
- Programmable clock polarity.
- Programmable data frame size (from 4 to 32 bits).
- Programmable delay options (time between CS, clocks and data).
- Received pattern matching before filling RX FIFO (SD-MMC read block feature)
- Transmit zero when TX FIFO empty (for generating dummy data during pattern matching read)
- Direct pin control to force value to 0, 1 or input.
- Special read mode with output enable control of the DO pin (selected input should be multiplexed with DO pin to use this feature).

4.12 Timer

There are three different timers.

- 1 24-bit decremental timer for OS, ticks of 16384Hz.

- 1 32-bit incremental hardware delay timer, ticks of 16384Hz.
- 1 24-bit decremental watchdog timer, ticks of 32768Hz.
- Multiple IRQ sources: timers wrap, interval arrives.

4.13 Debug Host

Debug Host module contains 1 normal Universal Asynchronous Receiver Transmitter channels (UART) and 1 Debug UART. The two UARTs share the same TX/RX engines, which sends and receives byte data from serial interface. Each UART has its own control sub-module and own APB interface. Debug Host module parses the incoming data from serial interface to switch between the normal UART and the Debug UART.

- Normal UART

  The normal UART can be used for traces and other purposes. For APB interface, it is exactly the same to the other UARTs in the system. However, if Debug UART is enabled, it should have the same serial interface configuration as the Debug UART. Some of its configuration options will be masked in this case. To adapt different clock frequency, the normal UART uses asynchronous FIFO, which uses gray code to represent the read and write pointer positions.
- Debug UART

  The Debug UART is specially designed for communicating debug information with a PC host. The serial interface of Debug UART is a simplified version of the normal UART and is less configurable. Each sample is sent serially, has 1 start bit (always zero), 8 data bits, and 1 stop bits (always one). Breaks (data line held low) can be generated and detected allowing resynchronizing the two devices.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
V_{CHG} - DC Power Supply	-0.3	+6	V
V_{BAT} - Input Voltage	Vss-0.3	+4.5	V
T_A - Operating Temperature	-20	+65	°C
T_{ST} - Storage Temperature	-40	+90	°C
I_{IO} - Maximum Current sunk by a I/O pin		12.8	mA
I_{IO} - Maximum Current sourced by a I/O pin		12.8	mA

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V_{CHG} - DC Power Supply	4.6	5	5.75	V
V_{BAT} - Input Voltage	2.4	3.7	4.35	V
T_A - Operating Temperature	-20	25	+65	°C
T_{ST} - Storage Temperature	-40	25	+90	°C
I_{IO} - Maximum Current sunk by a I/O pin	8	10	12	mA
I_{IO} - Maximum Current sourced by a I/O pin	8	10	12	mA

5.3 Input/output Terminal Characteristics(UART,USB,I/O)

Table 6: DC Characteristics (V_{DD} - V_{SS} = 3.5 ~ 6 V, T_A = 25°C)

Parameter	Min	Type	Max	Unit
V_{DD} - Operation Voltage	3	3.3	3.6	V
V_{SS} - Power Ground	-0.3	-	-	V
V_{DD12} - Core Logic and I/O Buffer Pre-Driver Voltage	1.08	1.2	1.32	V
V_{OH} - High Level Output Voltage	2.4	-	-	V
V_{OL} - Low Level Output Voltage	-	-	0.4	V
V_{IH} - Input High Voltage	2.0	-	-	V
V_{IL} - Input Low Voltage	-	-	0.8	V
V_{TH} - Switch Threshold(Schmitt-falling-trigger)	0.87	1.05	1.2	V
V_{TH} - Switch Threshold(Schmitt-rising-trigger)	1.65	1.9	2.1	V
R_{PU} - Input Pull-up Resist(V_{IN}=V_{SS})	32	53	120	KΩ
R_{PD} - Input Pull-down Resist(V_{IN}=V_{DD})	37	49	120	KΩ
I_L - Input Leakage Current	-10	-	10	uA
I_{OZ} - Tri-State Output Leakage Current	-10	-	10	uA
I_{OL} - Low level sink current(V_{OL}=0.4V)	4	-	-	mA
I_{OH} - High level source current (V_{OH}=2.4V)	4	-	-	mA

5.4 Specifications of Power-on Reset

Table 7: Specifications of Power-on Reset

Parameter	Min	Type	Max	Unit
T_A - Temperature	-20	25	+65	°C
I_{POR}- Quiescent Current(V_{DD}>Reset Voltage)	-	33	50	uA
V_{POR} - Reset Voltage(TA=-20~+65°C)	1.6	2	2.4	V
V_{POR} - VDD Start Voltage to Ensure Power on Reset	-	-	100	mV
PRV_{DD}- VDD Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms
t_{POR}- Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power on Reset	0.5	-	-	ms

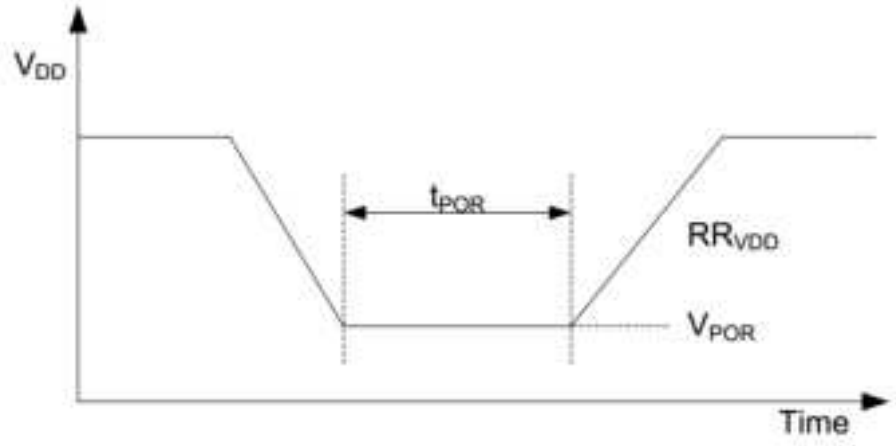


Figure 8: Power-up Ramp Condition

5.5 USB PHY Specifications

5.5.1 USB DC Electrical Characteristics

Table 8: USB DC Electrical Characteristics

Parameter	Min	Type	Max	Unit
V_{IH} - Input high(driven)	2.0	-	-	V
V_{IL}- Input low	-	-	0.8	V
V_{DI} - Differential input sensitivity(IUSB_DP-USB_DM)	0.2	-	-	V
V_{CM} - Differential common-mode rang (Includes V_{DI} range)	0.8	-	2.5	V
VSE- Single-ended receiver threshold	0.8	-	2.0	V
Receiver hysteresis	-	400	-	mV
V_{OL}- Output low (driven)	0	-	0.3	V
V_{OH}- Output high (driven)	2.8	-	3.6	V
V_{CRS}- Output signal cross voltage	1.3	-	2.0	V
R_{PU} - Pull-up resistor	1.425	-	1.575	KΩ
V_{TRM} - Pull-down resistor	14.25	-	15.75	KΩ
Z_{DRV} - Termination Voltage for upstream port pull up (R_{PU})	3.0	-	3.6	V
C_{IN} - Driver output resistance (Steady state drive*)	28	-	49.5	Ω
V_{IH} - Transceiver capacitance (Pin to V_{SS})	-	-	20	pF
Note: Driver output resistance does not include series resistor resistance.				

5.5.2 USB Full-Speed Driver Electrical Characteristics

Table 9: USB full-Speed Driver Electrical Characteristics

Parameter	Min	Type	Max	Unit
T_{FR} - Rising time (CL=5pF)	500	-	-	nS
T_{FF}- Falling time (CL=5pF)	500	-	-	nS
T_{FRFF} - Rising and falling time matching (T_{FRFF} = T_{FR} / T_{FF})	90	-	111	%

5.6 I2C Dynamic Characteristics

Table 10: I2C Dynamic Characteristics

Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
	Min	Max	Min	Max	
t_{LOW} - SCL low period	4.7	-	1.2	-	uS
T_{HIGH} - SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$ - Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$ - START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$ - STOP condition setup time	4	-	0.6	-	uS
t_{BUF} - Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$ - Data setup time	250	-	100	-	uS
$t_{HD;DAT}$ - Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r - SCL/SDA rise time	-	1000	20+0.1CB	300	uS
t_f- SCL/SDA fall time	-	300	-	300	uS
C_b - Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

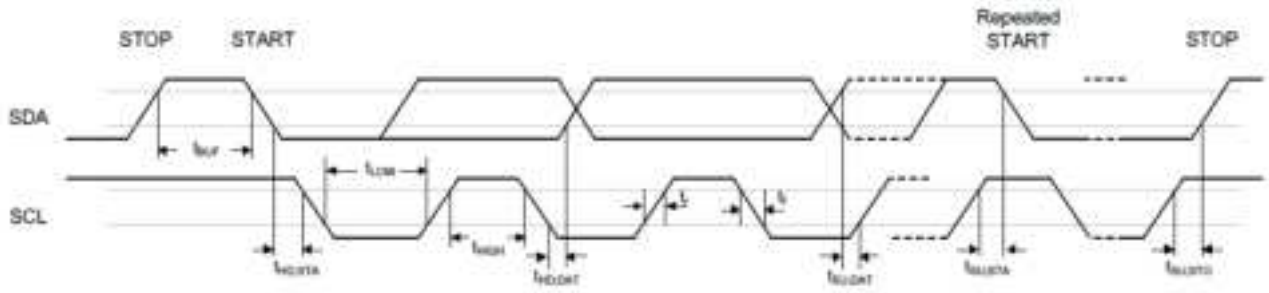


Figure 9: I2C Timing Diagram

5.7 Power consumptions(TBD)

Table 11: Power consumptions

Parameter	Test Conditions	Type	Unit
Search		~35	mA
Unconnected (Deep Sleep Idle Mode)	Low power consumption in both active and sleep mode	~12	mA
Connected Idle		~15	mA
Play with Minimum Volume		~12	mA
Play with Maximum Volume		~50	mA
Shutdown	No support	-	mA

6. MSL & ESD

Table 12: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade:	Human Body Model: Class-2 Machine Model: Class-B

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **next table** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **next table**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 13: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

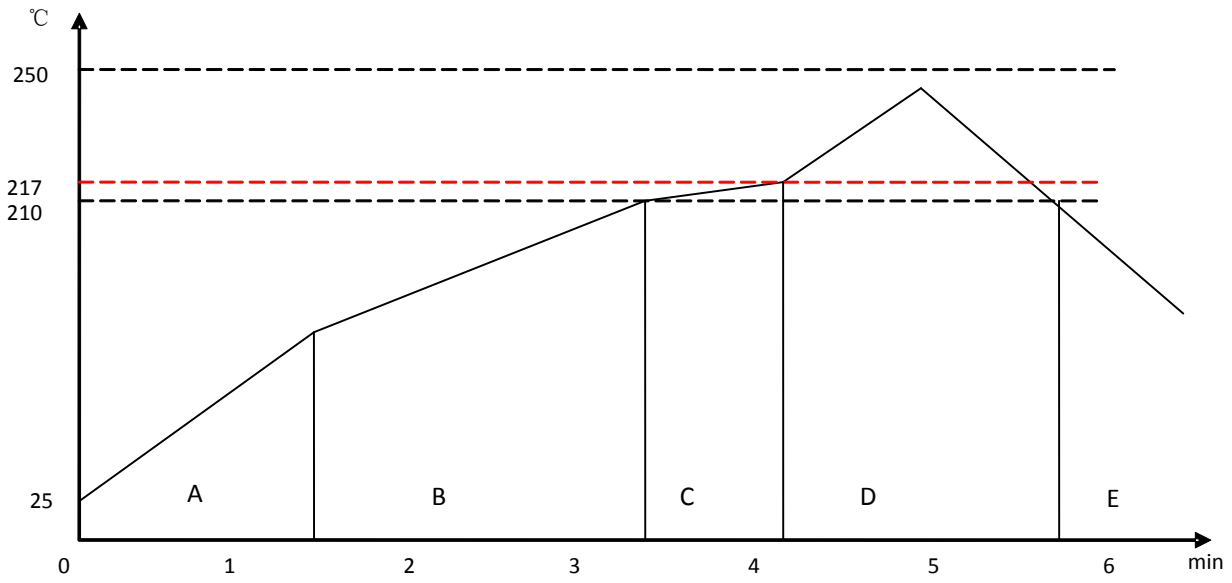


Figure 10: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

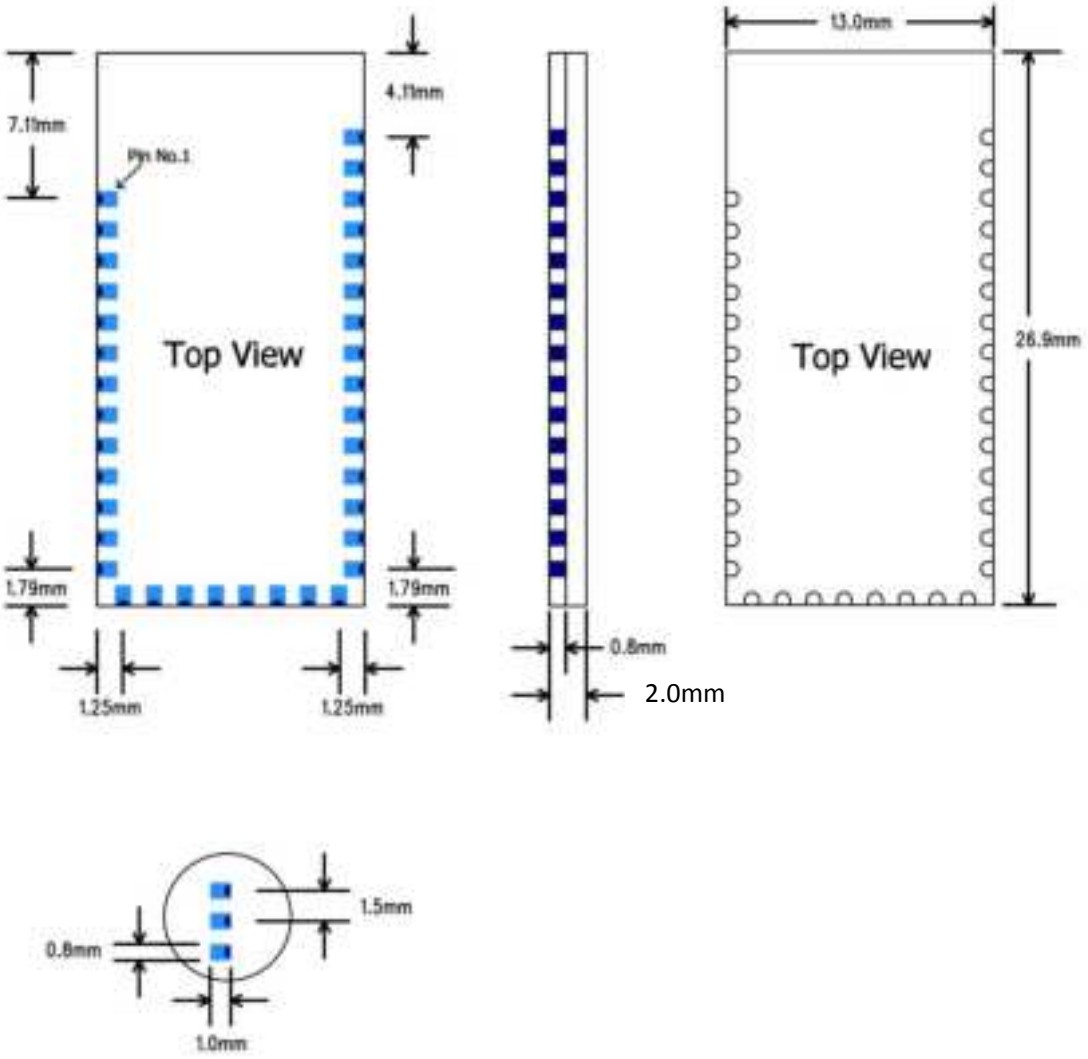


Figure 11: FSC-BT956B footprint

8.2 Host PCB Land Pattern and Antenna Keep-out for FSC-BT956B

Please check the picture below for Pad Structure and Keep Out Area:

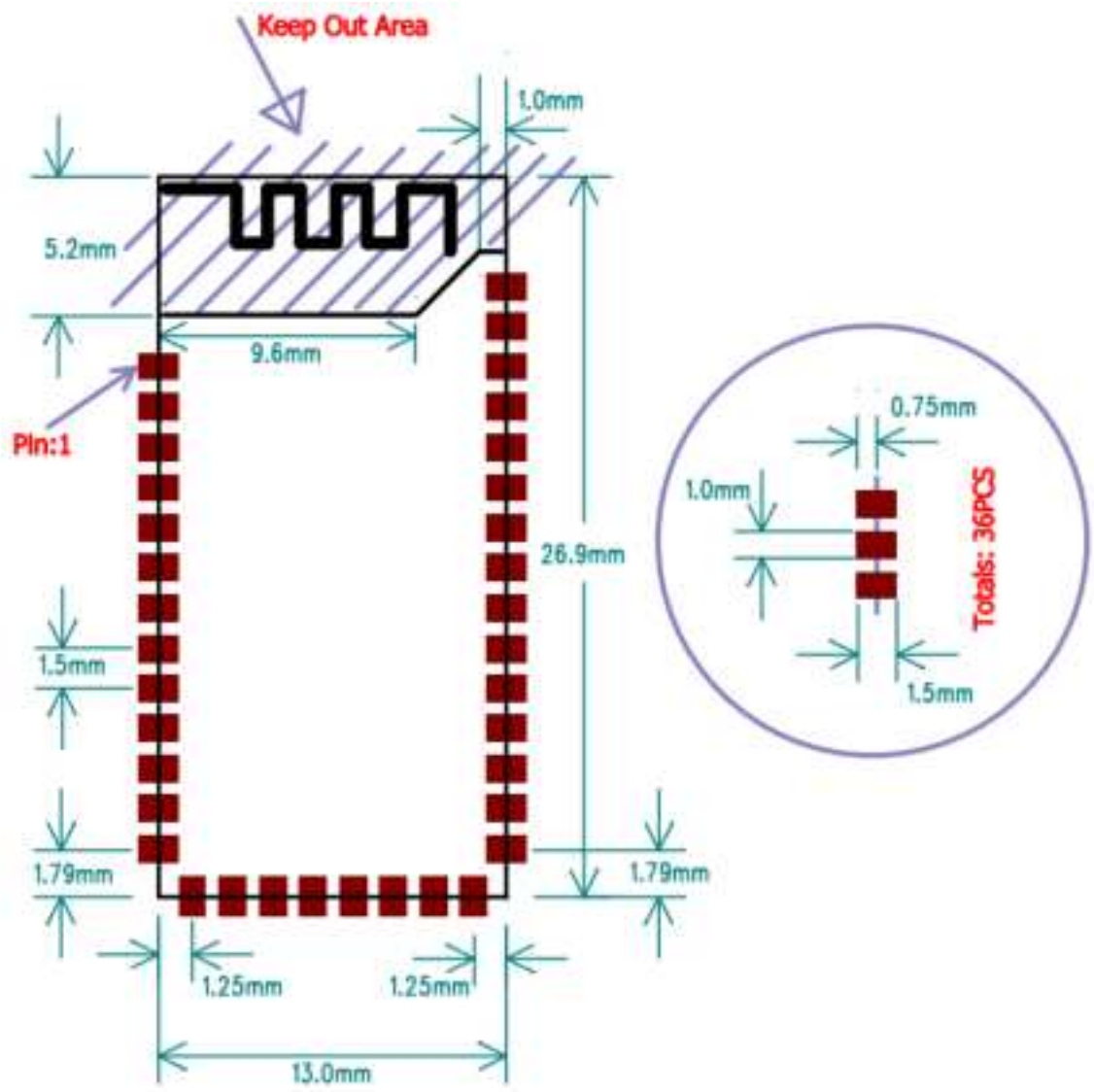


Figure 12: Host PCB-Top View

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT956B is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

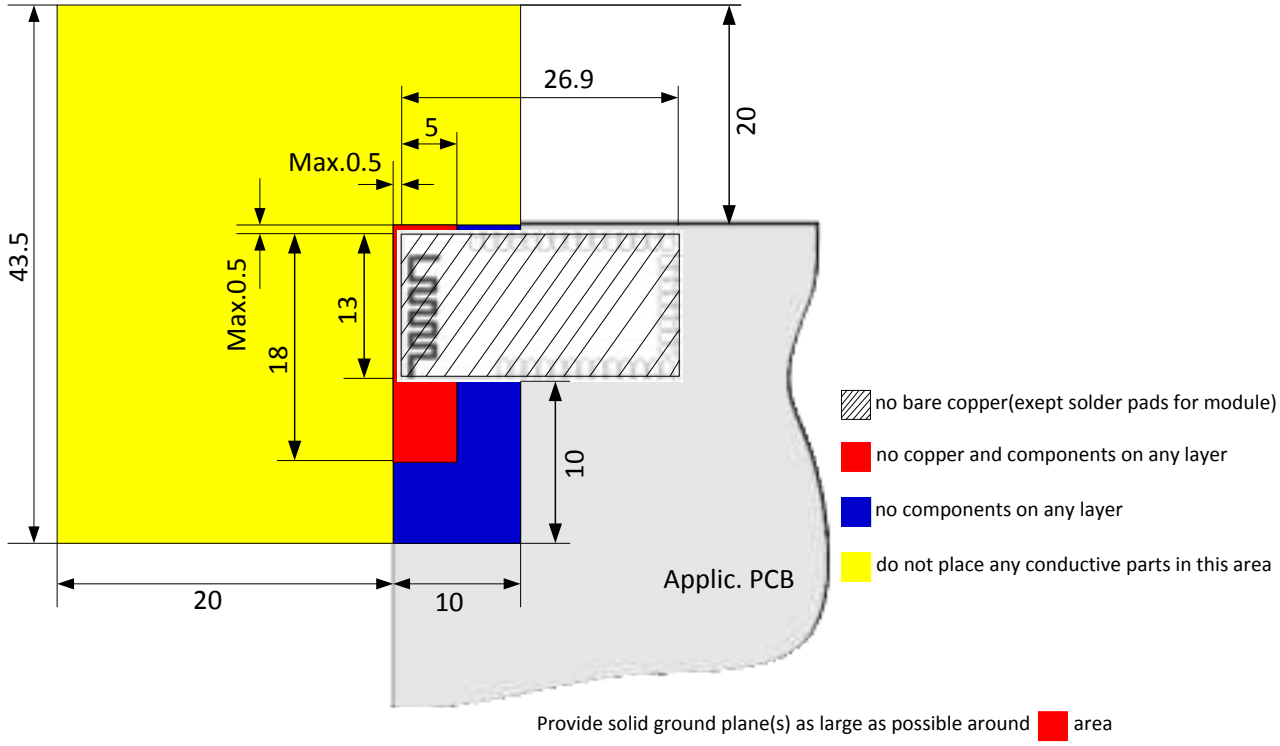


Figure 13: FSC-BT956B Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

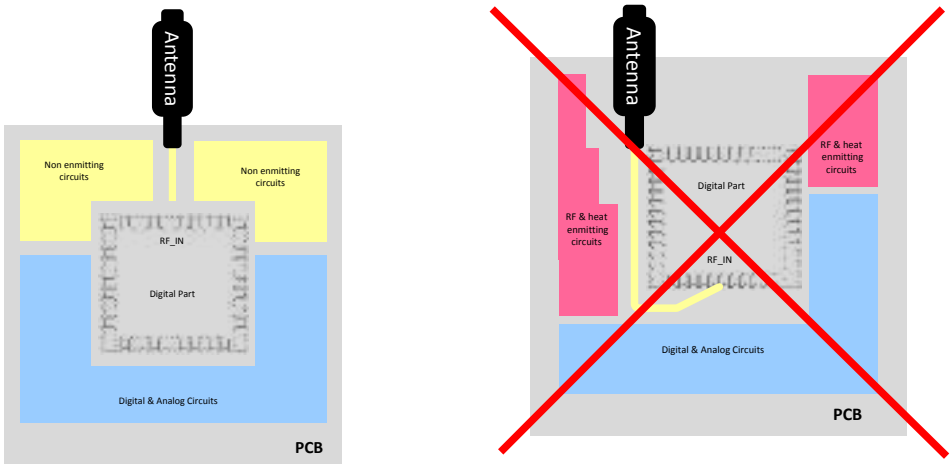


Figure 14: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

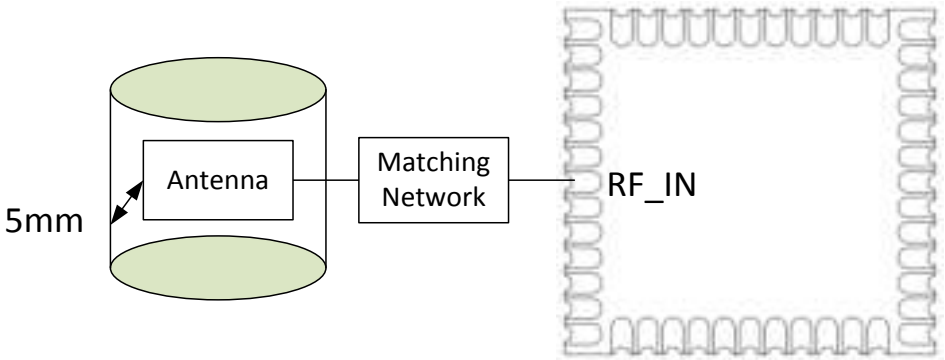


Figure 15: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

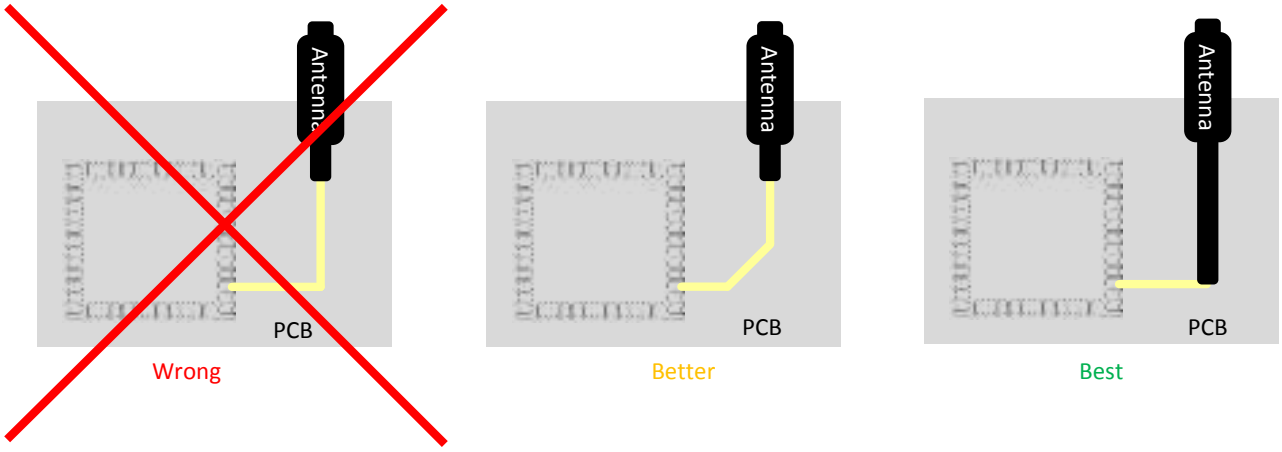


Figure 16: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

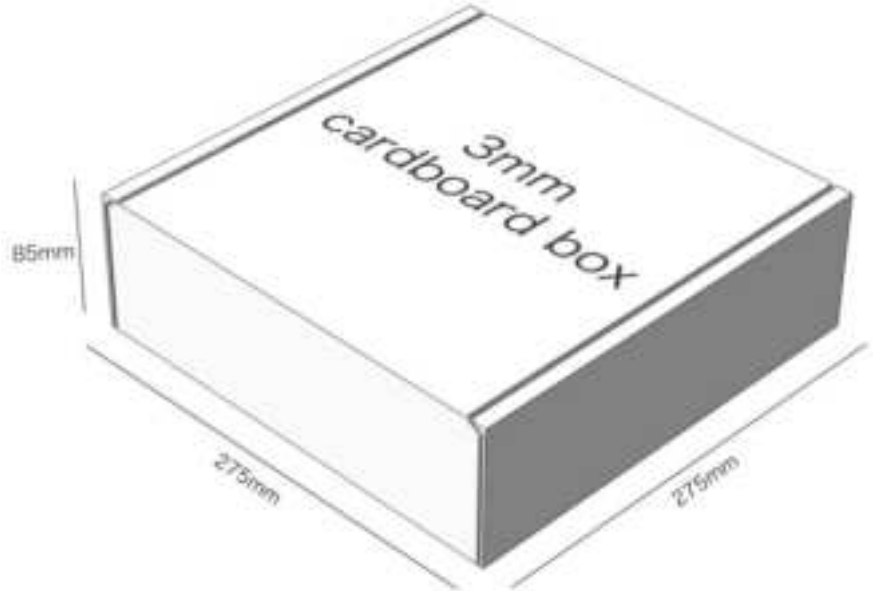
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 17: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 18: Packing Box

11. APPLICATION SCHEMATIC

FCC Statements
(OEM) Integrator has to assure compliance of the entire end-product incl. the integrated RF Module. For 15 B (§15.107 and if applicable §15.109) compliance, the host manufacturer is required to show compliance with 15 while the module is installed and operating.

Furthermore the module should be transmitting and the evaluation should confirm that the module's intentional emissions (15C) are compliant (fundamental / out-of-band). Finally the integrator has to apply the appropriate equipment authorization (e.g. Verification) for the new host device per definition in §15.101.

Integrator is reminded to assure that these installation instructions will not be made available to the end-user of the final host device.

The final host device, into which this RF Module is integrated" has to be labeled with an auxiliary label stating the FCC ID of the RF Module, such as "Contains FCC ID：2AMWOFSC-BT956B"
This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:
(1)this device may not cause harmful interference, and
(2)this device must accept any interference received, including interference that may cause undesired operation."
"Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment."
the Integrator will be responsible to satisfy SAR/ RF Exposure requirements, when the module integrated into the host device.

Module statement
The single-modular transmitter is a self-contained, physically delineated, component for which compliance can be demonstrated independent of the host operating conditions, and which complies with all eight requirements of § 15.212(a)(1) as summarized below.

1) The radio elements have the radio frequency circuitry shielded.
2) The module has buffered modulation/data inputs to ensure that the device will comply with Part 15 requirements with any type of input signal.
3) The module contains power supply regulation on the module.
4) The module contains a permanently attached antenna.
5) The module demonstrates compliance in a stand-alone configuration.
6) The module is labeled with its permanently affixed FCC ID label.
7) The module complies with all specific rules applicable to the transmitter, including all the conditions provided in the integration instructions by the grantee.
8) The module complies with RF exposure requirements.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules
FCC Part 15.247

2.3 Specific operational use conditions
This transmitter/module and its antenna(s) must not be co-located or operating in conjunction with any transmitter. This information also extends to the host manufacturer's instruction manual.

2.4 Limited module procedures
not applicable

2.5 Trace antenna designs
not applicable

2.6 RF exposure considerations
This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This compliance to FCC radiation exposure limits for an uncontrolled environment, and minimum of 5mm separation between antenna and body.
The host product manufacturer would provide the above information to end users in their end-product manuals.

2.7 Antennas
PCB antenna; 2dBi; 2.402 GHz～2.480GHz

2.8 Label and compliance information
The end product must carry a physical label or shall use e-labeling followed KDB784748D01 and KDB 784748 stating "Contains Transmitter Module FCC ID: 2AMWOFSC-BT956B".

2.9 Information on test modes and additional testing requirements

For more information on testing, please contact the manufacturer.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuity.