QLA12(SG636V)& QLB12(SG656V) Series Hardware Design

Smart Module Series

Version: 1.0.0

Date: 2024-07-08

Status: Preliminary

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2024-07-08	Paul WANG/ Xiong XIAO	Creation of the document
1.0.0	2024-07-08	Paul Wang/ Xiong XIAO	Preliminary

Contents

Table Index

Figure Index

1 Introduction

This document defines QLA12(SG636V) series and QLB12(SG656V) series modules and describes their air interfaces and hardware interfaces which are connected to your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
-- Reorient or relocate the receiving antenna.
-- Increase the separation between the equipment and receiver.
-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-- Consult the dealer or an experienced radio/TV technician for help.

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment. In order to avoid the possibility of exceeding the FCC radio frequency exposure limits, human proximity to the antenna shall not be less than 20cm (8 inches) during normal operation.
FCC 47 CFR Part 15.247, Part 15.407
This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Notice to OEM integrators
1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part

15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel Wireless Solutions Co., Ltd that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: 2AH2524QLB1220”

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

(4) The max allowed antenna gain is 2.0 dBi for 2.4G WIFI,3.0 dBi for 5G WIFI for external antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device complies with ISED’s licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

Radiation Exposure Statement:
This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:
Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)
1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:
In the event that these conditions can not be met (for example certain laptop configurations or co- location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:
Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances,

l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling
This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 22621-2024QLB1220”.

Plaque signalétique du produit final
Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 22621-2024QLB1220 ".

Manual Information To the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final
L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.
RSS-247 Section 6.4 (5) (6) (for local area network devices, 5GHz)

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.
Caution:

i) The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
ii) where applicable, antenna type(s), antenna models(s), and worst-case tilt angle(s) necessary to remain compliant with the e.i.r.p. elevation mask requirement set forth in section 6.2.2.3 shall be clearly indicated.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Avertissement:

i) Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;
ii) lorsqu’il y a lieu, les types d’antennes (s’il y en a plusieurs), les numéros de modèle de l’antenne et les pires angles

d’inclinaison nécessaires pour rester conforme à l’exigence de la

p.i.r.e. applicable au masque d’élévation, énoncée à la section 6.2.2.3, doivent être clairement indiqués.

i. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit

ii. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits as appropriate; and

iii. where applicable, antenna type(s), antenna models(s), and worst-case tilt angle(s) necessary to remain compliant with the e.i.r.p. elevation mask requirement set forth in section 6.2.2.3 shall be clearly indicated.

SUNMI product name	Internal product name	BB chip
QLA12-20	SG636V-WF	QCM4325
QLB12-20	SG656V-WF	SM6225
QLA12-21	SG636V-GL	QCM4325
QLB12-21	SG656V-GL	SM6225
QLA12-22	SG636V-EM	QCM4325
QLB12-22	SG656V-EM	SM6225

1.1. Special Marks

Table 1: Special Marks

Marks	Definitions
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

2 Product Overview

The module is a Smart LTE module based on Android operating systems, and provides industrial-grade performance. It is an SMD module with compact packaging and it supports built-in high performance Adreno™ 610 GPU graphics processing unit, abundant GPIO interfaces as well as external audio codec. With these, the module is engineered to meet most of the demands of M2M applications.

Table 2: Basic Information

Series	
Packaging type	LGA
Pin counts	636
Dimensions	(42.5 ±0.2 mm) × (56.5 ±0.2 mm) × (2.95 ±0.2 mm)
Weight	TBD
Models	QLB12-21(SG656V-GL), QLB12-22(SG656V-EM), QLB12-20(SG656V-WF) QLA12-21(SG636V-GL), QLA12-22(SG636V-EM), QLA12-20(SG636V-WF)

NOTE

QLB12(SG656V) series module all use SM6225 series chipset and QLA12(SG636V) series module all use QCM4325 series chipset.

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Network Type	QLB12-21(SG656V-GL) & QLA12-21(SG636V-GL)	QLB12-22(SG656V-EM) & QLA12-22(SG636V-EM)	QLB12-20(SG656V-WF) & QLA12-20(SG636V-WF)
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/ B18/B19/B20/B25/B26/B28/B30/B66/B71	B1/B2/B3/B4/B5/B7/B8/B18/B19/ B20/B26/B28	-
LTE-TDD	B34/B38/B39/B40/B41	B34/B38/B39/B40/B41	-
WCDMA	B1/B2/B4/B5/B6/B8/B19	B1/B2/B4/B5/B6/B8/B19	-
GSM	GSM850/EGSM900/DCS1800/PCS1900	GSM850/EGSM900/DCS1800/PCS1900	-
GNSS	BDS/Galileo/GLONASS/GPS/SBAS	BDS/Galileo/GLONASS/GPS/SBAS	-
Wi-Fi 802.11a/b/g/ n/ac	2401–2462 MHz 5180–5825 MHz	2401–2462 MHz 5180–5825 MHz	2401–2462 MHz 5180–5825 MHz
Bluetooth 5.1	2402–2480 MHz	2402–2480 MHz	2402–2480 MHz

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Application Processor	64-bit applications processor (Kryo): ● Kryo Gold: One high performance quad-core @ 2.4 GHz with 2 MB L2 cache ● Kryo Silver: One low power consumption quad-core @ 1.9 GHz with 512 KB L2 cache
Modem DSP	● Hexagon™ DSP, supports Dual HVX @ 614 MHz
GPU	● Adreno™ 610 GPU with 64-bit addressing @ 1.1 GHz
Memory	● 64 GB UFS + 4 GB LPDDR4X (default) ● 64 GB UFS + 3 GB LPDDR4X (option) ● 32 GB UFS + 3 GB LPDDR4X (option)
Operating System	Android 13
Supply Voltage	● 3.55–4.4 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: module by default
(U)SIM Interface	● Two (U)SIM interface ● 1.8 V and 2.95 V ● Dual SIM Dual Standby (supported by software by default)
SD Card Interface	● Complies with SD 3.0 specification ● 1.8/2.95 V SD card ● SD card hot-plug
LCM Interface	● One group of 4-lane MIPI_DSI ● Data rate: up to 1.5 Gbps/lane ● Supports up to 1080 × 2520 @ 90 fps
Camera Interface	● Three groups of 4-lane MIPI_CSI, up to 2.5 Gbps/lane ● Supports 3 concurrently working cameras (Triple ISP), supports up to (13 MP + 13 MP + 5 MP 30 fps @ ZSL) or up to (25 MP + 5 MP or 16 MP + 16 MP 30 fps @ ZSL) or up to 32 MP (30 fps @ ZSL) or 64 MP (no ZSL)
Video Codec	● Encoding: 1080P @ 60 fps, HEVC/H.264/H.265 ● Decoding: 1080P @ 60 fps, HEVC/H.264/H.265/VP9

Audio Interface	**Audio inputs:** • Two digital microphone inputs
Audio Codec	• EVS, EVRC, EVRC-B, EVRC-WB • G.711, G.729A/AB • GSM-FR, GSM-EFR, and GSM-HR • AMR-NB, AMR-WB
USB Interface	• Complies with USB 3.1 Gen 1 or 2.0 specifications • Date rate: up to 5 Gbps on USB 3.1 Gen 1 and 480 Mbps on USB 2.0 • Supports USB OTG and USB 3.1 Type-C interface, compatible with USB 2.0 • Use: AT command transmission, data communication with external AP, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB
SPI	• Up to five groups of SPI interfaces, one of them is default configuration, and four of them are multiplexed from other interfaces. • Master mode only
I2C Interfaces	• Up to six groups of I2C interfaces: – Four dedicated I2C interfaces: used for cameras, sensors and TPs. – Two generic I2C interface: used for other peripherals
I2S Interfaces	Up to two groups of I2S interfaces
UART	• Up to five groups of UART interfaces, two of them are default configurations, three of them are multiplexed from other interfaces: – Debug UART: 2-wire UART interface, dedicated for debugging by default – UART5: 4-wire UART with the speed rate up to 4 Mbps, which supports RTS and CTS hardware flow control – Three UART interfaces are multiplexed from other interfaces
ADC Interface	• Two generic ADC interfaces • Resolution: up to 15-bit
Antenna Interfaces	• Main antenna interface (50OHM_ANT_MAIN) • Rx-diversity antenna interface (50OHM_ANT_DRX) • GNSS antenna interface (50OHM_ANT_2.4G_WIFI_GNSS) • 2.4 GHz Wi-Fi & Bluetooth antenna interface (50OHM_ANT_2.4G_WIFI_GNSS) • 5 GHz Wi-Fi antenna interface (50OHM_ANT_5G_WIFI) • 50 Ω characteristic impedance
Transmitting Power	• LTE-TDD: Class 3 (23 dBm ±2 dB) • LTE-FDD: Class 3 (23 dBm ±2 dB) • WCDMA: Class 3 (23 dBm ±2 dB) • PCS1900 8-PSK: Class E2 (26 dBm ±3 dB) • DCS1800 8-PSK: Class E2 (26 dBm ±3 dB) • EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) • GSM850 8-PSK: Class E2 (27 dBm ±3 dB)

	• PCS1900: Class 1 (30 dBm ±2 dB) • DCS1800: Class 1 (30 dBm ±2 dB) • EGSM900: Class 4 (33 dBm ±2 dB) • GSM850: Class 4 (33 dBm ±2 dB)
LTE Features	• The module complies with 3GPP Rel-10 FDD and TDD • Max. LTE category: Cat4 • 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MHz RF bandwidths • DL modulations: QPSK, 16QAM, 64QAM • UL modulations: QPSK, 16QAM • DL 2 × 2 MIMO • LTE-FDD max. data rates: – DL: 150 Mbps – UL: 50 Mbps • LTE-TDD max. data rates: – DL: 130 Mbps – UL: 30 Mbps
UMTS Features	• The module complies with 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA • Modulations: QPSK, 16QAM and 64QAM • DC-HSDPA max. data rate: 42 Mbps (DL) • HSUPA max. data rate: 5.76 Mbps (UL) • WCDMA max. data rates: – DL: 384 kbps – UL: 384 kbps
GSM Features	**R99:** • CSD data rate: – DL: 14.4 kbps – UL: 9.6 kbps **GPRS:** • GPRS multi-slot class 33 (33 by default) • Coding scheme: CS 1–4 • Max. data rates: – DL: 107 kbps – UL: 85.6 kbps **EDGE:** • EDGE multi-slot class 33 (33 by default) • Coding scheme: GMSK and 8-PSK • DL coding schemes: MCS 1–9 • UL coding schemes: MCS 1–9 • Max. data rates: – DL: 296 kbps – UL: 236.8 kbps
GNSS Features	BDS/Galileo/GLONASS/GPS/SBAS

Wi-Fi Features	• Operating modes: AP and STA • Operating frequency: 2.4 GHz and 5 GHz • Protocol features: IEEE 802.11a/b/g/n/ac • Data rate: up to 433 Mbps
Bluetooth Features	• *Bluetooth Core Specification Version 5.1* • Bluetooth Classic & Bluetooth Low Energy (BLE)
Real Time Clock	The module supports RTC function
Temperature Ranges	• Normal operating temperature [1]: -25 to +75 °C • Storage temperature: -40 to +90 °C
Firmware Upgrade	• USB 2.0 interface • OTA
RoHS	All hardware components fully comply with EU RoHS directive

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- Memory (LPDDR4X + UFS flash)
- Radio frequency part
- Peripheral Interfaces

[1] Within this range, the module's indicators comply with 3GPP specification requirements.

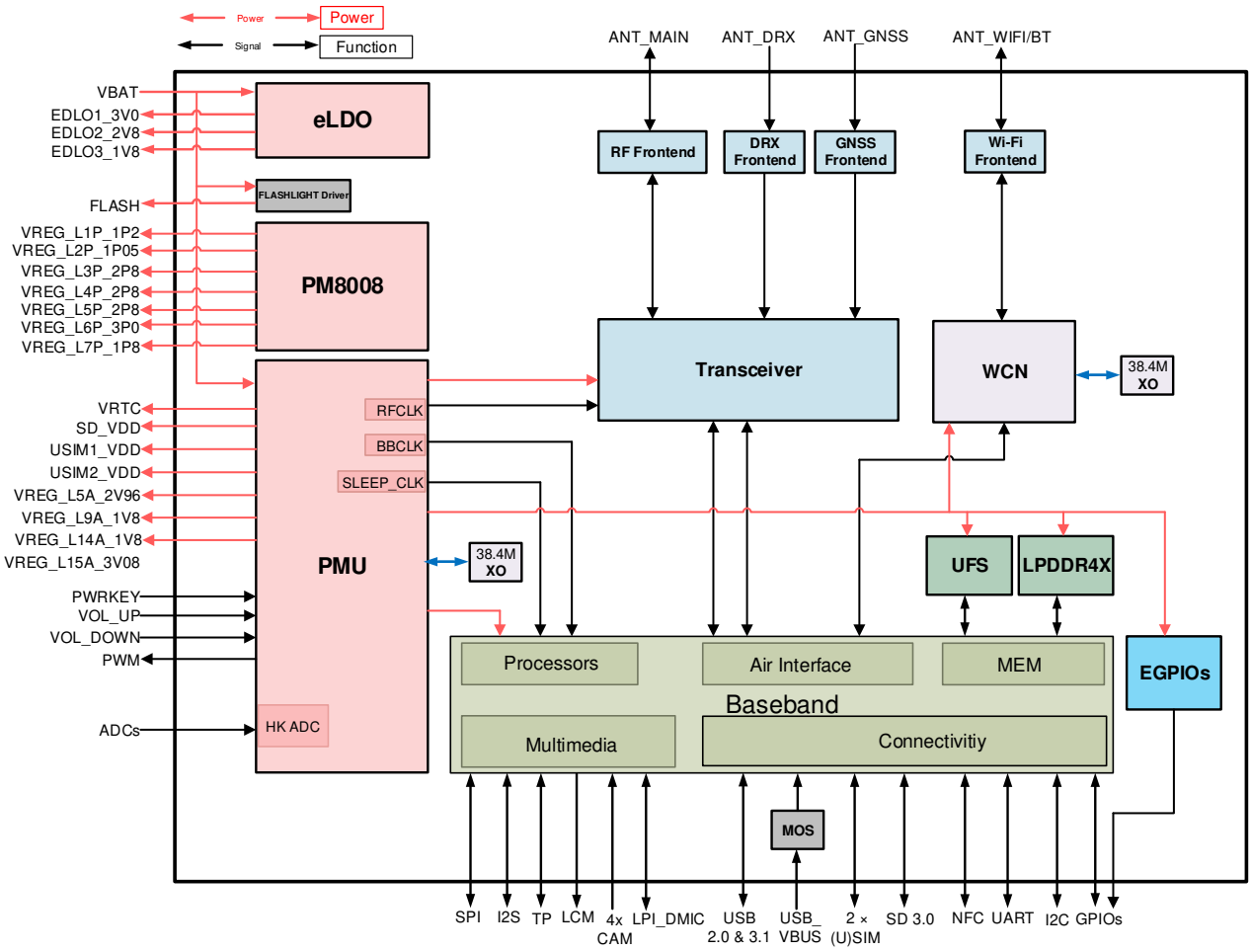


Figure 1: Functional Diagram

2.4. Pins Assignment

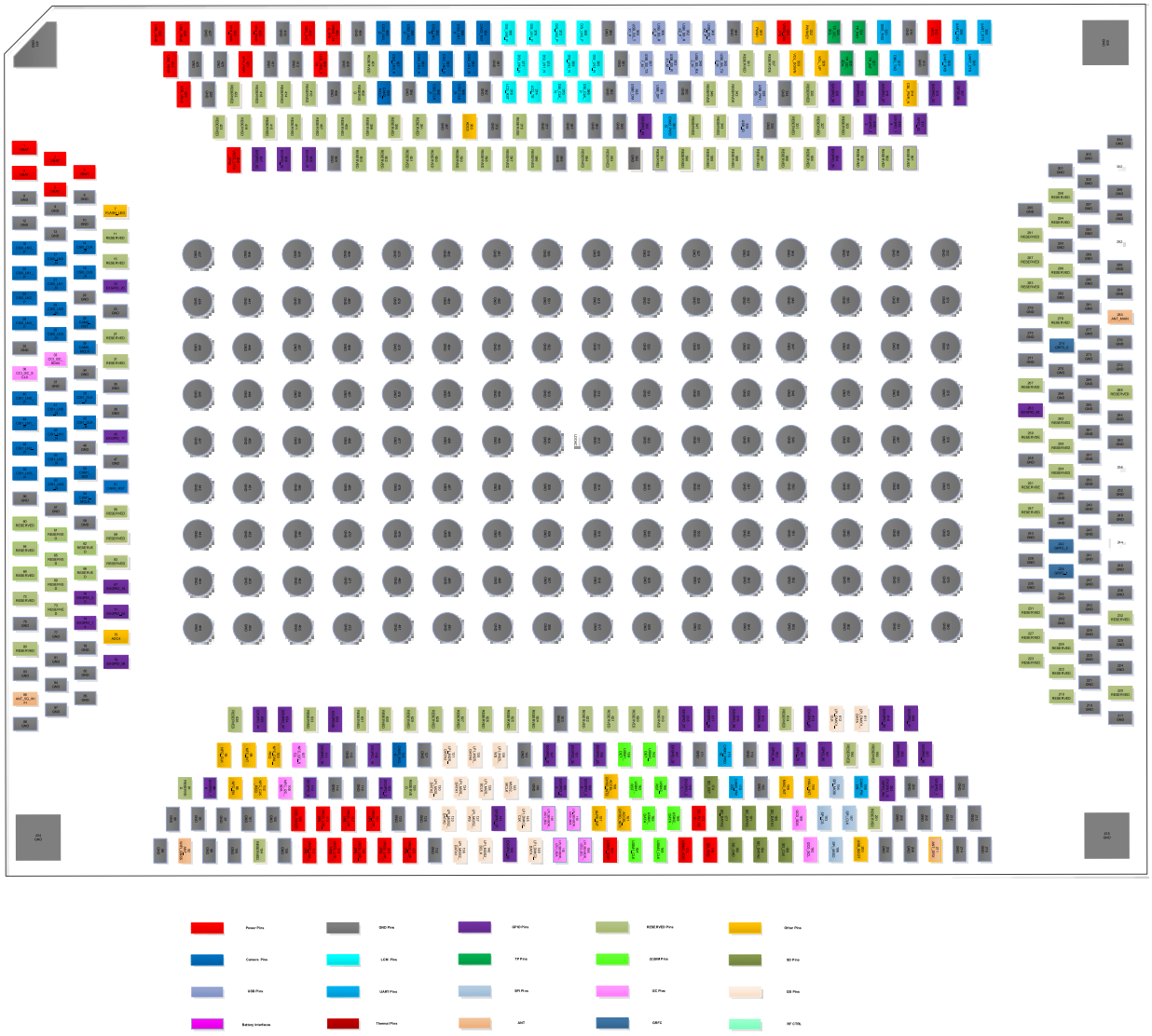


Figure 2: Pins Assignment (Top View)

NOTE

1. Keep all RESERVED pins unconnected.
2. All GND pins should be connected to the ground unless otherwise specified.

2.5. Pins Description

Table 5: Parameters Definition

Parameters	Descriptions
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output
PU	Pull Up
PD	Pull Down

DC characteristics include power domain and rated current in the table below.

Table 6: Pins Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	1–5	PIO	Power supply for the module	Vmin = 3.55 V Vnom = 4.0 V Vmax = 4.4 V	It must be able to provide sufficient current up to 5.0 A. It is suggested to add a TVS diode for surge protection.

VPH_PWR	420, 421, 424	PO	Power supply for peripherals	Vnom = VBAT	
LCD_IOVDD	109	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 300 mA	
VREG_L9A_1P8	112, 336	PO	1.8 V output for I/O power supply	Vnom = 1.8 V $I_O$max = 600 mA	
VREG_L3P_2P8	113	PO	2.8 V output	Vnom = 2.8 V $I_O$max = 300 mA	
VREG_14A_1V8	408	PO	1.8 V output for I/O power supply of sensor and LCM	Vnom = 1.8 V $I_O$max = 600 mA	
VREG_L15A_3P08	608	PO	3.0 V output	Vnom = 3.0 V $I_O$max = 150 mA	
LDO_2V8	409	PO	2.8 V output power for LCM	Vnom = 2.8 V $I_O$max = 500 mA	
VDD_3V0	412	PO	3.0 V output power for sensors and TP	Vnom = 3.0 V $I_O$max = 500 mA	
VRTC	312	PIO	Power supply for RTC	Vmin = 2.1 V Vnom = 3.0 V Vmax = 3.25 V	
GND	6, 8–10, 12, 13, 22, 23, 32, 34, 35, 37, 39, 46, 47, 56–58, 76–78, 81–85, 87–90, 93, 96, 97, 100, 101, 105, 108, 114, 115, 118, 125, 127, 129, 132, 143, 146, 171, 179, 182, 204–206, 208, 209, 212–218, 221, 224, 225, 228–230, 233–237, 239–241, 243, 245, 246, 248–250, 252, 253, 255, 257, 260, 261, 264–266, 269–273, 275–277, 279, 281, 282, 284, 285, 288–290, 293, 295–297, 299–301, 303, 304, 313, 316, 334, 335, 344, 350, 359, 361–364, 367, 371, 379, 381, 382, 387, 394, 404–406, 413, 416, 417, 425–428, 433–580, 592, 595, 604, 623				

Keypad Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	332	DI	Turn on/off the module	1.1 V	
VOL_DOWN	333	DI	Volume down	1.8 V	Cannot be multiplexed into generic GPIO.
VOL_UP	329	DI	Volume up		

USB Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	429–432	PIO	USB insertion interruption detect	Vnom = 5.0 V	A test point must be reserved.

USB_DP	354	AIO	USB0 2.0 differential data (+)	Requires differential impedance of 90 Ω. Complies with USB 2.0 specification. Supports OTG. Test points must be reserved.
USB_DM	358	AIO	USB0 2.0 differential data (-)	
USB_SS1_TX_P	360	AO	USB 3.1 channel 1 SuperSpeed transmit (+)	Requires differential impedance of 90 Ω. Complies with USB 3.1 Gen 1 specification.
USB_SS1_TX_M	357	AO	USB 3.1 channel 1 SuperSpeed transmit (-)	
USB_SS1_RX_P	356	AI	USB 3.1 channel 1 SuperSpeed receive (+)	
USB_SS1_RX_M	353	AI	USB 3.1 channel 1 SuperSpeed receive (-)	
USB_SS2_TX_P	348	AO	USB 3.1 channel 2 SuperSpeed transmit (+)	
USB_SS2_TX_M	345	AO	USB 3.1 channel 2 SuperSpeed transmit (-)	
USB_SS2_RX_P	352	AI	USB 3.1 channel 2 SuperSpeed receive (+)	
USB_SS2_RX_M	349	AI	USB 3.1 channel 2 SuperSpeed receive (-)	
USB_CC1	339	AI	USB Type-C detect 1	When Micro-USB mode is used, this pin can be used as USB_ID.
USB_PHY_PS	338	DI	Configuration channel status detection	When Micro-USB mode is used, this pin should be connected to the ground through a 1 kΩ resistor.

LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DSI_CLK_P	366	AO	LCD MIPI clock (+)		Requires differential impedance of 85 Ω.
DSI_CLK_N	370	AO	LCD MIPI clock (-)		
DSI_LN0_P	380	AO	LCD MIPI lane 0 data (+)		
DSI_LN0_N	377	AO	LCD MIPI lane 0 data (-)		
DSI_LN1_P	376	AO	LCD MIPI lane 1 data (+)		
DSI_LN1_N	373	AO	LCD MIPI lane 1 data (-)		
DSI_LN2_P	372	AO	LCD MIPI lane 2 data (+)		
DSI_LN2_N	369	AO	LCD MIPI lane 2 data (-)		
DSI_LN3_P	368	AO	LCD MIPI lane 3 data (+)		
DSI_LN3_N	365	AO	LCD MIPI lane 3 data (-)		
LCD_TE	374	DI	LCD tearing effect	VREG_L9A_1P8	
LCD_RST	378	DO	LCD reset		
PWM	340	DO	PWM output		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_P	14	AI	MIPI CSI0 clock (+)		Require differential impedance of 85 Ω.
CSI0_CLK_N	18	AI	MIPI CSI0 clock (-)		
CSI0_LN0_P	16	AI	MIPI CSI0 lane 0 data (+)		
CSI0_LN0_N	17	AI	MIPI CSI0 lane 0 data (-)		
CSI0_LN1_P	20	AI	MIPI CSI0 lane 1 data (+)		
CSI0_LN1_N	21	AI	MIPI CSI0 lane 1 data (-)		

CSI0_LN2_P	24	AI	MIPI CSI0 lane 2 data (+)		
CSI0_LN2_N	25	AI	MIPI CSI0 lane 2 data (-)		
CSI0_LN3_P	28	AI	MIPI CSI0 lane 3 data (+)		
CSI0_LN3_N	29	AI	MIPI CSI0 lane 3 data (-)		
CAM0_MCLK	30	DO	Master clock of camera 0		
CAM0_RST	26	DO	Reset of camera 0	VREG_L9A_1P8	
CAM0_PWDN	178	DO	Power down of camera 0		
CSI1_CLK_P	38	AI	MIPI CS1 clock (+)		
CSI1_CLK_N	42	AI	MIPI CSI1 clock (-)		
CSI1_LN0_P	40	AI	MIPI CSI1 lane 0 data (+)		
CSI1_LN0_N	41	AI	MIPI CSI1 lane 0 data (-)		
CSI1_LN1_P	44	AI	MIPI CSI1 lane 1 data (+)		Requires differential impedance of 85 Ω.
CSI1_LN1_N	45	AI	MIPI CSI1 lane 2 data (-)		
CSI1_LN2_P	48	AI	MIPI CSI1 lane 2 data (+)		
CSI1_LN2_N	49	AI	MIPI CSI1 lane 2 data (-)		
CSI1_LN3_P	52	AI	MIPI CSI1 lane 3 data (+)		
CSI1_LN3_N	53	AI	MIPI CSI1 lane 3 data (-)		
CAM1_MCLK	54	DO	Master clock of camera 1		
CAM1_RST	50	DO	Reset of camera 1	VREG_L9A_1P8	
CAM1_PWDN	198	DO	Power down of camera 1		
CSI2_CLK_P	390	AI	MIPI CSI2 clock (+)		Requires differential impedance of
CSI2_CLK_N	386	AI	MIPI CSI2 clock (-)		

CSI2_LN0_P	392	AI	MIPI CSI2 lane 0 data (+)		85 Ω.
CSI2_LN0_N	389	AI	MIPI CSI2 lane 0 data (-)		
CSI2_LN1_P	388	AI	MIPI CSI2 lane 1 data (+)		
CSI2_LN1_N	385	AI	MIPI CSI2 lane 1 data (-)		
CSI2_LN2_P	396	AI	MIPI CSI2 lane 2 data (+)		
CSI2_LN2_N	393	AI	MIPI CSI2 lane 2 data (-)		
CSI2_LN3_P	400	AI	MIPI CSI2 lane 3 data (+)		
CSI2_LN3_N	397	AI	MIPI CSI2 lane 3 data (-)		
CAM2_MCLK	398	DO	Master clock of camera 2		
CAM2_RST	384	DO	Reset of camera 2		
CAM2_PWDN	351	DO	Power down of camera 2		
CAM3_MCLK	123	DO	Master clock of camera 3	VREG_L9A_1P8	
CAM3_RST	51	DO	Reset of camera 3		
CAM3_PWDN	175	DO	Power down of camera 3		
CCI_I2C_SDA0	33	OD	I2C clock of camera 0 and 3		
CCI_I2C_SCL0	36	OD	I2C data of camera 0 and 3		
VREG_L1P_1P05	116	PO	DVDD for cameras 2	Vnom = 1.05 V $I_O$max = 800 mA	
VREG_L7P_1P8	117	PO	DOVDD for cameras 0, 1, 2 and 3	Vnom = 1.1 V $I_O$max = 300 mA	
VREG_L6P_2P8	120	PO	DOVDD for cameras 1, 2 and 3	Vnom = 2.8 V $I_O$max = 300 mA	
VREG_L2P_1P1	121	PO	DVDD for cameras 0 and 3	Vnom = 2.9 V $I_O$max = 800 mA	
VREG_L4P_2P9	124	PO	DOVDD for camera 0	Vnom = 2.8 V $I_O$max = 300 mA	

VREG_L5P_2P8	128	PO	AFVDD for cameras 0, 1, 2	Vnom = 1.8 V $I_O$max = 300 mA	
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	160	PO	(U)SIM1 card power supply	Iomax = 150mA Low-voltage: Vmax = 1.85 V Vmin = 1.75 V High-voltage: Vmax = 3.1 V Vmin = 2.8 V	Can recognize 1.8 V or 2.95 V (U)SIM card automatically.
USIM1_DATA	165	DIO	(U)SIM1 card data	USIM1_VDD	Pull it up to USIM1_VDD with an external 10 kΩ resistor. Cannot be multiplexed into generic GPIOs.
USIM1_CLK	164	DO	(U)SIM1 card clock		Cannot be multiplexed into generic GPIOs.
USIM1_RST	162	DO	(U)SIM1 card reset		
USIM1_DET	159	DI	(U)SIM1 card hot-plug detect	VREG_L9A_1P8	Active low. Externally pull it up to 1.8 V. If unused, keep it open.
USIM2_VDD	172	PO	(U)SIM2 card power supply	Iomax = 150mA Low-voltage: Vmax = 1.85 V Vmin = 1.75 V High-voltage: Vmax = 3.1 V Vmin = 2.8 V	Can recognize 1.8 V or 2.95 V (U)SIM card automatically.
USIM2_DATA	169	DIO	(U)SIM2 card data	USIM2_VDD	Pull it up to USIM2_VDD with an external 10 kΩ resistor. Cannot be multiplexed into generic GPIOs.
USIM2_CLK	168	DO	(U)SIM2 card clock		Cannot be

USIM2_RST	166	DO	(U)SIM2 card reset		multiplexed into generic GPIOs.
USIM2_DET	163	DI	(U)SIM2 card hot-plug detect	VREG_L9A_1P8	Active low. Externally pull it up to 1.8 V. If unused, keep it open.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	188	DO	SD card clock	SD_PU_VDD	Control characteristic impedance as 45 Ω.
SD_CMD	180	DIO	SD card command		
SD_DATA0	184	DIO	SDIO data bit 0		
SD_DATA1	185	DIO	SDIO data bit 1		
SD_DATA2	177	DIO	SDIO data bit 2		
SD_DATA3	181	DIO	SDIO data bit 3		
SD_DET	174	DI	SD card hot-plug detect	VREG_L9A_1P8	Active low by default. External 1.8 V pull-up is required.
SD_VDD	176	PO	Power supply for SD card	Vnom = 2.95 V $I_O$max = 600 mA	
SD_PU_VDD	173	PO	SD card pull-up power supply; 1.8/2.95 V output	Vnom = 1.8/2.95 V $I_O$max = 50 mA	Only for SD card pull-up.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	317	DO	Debug UART transmit	VREG_L9A_1P8	Cannot be multiplexed into generic GPIOs. If not used, keep them unconnected. Test points must be reserved.
DBG_RXD	320	DI	Debug UART receive		
UART_TXD	308	DO	UART transmit		If not used, keep them unconnected.
UART_RXD	309	DI	UART receive		

UART_RTS	305	DO	Request to send signal from the module		
UART_CTS	306	DI	Clear to send signal to the module		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C0_SCL	192	OD	I2C serial clock	VREG_L9A_1P8	External 1.8 V pull-up is required. If not used, keep them unconnected.
I2C0_SDA	189	OD	I2C serial data		
I2S Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MI2S2_MCLK	142	DO	I2S master clock	VREG_L9A_1P8	
LPI_MI2S2_SCLK	140	DO	I2S serial clock		
LPI_MI2S2_WS	137	DO	I2S word select		
LPI_MI2S2_DATA0	133	DIO	I2S data channel 0		
LPI_MI2S2_DATA1	136	DIO	I2S data channel 1		
LPI_MI2S_SCLK	138	DO	LPI I2S serial clock		
LPI_MI2S_WS	139	DO	LPI I2S word select		
LPI_MI2S_DATA0	135	DIO	LPI I2S data channel 0		
LPI_MI2S_DATA1	134	DIO	LPI I2S data channel 1		
LPI_MI2S_DATA2	130	DIO	LPI I2S data channel 2		
LPI_MI2S_DATA3	131	DIO	LPI I2S data channel 3		
DMIC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LPI_DMIC1_CLK	145	DO	LPI digital MIC1 clock	VREG_L9A_1P8	

LPI_DMIC1_DATA	148	DI	LPI digital MIC1 data		
LPI_DMIC2_CLK	612	DO	LPI digital MIC2 clock		
LPI_DMIC2_DATA	611	DI	LPI digital MIC2 data		
TP Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_RST	324	DO	TP reset	VREG_L9A_1P8	
TP_INT	321	DI	TP interrupt		
TP_I2C_SCL	328	OD	TP I2C clock		
TP_I2C_SDA	325	OD	TP I2C data		
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	197	DO	SPI clock	VREG_L9A_1P8	Supports master mode only.
SPI_CS	193	DO	SPI chip select		
SPI_MISO	196	DI	SPI master-in slave-out		
SPI_MOSI	194	DO	SPI master-out slave-in		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC4	75	AI	General-purpose ADC interface		
ADC5	383	AI			

Sensor Interrupt Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ACCEL_GYRO_INT1	161	DI	Acceleration/ gyroscope sensor interrupt 1	VREG_L9A_1P8	
ACCEL_GYRO_INT2	158	DI	Acceleration/ gyroscope sensor interrupt 2		
MAG_INT	186	DI	Geomagnetic sensor interrupt		
ALPS_INT	157	DI	Light/proximity sensor interrupt		
HALL_INT	190	DI	Hall sensor interrupt		
SENSOR_I2C1_SDA	152	OD	I2C data 1 for external sensor	VREG_L9A_1P8	External 1.8 V pull-up is required. If not used, keep them unconnected.
SENSOR_I2C1_SCL	149	OD	I2C clock 1 for external sensor		
SENSOR_I2C2_SDA	153	OD	I2C data 2 for external sensor		
SENSOR_I2C2_SCL	156	OD	I2C clock 2 for external sensor		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EXGPIO_20	19	DIO	General-purpose input/output	VREG_L9A_1P8	
EXGPIO_11	43	DIO			
EXGPIO_15	67	DIO			
EXGPIO_05	70	DIO			
EXGPIO_04	71	DIO			

EXGPIO_14	74	DIO		
EXGPIO_08	79	DIO		
EXGPIO_16	94	DIO		
EXGPIO_9	110	DIO		
EXGPIO_10	111	DIO		
EXGPIO_19	119	DIO		
EXGPIO_26	122	DIO		
EXGPIO_07	141	DIO		
EXGPIO_06	144	DIO		
EXGPIO_31	147	DIO		
EXGPIO_24	150	DIO		
EXGPIO_34	151	DIO		
EXGPIO_25	154	DIO		
EXGPIO_23	155	DIO		
EXGPIO_32	167	DIO		
EXGPIO_21	170	DIO		
GPIO_108	178	DIO		
GPIO_69	183	DIO		
GPIO_70	187	DIO		
QUP_GPIO_05	191	DIO		
QUP_GPIO_04	198	DIO		
EXGPIO_12(Compatibility GPIO_44)	202	DIO		
EXGPIO_17	203	DIO		
EXGPIO_28	207	DIO		

EXGPIO_13	210	DIO		
EXGPIO_42	263	DIO		
GPIO_84	307	DIO		
EXGPIO_33	310	DIO		
GPIO_83	311	DIO		
EXGPIO_18	315	DIO		
EXGPIO_27	318	DIO		
EXGPIO_22	319	DIO		
EXGPIO_29	322	DIO		
EXGPIO_30	326	DIO		
GPIO_52	351	DIO		
EXGPIO_43	355	DIO		
EXGPIO_35	583	DIO		
EXGPIO_01	605	DIO		
EXGPIO_02	606	DIO		
EXGPIO_03	607	DIO		
EXGPIO_41	609	DIO		
EXGPIO_40	610	DIO		
EXGPIO_45	613	DIO		
EXGPIO_38	615	DIO		
EXGPIO_39	616	DIO		
EXGPIO_36	617	DIO		
EXGPIO_37	618	DIO		
EXGPIO_46	632	DIO		
EXGPIO_47	634	DIO		

EXGPIO_44	635	DIO			
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	280	AIO	Main antenna interface		50 Ω impedance.
ANT_DRX	211	AI	Diversity antenna interface		
ANT_2.4G_WIFI_GNSS	92	AIO	GNSS/WIFI2.4G/ Bluetooth antenna interface		
ANT_5G_WIFI	86	AIO	WIFI 5G antenna interface		
ANT_2.4G_WIFI_GNSS	92	AIO	GNSS/WIFI 2.4G/ Bluetooth antenna interface		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH_LED	7	AO	Flash/torch driver output	$I_O$max = 1 A	
USB_BOOT	200	DI	Force the module into download mode	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
CBL_PWR_N	314	DI	Initiate turning-on when grounded		The module cannot be turned off when this pin is pulled down. If unused, keep it open.
Reserved Pins					
Pin Name	**Pin Name**				**Pin Name**
RESERVED	11, 15, 27, 31, 55, 59~66, 68, 69, 72, 73, 80, 91, 104, 126, 195, 199, 201, 219, 220, 222, 223, 226, 227, 231, 232, 247, 251, 254, 258, 259, 262, 267, 268, 278, 283, 286, 287, 291, 294, 298, 323, 327, 330, 331, 337, 341~343, 346, 347, 375, 395, 300, 391, 399, 401~403, 407, 410, 415, 418, 419, 422, 423, 581, 582, 584~591, 593, 594, 596~603, 614, 619~622, 624~631, 633, 636				Keep these pins open.

2.6. EVB Kit

We supplie an evaluation board (Smart EVB G5) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Interface

The module provides five VBAT pins, which are dedicated for connection to external power supply. The power supply range of the module is 3.55–4.4 V, and the recommended value is 3.8 V. VPH_PWR is used for powering peripherals.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	1–5	PIO	Power supply for the module	3.55	3.8	4.4	V

3.1.2. Reference Design for Power Supply

The power source is critical to the module's performance. The power supply of the module should be able to provide sufficient current of 5 A at least. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for 5 V input power supply:

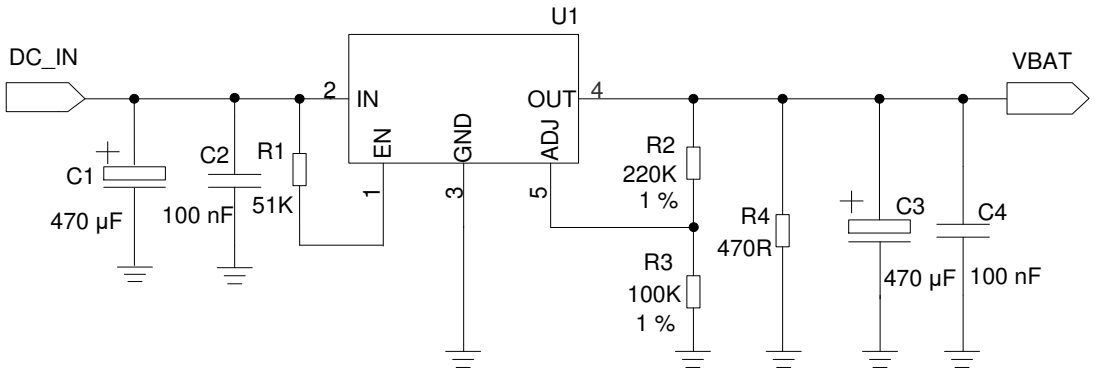


Figure 3: Reference Design of Power Input

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY, then you can cut off the power supply.

3.1.3. Requirements for Voltage Stability

The recommended power supply voltage of the module is 3.8 V. The power supply performance, such as load capacity, voltage ripple will directly influence the module's performance and stability. Under ultimate conditions, the module may have a transient peak current up to 5 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.2 V, the module will turn off automatically. Therefore, ensure the input voltage never drops below 3.2 V.

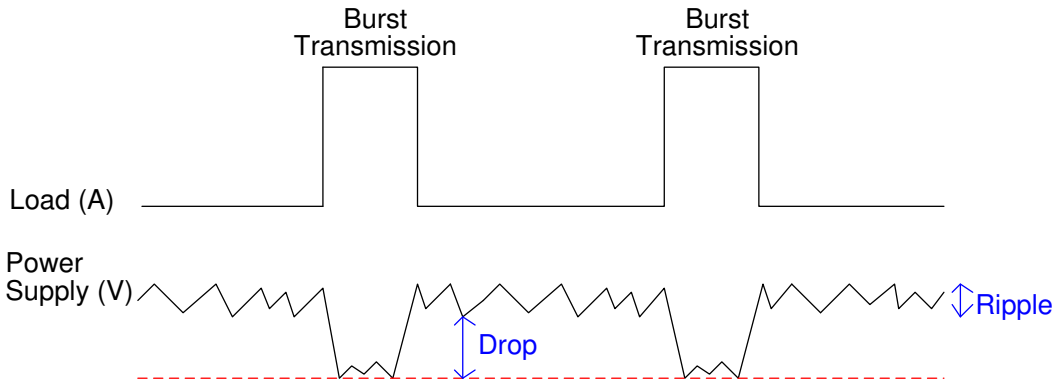


Figure 4: Power Supply Limits During Burst Transmission

To prevent the voltage from dropping below 3.2 V, it is recommended to connect a 100 µF bypass capacitor with low ESR as well as 100 nF, 33 pF and 10 pF and 4.7uF filter capacitors in parallel near the VBAT pins of the module. It is also recommended that the PCB traces of VBAT should be as short as possible and wide enough to reduce the equivalent impedance of the VBAT traces and ensure that there will be no large voltage drop under high current at the maximum transmission power. The width of VBAT trace should be at least 5 mm. As per design rules, the longer the VBAT trace is, the wider it should be. Additionally, the ground plane of the power supply part should be as complete as possible.

In addition, in order to get a stable power source, it is suggested to use a TVS diode and place it as close to the VBAT pin as possible to enhance surge protection. The following figure shows the structure of the power supply.

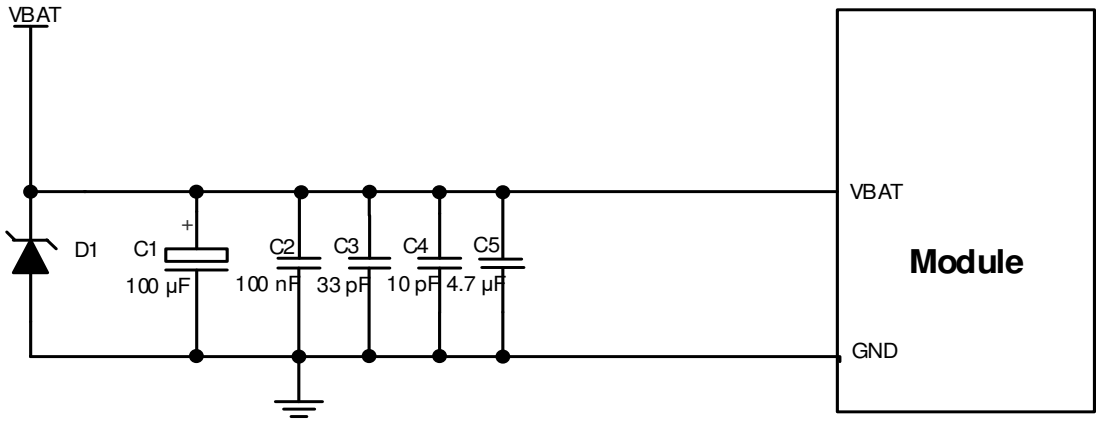


Figure 5: Reference Design of Power Supply

3.2. Turn On

3.2.1. Turn On with PWRKEY

Table 8: Pins Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	332	DI	Turn on/off the module	PWRKEY

When powering up the VBAT, it can be turned on by driving PWRKEY low for at least 1.6 s. It is recommended to use an open drain/collector driver to control the PWRKEY. PWRKEY is pulled up to VBAT internally.

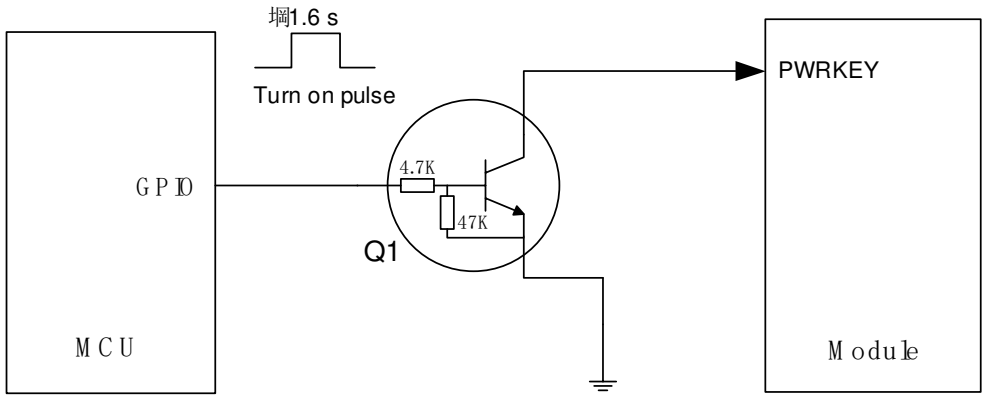


Figure 6: Reference Design of Turn On with Driving Circuit

Another way to control the PWRKEY is using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from finger. Therefore, you should place a TVS component near the keystroke for ESD protection. Additionally, a 1 kΩ resistor is connected in series to PWRKEY for ESD protection.

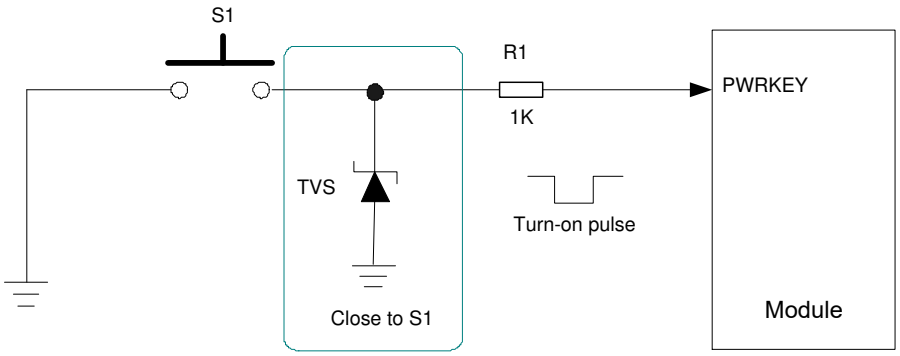


Figure 7: Reference Design of Turn On with Keystroke

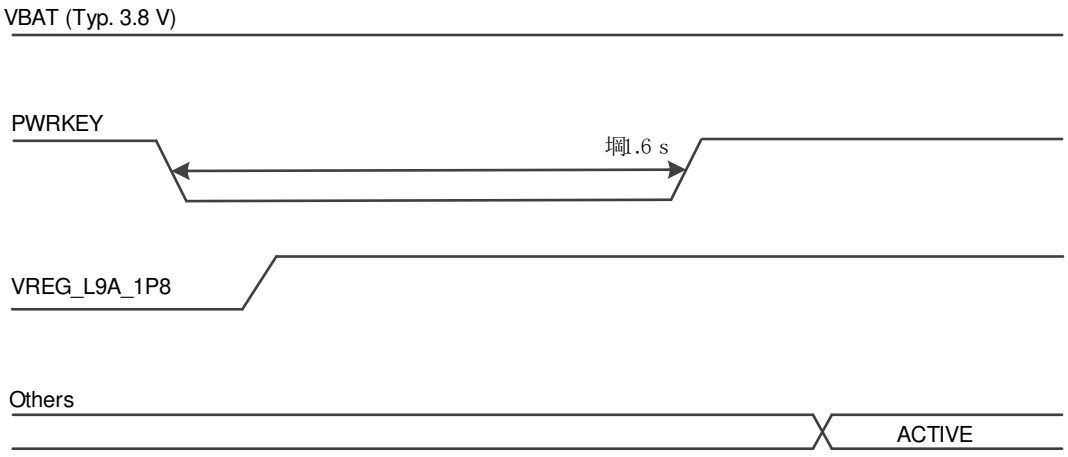


Figure 8: Timing of Turn On with PWRKEY

NOTE

1. When the module is powered up for the first time, its turn on timing may be different from that shown in the figure above.
2. Ensure the voltage of VBAT is stable before driving the PWRKEY low. It is recommended to drive PWRKEY low after VBAT reaches 3.8 V and remains stable for 30 ms. PWRKEY cannot be driven low all the time.

3.2.2. Turn On Automatically with CBL_PWR_N

Table 9: Pins Description of CBL_PWR_N

Pin Name	Pin No.	I/O	Description	Comment
CBL_PWR_N	314	DI	Initiate power-on when grounded	The module cannot be turned off when this pin is pulled down. If unused, keep it open.

The module can turn on automatically through CBL_PWR_N:

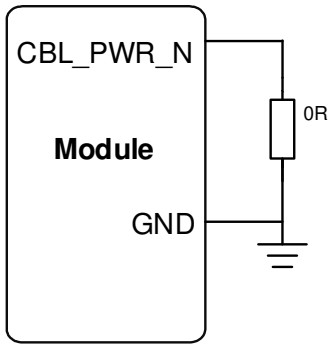


Figure 9: Reference Design of Turn On with CBL_PWR_N

NOTE

If the module turns on automatically through CBL_PWR_N, it cannot be turned off manually. In such case, it can be turned off only by cutting off the power supply of the system.

3.3. Restart/Turn Off

The module can be turned off by driving the PWRKEY pin low for at least 0.6 s. Choose whether to turn off the module when the prompt window comes up.

The other way to turn off the module is to drive PWRKEY low for at least 8 s. The module will execute the forced shut-down. The forced power-down scenario is illustrated in the following figure.

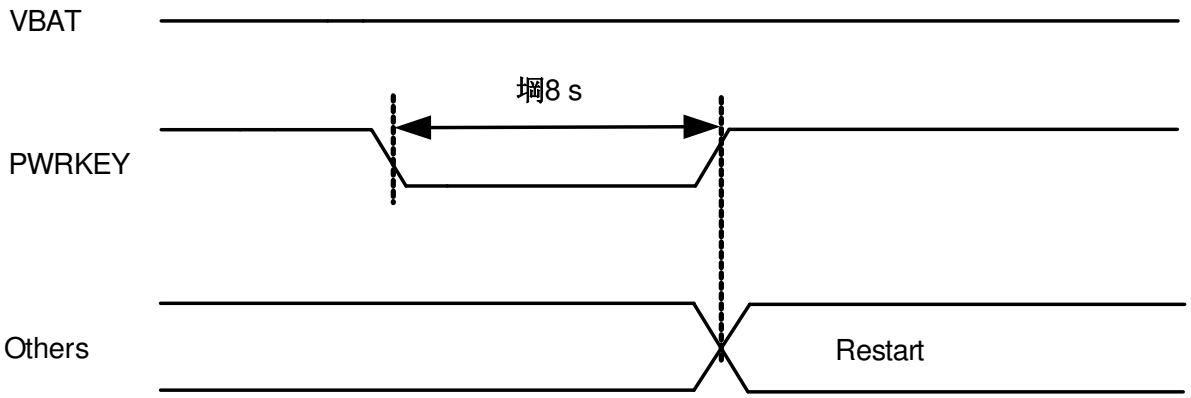


Figure 10: Timing of Restart

3.4. VRTC

Pin Name	Pin No.	I/O	Description	Comment
VRTC	312	PIO	Power supply for RTC	Power supply for RTC

The RTC of the module can be powered by an external power supply pin VRTC. When VBAT is disconnected and you need to reserve RTC function, then VRTC cannot be kept unconnected. The RTC can be powered by an external power source when the module is powered down and there is no power supply for the VBAT. The power source can be an external battery or capacitor according to application demands. The following are some reference circuit designs when an external battery or capacitor is utilized for powering RTC.

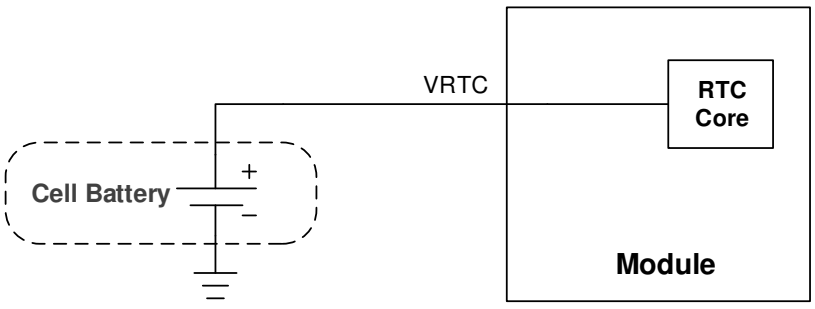


Figure 11: RTC Powered by Rechargeable Cell Battery

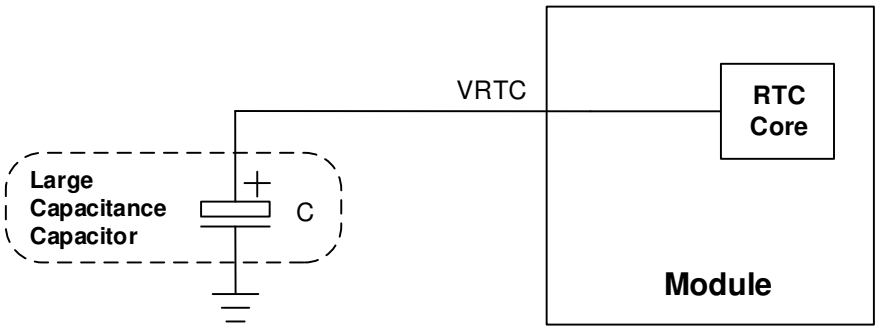


Figure 12: RTC Powered by Large Capacitance Capacitor

If RTC fails, the module can synchronize time over the network after being powering up.

- The recommended input voltage range for VRTC is 2.1–3.25 V and the recommended typical value is 3 V.
- When powered by VBAT, the RTC deviation is 50 ppm. When powered by VRTC, the RTC deviation is about 200 ppm.
- If a rechargeable battery is used, ESR of the battery should be less than 2 kΩ.
- If you do not need RTC function, a 4.7 μF capacitor need to be connected to VRTC.

3.5. Power Output

The module supports multiple regulated voltage output for peripheral circuits. In practical application, it is recommended to use a 10-pF and a 33-pF capacitor in parallel to suppress high-frequency noise.

Table 10: Power Information

Pin Name	Default Voltage (V)	Drive Current (mA)	Standby
VREG_L9A_1P8	1.8	600	Keeps ON
VREG_L14A_1V8	1.8	600	-
VREG_L15A_3P08	3.08	150	-
VREG_L1P_1P2	1.2	600	-
VREG_L2P_1P05	1.1	600	-
VREG_L3P_2P8	2.8	300	-
VREG_L4P_2P8	2.8	300	-

VREG_L5P_2P8	2.8	300	-
VREG_L6P_3P0	3.0	300	-
VREG_L7P_1P8	1.8	300	-
LDO_IOVDD	1.8	300	-
LDO_2V8	2.8	500	-
VDD_3V0	3.0	500	-

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface which complies with USB 3.1 Gen 1 and USB 2.0 specifications and supports USB OTG. It supports USB Type-C interface, DisplayPort mode and Micro USB interface. It also supports SuperSpeed mode (5 Gbps) for USB 3.1 Gen 1, high-speed (480 Mbps) and full-speed (12 Mbps) modes for USB 2.0. The USB interface is used for AT command transmission, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB.

4.1.1. Type-C Interface

4.1.1.1.Type-C Mode

Table 11: Pins Description of USB Type-C Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	429–432	PIO	USB insertion interruption detect	A test point must be reserved.
USB_DP	354	AIO	USB0 2.0 differential data (+)	Requires differential impedance of 90 Ω. Complies with USB 2.0 specification. Supports OTG. Test points must be reserved.
USB_DM	358	AIO	USB0 2.0 differential data (-)	
USB_SS1_TX_P	360	AO	USB 3.1 channel 1 SuperSpeed transmit (+)	Requires differential impedance of 90 Ω. Complies with USB 3.1 Gen 1 specification.
USB_SS1_TX_M	357	AO	USB 3.1 channel 1 SuperSpeed transmit (-)	
USB_SS1_RX_P	356	AI	USB 3.1 channel 1 SuperSpeed receive (+)	

USB_SS1_RX_M	353	AI	USB 3.1 channel 1 SuperSpeed receive (-)	
USB_SS2_TX_P	348	AO	USB 3.1 channel 2 SuperSpeed transmit (+)	
USB_SS2_TX_M	345	AO	USB 3.1 channel 2 SuperSpeed transmit (-)	
USB_SS2_RX_P	352	AI	USB 3.1 channel 2 SuperSpeed receive (+)	
USB_SS2_RX_M	349	AI	USB 3.1 channel 2 SuperSpeed receive (-)	
USB_CC1	339	AI	USB Type-C detect 1	When Micro-USB mode is used, this pin can be used as USB_ID.
USB_PHY_PS	338	DI	Configuration channel status detection	When Micro-USB mode is used, this pin should be connected to the ground through a 1 kΩ resistor.

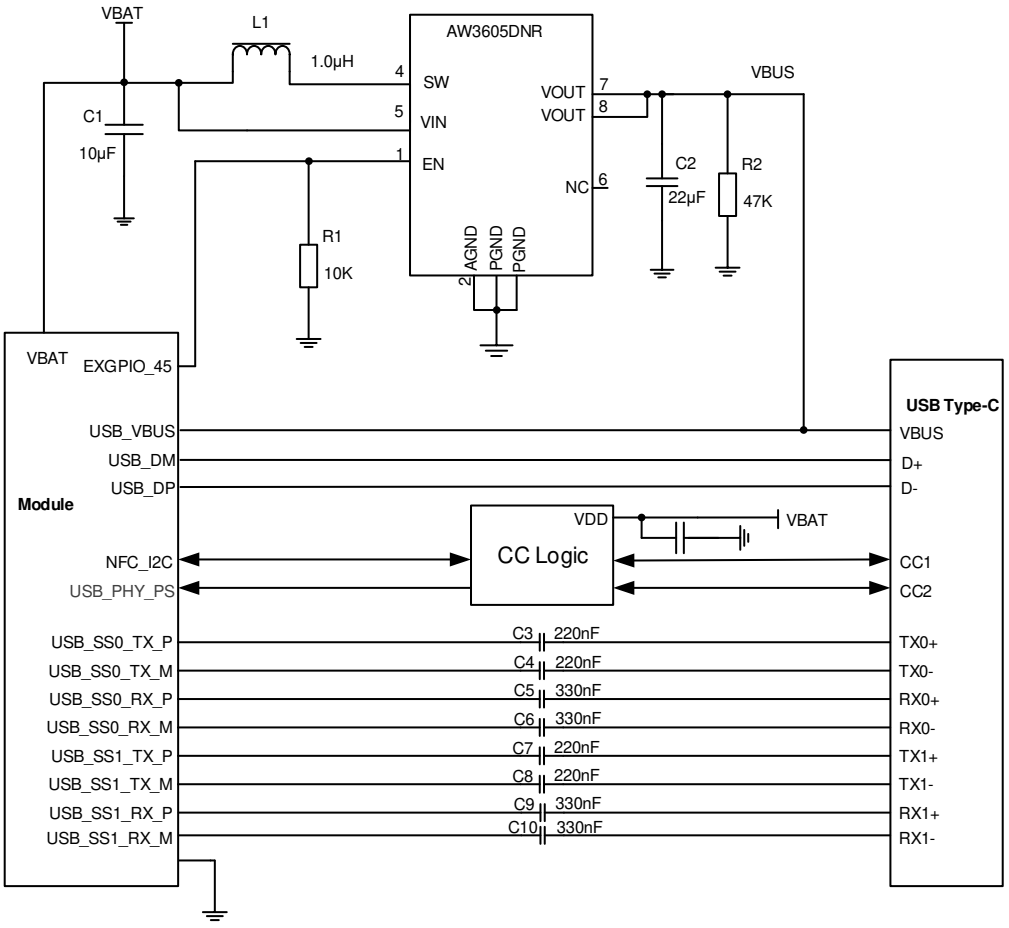


Figure 13: Reference Design of USB Type-C Mode

The USB interface of the module supports OTG function. If this function is required, please follow the design above to add an external 5 V power supply.

4.1.2. Micro USB Interface

The following table shows the pin definition of Micro USB interface:

Table 12: Pins Description of Micro USB

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	429–432	PIO	USB insertion interruption detect	A test point must be reserved.
USB_DP	354	AIO	USB0 2.0 differential data (+)	Requires differential impedance of 90 Ω. Complies with USB 2.0 specification. Supports OTG. Test points must be reserved.
USB_DM	358	AIO	USB0 2.0 differential data (-)	
USB_CC1	339	AI	USB Type-C detect 1	When Micro-USB mode is used, this pin can be used as USB_ID.

The reference design of Micro USB interface configured with USB is shown below:

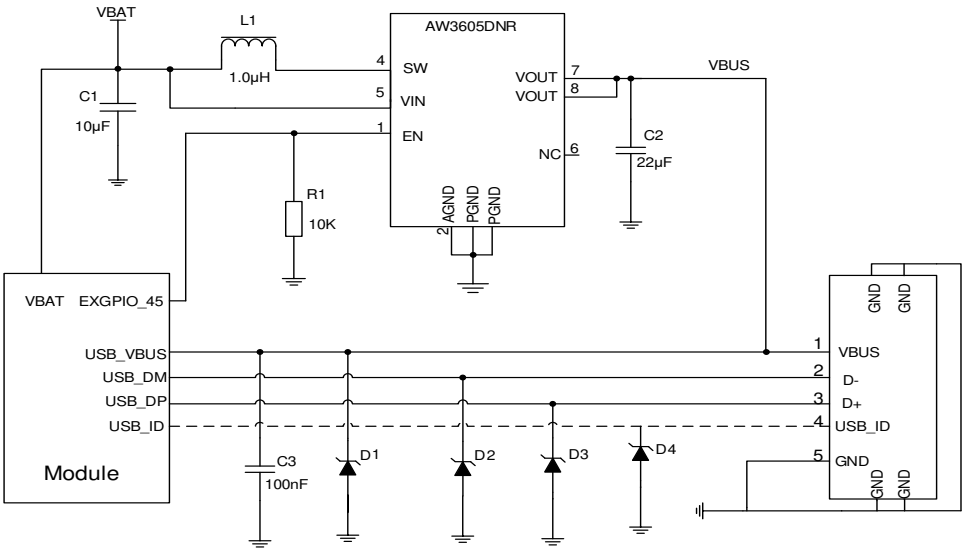


Figure 14: Reference Design of Micro USB Interface

In the design of USB 2.0 interface, it is suggested to connect USB_ID pin directly to USB_ID of the external Micro USB interface to detect USB ID. When inserted device of the external Micro USB interface is in slave mode, USB_ID will output low voltage level to pull USB_ID down and then notice the module to enter master mode.

4.1.3. USB Interfaces Design Considerations

Table 13: USB Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length	Length Mismatch
354	USB_DP	50.34	0.84
358	USB_DM	49.50	
360	USB_SS1_TX_P	33.74	-0.65
357	USB_SS1_TX_M	34.40	
356	USB_SS1_RX_P	35.04	-0.68
353	USB_SS1_RX_M	35.72	
348	USB_SS2_TX_P	37.97	0.19
345	USB_SS2_TX_M	37.78	
352	USB_SS2_RX_P	35.61	-0.70
349	USB_SS2_RX_M	36.31	

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC.
- The reference ground plane under the USB signal traces must be continuous without any cuts or vias to ensure impedance continuity.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, stray capacitance should be less than 2 pF for USB 2.0, and less than 0.5 pF for USB 3.1 Gen 1.

- Do not route USB 3.1 Gen 1 signal traces under RF signal traces. Crossing or being parallel with RF signal traces is forbidden. Isolation between USB 3.1 Gen 1 signals and RF signals should be over 90 dB. Otherwise, the RF signals will be seriously affected.
- For USB 3.1 Gen 1 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 0.7 mm.
- For USB 3.1 Gen 1, the clearance between Rx and Tx signal traces should be three times the signal trace width. The clearance between USB 3.1 Gen 1 signal traces and other signal traces should be four times the signal trace width.
- For USB 2.0 signal traces, the differential data pair matching (P/M) should be less than 2 mm.
- For USB 2.0, the clearance between DP and DM signal traces should be three times the signal trace width and the clearance between USB 2.0 signal traces and other signal traces should be four times the signal trace width.

4.2. USB_BOOT

The module provides a USB_BOOT for emergency download. Pulling up USB_BOOT to LAO9A_1V8 before turning on the module, and then the module will enter emergency download mode. This is an emergency option when failures such as abnormal start-up or running occur. For firmware upgrade and software debugging in the future, reserve the following reference design.

Table 14: Pins Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	1	DI	Force the module into download mode	Force the module to enter download mode by pulling this pin up to VREG_L9A_1P8 when the module is turning on. A test point is recommended to be reserved.

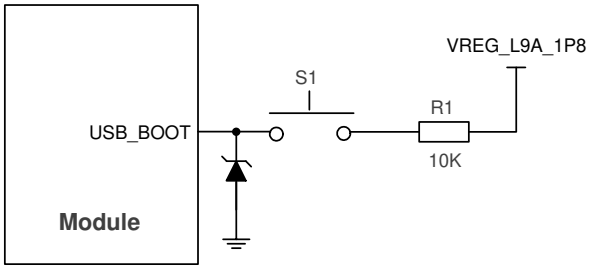


Figure 15: Reference Design of USB_BOOT

4.3. (U)SIM Interface

The (U)SIM interface meets ETSI and IMT-2000 requirements. Dual SIM Dual Standby function is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM card is powered by the internal power supply of the module.

Table 15: Pins Description of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	160	PO	(U)SIM1 card power supply	Can recognize 1.8 V or 2.95 V (U) SIM card automatically.
USIM1_DATA	165	DIO	(U)SIM1 card data	Pull it up to USIM1_VDD with an external 10 kΩ resistor. Cannot be multiplexed into generic GPIOs.
USIM1_CLK	164	DO	(U)SIM1 card clock	Cannot be multiplexed into generic GPIOs.
USIM1_RST	162	DO	(U)SIM1 card reset	
USIM1_DET	159	DI	(U)SIM1 card hot-plug detect	Active low. Externally pull it up to 1.8 V. If unused, keep it open.
USIM2_VDD	172	PO	(U)SIM2 card power supply	Can recognize 1.8 V or 2.95 V (U) SIM card automatically.
USIM2_DATA	169	DIO	(U)SIM2 card data	Pull it up to USIM2_VDD with an external 10 kΩ resistor. Cannot be multiplexed into generic GPIOs.
USIM2_CLK	168	DO	(U)SIM2 card clock	Cannot be multiplexed into generic GPIOs.
USIM2_RST	166	DO	(U)SIM2 card reset	
USIM2_DET	163	DI	(U)SIM2 card hot-plug detect	Active low. Externally pull it up to 1.8 V. If unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET. This function is disabled by default via software. To enable it, please contact Technical Support. A reference circuit for (U)SIM card interface with an 8-pin (U)SIM card connector is illustrated in the following figure.

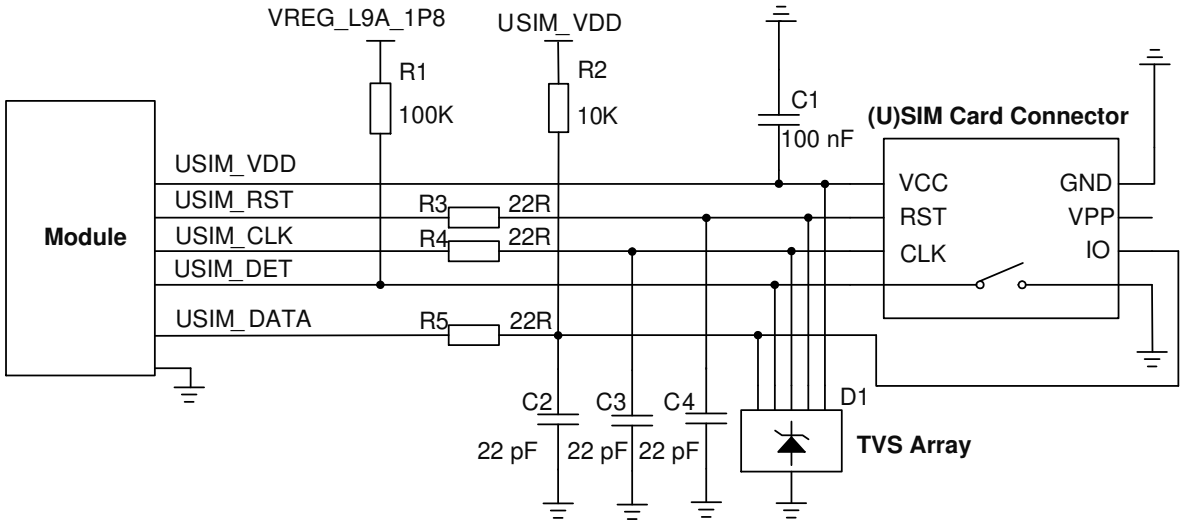


Figure 16: Reference Design of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the function of (U)SIM card hot-swap is not needed, keep USIM_DET disconnected.

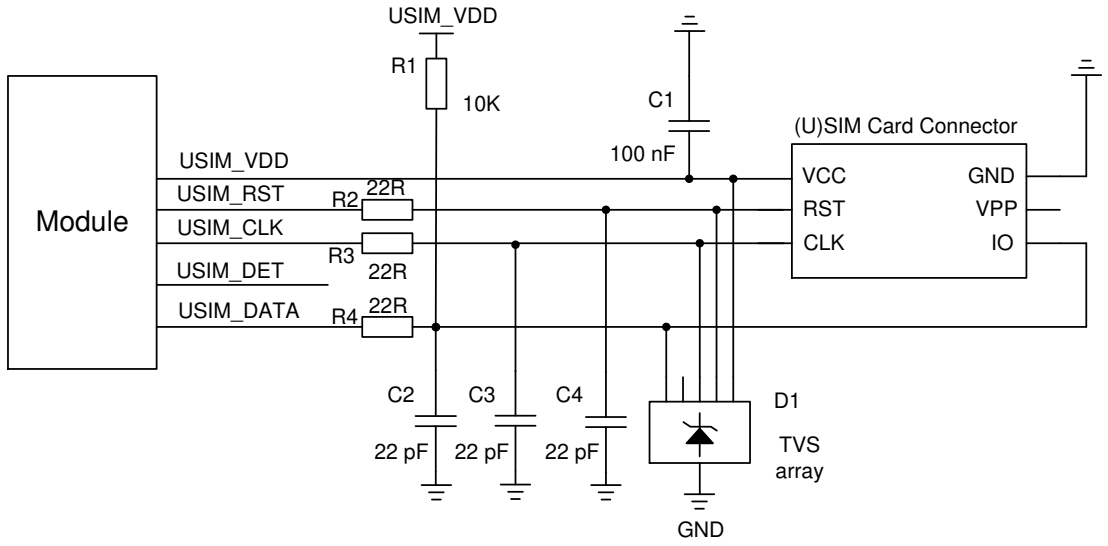


Figure 17: Reference Design of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, you should follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector close to the module. Keep the trace length less than 200 mm if possible.
- Route (U)SIM card traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals such as RF signals, analog signals, and noisy signals generated by clock, DC-DC.
- Ensure the tracing between the (U)SIM card connector and the module is short and wide. Keep the trace width of ground and USIM_VDD at least 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- Reserve a filter capacitor for USIM_VDD, and its maximum capacitance should not exceed 1 μF. Additionally, place the capacitor near the (U)SIM card connector.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should be less than 30 pF. Add 22 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 22 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference.
- For USIM_DATA, it is recommended to add a 10 kΩ pull-up resistor near the (U)SIM card connector to improve the anti-jamming capability of the (U)SIM card.

4.4. SD Card Interface

SD card interface of the module complies with SD 3.0 specifications:

Table 16: Pins Description of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	188	DO	SD card clock	Control characteristic impedance as 45 Ω.
SD_CMD	180	DIO	SD card command	
SD_DATA0	184	DIO	SDIO data bit 0	
SD_DATA1	185	DIO	SDIO data bit 1	
SD_DATA2	177	DIO	SDIO data bit 2	
SD_DATA3	181	DIO	SDIO data bit 3	
SD_DET	174	DI	SD card hot-plug detect	Active low by default. External 1.8 V pull-up is required.

SD_VDD	176	PO	Power supply for SD card	
SD_PU_VDD	173	PO	SD card pull-up power supply; 1.8/2.95 V output	Only for SD card pull-up.

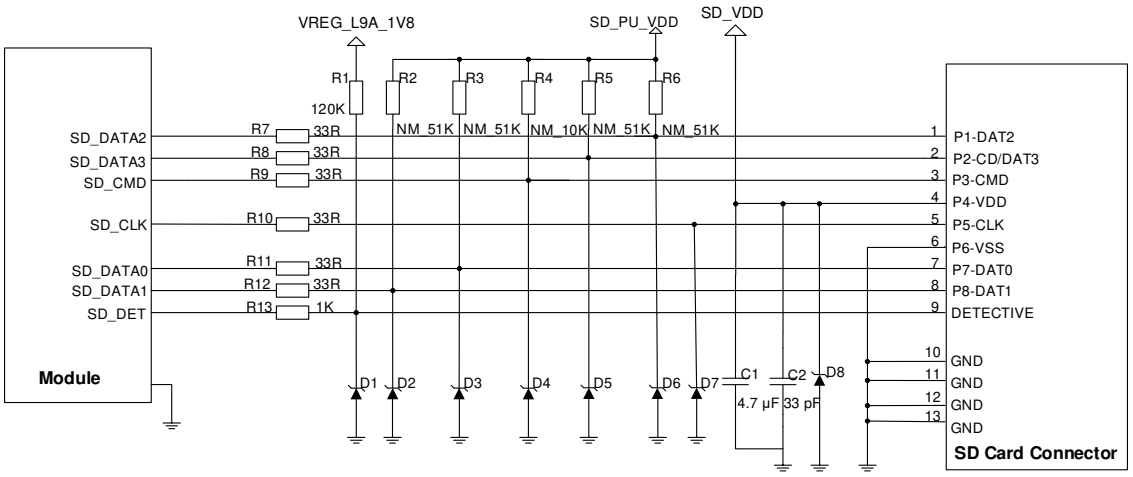


Figure 18: Reference Design of SD Card Interface

SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 600 mA. Because of the high drive current, it is recommended to keep the trace width as at least 0.6 mm. To ensure the stability of drive power, you should add a 4.7-µF and a 33-pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK and SD_DATA [0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of these traces as 45 Ω, shield them and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB and keep their lengths the same. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 45 Ω ±10 %, and add ground shielding.
- Trace length matching between SD_CLK and SD_CMD/SD_DATA should be less than 2 mm.
- Trace length requirements: less than 150 mm for SDR50 mode; less than 50 mm for SDR104 mode.
- Clearance between signal traces should be 1.5 times the trace width.
- The capacitive reactance of SD_DATA [0:3], SD_CLK and SD_CMD traces should be less than 8 pF.
- The capacitive reactance of D1–D7 should be less than 5 pF.

Table 17: SD Card Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length
188	SD_CLK	26.70
180	SD_CMD	28.94
184	SD_DATA0	29.97
185	SD_DATA1	30.18
177	SD_DATA2	29.20
181	SD_DATA3	29.20

4.5. UART

The module supports up to five groups of UART interfaces. Two of them are configured by default, see ***Table 18.*** Three of them are multiplexed from other interfaces, see ***Table 22***.

Two UART:

- UART0: 4-wire UART, supports RTS and CTS hardware flow control, up to 4 Mbps.
- Debug: 2-wire UART, used for debugging only.

Table 18: Pins Description of UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	317	DO	Debug UART transmit	If not used, keep them unconnected. Cannot be multiplexed into generic GPIOs. Test points must be reserved.
DBG_RXD	320	DI	Debug UART receive	
UART_TXD	308	DO	UART transmit	If not used, keep them unconnected.
UART_RXD	309	DI	UART receive	
UART_RTS	305	DO	Request to send signal from the module	
UART_CTS	306	DI	Clear to send signal to the module	

UART0 is a 4-wire UART with 1.8 V power domain. You can use a level-shifting chip between the module and host's UART if the host is equipped with a 3.3 V UART:

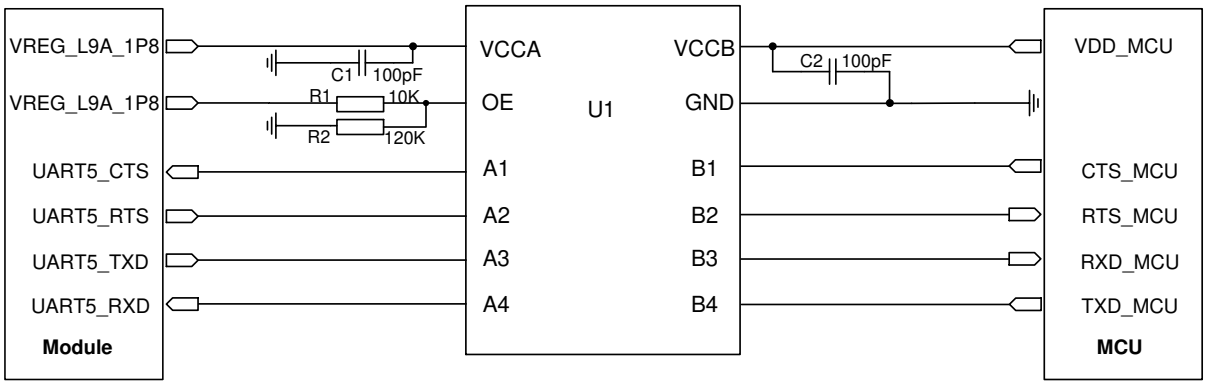


Figure 19: Reference Design of UART with Level-shifting Chip (for UART0)

The following circuit shows a reference design for the communication between the module and a PC with a standard RS-232 level-shifting chip:

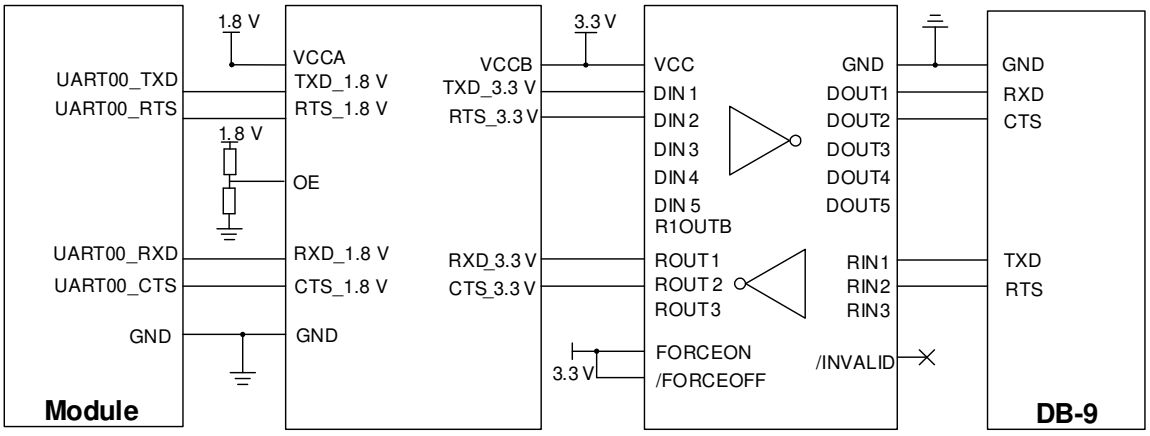


Figure 20: Reference Design of UART with RS-232 Level-shifting Chip (for UART0)

NOTE

Debug UART is similar to UART0. For the reference designs, refer to that of UART0.

4.6. SPI

The module provides five groups of SPI which only support master mode. It can be used for fingerprint recognition. One of them is default configuration, see ***Table 19***; The other four of them are multiplexed from other interfaces, see ***Table 23***.

Table 19: Pins Description of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	197	DO	SPI clock	1.8 V power domain. Supports master mode only.
SPI_CS	193	DO	SPI chip select	
SPI_MISO	196	DI	SPI master-in salve-out	
SPI_MOSI	194	DO	SPI master-out slave-in	

4.7. I2C Interface

The module supports up to nine groups of I2C interfaces. three of them are generic I2C interfaces, three of them are dedicated I2C interface, and three of them are multiplexed from other interfaces, see ***Table {num}***. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. SENSOR_I2C only supports sensors of ADSP architecture. CAM_I2C signals are controlled by Linux Kernel code and supports connection with video output related devices.

Table 20: Pins Description of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C0_SCL	192	OD	I2C serial clock	External 1.8 V pull-up is required. If not used, keep them unconnected.
I2C0_SDA	189	OD	I2C serial data	

4.8. I2S Interface

The module supports up to two groups of I2S interfaces. one of them are generic I2S interfaces. one of them are dedicated I2S interfaces used for audio. The reference power domain is 1.8 V, see ***Table {num}***.

Table 21: Pins Description of I2S Interface

Pin Name	Pin No.	I/O	Description
MI2S2_MCLK	142	DO	I2S master clock
LPI_MI2S2_CLK	140	DO	I2S serial clock
LPI_MI2S2_WS	137	DO	I2S word select
LPI_MI2S2_DATA0	133	DIO	I2S data channel 0
LPI_MI2S2_DATA1	136	DIO	I2S data channel 1
LPI_MI2S_SCLK	138	DO	LPI I2S serial clock
LPI_MI2S_WS	139	DO	LPI I2S word select
LPI_MI2S_DATA0	135	DIO	LPI I2S data channel 0
LPI_MI2S_DATA1	134	DIO	LPI I2S data channel 1
LPI_MI2S_DATA2	130	DIO	LPI I2S data channel 2
LPI_MI2S_DATA3	131	DIO	LPI I2S data channel 3
CODEC_RST_N	126	DO	Audio codec reset

4.9. UART/SPI/I2C/I2S Multiplexing Relationship

The module supports up to five groups of configurable interfaces, which can be configured as UART, SPI, I2C or I2S interfaces. Specific multiplexing relationship is shown in the following table (dedicated I2C interfaces, dedicated debug UART and interfaces already used inside the module are not included):

Table 22: UART/SPI/I2C/I2S Multiplexing Relationship

Channels	Pin No.	Pin Name	GPIO No.	Multiplexing Functions		
				UART	SPI	I2C
QUP0-SE0	306	UART0_CTS	GPIO_0	UART00_CTS	SPI00_MISO	I2C00_SDA
	305	UART0_RTS	GPIO_1	UART00_RFR	SPI00_MOSI	I2C00_SCL
	308	UART0_TXD	GPIO_2	UART00_TX	SPI00_SCLK	-
	309	UART0_RXD	GPIO_3	UART00_RX	SPI00_CS_N	-
	378	LCD_RST	GPIO_82	-	SPI00_CS_N_1	-
	324	TP_RST	GPIO_86	-	SPI00_CS_N_2	-
QUP0-SE1	198	QUP0_GPIO_04	GPIO_4	UART01_CTS	SPI01_MISO	I2C01_SDA
	191	QUP0_GPIO_05	GPIO_5	UART01_RFR	SPI01_MOSI	I2C01_SCL
	183	GPIO_69	GPIO_69	UART01_TX	SPI01_SCLK	-
	187	GPIO_70	GPIO_70	UART01_RX	SPI01_CS_N	-
QUP0-SE2						
	321	TP_INT	GPIO_80	UART02_RX	SPI02_CS_N	-
QUP0-SE4	317	DBG_TXD	GPIO_12	UART04_TX	SPI04_SCLK	-
	320	DBG_RXD	GPIO_13	UART04_RX	SPI04_CS_N	-
	189	I2C4_SDA	GPIO_96	UART04_CTS	SPI04_MISO	I2C04_SDA
	192	I2C4_SCL	GPIO_97	UART04_RFR	SPI04_MOSI	I2C04_SCL
QUP0-SE5	196	SPI5_MISO	GPIO_14	UART05_CTS	SPI05_MISO	I2C05_SDA

	194	SPI5_MOSI	GPIO_15	UART05_RFR	SPI05_MOSI	I2C05_SCL
	197	SPI5_CLK	GPIO_16	UART05_TX	SPI05_SCLK	-
	193	SPI5_CS	GPIO_17	UART05_RX	SPI05_CS_N	-
-	152	SENSOR_I2C_SDA	GPIO_109	LPI_GPIO_19:I3C_SDA	-	-
-	149	SENSOR_I2C_SCL	GPIO_110	LPI_GPIO_20:I3C_SCL	-	-
-	153	LPI_I2C_SDA	GPIO_111	LPI_GPIO_23:UART_TX	-	-
-	156	LPI_I2C_SCL	GPIO_112	LPI_GPIO_24:UART_RX	-	-

NOTE

1. QUP-SE is flexible and supports three types of interfaces: UART, SPI, I2C.
2. Note that the same set of QUP-SE cannot support two protocols at the same time. For example: the same set of QUP cannot support UART and I2C at the same time. If a protocol only occupies part of the pins of this group of QUP, other pins can only be used for GPIO.

4.10. ADC Interface

The module provides two ADC interface which support up to 15-bit resolution.

Table 23: Pins Description of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC4	128	AI	General-purpose ADC interface	The maximum input voltage is 1.875 V.
ADC5	243	AI		

4.11. LCM Interface

The module provides one LCM interface, which is MIPI_DSI standard compliant. The interface supports one group of 4-lane high-speed differential data transmission with maximum speed rate of 1.5 Gbps/lane

and supports FHD + (1080 × 2520 @ 90 fps).

Table 24: Pins Description of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
DSI_CLK_P	366	AO	LCD MIPI clock (+)	Requires differential impedance of 85 Ω.
DSI_CLK_N	370	AO	LCD MIPI clock (-)	
DSI_LN0_P	380	AO	LCD MIPI lane 0 data (+)	
DSI_LN0_N	377	AO	LCD MIPI lane 0 data (-)	
DSI_LN1_P	376	AO	LCD MIPI lane 1 data (+)	
DSI_LN1_N	373	AO	LCD MIPI lane 1 data (-)	
DSI_LN2_P	372	AO	LCD MIPI lane 2 data (+)	
DSI_LN2_N	369	AO	LCD MIPI lane 2 data (-)	
DSI_LN3_P	368	AO	LCD MIPI lane 3 data (+)	
DSI_LN3_N	365	AO	LCD MIPI lane 3 data (-)	
LCD_TE	374	DI	LCD tearing effect	VREG_L9A_1P8
LCD_RST	378	DO	LCD reset	
PWM	340	DO	PWM output	Backlight control

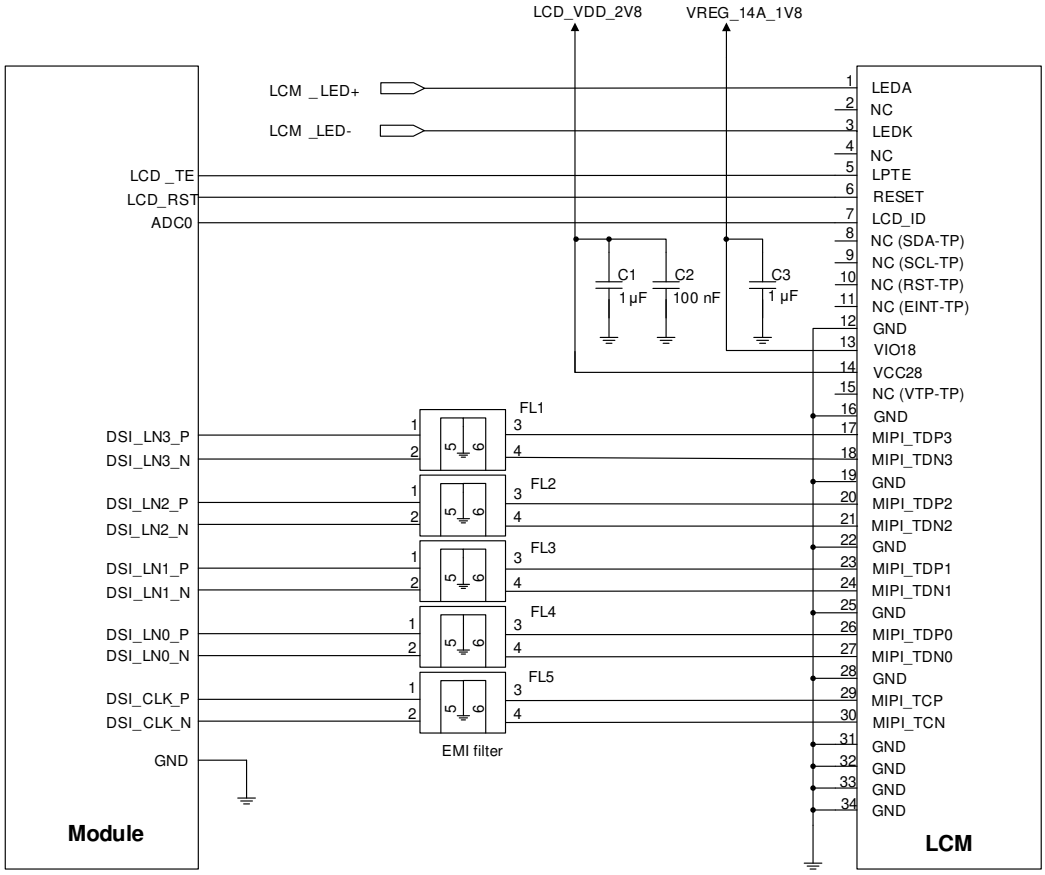


Figure 21: Reference Design of LCM Interface

MIPI are high-speed signal traces. It is recommended to add common-mode chokes in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that LCM factory burn an OTP register to distinguish different screens. You can also connect the LCD_ID of LCM to the GPIOs of the module to distinguish different screens by level detection. But note that the output voltage of LCD_ID should not exceed the voltage range of the GPIOs.

You can design an external backlight drive circuit for LCM according to actual requirement. PWM can be used for backlight brightness adjustment.

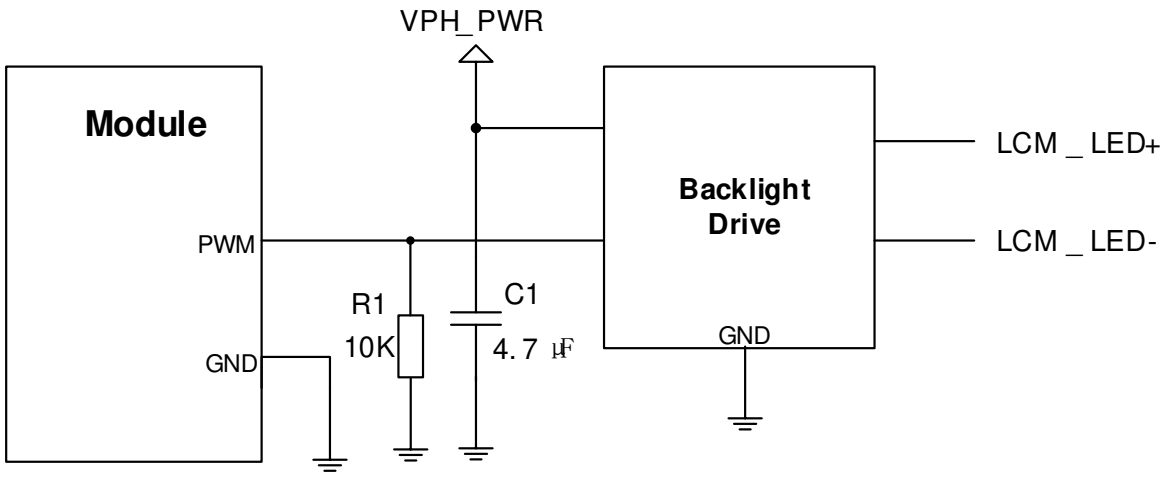


Figure 22: Reference Design of LCM Interface External Backlight Drive

4.12. Camera Interface

Based on MIPI_CSI standard, the maximum data rate is up to 2.5 Gbps/lane. The module supports up to four cameras and supports 3 concurrently working cameras. It supports up to (13 MP + 13 MP + 5 MP 30 fps @ ZSL) or up to (25 MP + 5 MP or 16 MP + 16 MP 30 fps @ ZSL) or up to 32 MP (30 fps @ ZSL) or 64 MP (no ZSL). The video and photo quality are determined by various factors such as the camera sensor, camera lens.

Table 25: Pins Description of Camera Interface

Camera Interfaces				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
CSI0_CLK_P	14	AI	MIPI CSI0 clock (+)	Require differential impedance of 85 Ω.
CSI0_CLK_N	18	AI	MIPI CSI0 clock (-)	
CSI0_LN0_P	16	AI	MIPI CSI0 lane 0 data (+)	
CSI0_LN0_N	17	AI	MIPI CSI0 lane 0 data (-)	
CSI0_LN1_P	20	AI	MIPI CSI0 lane 1 data (+)	
CSI0_LN1_N	21	AI	MIPI CSI0 lane 1 data (-)	
CSI0_LN2_P	24	AI	MIPI CSI0 lane 2 data (+)	

CSI0_LN2_N	25	AI	MIPI CSI0 lane 2 data (-)	
CSI0_LN3_P	28	AI	MIPI CSI0 lane 3 data (+)	
CSI0_LN3_N	29	AI	MIPI CSI0 lane 3 data (-)	
CAM0_MCLK	30	DO	Master clock of camera 0	
CAM0_RST	26	DO	Reset of camera 0	VREG_L9A_1P8
CAM0_PWDN	178	DO	Power down of camera 0	
CSI1_CLK_P	38	AI	MIPI CS1 clock (+)	
CSI1_CLK_N	42	AI	MIPI CSI1 clock (-)	
CSI1_LN0_P	40	AI	MIPI CSI1 lane 0 data (+)	
CSI1_LN0_N	41	AI	MIPI CSI1 lane 0 data (-)	
CSI1_LN1_P	44	AI	MIPI CSI1 lane 1 data (+)	Requires differential impedance of 85 Ω.
CSI1_LN1_N	45	AI	MIPI CSI1 lane 1 data (-)	
CSI1_LN2_P	48	AI	MIPI CSI1 lane 2 data (+)	
CSI1_LN2_N	49	AI	MIPI CSI1 lane 2 data (-)	
CSI1_LN3_P	52	AI	MIPI CSI1 lane 3 data (+)	
CSI1_LN3_N	53	AI	MIPI CSI1 lane 3 data (-)	
CAM1_MCLK	54	DO	Master clock of camera 1	
CAM1_RST	50	DO	Reset of camera 1	VREG_L9A_1P8
CAM1_PWDN	198	DO	Power down of camera 1	
CSI2_CLK_P	390	AI	MIPI CSI2 clock (+)	
CSI2_CLK_N	386	AI	MIPI CSI2 clock (-)	
CSI2_LN0_P	392	AI	MIPI CSI2 lane 0 data (+)	Requires differential impedance of 85 Ω.
CSI2_LN0_N	389	AI	MIPI CSI2 lane 0 data (-)	
CSI2_LN1_P	388	AI	MIPI CSI2 lane 1 data (+)	
CSI2_LN1_N	385	AI	MIPI CSI2 lane 1 data (-)	

CSI2_LN2_P	396	AI	MIPI CSI2 lane 2 data (+)	
CSI2_LN2_N	393	AI	MIPI CSI2 lane 2 data (-)	
CSI2_LN3_P	400	AI	MIPI CSI2 lane 3 data (+)	
CSI2_LN3_N	397	AI	MIPI CSI2 lane 3 data (-)	
CAM2_MCLK	398	DO	Master clock of camera 2	VREG_L9A_1P8
CAM2_RST	384	DO	Reset of camera 2	
CAM2_PWDN	351	DO	Power down of camera 2	
CAM3_MCLK	123	DO	Master clock of camera 3	
CAM3_RST	51	DO	Reset of camera 3	
CAM3_PWDN	175	DO	Power down of camera 3	
CCI_I2C_SDA0	33	OD	I2C clock of camera 0&3	
CCI_I2C_SCL0	36	OD	I2C data of camera 0&3	

The following is a reference design of dual-camera application:

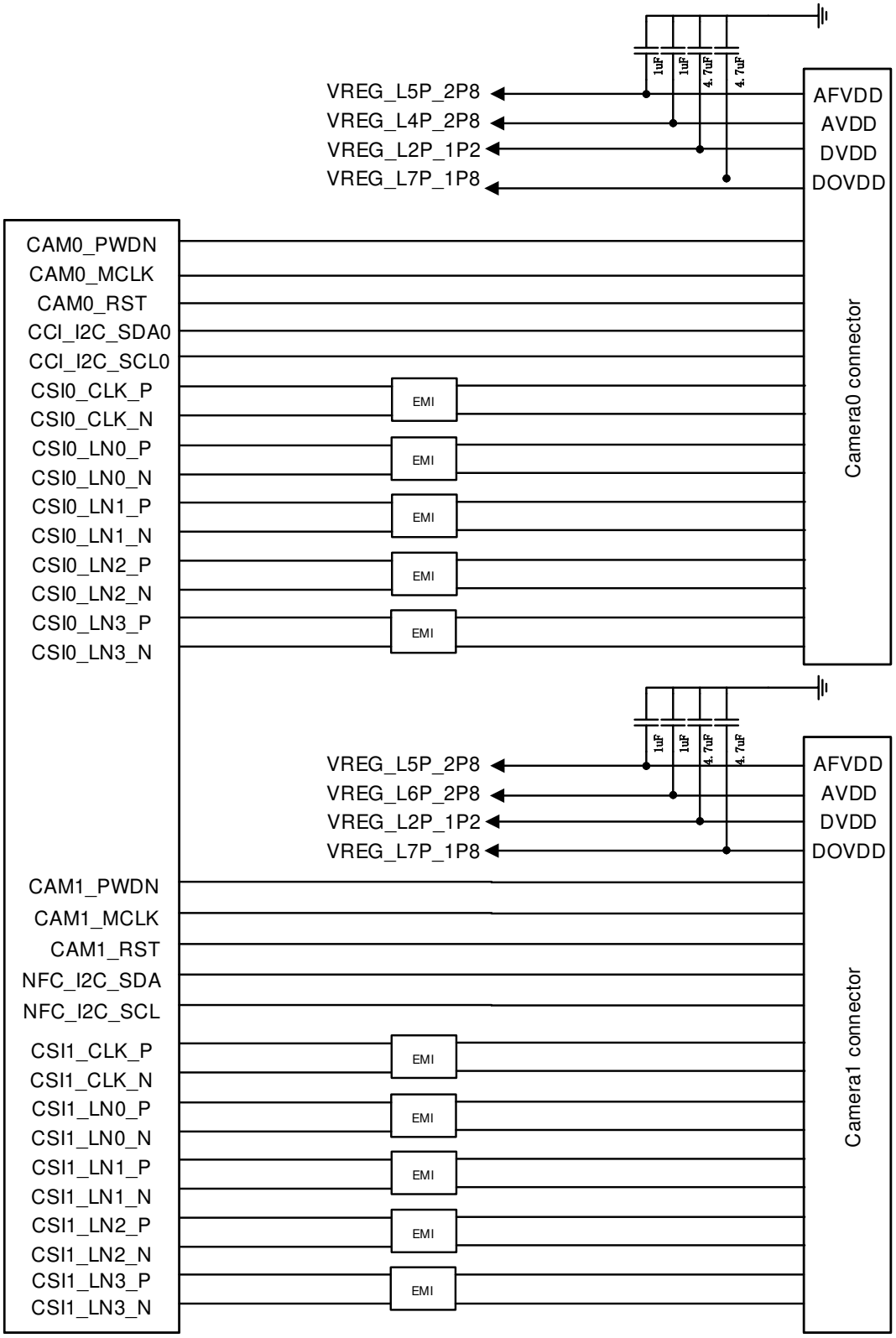


Figure 23: Reference Design of Dual-Camera Application

The following is a reference design of triple-camera application:

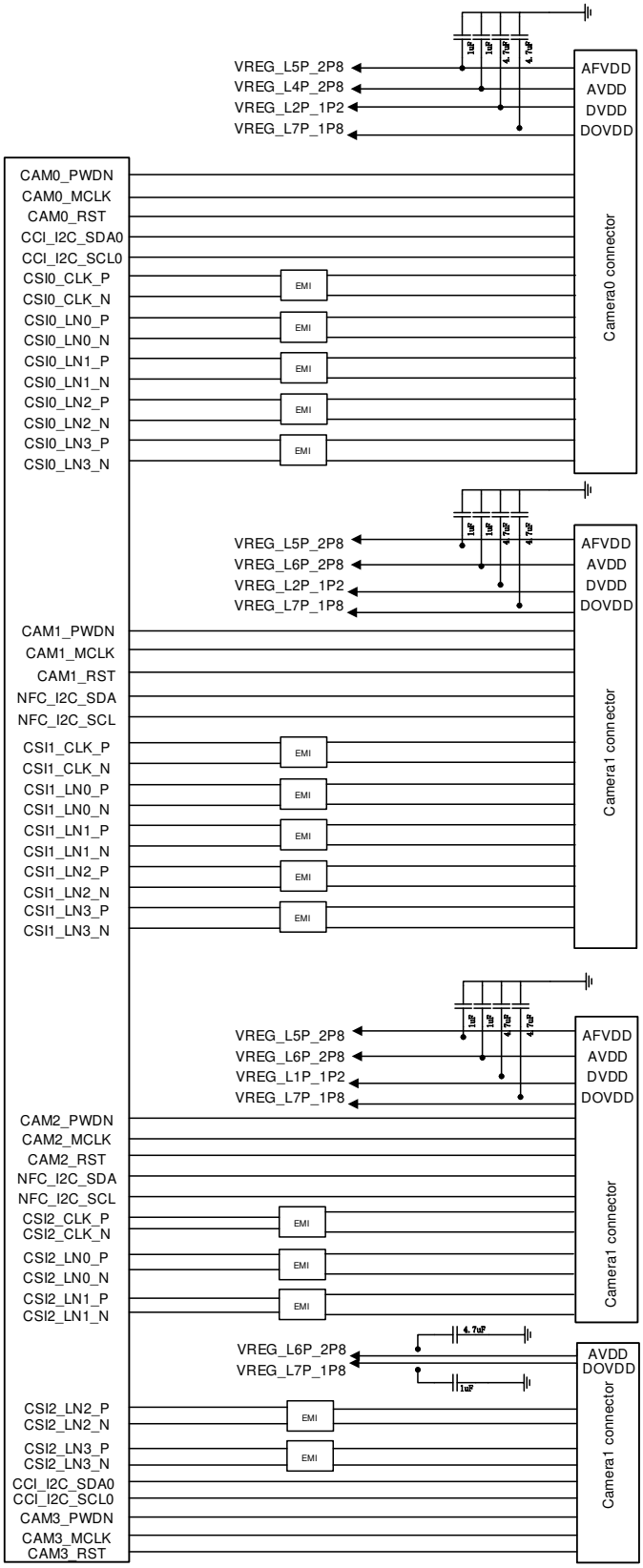


Figure 24: Reference Design of Triple-Camera Application

4.12.1. MIPI Design Considerations

To ensure performance, the following principles should be complied with when designing LCM and camera interfaces:

- Special attention should be paid to the pin description of LCM and camera interfaces. Different video devices will have varied definitions for their corresponding connectors. Ensure that the devices and the connectors are correctly connected.
- MIPI are high-speed signal traces, supporting maximum data rate up to 1.5 Gbps. The differential impedance should be controlled to 85 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB and do not cross it with other traces. For the same video device, keep all the MIPI traces be of the same length. To avoid crosstalk, a clearance of 1.5 times the trace width is recommended among MIPI signal traces. During impedance matching, do not connect MIPI signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a TVS component of low capacitance for ESD protection and the recommended parasitic capacitance should be lower than 1 pF.
- Route MIPI traces according to the following requirements:
  a) When the MIPI signal line rate is 1.5 Gbps/lane, the FPC trace length is 76.2 mm, and the insertion loss of the FPC cable is -0.9 dB, the PCB trace length should not exceed 135 mm;
  b) Control the differential impedance to 85 Ω ±10 %;
  c) Control intra-lane length matching within 0.7 mm;
  d) Control inter-lane length matching within 1.4 mm.

Table 26: MIPI Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length	Length Mismatch
366	DSI_CLK_P	24.55	0.63
370	DSI_CLK_N	23.92	
380	DSI_LN0_P	23.93	0.49
377	DSI_LN0_N	23.44	
376	DSI_LN1_P	24.32	0.59
373	DSI_LN1_N	23.73	
372	DSI_LN2_P	24.77	0.68
369	DSI_LN2_N	24.09	
368	DSI_LN3_P	24.54	0.70

365	DSI_LN3_N	23.84	
14	CSI0_CLK_P	43.87	-0.50
18	CSI0_CLK_N	44.37	
16	CSI0_LN0_P	44.74	-0.53
17	CSI0_LN0_N	45.27	
20	CSI0_LN1_P	45.20	0.59
21	CSI0_LN1_N	44.61	
24	CSI0_LN2_P	44.39	0.36
25	CSI0_LN2_N	44.03	
28	CSI0_LN3_P	44.11	
29	CSI0_LN3_N	44.55	-0.44
38	CSI1_CLK_P	49.33	
42	CSI1_CLK_N	49.91	-0.58
40	CSI1_LN0_P	49.59	
41	CSI1_LN0_N	50.23	-0.64
44	CSI1_LN1_P	50.10	
45	CSI1_LN1_N	50.71	-0.61
48	CSI1_LN2_P	49.89	
49	CSI1_LN2_N	49.32	0.57
52	CSI1_LN3_P	49.72	
53	CSI1_LN3_N	50.32	-0.60
390	CSI2_CLK_P	78.50	-0.56
386	CSI2_CLK_N	79.06	
392	CSI2_LN0_P	78.45	-0.61
389	CSI2_LN0_N	79.06	

388	CSI2_LN1_P	78.95	0.54
385	CSI2_LN1_N	78.41	
396	CSI2_LN2_P	78.60	-0.49
393	CSI2_LN2_N	79.09	
400	CSI2_LN3_P	79.78	0.33
397	CSI2_LN3_N	79.45	

Table 27: Mapping of CSI Data Rates and Trace Length (D-PHY)

Data Rates	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
2.5 Gbps/lane	76.2	-2.1	< 210
	152.4	-3.5	< 150

Table 28: Mapping of DSI Data Rates and Trace Length (D-PHY)

Data Rates	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
1.5 Gbps/lane	76.2	-0.9	< 135
	152.4	-1.8	< 40

4.13. Touch Panel Interface

The module provides one I2C interfaces for connection with Touch Panel (TP), and provides the corresponding power supply and interrupt pins.

Table 29: Pins Description of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	324	DO	TP reset	
TP_INT	321	DI	TP interrupt	

TP_I2C_SCL	328	OD	TP I2C clock
TP_I2C_SDA	325	OD	TP I2C data

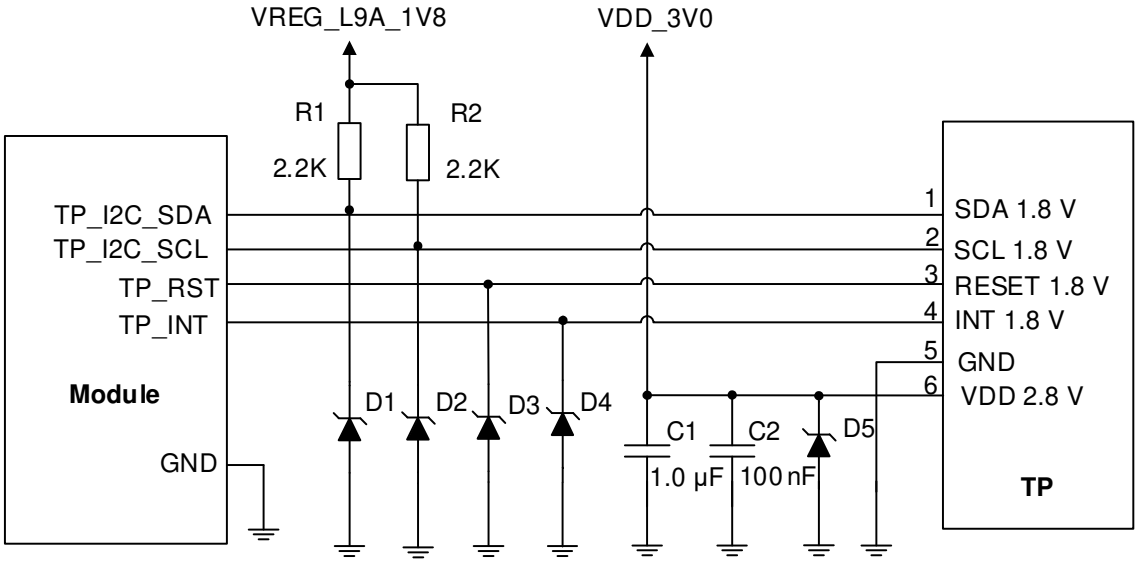


Figure 25: Reference Design of Touch Panel Interface

4.14. Sensor Interface

The module supports communication with sensors via I2C interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, light sensor, temperature sensor, pressure sensor.

Table 30: Pins Description of Sensor Interface

Pin Name	Pin No.	I/O	Description	Comment
ACCEL_GYRO_INT1	161	DI	Acceleration/ gyroscope sensor interrupt 1	VREG_L9A_1P8
ACCEL_GYRO_INT2	158	DI	Acceleration/ gyroscope sensor interrupt 2	
MAG_INT	186	DI	Geomagnetic sensor interrupt	
ALPS_INT	157	DI	Light/proximity sensor interrupt	

HALL_INT	190	DI	Hall sensor interrupt

4.16. GPIO

The module provides 52 GPIOs with the power domain of 1.8 V:

Table 32: Pins Description of GPIO

Pin Name	Pin No.	I/O	Description	Comment
EXGPIO_20	19	DIO	General-purpose input/output	
EXGPIO_11	43	DIO		
EXGPIO_15	67	DIO		

EXGPIO_05	70	DIO		
EXGPIO_04	71	DIO		
EXGPIO_14	74	DIO		
EXGPIO_08	79	DIO		
EXGPIO_16	94	DIO		
EXGPIO_9	110	DIO		
EXGPIO_10	111	DIO		
EXGPIO_19	119	DIO		
EXGPIO_26	122	DIO		
EXGPIO_07	141	DIO		
EXGPIO_06	144	DIO		
EXGPIO_31	147	DIO		
EXGPIO_24	150	DIO		
EXGPIO_34	151	DIO		
EXGPIO_25	154	DIO		
EXGPIO_23	155	DIO		
EXGPIO_32	167	DIO		
EXGPIO_21	170	DIO		
GPIO_69	183	DIO		
GPIO_70	187	DIO		
QUP_GPIO_05	191	DIO		
EXGPIO_12 (Compatibility GPIO_44)	202	DIO		
EXGPIO_17	203	DIO		
EXGPIO_28	207	DIO		

EXGPIO_13	210	DIO		
EXGPIO_42	263	DIO		
GPIO_84	307	DIO		
EXGPIO_33	310	DIO		
GPIO_83	311	DIO		
EXGPIO_18	315	DIO		
EXGPIO_27	318	DIO		
EXGPIO_22	319	DIO		
EXGPIO_29	322	DIO		
EXGPIO_30	326	DIO		
EXGPIO_43	355	DIO		
EXGPIO_35	583	DIO		
EXGPIO_01	605	DIO		
EXGPIO_02	606	DIO		
EXGPIO_03	607	DIO		
EXGPIO_41	609	DIO		
EXGPIO_40	610	DIO		
EXGPIO_45	613	DIO		
EXGPIO_38	615	DIO		
EXGPIO_39	616	DIO		
EXGPIO_36	617	DIO		
EXGPIO_37	618	DIO		
EXGPIO_46	632	DIO		
EXGPIO_47	634	DIO		
EXGPIO_44	635	DIO		

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to conduct a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 33: Pins Description of Cellular Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
50OHM_ANT_MAIN	280	AIO	Main antenna interface	50 Ω impedance.
50OHM_ANT_DRX	211	AI	Diversity antenna interface	

NOTE

Only passive antennas are supported.

Table 34: Operating Frequency of QLB12-21(SG656V-GL)/QLA12-21(SG636V-GL) (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE–FDD B1	1920–1980	2110–2170
LTE–FDD B2	1850–1910	1930–1990
LTE–FDD B3	1710–1785	1805–1880
LTE–FDD B4	1710–1755	2110–2155

LTE–FDD B5	824–849	869–894
LTE–FDD B7	2500–2570	2620–2690
LTE–FDD B8	880–915	925–960
LTE–FDD B12	699–716	729–746
LTE–FDD B13	777–787	746–756
LTE–FDD B14	788–798	758–768
LTE–FDD B17	704–716	734–746
LTE–FDD B18	815–830	860–875
LTE–FDD B19	830–845	875–890
LTE–FDD B20	832–862	791–821
LTE–FDD B25	1850–1915	1930–1995
LTE–FDD B26	814–849	859–894
LTE–FDD B28	703–748	758–803
LTE–FDD B30	2305-2315	2350-2360
LTE–FDD B66	1710–1780	2110–2200
LTE–FDD B71	663–698	617–652
LTE–TDD B34	2010-2025	2010-2025
LTE–TDD B38	2570–2620	2570–2620
LTE–TDD B39	1880-1920	1880-1920
LTE–TDD B40	2300–2400	2300–2400
LTE–TDD B41	2496–2690	2496–2690
WCDMA B1	1920–1980	2110–2170
WCDMA B2	1850–1910	1930–1990
WCDMA B4	1710–1755	2110–2155
WCDMA B5	824–849	869–894
WCDMA B6	830–840	875–885

WCDMA B8	880–915	925–960
WCDMA B19	830-845	875-890
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990

Table 35: Operating Frequency of QLB12-22(SG656V-EM)/QLA12-22(SG636V-EM) (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE–FDD B1	1920–1980	2110–2170
LTE–FDD B2	1850–1910	1930–1990
LTE–FDD B3	1710–1785	1805–1880
LTE–FDD B4	1710–1755	2110–2155
LTE–FDD B5	824–849	869–894
LTE–FDD B7	2500–2570	2620–2690
LTE–FDD B8	880–915	925–960
LTE–FDD B18	815–830	860–875
LTE–FDD B19	830–845	875–890
LTE–FDD B20	832–862	791–821
LTE–FDD B26	814–849	859–894
LTE–FDD B28	703–748	758–803
LTE–TDD B34	2010-2025	2010-2025
LTE–TDD B38	2570–2620	2570–2620
LTE–TDD B39	1880-1920	1880-1920
LTE–TDD B40	2300–2400	2300–2400
LTE–TDD B41	2496–2690	2496–2690

WCDMA B1	1920–1980	2110–2170
WCDMA B2	1850–1910	1930–1990
WCDMA B4	1710–1755	2110–2155
WCDMA B5	824–849	869–894
WCDMA B6	830–840	875–885
WCDMA B8	880–915	925–960
WCDMA B19	830–845	875–890
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990

5.1.2. Transmitting Power

Table 36: RF Transmitting Power

Modes	Frequency Bands	Max.	Min.
GSM	GSM850	33 dBm ±2 dB	5 dBm ±5 dB
	EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
	DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
	PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE	FDD/TDD	23 dBm ±2 dB	< -39 dBm
WCDMA	B1/B2B/4/B5/B6/B8/B19	23 dBm ±2 dB	< -49 dBm

NOTE

In GPRS 4 slots transmit mode, the maximum output power is reduced by 3 dB. The design conforms to the GSM specification as described in ***Clause 13.16*** of *3GPP TS 51.010-1*.

5.1.3. Receiver Sensitivity

Table 37: Conducted RF Receiver Sensitivity of QLB12-21(SG656V-GL)/QLA12-21(SG636V-GL) (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO	
GSM850	TBD	TBD	TBD	-102.4
EGSM900	TBD	TBD	TBD	-102.4
DCS1800	TBD	TBD	TBD	-102.4
PCS1900	TBD	TBD	TBD	-102.4
WCDMA B1	TBD	TBD	TBD	-106.7
WCDMA B2	TBD	TBD	TBD	-104.7
WCDMA B4	TBD	TBD	TBD	-106.7
WCDMA B5	TBD	TBD	TBD	-104.7
WCDMA B6	TBD	TBD	TBD	-106.7
WCDMA B8	TBD	TBD	TBD	-103.7
WCDMA B19	TBD	TBD	TBD	-106.7
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B12 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B13 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B14 (10 MHz)	TBD	TBD	TBD	-93.3

LTE-FDD B17 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B25 (10 MHz)	TBD	TBD	TBD	-92.8
LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	-93.8
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8
LTE-FDD B30 (10 MHz)	TBD	TBD	TBD	-95.3
LTE-FDD B66 (10 MHz)	TBD	TBD	TBD	-95.8
LTE-FDD B71 (10 MHz)	TBD	TBD	TBD	-93.5
LTE-TDD B34 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B39 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3

Table 38: Conducted RF Receiver Sensitivity of QLB12-22(SG656V-EM)/QLA12-22(SG636V-EM) (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO	
GSM850	TBD	TBD	TBD	-102.4
EGSM900	TBD	TBD	TBD	-102.4
DCS1800	TBD	TBD	TBD	-102.4
PCS1900	TBD	TBD	TBD	-102.4
WCDMA B1	TBD	TBD	TBD	-106.7
WCDMA B2	TBD	TBD	TBD	-104.7
WCDMA B4	TBD	TBD	TBD	-106.7

WCDMA B5	TBD	TBD	TBD	-104.7
WCDMA B6	TBD	TBD	TBD	-106.7
WCDMA B8	TBD	TBD	TBD	-103.7
WCDMA B19	TBD	TBD	TBD	-106.7
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	-93.8
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8
LTE-TDD B34 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B39 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3

5.1.4. Reference Design

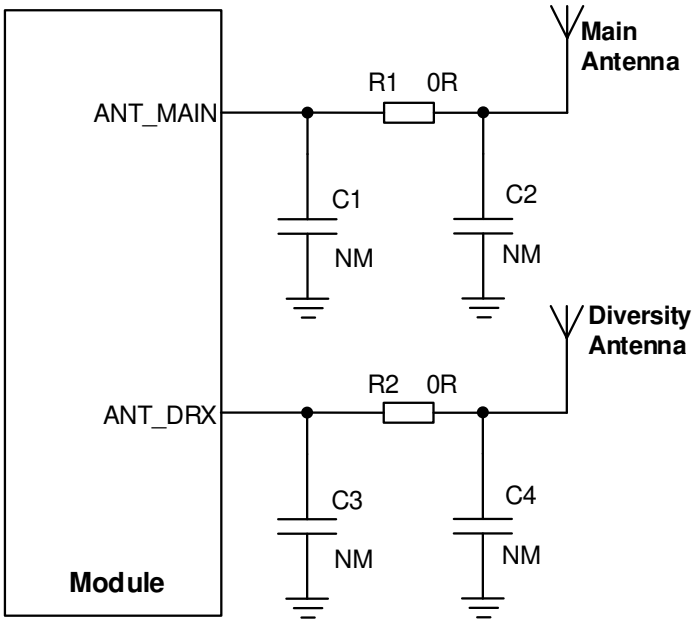


Figure 26: Reference Design of Main Antenna and Diversity Antenna

NOTE

1. To improve receiver sensitivity, ensure that the clearance among antennas is appropriate.
2. Use a π-type matching circuit for all the antenna interfaces for better RF performance and for the ease of debugging.
3. Capacitors are not mounted by default.
4. Place the π-type matching components (R1/C1/C2 and R2/C3/C4) to antennas as close as possible.

5.2. GNSS

The module integrates the IZat™ GNSS engine (Gen 9) which supports multiple positioning and navigation systems, including GPS, GLONASS, BDS，Galileo，SBAS. With an embedded LNA, the positioning accuracy of the module can be greatly improved.

5.2.1. Antenna Interface & Frequency Bands

The following table lists the GNSS performance of the module in conduction mode:

Table 39: Pins Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
50OHM_ANT_2.4G _WIFI_GNSS	92	AIO	GNSS/WIFI2.4G/ Bluetooth antenna interface	

Table 40: GNSS Frequency (Unit: MHz)

Antenna Types	Frequency
GPS	1575.42 ±1.023 (L1)
GLONASS	1597.5–1605.8 (G1)
BDS	1561.098 ±2.046 (B1I)
Galileo	1575.42 ±2.046 (E1)
SBAS	1575.42 ±1.023 (L1)

5.2.2. GNSS Performance

Table 41: GNSS Performance

Parameters	Modes	Conditions	Typ.	Units
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition		-158	
	Tracking		-158	
TTFF	Cold start @ open sky	Autonomous	27.7	s
		XTRA start	8.9	
	Warm start @ open sky	Autonomous	23.5	
		XTRA start	3.15	
	Hot start @ open sky	Autonomous	1.49	
		XTRA start	1.53	
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock of navigation signals (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

5.2.3.1.GNSS Active Antenna

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design. The active antenna is powered by a 56-nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies, it is recommended to use a high-performance LDO:

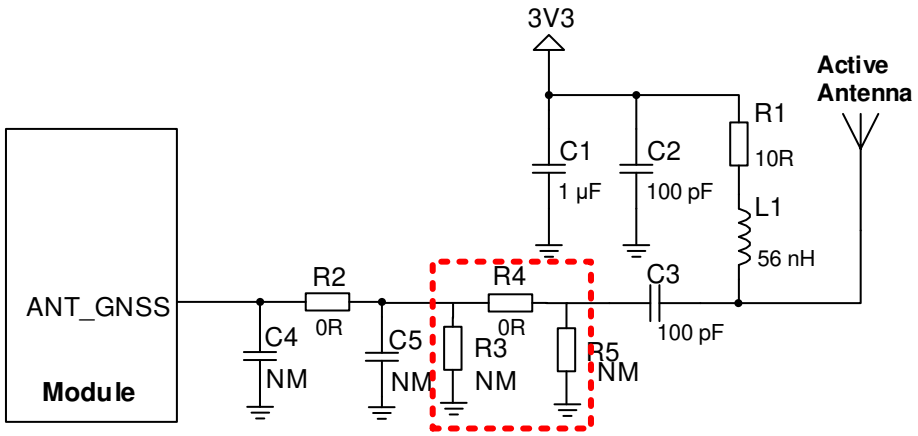


Figure 27: Reference Design of GNSS Active Antenna

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.2.3.2.GNSS Passive Antenna

You can also use passive ceramic antennas or other types of passive antennas:

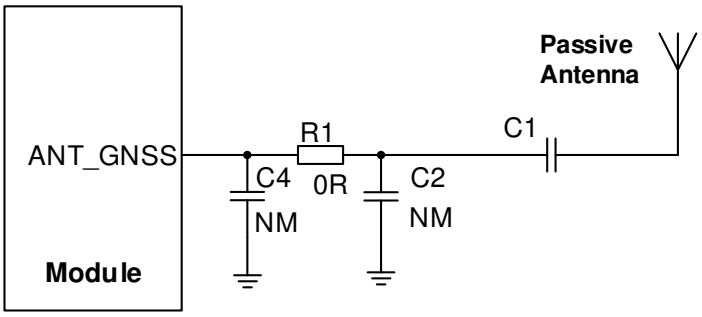


Figure 28: Reference Design of GNSS Passive Antenna

NOTE

It is not recommended to add an external LNA when using a passive antenna.

5.2.3.3.GNSS RF Design Guidelines

Improper design of antenna and layout may cause reduced GNSS receiver sensitivity, longer GNSS positioning period, or reduced positioning accuracy. Thus, follow the design rules as below:

- Maximize the clearance between GNSS RF part and other RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, place GNSS RF signal traces and RF components far away from high-speed circuits, switch-mode power supplies, power inductors and the clock circuit of single-chip microcomputers.
- For applications with a harsh electromagnetic environment or with high requirement on ESD protection, it is recommended to add ESD protection components for the antenna interface. Only diodes with ultra-low junction capacitance such as 0.5 pF can be selected. Otherwise, there will be effects on the impedance characteristic of the RF circuit loop or attenuation of the bypass RF signal may be caused.
- Keep the impedance of either feeder line or PCB trace as 50 Ω, and keep the trace length as short as possible.

5.3. Wi-Fi & Bluetooth

The module provides a shared antenna interface: ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The impedance shall be kept as 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna or ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

Table 42: Pins Description of Wi-Fi & Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
50OHM_ANT_5G_WIFI	86	AIO	WIFI 5G antenna interface	
50OHM_ANT_2.4G_WIFI_GNSS	92	AIO	GNSS/WIFI 2.4G/ Bluetooth antenna interface	

Table 43: Wi-Fi & Bluetooth Frequency (Unit: MHz)

Types	Frequency
Wi-Fi 802.11 a/b/g/n/ac	2412–2462 5180–5825
Bluetooth 5.1	2402–2480

5.3.1. Wi-Fi Overview

The module supports 2.4 GHz & 5 GHz dual-band Wi-Fi wireless communication based on Wi-Fi 802.11 a/b/g/n/ac standard protocols. The maximum data rate is up to 433 Mbps. The supported features are as below:

- Wake-on-WLAN (WoWLAN)
- WAPI SMS4 hardware encryption
- AP and STA mode
- Wi-Fi Direct
- MCS 0–MCS 7: HT20 and HT40
- MCS 0–MCS 8: VHT20
- MCS 0–MCS 9: VHT40 and VHT80

Table 44: Wi-Fi Transmitting Performance of QLA12(SG636V) & QLB12(SG656V) Series

Bands	Standards	Speed Rates	Output Power
2.4 GHz	802.11b	1 Mbps	18 dBm ±2.5 dB
	802.11b	11 Mbps	18 dBm ±2.5 dB
	802.11g	6 Mbps	18 dBm ±2.5 dB
	802.11g	54 Mbps	16 dBm ±2.5 dB
	802.11n @ HT20	MCS 0	18 dBm ±2.5 dB
	802.11n @ HT20	MCS 7	15 dBm ±2.5 dB
	802.11n @ HT40	MCS 0	18 dBm ±2.5 dB
	802.11n @ HT40	MCS 7	15 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	19.5 dBm ±2.5 dB
	802.11a	54 Mbps	18.5 dBm ±2.5 dB
	802.11n @ HT20	MCS 0	19.5 dBm ±2.5 dB
	802.11n @ HT20	MCS 7	17.5 dBm ±2.5 dB
	802.11n @ HT40	MCS 0	19.5 dBm ±2.5 dB
	802.11n @ HT40	MCS 7	17.5 dBm ±2.5 dB
	802.11ac @ VHT20	MCS 0	19.5 dBm ±2.5 dB
	802.11ac @ VHT20	MCS 8	17 dBm ±2.5 dB
	802.11ac @ VHT40	MCS 0	19.5 dBm ±2.5 dB
	802.11ac @ VHT40	MCS 9	15.5 dBm ±2.5 dB
	802.11ac @ VHT80	MCS 0	19.5 dBm ±2.5 dB
	802.11ac @ VHT80	MCS 9	15.5 dBm ±2.5 dB

Table 45: Wi-Fi Receiving Performance of QLA12(SG636V) & QLB12(SG656V) Series

Bands	Standards	Speed Rates	Sensitivity (dBm)
2.4 GHz	802.11b	1 Mbps	-96
	802.11b	11 Mbps	-89
	802.11g	6 Mbps	-91
	802.11g	54 Mbps	-75
	802.11n @ HT20	MCS 0	-91
	802.11n @ HT20	MCS 7	-72
	802.11n @ HT40	MCS 0	-88
	802.11n @ HT40	MCS 7	-70
5 GHz	802.11a	6 Mbps	-92
	802.11a	54 Mbps	-76
	802.11n @ HT20	MCS 0	-92
	802.11n @ HT20	MCS 7	-74
	802.11n @ HT40	MCS 0	-89
	802.11n @ HT40	MCS 7	-72
	802.11ac @ VHT20	MCS 0	-91
	802.11ac @ VHT20	MCS 8	-70
	802.11ac @ VHT40	MCS 0	-89
	802.11ac @ VHT40	MCS 9	-66
	802.11ac @ VHT80	MCS 0	-85
	802.11ac @ VHT80	MCS 9	-61

NOTE

The product complies with the IEEE specifications.

5.3.2. Bluetooth Overview

Models with built-in Bluetooth function provide Bluetooth antenna interfaces. The module supports Bluetooth 5.1 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulations. Supported characteristics include:

- Up to 7-lane wireless connections.
- Up to 3.5 Piconets simultaneously.
- One SCO or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 46: Bluetooth Data Rates and Versions

Versions	Data Rates (Mbit/s)	Maximum Application Throughput
1.2	1	> 80 kbit/s
2.0 + EDR	3	> 80 kbit/s
3.0 + HS	24	Refer to 3.0 + HS
4.0	24	Refer to 4.0 LE
5.0	48 Mbit/s	Refer to 5.0 LE
5.1	TBD	TBD

Referenced specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016*

Table 47: Bluetooth Transmitting and Receiving Performance (Unit: dBm)

Transmitting Performance			
Packet types	DH5	2-DH5	3-DH5
Transmitting power	7.5 ±2.5	7.5 ±2.5	7.5 ±2.5

Receiving Performance			
Packet types	DH5	2-DH5	3-DH5
Receiving sensitivity	-92	-91	-86

5.3.3. Reference Design

A reference design of Wi-Fi & Bluetooth antenna interface is shown as below. C1 and C2 are not mounted by default. Only a 0 Ω resistor is mounted on R1.

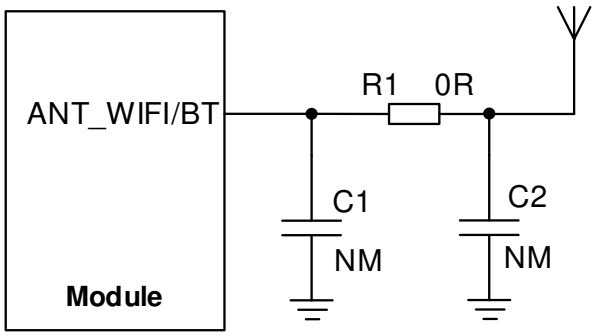


Figure 29: Reference Design of Wi-Fi & Bluetooth Antenna

5.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

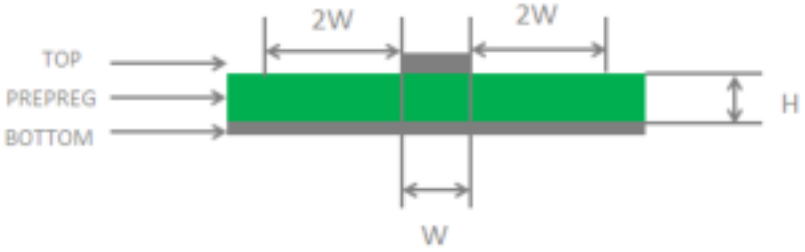


Figure 30: Microstrip Design on a 2-layer PCB

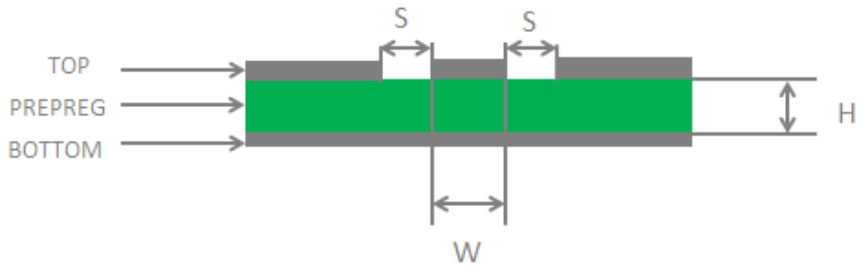


Figure 31: Coplanar Waveguide Design on a 2-layer PCB

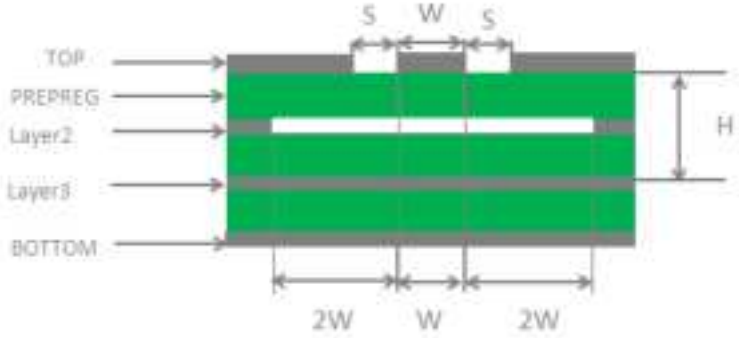


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

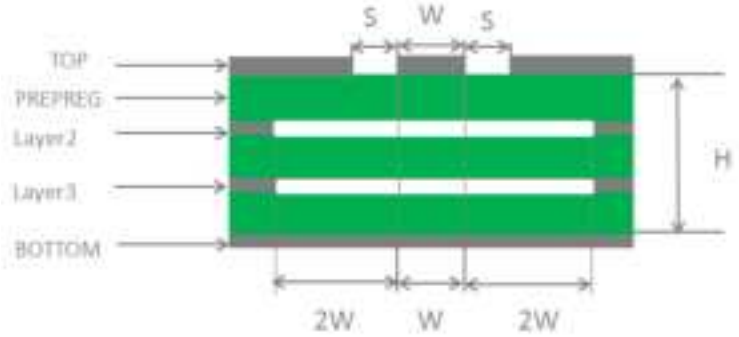


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to

50 Ω.

- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.5. Requirements for Antenna Design

Table 48: Requirements for Antenna Design

Antenna Types	Requirements
GNSS	**Frequency range:** • L1: 1559–1609 MHz RHCP or linear polarization VSWR: ≤ 2 (Typ.)
	For passive antenna application: Passive antenna gain: > 0 dBi
	For active antenna application: Active antenna noise coefficient: < 1.5 dB Active antenna embedded LNA gain: < 17 dB
Cellular	VSWR: ≤ 2 Gain: 1 dBi Max input power: 50 W Input impedance: 50 Ω Vertical polarization **Cable insertion loss:** • < 1 dB: LB (< 1 GHz) • < 1.5 dB: MB (1–2.3 GHz) • < 2 dB: HB (> 2.3 GHz)
Wi-Fi & Bluetooth	VSWR: ≤ 2 Gain: 1 dBi Max input power: 50 W

	Input impedance: 50 Ω Vertical polarization Cable insertion loss: < 1 dB

5.6. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

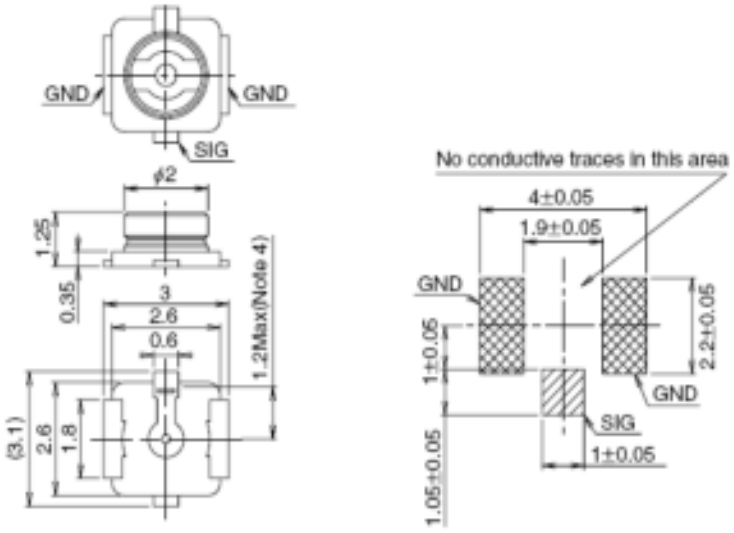


Figure 34: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

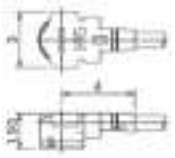
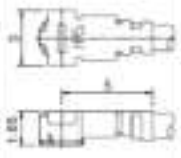
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 35: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

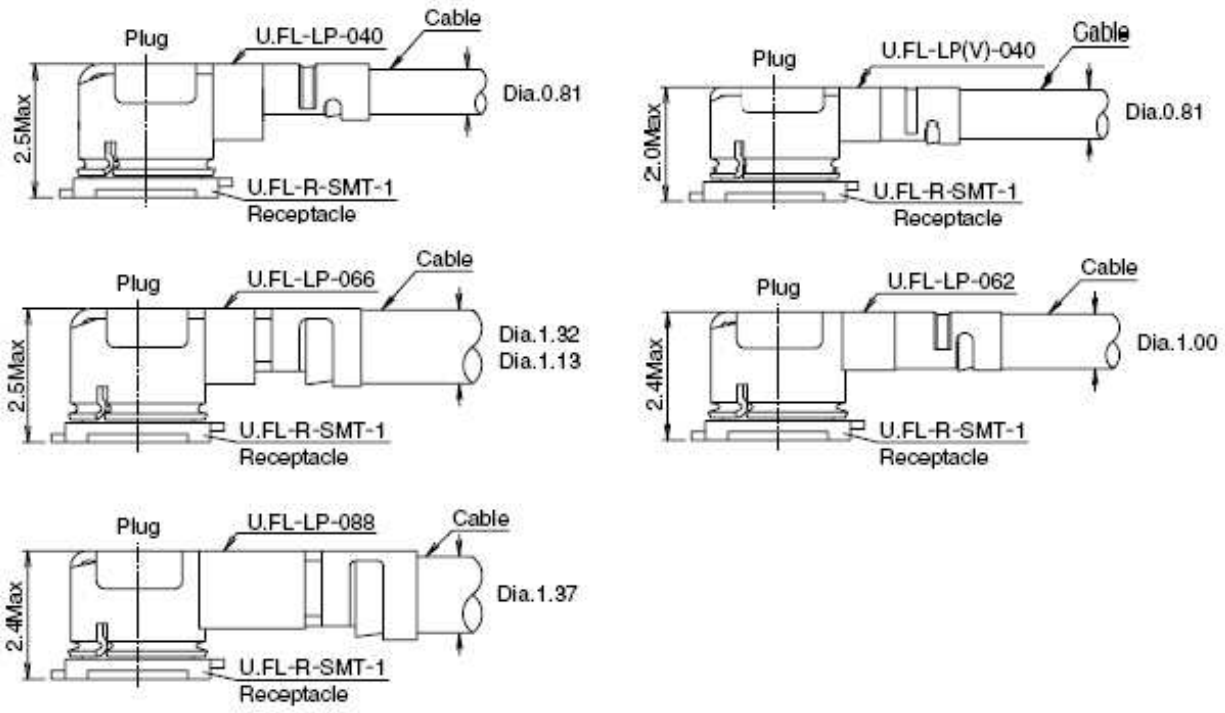


Figure 36: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 49: Absolute Maximum Ratings

Parameters	Min.	Max.	Units
Voltage at VBAT_RF & VBAT_BB	-0.3	4.75	V
Voltage at USB_VBUS	-0.3	16	V
Voltage at digital pins	-0.3	2.2	V
Current at VBAT	-	5	A

6.2. Power Supply Ratings

Table 50: Module's Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Units
VBAT	VBAT	The actual input voltage must be within this range	3.55	3.8	4.4	V
I_{VBAT}	Peak supply current	Maximum power control level (At the maximum transmitting power)	-	1.8	3.0	A
USB_VBUS	USB connection detection		4.0	5.0	6.0	V
VRTC	Supply voltage of the backup battery		2.1	3.0	3.25	V

6.3. Power Consumption

Table 51: QLA12(SG636V) Series &QLB12(SG656V) Series Power Consumption

Modes	Conditions	Typ.	Units
OFF state	Power off	47	μA
Sleep state (USB disconnected)	TBD	4.5	mA
WCDMA voice call	TBD	TBD	mA
	TBD	TBD	mA
GPRS data transmission	TBD	TBD	mA
	TBD	TBD	mA
EDGE data transmission	TBD	TBD	mA
	TBD	TBD	mA
LTE data transmission	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
WCDMA data transmission	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
	TBD	TBD	mA
EV-DO data transmission	TBD	TBD	mA

GSM voice call	TBD	TBD	mA
CDMA voice call	TBD	TBD	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 52: 1.8 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.17	2.1
V_{IL}	Low-level input voltage	-0.3	0.63
V_{OH}	High-level output voltage	1.35	1.8
V_{OL}	Low-level output voltage	0	0.45

Table 53: SD Card Low-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.27	2
V_{IL}	Low-level input voltage	-0.3	0.58
V_{OH}	High-level output voltage	1.4	1.8
V_{OL}	Low-level output voltage	0	0.45

Table 54: SD Card High-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.84	3.25
V_{IL}	Low-level input voltage	-0.3	0.74
V_{OH}	High-level output voltage	2.21	2.95
V_{OL}	Low-level output voltage	0	0.37

Table 55: (U)SIM Low-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.26	2.1
V_{IL}	Low-level input voltage	-0.3	0.36
V_{OH}	High-level output voltage	1.44	1.8
V_{OL}	Low-level output voltage	0	0.4

Table 56: (U)SIM High-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	2.07	3.25
V_{IL}	Low-level input voltage	-0.3	0.59
V_{OH}	High-level output voltage	2.36	2.95
V_{OL}	Low-level output voltage	0	0.4

6.5. ESD

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 57: ESD Characteristics (Temperature: 25–30°C, Humidity: 40 ±5 %; Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT & GND	±5	±10
All antenna interfaces	±5	±10
Other interfaces	±0.5	±1

6.6. Operating and Storage Temperatures

Table 58: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature [2]	-35	+25	+75
Storage Temperature	-40	-	+90

[2] Within this range, the module's related indicators can meet 3GPP specifications.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

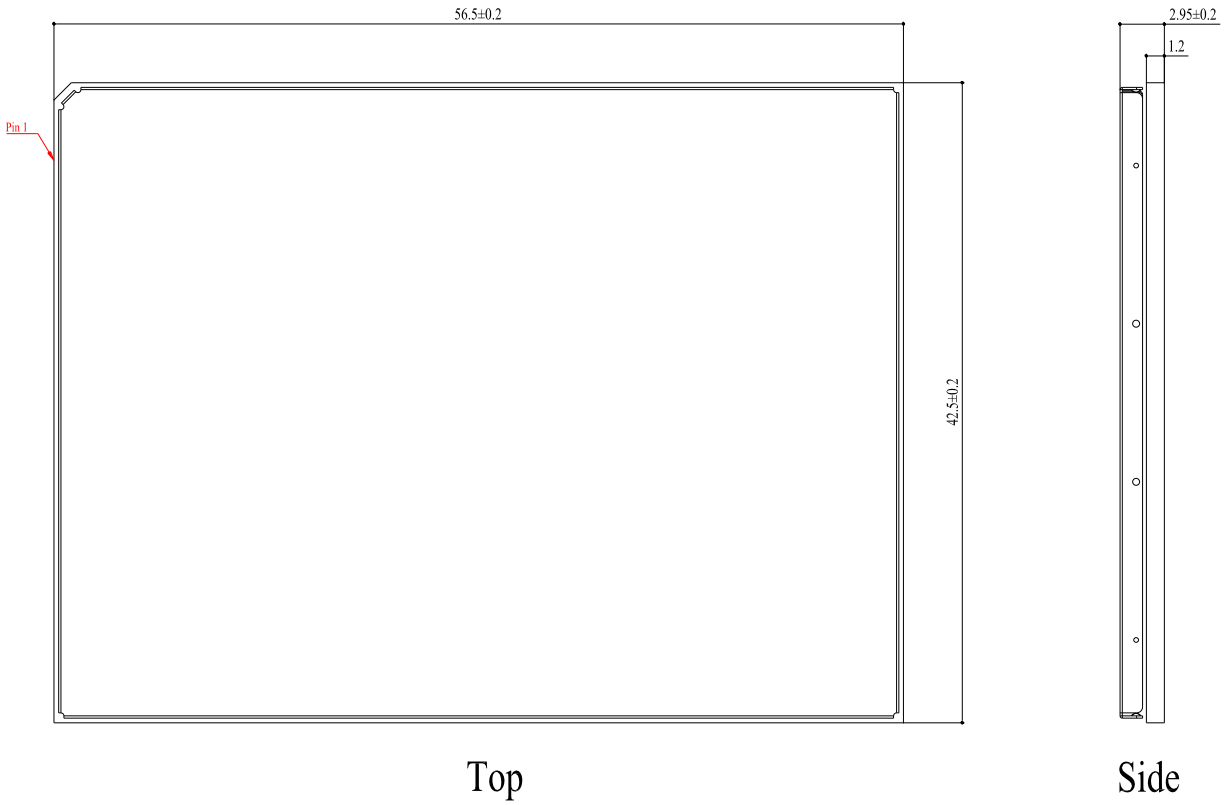


Figure 37: Module Top and Side Dimensions

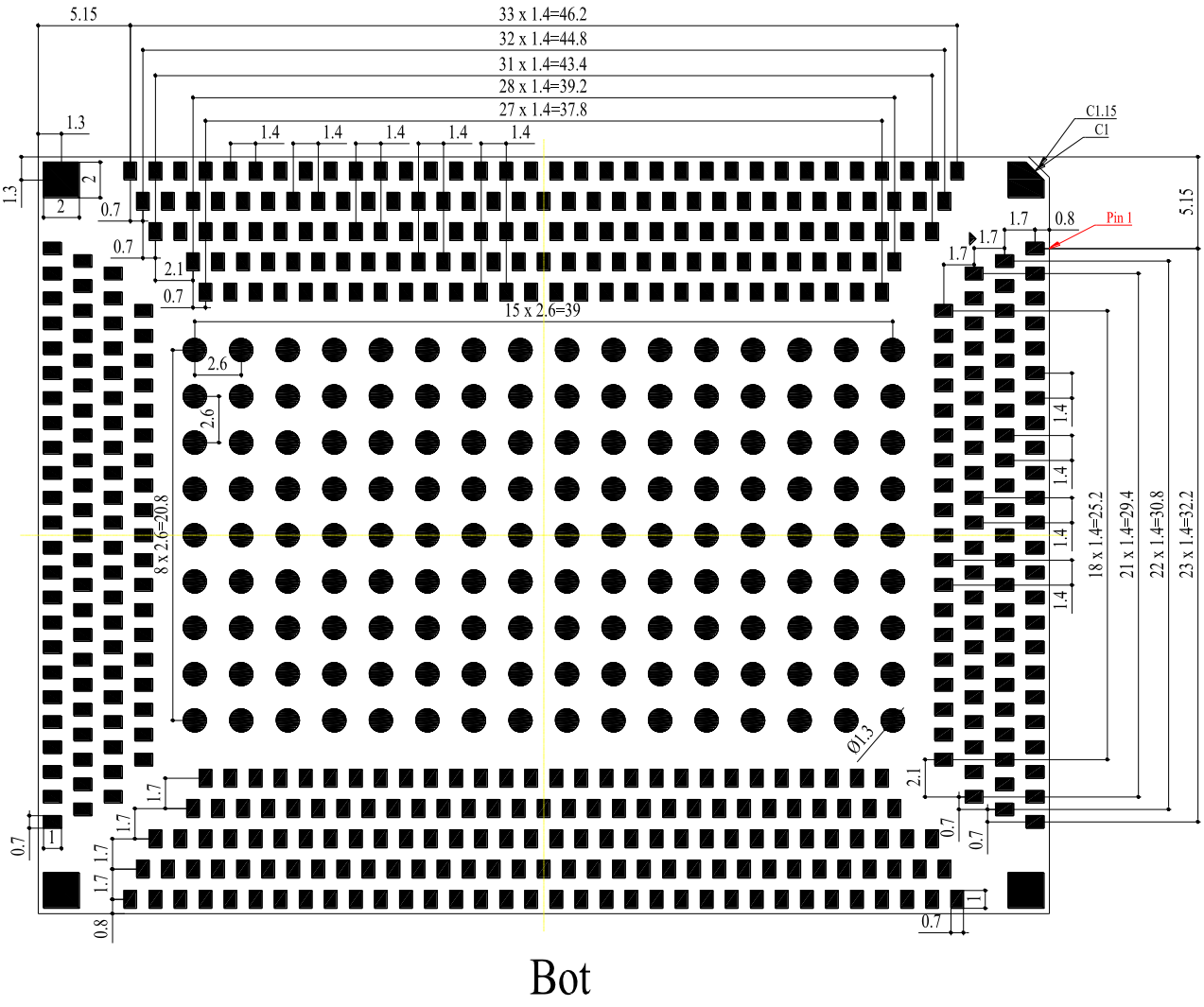


Figure 38: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to *JEITA ED-7306* standard.

7.2. Recommended Footprint

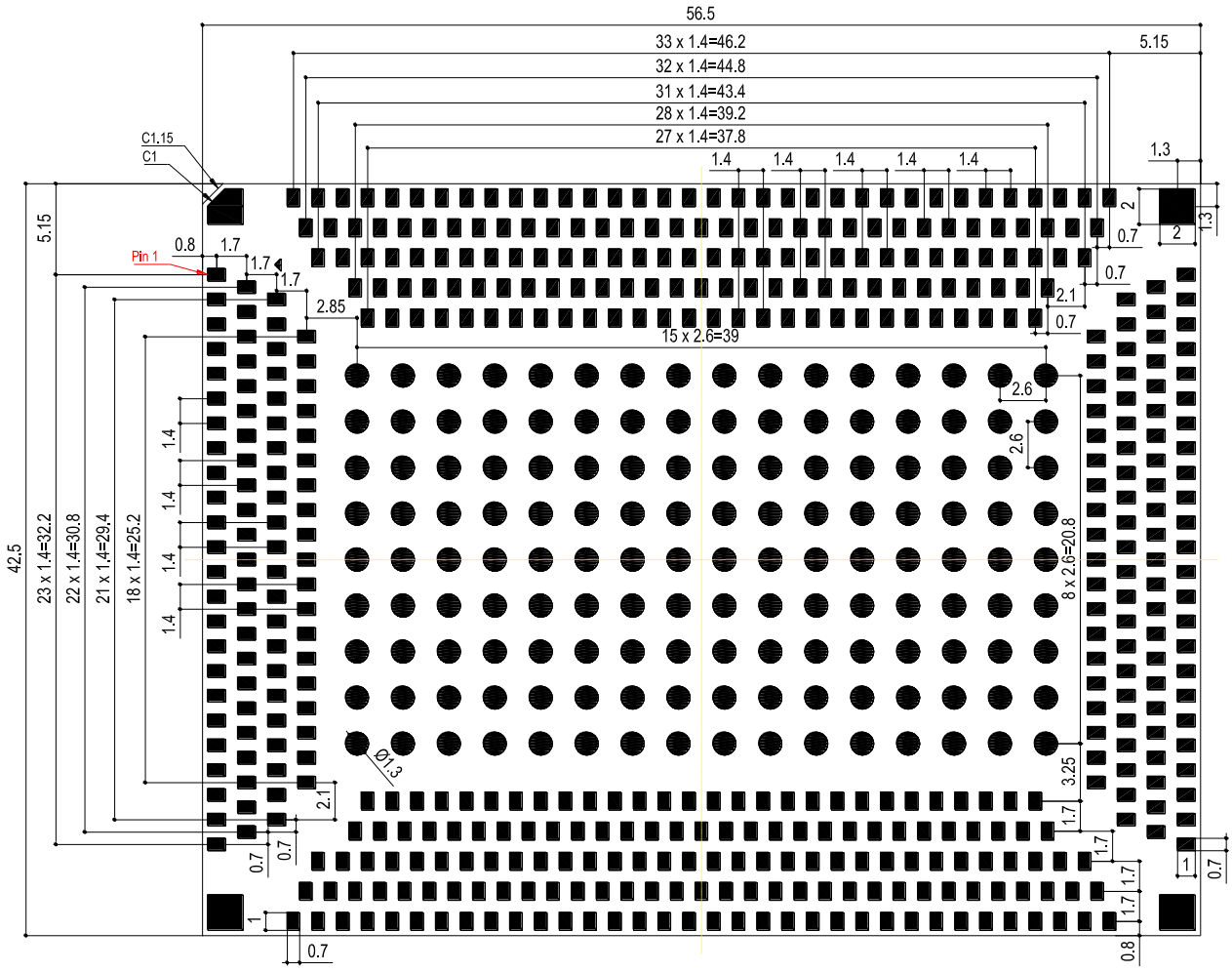


Figure 39: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

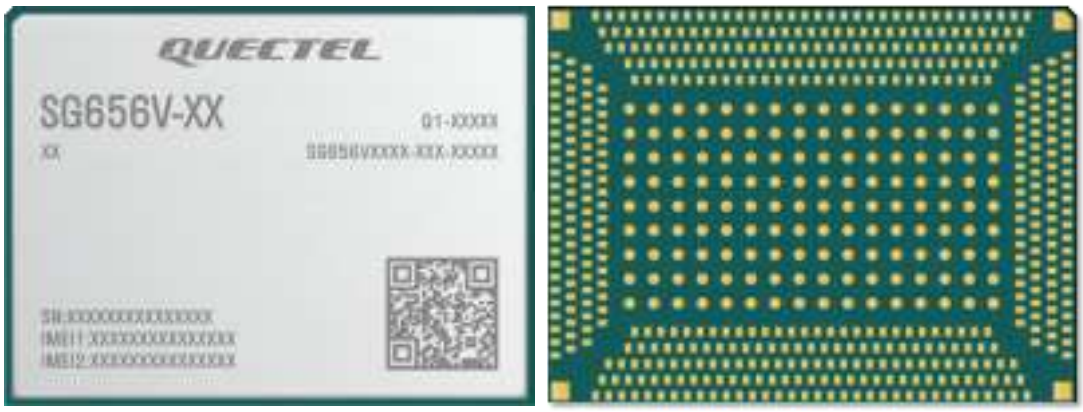


Figure 40: Top and Bottom Views of QLB12(SG656V) Series

Figure 41: Top and Bottom Views of QLA12(SG636V) Series

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [3] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

[3] This floor life is only applicable when the environment conforms to IPC/JEDEC J-STD-033. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to IPC/JEDEC J-STD-033. Do not unpack the modules in large quantities until they are ready for soldering.

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [4]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

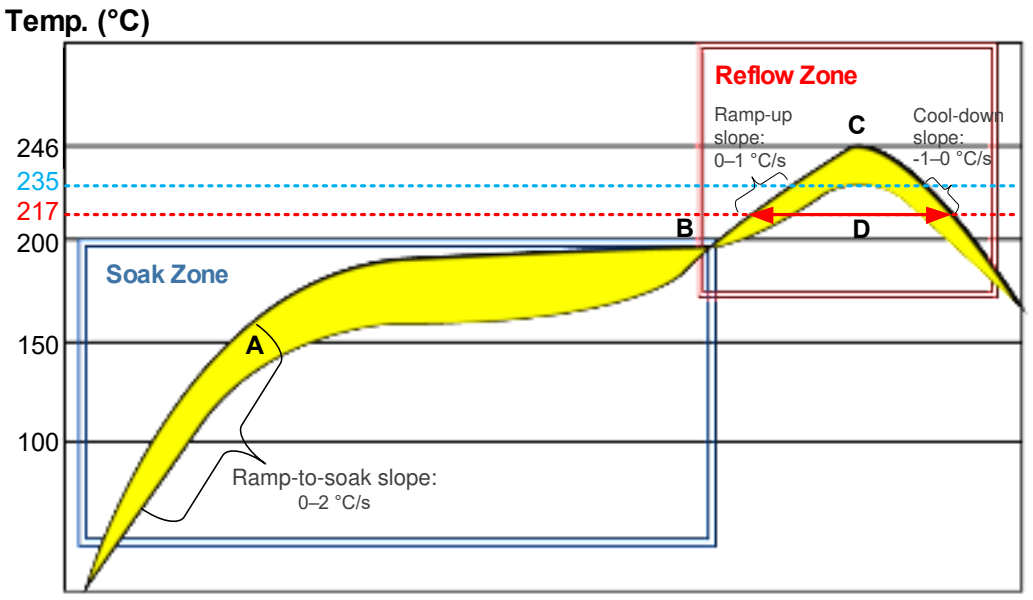


Figure 42: Recommended Reflow Soldering Thermal Profile

Table 59: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–2 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C ramp-up slope	0–1 °C/s
Reflow time (D: over 217°C)	40–65 s
Max temperature	235–246 °C
235–217 °C cool-down slope	-1–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, to avoid excessive temperature change, which may cause excessive thermal deformation of the metal shielding frame and cover, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste. If possible, please choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Due to the complexity of the SMT process, please contact Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [5]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in an injection tray packaging as specified in the sub-chapters below.

8.3.1. Injection Tray

Injection tray dimensions are illustrated in the following figure:

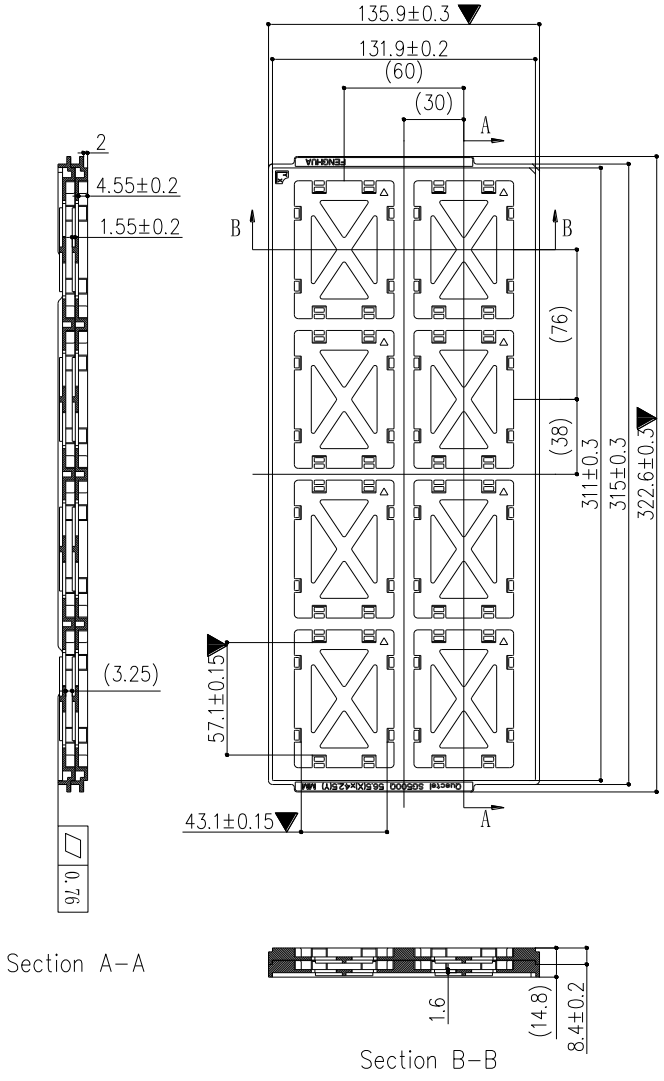
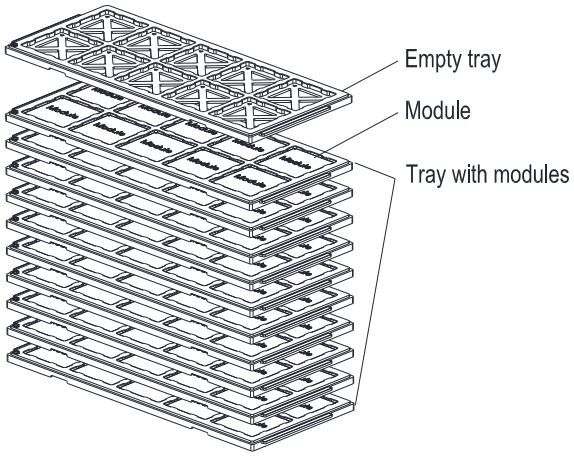


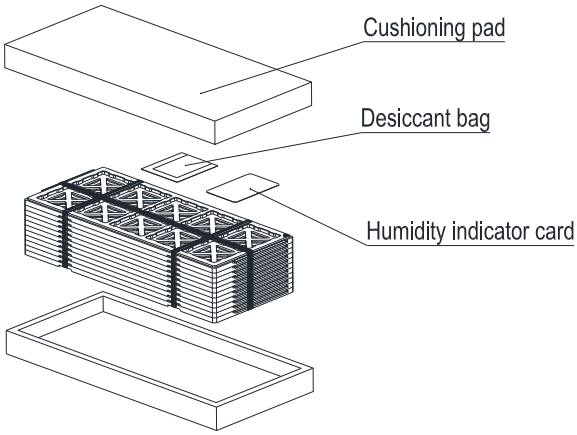
Figure 1: Injection Tray Dimension Drawing (Unit: mm)

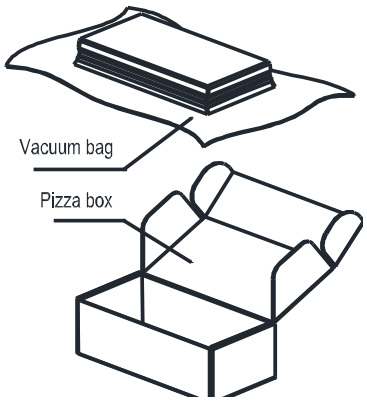
8.3.2. Packaging Process



Each injection tray packs 8modules. Stack 10 trays with modules, and place 1 empty tray on top.

Fasten the 11 trays. Add the humidity indicator card and desiccant bag on top, and place 2 cushioning pads on the top and bottom of the trays.





Place the injection trays with cushioning pads into a vacuum bag, and vacuumize it. Then, place the vacuum-packed trays into a pizza box. 1 pizza box can pack 80 modules.

Place 2 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 160 modules.

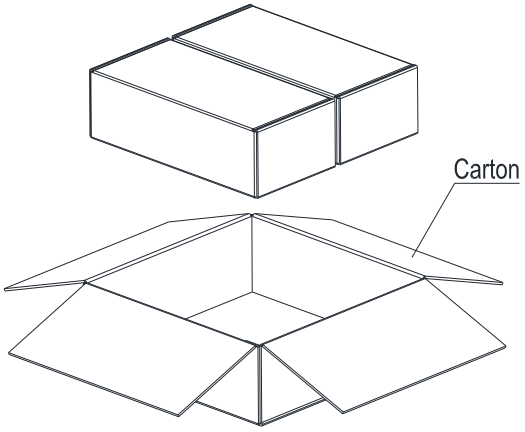


Figure 43: Packaging Process

9 Appendix References

Table 60: Related Documents

Document Name
[1] Smart_EVB_G5_User_Guide
[2] SG656V_Series_GPIO_Configuration
[3] RF_Layout_Application_Note
[4] Module_Stencil_Design_Requirements
[5] Module_SMT_Application_Note

Table 61: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
ADSP	Audio Digital Signal Processor
ALS	Ambient Light Sensor
AMR-NB	Adaptive Multi Rate-Narrow Band Speech Codec
AMR-WB	Adaptive Multi-Rate Wideband
AP	Access Point/Application Processor
ARM	Advanced RISC Machine
BDS	BeiDou Navigation Satellite System
BLE	Bluetooth Low Energy
bps	Bits per Second

BR	Basic Rate
CDMA	Code Division Multiple Access
CEP	Circular Error Probable
Cj	Junction Capacitance
CPE	Customer-Premise Equipment
CS	Coding Scheme
CSD	Circuit Switched Data
CSI	Camera Serial Interface
CTS	Clear to Send
DC	Dual Carrier
DC-HSPA+	Dual Carrier High Speed Packet Access Plus
DCS	Digital Cellular System
DL	Downlink
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Reference Phase Shift Keying
DRX	Discontinuous Reception
DSI	Display Serial Interface
DSP	Digital Signal Processor
ECM	Electret Condenser Microphone
EDGE	Enhanced Data Rate for GSM Evolution
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EGSM	Extended GSM
eMMC	Embedded Multimedia Card
eSCO	Extended Synchronous Connection Oriented

ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
EVDO	Evolution-Data Optimized
EVRC	Enhanced Variable Rate Codec
FDD	Frequency Division Duplex
fps	Frame per Second
FR	Full Rate
Galileo	Galileo Satellite Navigation System (EU)
GFSK	Gaussian Frequency Shift Keying
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GPU	Graphics Processing Unit
GRFC	Generic RF control
GSM	Global System for Mobile Communications
HR	Half Rate
HS	High Speed
HSDPA	High Speed Downlink Packet Access
HSPA+	High-Speed Packet Access+

HSUPA	High Speed Uplink Packet Access
HT	High Throughput
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IMT-2000	International Mobile Telecommunications for the year 2000
I/O	Input/Output
$I_I$max	Maximum Input Load Current
$I_O$max	Maximum Output Load Current
ISP	Image Signal Processor/Internet Service Provider
LCC	Leadless Chip Carrier
LCD	Liquid Crystal Display
LCM	LCD Module
LDO	Low Dropout Regulator
LE	Low Energy
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPDDR	Low-Power Double Data Rate
LTE	Long-Term Evolution
M2M	Machine to Machine
MAC	Media Access Control
MCS	Modulation and Coding Scheme
MEMS	Micro-Electro-Mechanical System
MIC	Microphone

MIMO	Multi-Input Multi-Output / Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
MP	Megapixel
MSL	Moisture Sensitivity Levels
MT	Mobile Terminating/Terminated
NTC	Negative Temperature Coefficient
OTA	Over-the-Air Upgrade
OTG	On-The-Go
OTP	One Time Programable
PAM	Power Amplifier Module
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication Service
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMU	Power Management Unit
POS	Point of Sale
PWM	Pulse Width Modulation
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System

RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation System
SCO	Synchronous Connection Oriented
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mounting Device
SMS	Short Message Service
SMT	Surface Mount Technology
STA	Station
TDD	Time-Division Duplex
TP	Touch Panel
TTFF	Time to First Fix
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
VHT	Very High Throughput

Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
$V_I$max	Absolute Maximum Input Voltage
$V_I$min	Absolute Minimum Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
$V_O$max	Maximum Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
Vrms	Root Mean Square Voltage
VSWR	Voltage Standing Wave Ratio
WAPI	WLAN Authentication and Privacy Infrastructure
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Network