1.0 HUGHES MODEL 9101 REGIONAL-BGAN SATELLITE IP MODEM: OSCILLATOR FREQUENCIES & CLOCK DISTRIBUTION

1.1 RF BLOCK DIAGRAM

Figure 1, is the proposed approach to implementing the IEET RF.

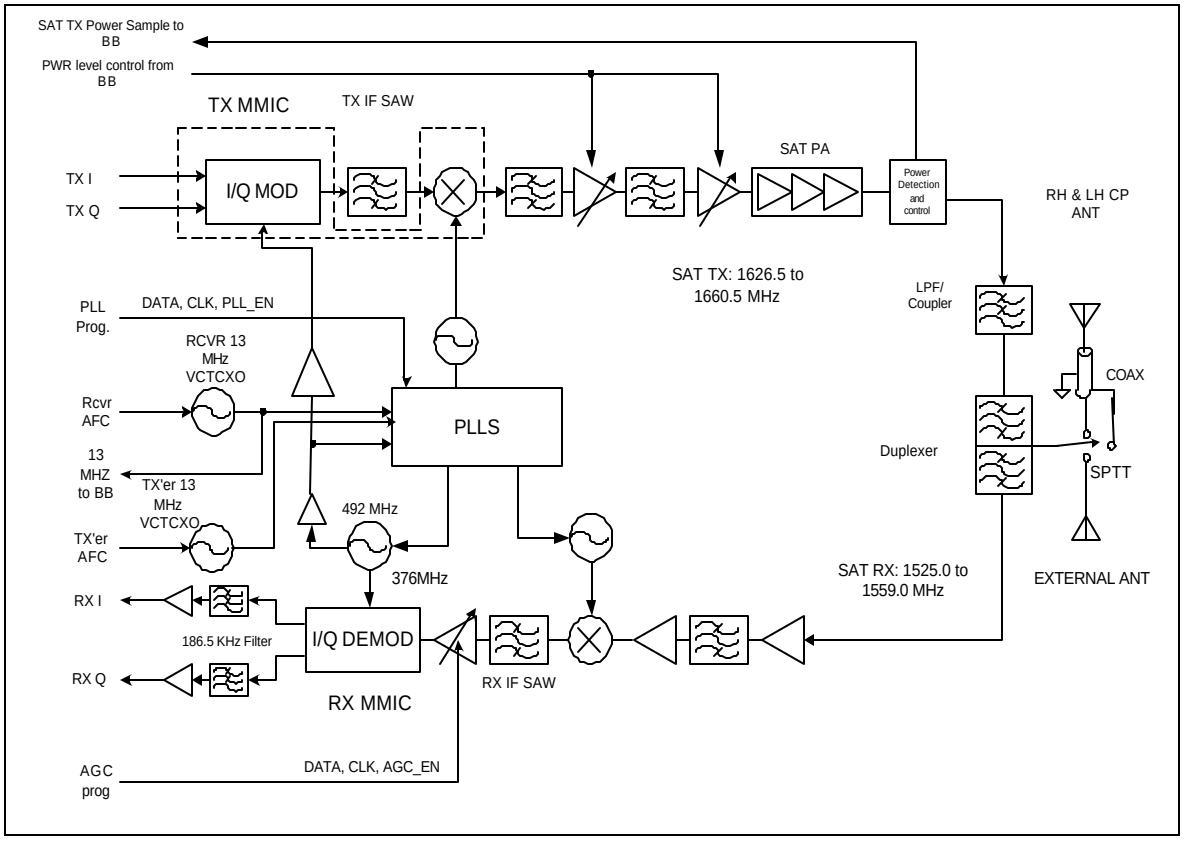

Figure 1. RF Block Diagram

The method of frequency synthesis is by PLL, with each chain having its own independent 13 MHz Voltage controlled temperature compensated oscillators Voltage Controlled/Temperature Controlled Crystal Oscillator (VCTCXO), a National Semiconductor LMX2336L dual PLL IC, L-band VCO(s), and discrete 376 MHz and 492 MHz VCOs.

1.2 L-BAND VCO(s) SPECIFICATIONS

Table 1. Summary Specifications

Parameter	Description	Requirement	Notes
TX RFLO	Transmit chain main loop, local oscillator	(1380.5 + 0.015625 x N) MHz	1 / N / 2175 TX IF = 246 MHz
RX RFLO	Receiver chain main loop, local oscillator	(1337.0 + 0.015625 x N) MHz	1 / N / 2175 188 MHz RF IF

Table 1. Summary Specifications

Parameter	Description	Requirement	Notes
TX IFLO	Transmit quad modulator IF local oscillator	492 MHz	2 x TX IF
RX IFLO	Receiver quad demod IF local oscillator	376 MHz	2 x RX IF

1.3 CLOCK DISTRIBUTION

The following provides the clocking distribution information for the MT Baseband circuit.
(Please refer to FPGA HLD Specification for internal FPGA clocking information) and see Figure 1.

- 13 MHz VCO for RF
  - 28.08 MHz (Generated by PLL circuit from 13 MHz) to FPGA

- 56.16 MHz (28.08 MHz multiplied by 2 in FPGA) for DSP McBSP interface

- 5.616 MHz (28.08 MHz divided by 5 in FPGA) for TX/RX ADC/DACs

- 14.04 MHz (28.08 MHz divided by 2 in FPGA) for Aux DAC

- 73.125 kHz (14.04 MHz divided by 192 in FPGA) for Aux ADC

- 20 MHz oscillator for Ethernet IC
  - 200 MHz for DSP (Generated in DSP internal PLL from 20 MHz clock in DSP)
  - 100 MHz DSP Memory Bus Clock (200 MHz divided by 2 in DSP) to FPGA

- 13 MHz Crystal oscillator for Bluetooth. Used by Bluetooth Controller IC's internal ARM7 processor to operate.

- 32 MHz oscillator for Bluetooth RF circuit

- 32 kHz oscillator for Bluetooth RF circuitry during low power modes to conserve power.

- 3.6864 MHz crystal to Microprocessor
  - 206 MHz for Microprocessor core (Generated in Microprocessor internal PLL from 32.768 MHz crystal)

  - 103 MHz Microprocessor Memory Bus clock (206 MHz divided by 2 in Microprocessor) to FPGA

- 32.768 kHz crystal for Microprocessor peripherals

- 16.368 MHz XTAL to GPS RF and GPS Baseband

- 32.768 kHz XTAL to GPS Baseband

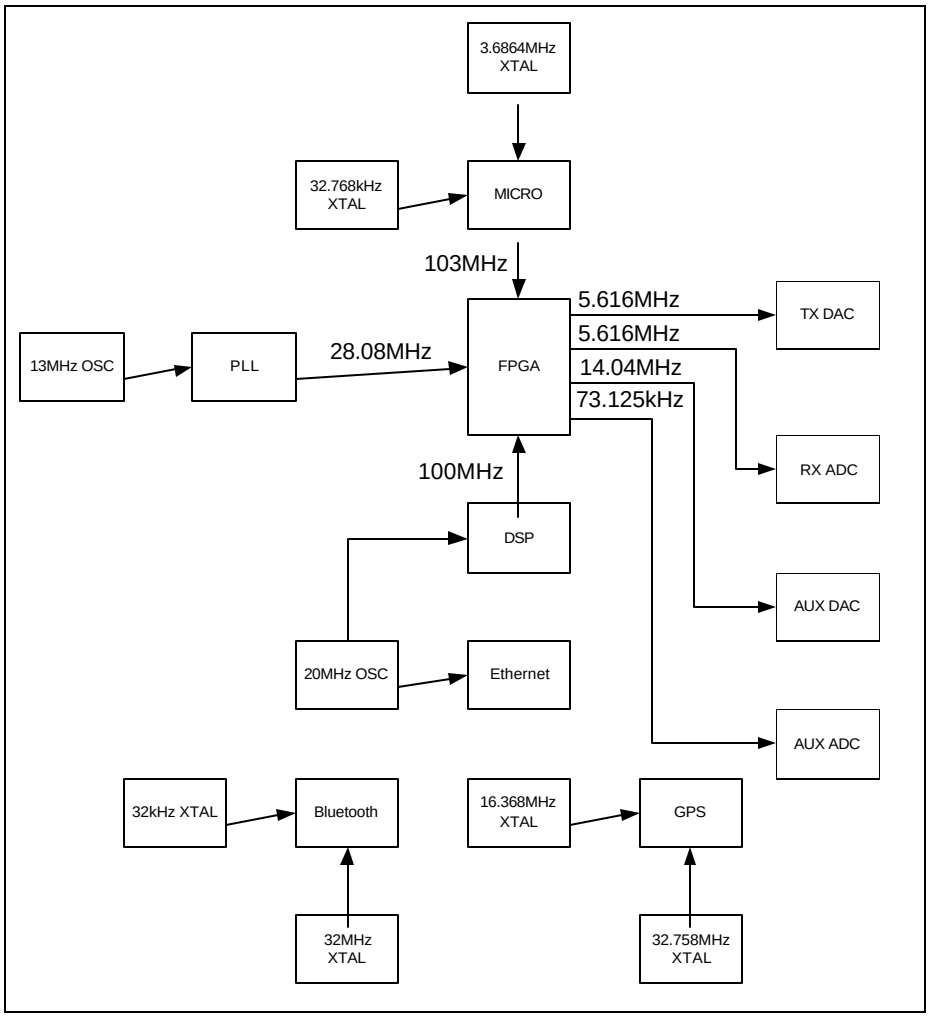

Figure 2. Clock Diagram