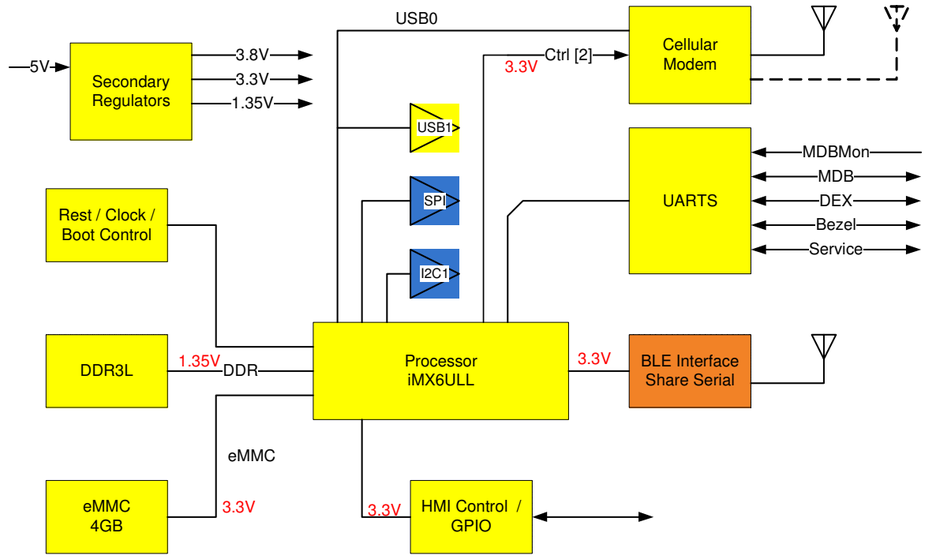
REVISIONS			
REV	ECN	DATE	CHECKED

SEE CPI MRP DATABASE FOR CHANGE HISTORY AFTER INITIAL DESIGN RELEASE



Required

"Free" Intfc

BLE Svc

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Crane Payment Innovations
Vending Machine Services Engineering

Title:

Alliance Family
"Irene" Processor Board Architecture

Drawn By:

Checked:

Project Engineer: Tony Radice

Size: B | File:

Scale: (none) | Sheet: ___ of ___ | Rev:

Applicable Spec(s): | Subject: | Alliance Program; MX6ULL Implementation Hardware Description Document | REF: | ECN: | Sheet: G1 | Page: 1 of 1

CRANE PAYMENT INNOVATIONS

3222 Phoenixville Pike Malvern, PA. 19355
Tel: (610) 430-2000 Fax: (610) 430-2004

TITLE	:	Advanced Feature Telemeter (AFT) Hardware Design Document Alliance Program; MX6ULL Implementation
NUMBER	:	300008362C
ISSUE	:	G1
ECN	:	N/A
DATE	:	12 September 2018
AUTHORS	:	Tony Radice/ Michael Perreca

LAST REVISED
DATE: 9/12/2018
TIME: 3:18:19 PM

MECHANICAL PARTS

CRANE PAYMENT INNOVATIONS

CIRCUIT DESIGN NOTEBOOK

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INITIAL END PRODUCT: Alliance

THIS DRAWING REPLACES:

REFERENCE PART NO.:

DRAWN: Mike Perreca	DATE	
CHECKED: Tony Radice	DATE	-
PROJECT ENGINEER: Tony Radice	DATE	-

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CRANE PAYMENT INNOVATIONS

TITLE: Alliance Control PCB

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1 | VOLUME: (CUBIC MM) | SHEET 1 OF 16

Revision History:

R1	11/2016	Initial Development - Project Alliance, Variant "Irene" developed from "Amy"	tr
Y2	8/2017	Added capacitors for EMI Mitigation	tr

REVISIONS			
REV	ECN	DATE	CHECKED

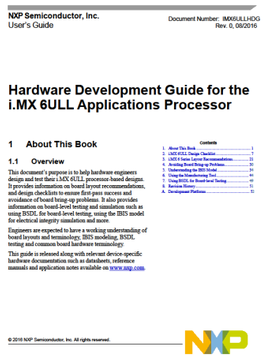
PC Board Stackup

1 - S1 - (TOP) "Component" Layer; Signal 1
2 - G1 - Ground Reference Layer;
3 - S2 - Signal Layer
4 - P1 - Power Layer; (Floods Only)
5 - P2 - Power Layer; (Floods Only)
6 - S3 - Signal Layer
7 - G2 - Ground Reference Layer
8 - S4 - (BOTTOM) Signal Layer

Notes:
1: NO signal traces permitted on layers G1 or G2
2: High Speed trace Requirements:
   a) Not Permitted on G1, G2, P1 or P2
   b) Should be predominantly run on S1/S2 pair OR S3/S4 pair.
   c) If transition between S1/S2 pair and S3/S4 pair must have a via connecting G1 and G2 no greater than 100 mils away from transition via.
3: Connections to ground (bypass caps) should minimize inductance. ie: Use largest trace width b/t pad & via practical.
4: Board should predominantly use RF Design Rules, especially in Processor / Memory region.
5: Gate drives for FETs should be run with floods, not traces.
6: Nets with prefix "V" should be run with floods, not traces.
7. Many Testpoints have the reference designator (TP) NOT Visible. They may be toggled to visible as required. This is done to reduce schematic clutter.

Variant Table

BOM		Processor	SW Structure	Cellular Radio	U10	Antenna Configuration
111556741C	Irene	i.MX6ULL	Linux / App	Telit LE-910	218505030C	2 x FAKRA
11155XXXXC	Julie	i.MX6ULL	Linux / App	Telit HE-910	218506021C	1 x SMA
	Krista	i.MX6ULL	Linux / App	Gemalto ELS-31		2 x FAKRA (?)


NXP Semiconductor, Inc.
User's Guide

Document Number: IMX6ULLHDG
Rev. 0, 08/2016

Hardware Development Guide for the i.MX 6ULL Applications Processor

1 About This Book

1.1 Overview

This document's purpose is to help hardware engineers design and test their i.MX 6ULL processor-based designs. It provides information on board layout recommendations, and design checklists to ensure first-pass success and avoidance of board bring-up problems. It also provides information on board-level testing and simulation such as using BSDL for board-level testing, using the IBIS model for electrical integrity simulation and more.

Engineers are expected to have a working understanding of board layouts and terminology, IBIS modeling, BSDL testing and common board hardware terminology.

This guide is released along with relevant device-specific hardware documentation such as datasheets, reference manuals and application notes available on www.nxp.com.

Contents

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TITLE: Alliance Control PCB Variant Table

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

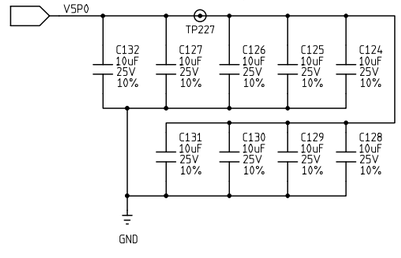
SCALE: 1/1 | VOLUME: (CUBIC MM) | SHEET 2 OF 16

Power Supply Manifest		Voltage			Current (mA)	
		Min	Typ	Max	Reqd	Design
V5P0						
V3P8	Cellular Modem Supply				2000	2000
V3P3_SNVS	SNVS Supply				0.5	50
V3P3_VDD_HIGH	VDD_HIGH Supply				200	350
V3P3	GPIO				2000	2000
V3P3_AUX	Auxilary Supply				0	1000
V1P35	DDR3L Supply					1000
V1P3	Core supply				500	1000

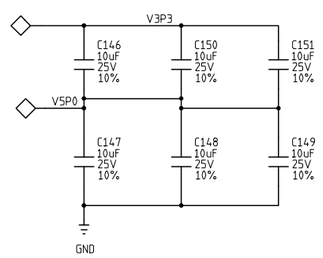
Design Rules:
1. All "V" Prefix nets biased toward layers 4 & 5
2. All nets on layers 4 & 5 intended to be routed by floods rather than trace.
3. Please make V5P0 a FLOOD.

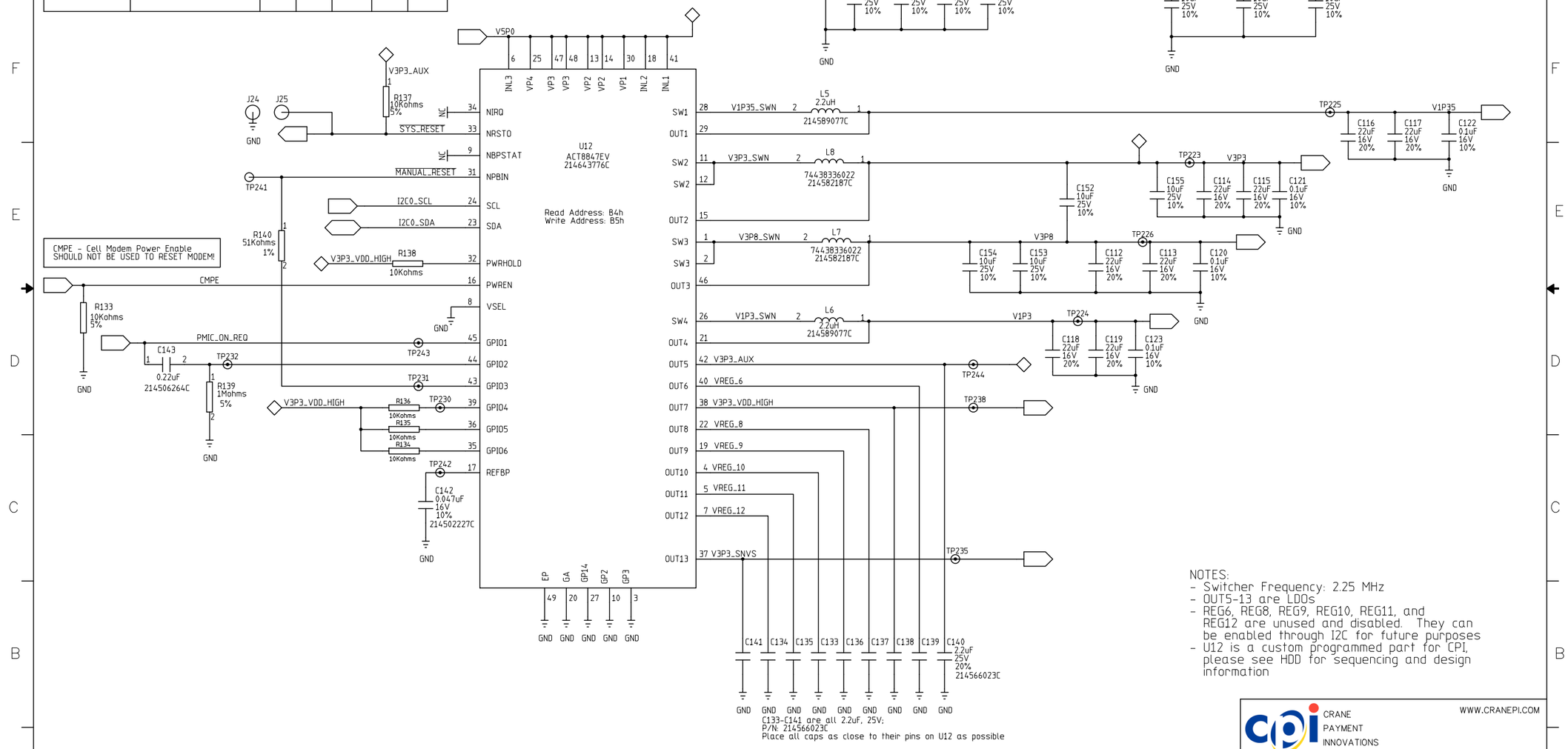
REVISIONS			
REV	ECN	DATE	CHECKED

Please plpace 10uF Caps as close as practical to each INLx and VPx pin



Please place these components per EMI mitigation recommendations (Along with C___ thru ___)





NOTES:
- Switcher Frequency: 2.25 MHz
- OUT5-13 are LDOs
- REG6, REG8, REG9, REG10, REG11, and REG12 are unused and disabled. They can be enabled through I2C for future purposes
- U12 is a custom programmed part for CPI, please see HDD for sequencing and design information

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TITLE				
Alliance Control PCB Power Supply				
SIZE: C	DESIGN CENTER: MVN	DOC CL: CD	DWG NO.: 300008362C	REV: G1
SCALE: 1/1	VOLUME:	(CUBIC MM)	SHEET 3 OF 16	

REVISIONS			
REV	ECN	DATE	CHECKED

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TITLE

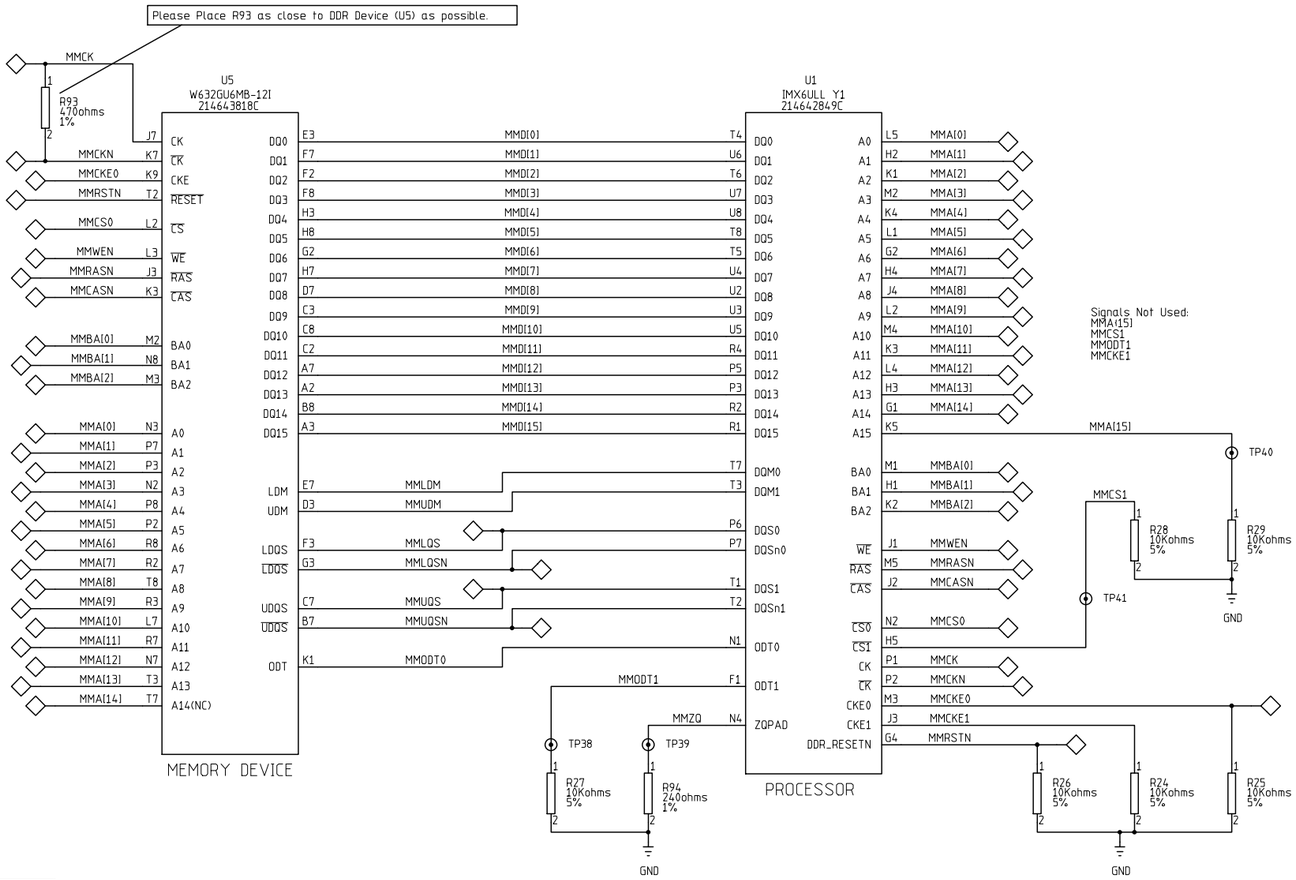
Alliance Control PCB
Page Intentionally blank

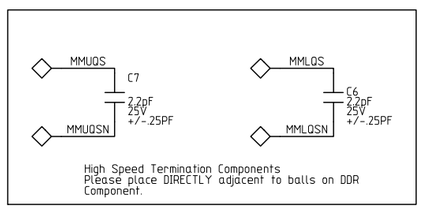
SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1	VOLUME: (CUBIC MM)	SHEET 4 OF 16

REVISIONS			
REV	ECN	DATE	CHECKED

Please Place R93 as close to DDR Device (U5) as possible.





Please refer to Hardware Design Guide,
Checklist 2.1, Table 4 - DDR recommendations
and sections 3.3 through 3.6
for Layout Guidance.

CRITICAL NOTE:
NO ADDITIONAL TESTPOINTS ARE AUTHORIZED ON THIS PAGE.

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TITLE				
Alliance Control PCB DDR3 Subsystem				
SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1
SCALE: 1/1	VOLUME:	(CUBIC MM)	SHEET 5 OF 16	

REVISIONS			
REV	ECN	DATE	CHECKED

Note on eMMC Frequency Content:
1) Max Clock Frequency: 52 MHz
2) Rise / Fall time(s): 3 nS MAX (@35MHz)

U4
MTFC4GACAJCN-4M IT
214644642C

eMMC MEMORY

U1
IMX6ULL Y1
214642849C

PROCESSOR

Extra ports to NC Pins for Routing Purposes.

Extra pins are utilized to allow fine pitch routing - traces are allowed to touch NC pads in order to reach pads closer to core of device.
Methodology is suggested by IC manufacturer.

Design Intent:
IF Ethernet External adapter to be used:
GPIO1_21 to be used for Ethernet Reset
GPIO1_23 is unallocated

J4
2053390960
14 PIN ZIF RA
DO NOT POPULATE

SIZE	C
DESIGN CENTER	MVN
DOC CL	CD
DWG NO.	300008362C
REV	G1
SCALE:	1/1
VOLUME:	(CUBIC MM)
SHEET	6 OF 16

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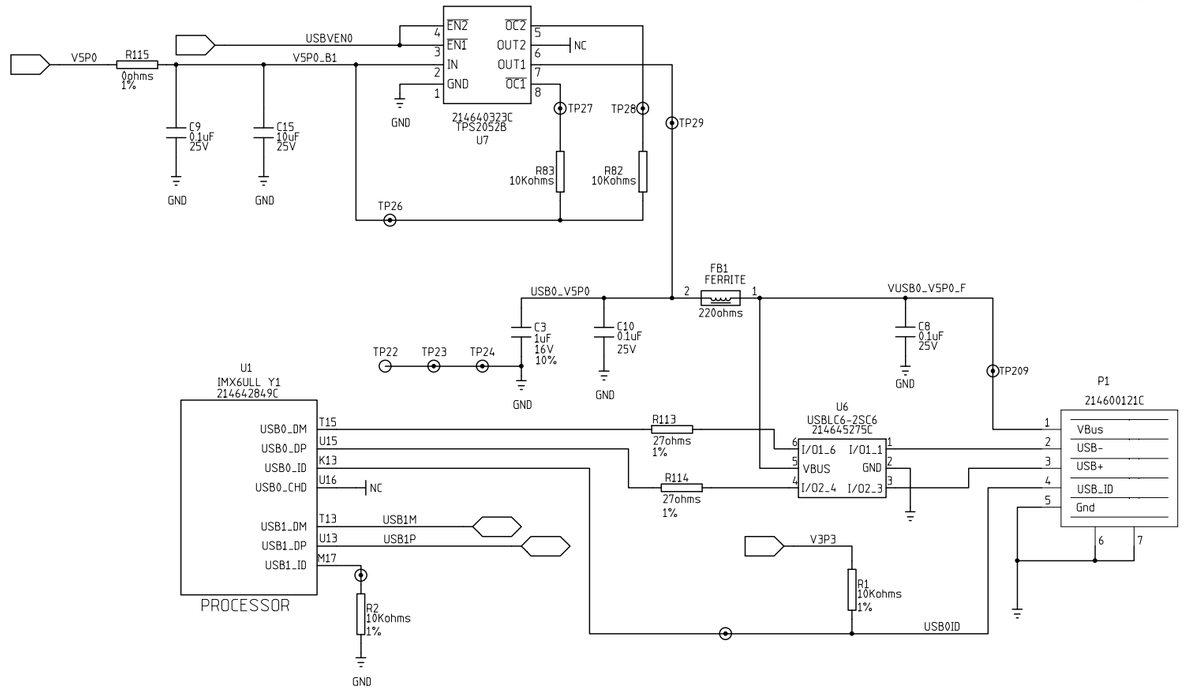
USB Current Limited Switch

USB Channel 0 to OTG Connector
USB Channel 1 to Cellular Radio

REVISIONS			
REV	ECN	DATE	CHECKED



USB0_CHD Pin OK to leave NC
Design Checklist iMX6ULHDG Table 18

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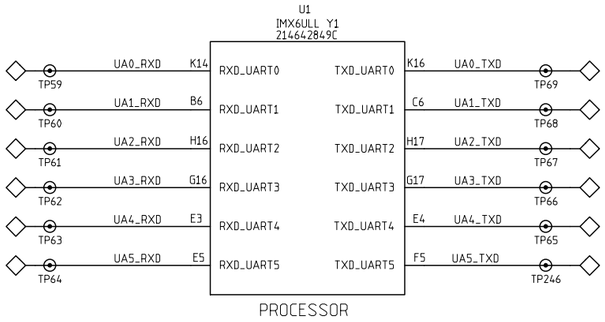
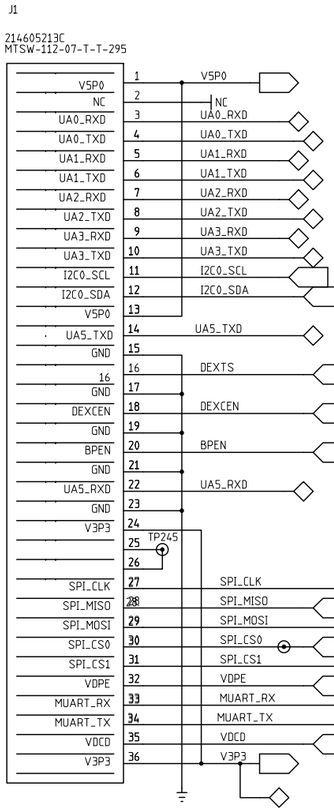
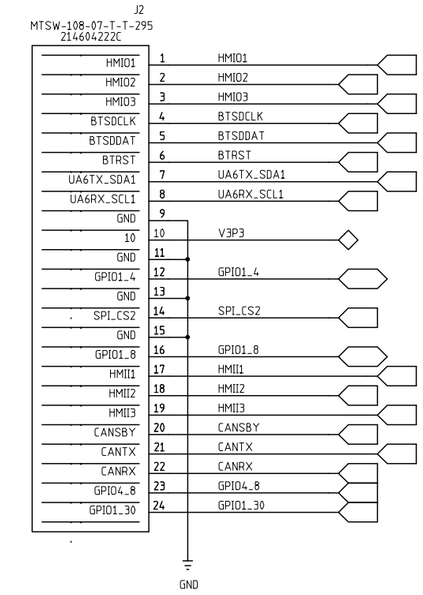
TITLE				
Alliance Control PCB USB Subsystem				
SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1
SCALE: 1/1	VOLUME:	(CUBIC MM)	SHEET 7 OF 16	



UART Assignments		Notes
0	MDB Comms	Isolated comm to VMC
1	DEX	
2	Bezel	
3	Service Tool	
4	Terminal (Monitor)	Aux Serial Channel for Cell Modem
5	MDB Monitor	RX Only
6	Bluetooth Serial	

REVISIONS			
REV	ECN	DATE	CHECKED





FOR CELL MODEMS WITH ONLY UART CAPABILITY
1) Depopulate R__ and R__
2) Populate R___ and R___
UART 4 is now redirected to Cell Radio

IF UART IS REMOVED FROM INTERFACE
GPIO lines may be utilized by populating R___ and R___

Please see Connection Map
Connector Numbering Rule:

Column	J1	J2
A	1 - 12	1 - 8
B	13 - 24	9 - 16
C	25 - 36	17 - 24

J1

A	B	C		A	B	C
5V	5V	(Pwr En)	1	HMIO1	GND	HMII1/ADC6
nc	nc	(Pwr En)	2	HMIO2	V3P3	HMII2/ADC7
UA1RX	GND	SPICLK	3	HMIO3	GND	HMII3/ADC8
UA1TX	DEXTS	SPIMISO	4	BTSDCLK	(PWM 3)	CANSBY
UA2RX	GND	SPIMOSI	5	BTSDDAT	GND	CANTX
UA2TX	DEXCEN	SPICS1	6	BTRST	SPICS3	CANRX
UA3RX	GND	SPICS2	7	UA7TX	GND	
UA3TX	BPEN	VDPE	8	UA7RX		
UA4RX	GND	UA5RX	9			
UA4TX	UA6RX	UA5TX	10	Note:		
I2C0_N	GND	VDCD	11	BT SDCLK – Alt Use: ADC 1		
I2CDat	V3P3	V3P3	12	BT SDDAT – Alt Use: ADC 2		

Signal	Description	D	Lvl
V5P0	Power to Module	I	5
V3P3	Interface / Signal Lvl	O	3.3
I2C0_N	I2C Interface C/N	O	3.3
I2CDat	I2C Interface Data	B	3.3
UA1RX	MDB – VMC OUTPUT	I	3.3
UA1TX	MDB – VMC INPUT	O	3.3
UA2xx	DEX UART	-	3.3
UA3xx	Bezel UART	-	3.3
UA4xx	Service Port UART	-	3.3
UA5xx	Utility Port UART	-	3.3
UA6RX	MDB Monitor – VMC Input	I	3.3
BPEN	Bezel Power Enable	O	3.3
DEXCEN	DEX Com Enable*	O	3.3
DEXTS	DEX Com Tri-State*	O	3.3
VDPE	Video Display Power En.	O	3.3
VDCD	Video Display Comm Dr.	O	3.3
SPICLK	Ser Per Intfc Clock	O	3.3
SPIMOSI	Ser Per Intfc Master Out	O	3.3
SPIMISO	Ser Per Intfc Master In	I	3.3
SPICSn	Ser Per Intfc Select Out	O	3.3
(Pwr En)	Pins shorted to enable PS	-	-

Signal	Description	D	Lvl
HMIIn	HMI Inputs (to GPIO)	I	3.3
HMIOn	HMI Outputs (LED PWM)	O	3.3
BTSDCLK	Bluetooth Programming	O	3.3
BTSDDAT	Bluetooth Programming	B	3.3
BTRST	Bluetooth Reset	O	3.3
CANTX	CAN Adapter TX Data	O	3.3
CANRX	CAN Adapter RX Data	I	3.3
CANSBY	CAN Standby Status	O	3.3
UA7xx	Bluetooth Comm	*	3.3
(PWM1)	Reserved	*	3.3

Note:
SPICS1: Utility Port
SPICS2: Interface Board Bluetooth CS
SPICS3: (Reserved)
SPICS4: (Not on Interface) BT / Proc Brd

' Necta Machine Support
* Seilaf Machine Support

Crane Payment Innovations
VMS Engineering

Title:
Interface Layout - Pin Map
Alliance Architecture

Drawn By:
Checked:
Project Engineer: Tony Radice
Size: A | File:
Scale: (none) | Sheet: 1 of 1 | Rev: 3.0

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TITLE
Alliance Control PCB
Serial Interfaces I

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1 | VOLUME: (CUBIC MM) | SHEET 8 OF 16

REVISIONS			
REV	ECN	DATE	CHECKED

BootConfig Port Mapping	
BOOTCFG[0]	BOOT_CFG1[0]
BOOTCFG[1]	BOOT_CFG1[1]
BOOTCFG[2]	BOOT_CFG1[2]
BOOTCFG[3]	BOOT_CFG1[3]
BOOTCFG[4]	BOOT_CFG1[4]
BOOTCFG[5]	BOOT_CFG1[5]
BOOTCFG[6]	BOOT_CFG1[6]
BOOTCFG[7]	BOOT_CFG1[7]
BOOTCFG[8]	BOOT_CFG2[0]
BOOTCFG[9]	BOOT_CFG2[1]
BOOTCFG[10]	BOOT_CFG2[2]
BOOTCFG[11]	BOOT_CFG2[3]
BOOTCFG[12]	BOOT_CFG2[4]
BOOTCFG[13]	BOOT_CFG2[5]
BOOTCFG[14]	BOOT_CFG2[6]
BOOTCFG[15]	BOOT_CFG2[7]
BOOTCFG[16]	BOOT_CFG4[0]
BOOTCFG[17]	BOOT_CFG4[1]
BOOTCFG[18]	BOOT_CFG4[2]
BOOTCFG[19]	BOOT_CFG4[3]
BOOTCFG[20]	BOOT_CFG4[4]
BOOTCFG[21]	BOOT_CFG4[5]
BOOTCFG[22]	BOOT_CFG4[6]
BOOTCFG[23]	BOOT_CFG4[7]

U1
IMX6ULL_Y1
214642849C

GPIO3_5	B9	BOOTCFG[0]	TP70
GPIO3_6	A9	BOOTCFG[1]	TP71
GPIO3_7	E10	BOOTCFG[2]	TP72
GPIO3_8	D10	BOOTCFG[3]	TP73
GPIO3_9	C10	BOOTCFG[4]	TP74
GPIO3_10	B10	BOOTCFG[5]	TP75
GPIO3_11	A10	BOOTCFG[6]	TP76
GPIO3_12	D11	BOOTCFG[7]	TP77
GPIO3_13	B11	BOOTCFG[8]	TP78
GPIO3_14	A11	BOOTCFG[9]	TP79
GPIO3_15	E12	BOOTCFG[10]	TP80
GPIO3_16	D12	BOOTCFG[11]	TP81
GPIO3_17	C12	BOOTCFG[12]	TP82
GPIO3_18	B12	BOOTCFG[13]	TP83
GPIO3_19	A12	BOOTCFG[14]	TP84
GPIO3_20	D13	BOOTCFG[15]	TP85
GPIO3_21	C13	BOOTCFG[16]	TP86
GPIO3_22	B13	BOOTCFG[17]	TP87
GPIO3_23	A13	BOOTCFG[18]	TP88
GPIO3_24	D14	BOOTCFG[19]	TP89
GPIO3_25	C14	BOOTCFG[20]	TP90
GPIO3_26	B14	BOOTCFG[21]	TP91
GPIO3_27	A14	BOOTCFG[22]	TP92
GPIO3_28	B16	BOOTCFG[23]	TP93
GPIO3_2	D9		
GPIO3_3	C9		
GPIO3_0	A8		

GND

PROCESSOR

Notes:
Select SD1 for Boot Mode

V3P3

5 Places
R98
1Kohms
1%

DO NOT POPULATE
DO NOT POPULATE
1Kohms
1Kohms
1Kohms
1Kohms

R60
10Kohms
5%
19 Places

TP94
TP95
TP96
TP97

214780009C
S1
DO NOT POPULATE
5 6 7 8
11 10
12 9
1
GND 4 3 2 1 GND

4 Places
R4
0ohms
5%

DO NOT POPULATE
DO NOT POPULATE
0ohms
0ohms
0ohms

BOOTCFG[0]
BOOTCFG[1]
BOOTCFG[2]
BOOTCFG[3]
BOOTCFG[4]
BOOTCFG[5]
BOOTCFG[6]
BOOTCFG[7]
BOOTCFG[8]
BOOTCFG[9]
BOOTCFG[10]
BOOTCFG[11]

BOOTCFG[12]
BOOTCFG[13]
BOOTCFG[14]
BOOTCFG[15]
BOOTCFG[16]
BOOTCFG[17]
BOOTCFG[18]
BOOTCFG[19]
BOOTCFG[20]
BOOTCFG[21]
BOOTCFG[22]
BOOTCFG[23]

R37
10Kohms
5%
24 Places

DO NOT POPULATE
DO NOT POPULATE

GND

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TITLE
Alliance Control PCB
LCD Interface / Boot Mode

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 9 OF 16

REVISIONS			
REV	ECN	DATE	CHECKED

Note:
JTAG Pins have no alternate use.
They may disabled in the Pin Config tool.
Values and rail per iMX6ULHDG Table 8.

V3P3
R30 10Kohms 5%
R31 10Kohms 5%
R33 10Kohms 5%
TP98
TP99
TP100
TP101
TP102
TP103
TA1
TESTPAD8
DO NOT POPULATE
R32 10Kohms 5%
R111 1Kohms 1%
GND

U1
IMX6ULL_Y1
214642849C
TRSTn N14
TCK M14
TDI N16
TDO N15
TMS P14
MOD P15
XTALO T17
XTALI T16
RTC_OUT U11
RTC_IN T11
CLKP P17
CLKM P16

R103 1Kohms 1%
Y101DRV
Y101RTN
Y102DRV
Y102RTN
Y3 24M
Y1 32.768k
C33 18pF 25V
C32 18pF 25V
R120 2.2Mohms 5%
C30 10pF 50V +/-.25PF
C29 10pF 50V +/-.25PF
J19
J20
TP104
TP105
R34 10Kohms 5%
R35 10Kohms 5%

PROCESSOR

Recommendation - IMX6ULHDG
Table 11, #7

Testpoints are NOT authorized on the nodes containing the following endpoints:
U1.T17 U1.T11 Y3.3
U1.T16 U1.U11

U13
STSAF-A100
214642920C
V3P3
C145 10uF 25V 10% 2145002240C
C144 0.1uF 25V 10% 2145091340C
I2C0_SCL 7
I2C0_SDA 5
STSAFE_RESET 8
VCC 2
SCL
SDA
RESET
NC1 1
NC3 3
NC6 6
GND 4
Address: 20h

Recommendation - IMX6ULHDG
Table 12, #2

NOTE: See reference manual for specific boot device and mode. Boot depends on S7 AND LCD settings.

U1
ON_OFF R8 NC
POR_B P8 SYS_RESET TP107
GPIO5_0 R10
GPIO5_1 R9
GPIO5_2 P11
GPIO5_3 P10
GPIO5_4 P9
GPIO5_5 N8
GPIO5_6 N11
GPIO5_7 N10
GPIO5_8 N9
GPIO5_9 R6
PMIC_ON_REQ T9 PMIC_ON_REQ J12
PMIC_SBY_REQ U9 J11
BOOTMODE0 T10 TP108 BOOTMODE0
BOOTMODE1 U10 TP109 BOOTMODE1
TEST_MODE N7
IMX6ULL_Y1
214642849C
PROCESSOR

V3P3
R80 10Kohms
R81 10Kohms
TP110
TP111
USER_SEL
DIAG_MODE
R4 0ohms 5% DO NOT POPULATE
R5 0ohms 5% DO NOT POPULATE
S2
214780009C
DO NOT POPULATE

Note: Set GPIO for DIAG_MODE to INTERNAL PULLUP.

V3P3
R116 3.3Kohms 5%
R117 3.3Kohms 5%
R118 3.3Kohms 5%
R119 3.3Kohms 5%
DO NOT POPULATE
DO NOT POPULATE

U1
IMX6ULL_Y1
214642849C
I2C0SCL F3 I2C0_SCL
I2C0SDA F2 I2C0_SDA
I2C1SCL B17 UA6RX_SCL1
I2C1SDA A15 UA6TX_SDA1
SPICLK A16 SPI_CLK
SPID0 D17 SPI_MISO
SPID1 B15 SPI_MOSI
SPICS0 A5 SPI_CS0
SPICS1 B7 SPI_CS1
PROCESSOR

CRANE PAYMENT INNOVATIONS
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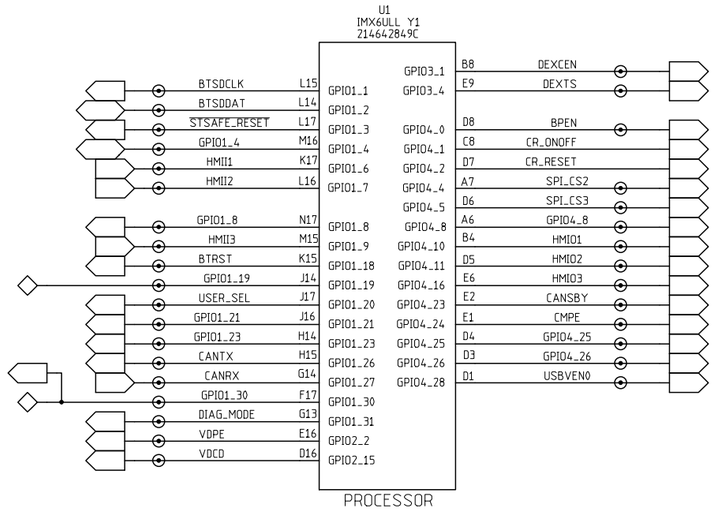
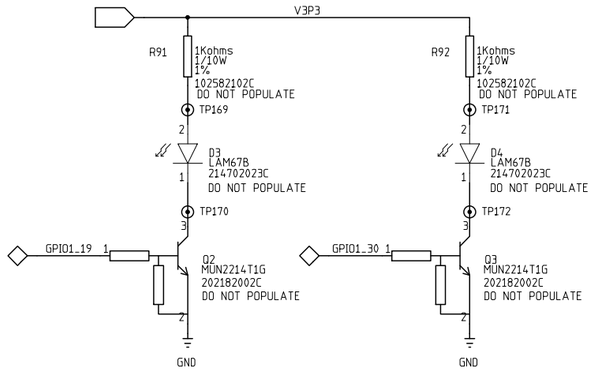
TITLE: Alliance Control PCB Support / Security

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 10 OF 16



Note: Set GPIOs for DIAG_MODE and USER_SEL to INTERNAL PULLUP.



Proc ID	Pin #	Signal Name	Purpose	Notes
GPIO1_0	K13	USB0ID	USB OTG Port ID	Bootable Port
GPIO1_1	L15	BTSDCLK	Bluetooth Interface two wire clock	
GPIO1_2	L14	BTSSDAT	Bluetooth Interface Data Port	
GPIO1_3	L17	STSAFE_RESET	STSafe Reset Line Active Low	
GPIO1_4	M16	GPIO1_4	Interboard - Optional for GPIO, PWM or ADC, Interface J2 Pin B4	
GPIO1_6	K17	HDMII1	HMI Input 1	
GPIO1_7	L16	HDMII2	HMI Input 2	
GPIO1_8	N17	GPIO1_8	InterBoard - Optional for GPIO, PWM or ADC, Interface J2 Pin B8	
GPIO1_9	M15	HDMII3	HMI Input 3	
GPIO1_18	K15	BTRST	Bluetooth Interface Reset	
GPIO1_19	J14	GPIO1_19	If populated use for diagnostic LED	
GPIO1_20	J17	USER_SEL	User (programming) test switch - generally unallocated	
GPIO1_21	J16	GPIO1_21	Reserved for Ethernet Adapter: ENET_RESET	
GPIO1_23	H14	GPIO1_23	Reserved for Ethernet Adapter: (Unallocated)	
GPIO1_26	H15	CANTX	CAN Interface Data Output	
GPIO1_27	G14	CANRX	CAN Interface Data Input	
GPIO1_30	F17	GPIO1_30	If populated use for diagnostic LED	
GPIO1_31	G13	DIAG_MODE	Diagnostic Mode when Grounded	
GPIO2_2	E16	VDPE	Video Display Power Enable	
GPIO2_15	D16	VDCD	Video Display Communications Direction	
GPIO3_1	B8	DEXCEN	DEX Communications Enable	
GPIO3_4	E9	DEXTS	DEX Tri-State COntrol	
GPIO4_0	D8	BPEN	Bezel Power Enable	
GPIO4_1	C8	CR_ONOFF	Cellular Radio On Off	
GPIO4_2	D7	CR_RESET	Cellular Radio Emergency Reset	
GPIO4_4	A7	SPI4_CS2	SPI Reserved CS	
GPIO4_5	D6	SPI_CS3	Processor Board Bluetooth SPI Enable	
GPIO4_8	A6	GPIO4_8	Bluetooth Adapter GPIO Port B Bit 3	
GPIO4_10	B4	HMIO1	HMI Output 1	
GPIO4_11	D5	HMIO2	HMI Output 2	
GPIO4_16	E6	HMIO3	HMI Output 3	
GPIO4_23	E2	CANSBY	CAN Interface Standby Signal	
GPIO4_24	E1	CMPE	Cell Modem Power Enable (Pull down by default!)	
GPIO4_25	D4	GPIO4_25	Alternate signal for UART4 RXD Interface Pin	
GPIO4_26	D3	GPIO4_26	Alternate signal for UART4 TXD Interface Pin	
GPIO4_28	D1	USBVEN0	USB 5V Out Enable	

Notes:
1) Please place pullup / pulldown at target location for GPIO.

REVISIONS			
REV	ECN	DATE	CHECKED

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TITLE: Alliance Control PCB GPIO Definition

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 11 OF 16

REVISIONS			
REV	ECN	DATE	CHECKED

Keep nets ANTx as short as possible. Must be 50 Ohms. NO VIAS - NO TESTPOINTS

The USBP and USBN Nets Are to be routed 90 Ohm Differential Drive

NOTE
When DIR Grounded, dir is from B to A

U2
SN74AVCH1T45DCKR
214648461C

U3
SN74AVCH1T45DCKR
214648461C

U10
LE910-SVL
218505030C

Pri Ant
J21
CONN COAX SMB RA
214602206C

Sec Ant
J22
CONN COAX SMB RA
214600207C

R86 10Kohms 5%
R87 10Kohms 5%
R90 1Kohms 1/10W 1% 102582102C

D2
LAM67B
214702023C

Q1
MUN2214T1G
202182002C

Q4
RN1401
105167001C

Q5
RN1401
105167001C

U9
214620087C
DIODE4C1A_SOT353

J23
693-012-040-811
214668062C

R121 22ohms 5%
R122 22ohms 5%
R123 22ohms 5%

C12 10uF 25V 10%
C35 100pF 50V 20%
C34 100pF 50V 20%
C58 33pF 25V 5%
C57 33pF 25V 5%
C56 33pF 25V 5%
C47 0.1uF 16V 10% 214509091C

J5 DO NOT POPULATE
J6 DO NOT POPULATE
J7 DO NOT POPULATE
J8 DO NOT POPULATE
J9 DO NOT POPULATE
J10 DO NOT POPULATE

Please place capacitor as close as practicable to pin, even on opposite side of board. Please minimize inductance to pads.

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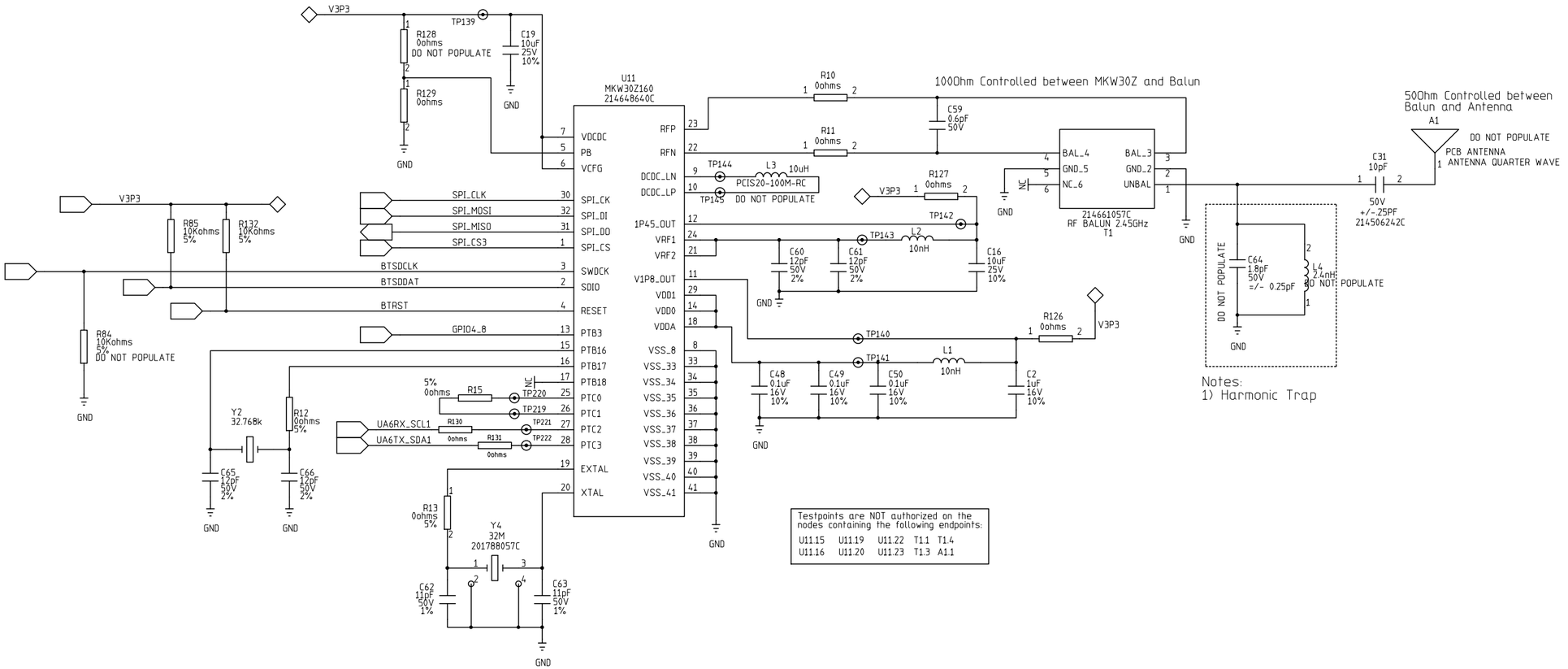
TITLE
Alliance Control PCB
Cellular Radio Module

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 12 OF 16

REVISIONS			
REV	ECN	DATE	CHECKED



Testpoints are NOT authorized on the nodes containing the following endpoints:

U11.15	U11.19	U11.22	T1.1	T1.4
U11.16	U11.20	U11.23	T1.3	A1.1

Bluetooth Subsystem is Do No Populate!
If populated, All visible DNP's are valid
Please see HDD for clarification

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TITLE
Alliance Control PCB
Bluetooth Low Energy Interface

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 13 OF 16

REVISIONS			
REV	ECN	DATE	CHECKED

U1
IMX6ULL Y1
214642849C

V1P3
C109 22uF 16V 20%
C69 4.7uF 25V 20%
C84 0.22uF 10V 15%
C83 0.22uF 10V 15%
GND

V1P35
C13 10uF 25V 10%
C86 0.22uF 10V 15%
C85 0.22uF 10V 15%
C87 0.22uF 10V 15%
C89 0.22uF 10V 15%
C88 0.22uF 10V 15%
C90 0.22uF 10V 15%
GND

V3P3_SNVS
C99 0.22uF 10V 15%
GND

V3P3_VDD_HIGH
C71 4.7uF 25V 20%
C98 0.22uF 10V 15%
GND
GND

V3P3
FERRITE FB2 220ohms
FERRITE FB3 220ohms
FERRITE FB4 220ohms
FERRITE FB5 220ohms
VCC_CSI
VCC_ENET
VCC_GPIO
VCC_LED
TP118
TP119
TP120
TP121
C103 0.22uF 10V 15%
C102 0.22uF 10V 15%
C101 0.22uF 10V 15%
C104 0.22uF 10V 15%
GND

FERRITE FB6 220ohms
FERRITE FB7 220ohms
FERRITE FB8 220ohms
VCC_NAND
VCC_SD1
VCC_UART
TP122
TP123
TP124
C106 0.22uF 10V 15%
C105 0.22uF 10V 15%
C107 0.22uF 10V 15%
GND

V5P0
C4 1uF 16V 10%
C5 1uF 16V 10%
GND

U1 pin		U1 pin	
H9	VDD_SOC_H9	G8	VDD_SOC_CAP_G8
H10	VDD_SOC_H10	H8	VDD_SOC_CAP_H8
J9	VDD_SOC_J9	J8	VDD_SOC_CAP_J8
J10	VDD_SOC_J10	J11	VDD_SOC_CAP_J11
K9	VDD_SOC_K9	K8	VDD_SOC_CAP_K8
K10	VDD_SOC_K10	K11	VDD_SOC_CAP_K11
		L8	VDD_SOC_CAP_L8
		L9	VDD_SOC_CAP_L9
		L10	VDD_SOC_CAP_L10
		L11	VDD_SOC_CAP_L11
G6	VCC_DRAM_G6	R12	VDD_USB_CAP
H6	VCC_DRAM_H6		
J6	VCC_DRAM_J6	N6	VCC_DRAM_2P5
K6	VCC_DRAM_K6	R14	VDD_HIGH_CAP_R14
L6	VCC_DRAM_L6	R15	VDD_HIGH_CAP_R15
M6	VCC_DRAM_M6	N12	VDD_SNVS_CAP_N12
P4	DRAM_VREF	G9	VDD_ARM_CAP_G9
N13	VDD_HIGH	G10	VDD_ARM_CAP_G10
P12	VDD_SNVS	G11	VDD_ARM_CAP_G11
P13	VCC_PLL	H11	VDD_ARM_CAP_H11
F4	VCC_CSI	R13	GPANIO
F13	VCC_ENET	M12	NGND_KEL0
J13	VCC_GPIO		
E13	VCC_LCD		
E7	VCC_NAND		
C4	VCC_SD1		
H13	VCC_UART		
L13	VDDA_ADC_3P3		
M13	ADC_VREFH		
T12	VUSB0		
U12	VUSB1		

TP113 VDD_SOC_CAP
C111 22uF 16V 20%
C96 0.22uF 10V 15%
C95 0.22uF 10V 15%
C97 0.22uF 10V 15%

TP114 VDD_USB_CAP
C18 10uF 25V 10%
C51 0.1uF 16V 10%

TP115 VDD_HIGH_CAP
C94 0.22uF 10V 15%
C14 10uF 25V 10%
C93 0.22uF 10V 15%

TP116
TP117 VDD_ARM_CAP
C110 22uF 16V 20%
C92 0.22uF 10V 15%
C91 0.22uF 10V 15%
GND

PROCESSOR

U5
W632GU6MB-12I
214643818C

V1P35
C108 22uF 16V 20%
C72 0.22uF 10V 15%
C73 0.22uF 10V 15%
C74 0.22uF 10V 15%
C82 0.22uF 10V 15%
C77 0.22uF 10V 15%
C75 0.22uF 10V 15%
C76 0.22uF 10V 15%
C78 0.22uF 10V 15%
C79 0.22uF 10V 15%
C80 0.22uF 10V 15%
C81 0.22uF 10V 15%
GND

C70 4.7uF 25V 20%
R124 1.5Kohms 1%
R125 1.5Kohms 1%
C45 0.1uF 16V 10%
C46 0.1uF 16V 10%
GND

VREFDDR
Please keep these three components as physically close to pin H1 on the DDR as practical.

U5 pin		U5 pin	
N1	VDD_N1	E1	VSS_E1
R1	VDD_R1	M1	VSS_M1
B2	VDD_B2	P1	VSS_P1
K2	VDD_K2	T1	VSS_T1
G7	VDD_G7	J2	VSS_J2
K8	VDD_K8	B3	VSS_B3
D9	VDD_D9	G8	VSS_G8
N9	VDD_N9	J8	VSS_J8
R9	VDD_R9	A9	VSS_A9
		M9	VSS_M9
		P9	VSS_P9
		T9	VSS_T9
A1	VDDQ_A1	B1	VSSQ_B1
C1	VDDQ_C1	D1	VSSQ_D1
F1	VDDQ_F1	G1	VSSQ_G1
D2	VDDQ_D2	E2	VSSQ_E2
H2	VDDQ_H2	D8	VSSQ_D8
E9	VDDQ_E9	E8	VSSQ_E8
A8	VDDQ_A8	F9	VSSQ_F9
C9	VDDQ_C9	B9	VSSQ_B9
H9	VDDQ_H9	G9	VSSQ_G9
M8	VREFCA		
H1	VREFDQ		
J1	NC_J1		
L1	NC_L1		
M7	NC_M7		
L8	ZQ		
J9	NC_J9		
L9	NC_L9		

TP125
R95 240ohms 1%
GND

DDR3

V3P3
C68 4.7uF 25V 20%
C44 0.1uF 16V 10%
C43 0.1uF 16V 10%
C67 4.7uF 25V 20%
C40 0.1uF 16V 10%
C39 0.1uF 16V 10%
C41 0.1uF 16V 10%
C38 0.1uF 16V 10%
C37 0.1uF 16V 10%
C42 0.1uF 16V 10%
VDDIM
C1 1uF 16V 10%
C36 0.1uF 16V 10%
GND

U4
MTFC4GACAJCN-4M IT
214644642C

U4 pin		U4 pin	
E6	VCC_E6	E7	VSS_E7
F5	VCC_F5	G5	VSS_G5
J10	VCC_J10	H10	VSS_H10
K9	VCC_K9	K8	VSS_K8
C6	VCCQ_C6	C4	VSSQ_C4
M4	VCCQ_M4	N2	VSSQ_N2
N4	VCCQ_N4	N5	VSSQ_N5
P3	VCCQ_P3	P4	VSSQ_P4
P5	VCCQ_P5	P6	VSSQ_P6
C2	VDDIM		

GND

eMMC FLASH DEVICE

Note:
Micron Documentation: VDDIM is an internal voltage node. Do not tie to Voltage or Ground. (7/6/16 tr)

VCC_PLL
C100 0.22uF 15% 10V
C17 10uF 10% 25V
GND

Note:
According to NXP Documentation, NVCC_PLL is an OUTPUT to capacitors, it is internally regulated and distributed in the uP IC. (7/6/16 tr)

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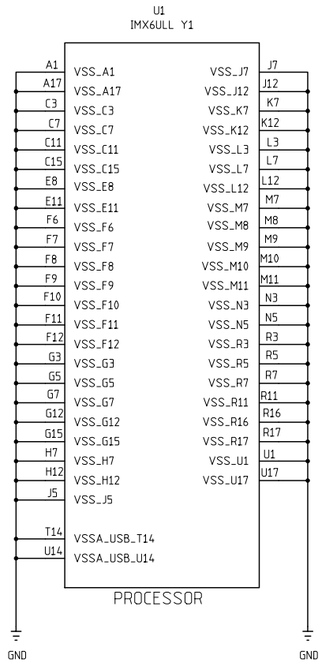
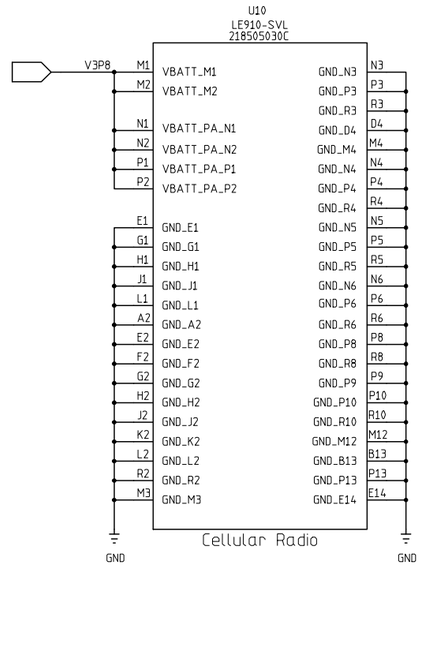
TITLE
Alliance Control PCB
Power Blocks

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1 | VOLUME: (CUBIC MM) | SHEET 14 OF 16

REVISIONS			
REV	ECN	DATE	CHECKED





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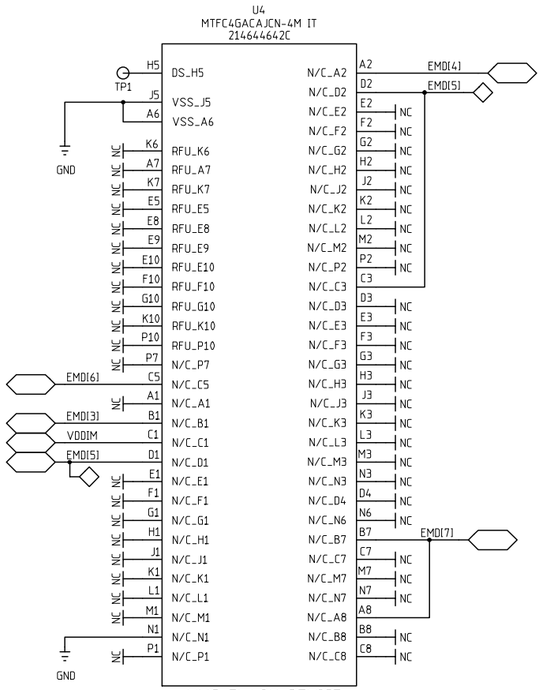
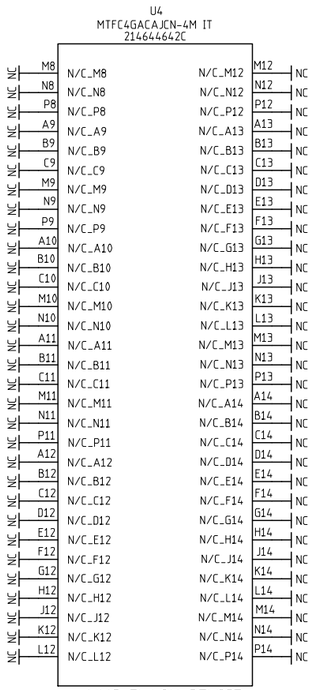
TITLE: Alliance Control PCB
Ground Blocks

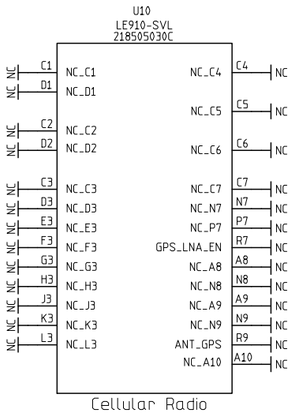
SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

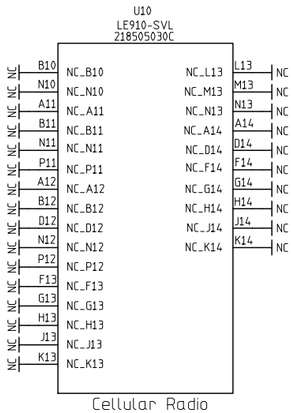
SCALE: 1/1 | VOLUME: (CUBIC MM) | SHEET 15 OF 16

REVISIONS			
REV	ECN	DATE	CHECKED









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TITLE: Alliance Control PCB
No Connect Devices

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300008362C	G1

SCALE: 1/1	VOLUME: (CUBIC MM)	SHEET 16 OF 16