7.1 PLL

See Frequency Synthesizer Block Diagram and Schematic

1. Introduction

The Synthesizer is implemented with the following.
Components: PLL IC (IC6)
X-TAL (X2)
Varicap Diode (D24)
Transistor (Q408,Q411,Q603,Q406)
LED Display (LED999)

IC6 is a cmos LSI that includes most of the PLL block.
The VCO with Varicap Diode D24 as part of the oscillator tank circuit.
Q406 is a switching transistor to connect or disconnect the tuning capacitor in the VCO oscillator tank circuit for transmitter or receiver.

2. Reference Frequency

The crystal X2 (10.240 MHz) and other component at pins 1 and 16 of IC6 from an oscillator with an amplifier internal to IC6.
The oscillator output is internally fed to a divide by 4096 to produce a 2.5 KHz square wave which is the reference input to the phase detector.

3. VCO

Q408 is connected as a hartley type oscillator with varicap diode as part of the tank circuit. With appropriate control voltage on D24 the VCO can be made to oscillate over the required rang of 13.4825 MHz to 16.710 MHz.

4. Programmable Divider and its Control

The programmable inputs (7-segment code) are fed to pins 71 to 78 IC2 the programmable inputs consist a 7 segment code to light channel indicator LED (LED999) For CH.1 “B” and “C” of the first LED element of LED999 will light. The programmable input “B” goes low to produce CH.1 devide (RX : N = 6508, TX : N = 5393)
For each channel number input, an internal code converter ROM provides the appropriate binary control to the programmable divider for channel, since the binary number required is difference during transmit and receive, an additional bit is required at pin 27 of IC2 to allow the ROM to recognize the TX/RX status.
The programmable divider output is fed to the phase detector for comparison with the 2.5 KHz reference.

5. Phase Detector and VCO Control

The phase detector is a digital phase comparator which compares the leading edges of the reference with programmable divider output square waves and develops a series of pulses whose DC level depends on whether the phase error is leading or lagging. The phase detector pulse output is fed to a charge pump and then to base of Q412. The charge pump output is fed to an active low pass filter which consist of R79,C5 and the C53. The low pass filter output at pin 14 of IC6 is further filtered and fed to varicap D24 to control the VCO frequency.
The result is a second order PLL with the loop dynamics essentially controlled by the active low pass filter.

6. Transmit / Receive, Buffer AMP.

The VCO output is fed into buffer AMP Q411 from secondary of L502

7. Transmit Doubler

The Q411 output obtained as base output and fed to the base of double transistor Q41
At this stage, the frequency is doubled. The Q41 output tank circuit is double tuning circuitries (27 MHz) L10 and L11 to stop the 13.5 MHz, frequency.

8. Switching of Tuning Capacitor in VCO Oscillator Tank Circuit

The VCO circuit must tune with a wide rang of frequencies 13.4825 MHz ~ 13.7025 MHz for transmitter and 16.27 MHz ~ 16.710 MHz for receiver.
The use for one tuning capacitor in common has such adverse effects and a decreases in the tuning circuit and the occurrence of may spuriouses. To eliminate these effect, the tuning capacitance is switched for transmission or reception.
The tank circuit consist of the primary of L501, C416 and C413 when receiving, Q406becomes off so, the primary of L501 and make tuning function. When transmiting, Q406 becomes on. So, the primary of L501 and the parallel capacitance of C413 and C421 make turning function.

9. Receiver Local Oscillator Outputs

First Mixer :

The secondary output of VCO tank circuit L501 is injected through buffer AMP Q411and the buffer CKT output through the dain of 1st mixer.

Second Mixer :

The oscillation output, oscillated with 10.240 MHz crystal X-1 across pins 1,16 of IC6, is output from pin 16 and injected into the C124.

10. Frequency Stability

LET : FO = Crystal Oscillator Frequency
FR = Phase Detector Reference Frequency
FVCO = VCO Frequency
FT = Transmit Frequency

THEN = FR = FO/4096
And under locked conditions :
FR = FVCO / N Where N is the programmable divider divide ratio
THEN : FVCO = N X FR = N (FO / 4096)

From which it can be seen that the percentage error in FT is the same as the percentage error in FO.
The stability of the crystal oscillator is determined primarily by the crystal and to a lesser extent by the active and passive components of the oscillator. The choice of crystal and components is such that the required frequency stability is maintained over the required voltage and temperature rang.

7.2. Transmitter

1. RF Amplification

The output of double AMP Q41 is fed through double tuning (27 MHz) L10 and L11 to the base of PRE AMP. The output is then supplied through tuning circuit C77 to RF driver AMP Q301 output is capacitance divided by matching circuit and passed through the base Q302 and passed through power amplifier the base Q303 output is supplied to the antenna through L-C tuning circuit.

2. Circuit For Suppression Of Spurious Radiation

The tuning circuit between frequency synthesizer and final AMP Q303 and 3-stage “PI” network L305,C706,C324,L306,C327,L307 in the Q303 output circuit sever to suppress spurious radiation. This network serves to impedance match Q303 to the antenna and to reduce spurious content to acceptable levels. In the frequency synthesizer.

3. Circuits For Limiting Power

During factory alignment, the series base resistor RV102 is selected to limit the available power to sightly more than 4 watts. The tuning is adjusted so that the actual power is from 3.6 to 4.4 watts, there are no other controls for adjusting power.

4. Modulation

The MIC input is fed to C.R. and then audio power IC1 which feeds modulation transformer T202. The audio output at the secondary of T202 is fed in series with the B+ voltage the diode D12 to the collectors of driver Q302 and final Q303 to collector modulate both these stages.

5. Circuits For Limiting Modulation

A portion of the modulating voltage is rectified by D12which turns on Q14 which attenuates the MIC input to MIC AMP IC1 the resulting feedback loop-keeps the modulation from exceeding 100% inputs approximately 40 dB greater than that required to produce 50% modulation. The attack time is about 50 ms and the release time is about 300 ms

6. AWI
Carrie is send pass D402 for referent and send to ant. IF ant not matching carrie will send back to D401 and compare with referent at Q304 and turn on D306.

7.3. Receiver

The receiver is a double conversion super heterodyne with the first IF at 10.695 MHz and the second IF at 455 kHz. The synthesizer supplies the first local oscillator 10.695 MHz below the received frequency and the second local oscillator at 10.240 MHz. The detector output provides reverse AGC to all previous stages except. Squelch is controlled by Q12.

- In the receiver model of operation, Q18 transistor is turned off. Also bias voltage is applies Q23 and a proper bias and AGC voltage is established to Q1,4, and 5.

- Q1 is a 27 MHz input amplifier, and any excessive input signal is limited by diodes D101,D102 The amplified 27 MHz is mixed with VCO frequency selected by channel switch.
  For CH.1 VCO is set at 16.27 MHz. The resulting first IF is 26.965-16.27=10.695 MHz

- Q4,5 is the first converter, and the 10.695 MHz is sharply filtered by L104 and a ceramic filter CF101 The first IF is again mixed with a second local oscillator of 10.24 MHz. 10.695-10.24 = 0.455 MHz.

- L4 is the second converter. Second IF is filtered by a razor sharp ceramic filter of CF201.

- Audio output frompin13 of IC 3 pass pre amplifier at base of Q9 then though a volume control VR102 and finally amplified by audio amplifier IC1.

- SQ is controled by Q12