Figure 23: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as follows. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but please pay attention to the direction of connection.

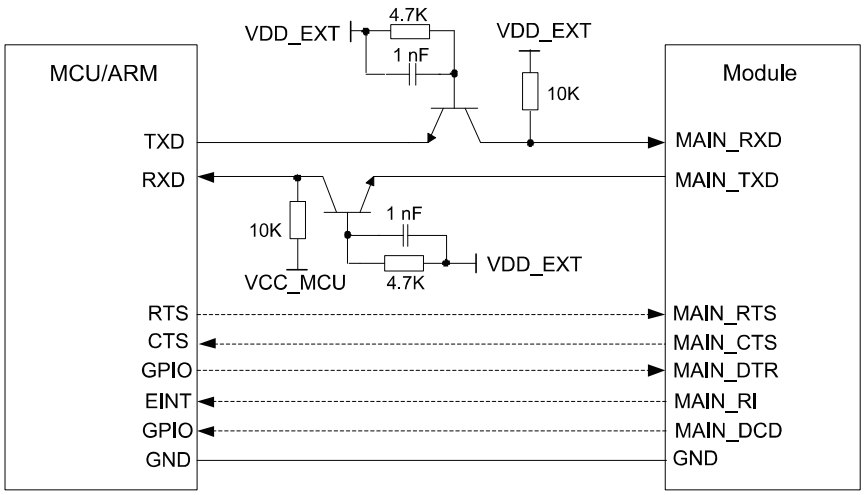


Figure 24: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

4.7. ADC Interface

The module provides two analog-to-digital converter (ADC) interfaces. You can use **AT+QADC=0** to read the voltage value on ADC0 pin, **AT+QADC=1** to read the voltage value on ADC1, See ***document [2]*** for more details.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 17: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	A 1 kΩ series resistor is required for use. If unused, keep it open.
ADC1	2	AI		

Table 21: Characteristics of ADC Interface

Name	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.1	-	VBAT	V
ADC1 Voltage Range	0.1	-	VBAT	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.
4. If input voltage of ADC interface is designed with a resistor divider circuit, the resistance value of the external divider resistor must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be reduced significantly.

4.8. SPI Interface

The module provides one SPI interface that only supports master mode. It has a working voltage of 1.8 V and a maximum clock frequency of 25 MHz.

Table 22: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	Just master mode only. 1.8 V power domain. If unused, keep it open.
SPI_CS	25	DO	SPI chip select	
SPI_DIN	88	DI	SPI master mode input	
SPI_DOUT	64	DO	SPI master mode output	

NOTE

When the universal 4-wire SPI interface is connected to NOR Flash, it supports basic Flash reading, writing, erasing and other operations, but you need to perform wear leveling. It does not support file system and can only be used for storage purpose.

4.9. PSM Interface*

The module supports power saving mode (PSM). It enters the PSM mode through the following AT commands when working normally.

- **AT+CFUN=4:** Enter airplane mode.
- **AT+QSCLK=3:** Enable PSM.
- **AT+CFUN=1:** Exit airplane mode.

Pulling the PSM_EINT pin up externally or setting the timer in software will enable the module to exit PSM.

Table 18: Pin Definition of PSM Interface

Pin Name	Pin No.	I/O	Description	Comment
PSM_IND	1	DO	Indicate the module's power saving mode	VRTC power domain
PSM_EINT	96	DI	External interrupt pin; Wake up the module from PSM.	VRTC power domain

A reference circuit is shown in the following figure.

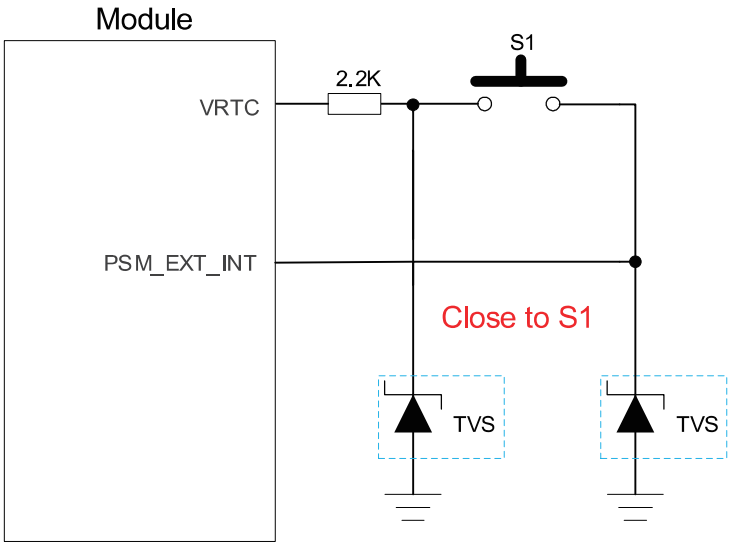


Figure 25: Reference Circuit of Wake up Module from PSM

4.10. Indication Signal

Table 19: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.
AP_READY	19	DI	Application processor ready	
NET_STATUS	21	DO	Indicate the module's network activity status	

4.10.1. Network Status Indication

The network indication pins NET_STATUS can drive the network status indicators. The following tables describe pin definition and logic level changes in different network status.

Table 20: Working State of Network Connection Status/Activity Indication

Pin Name	Status	Network Status
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Idle
	Flicker rapidly (63 ms low /62 ms high)	Data transfer is ongoing
	Always high	Voice calling

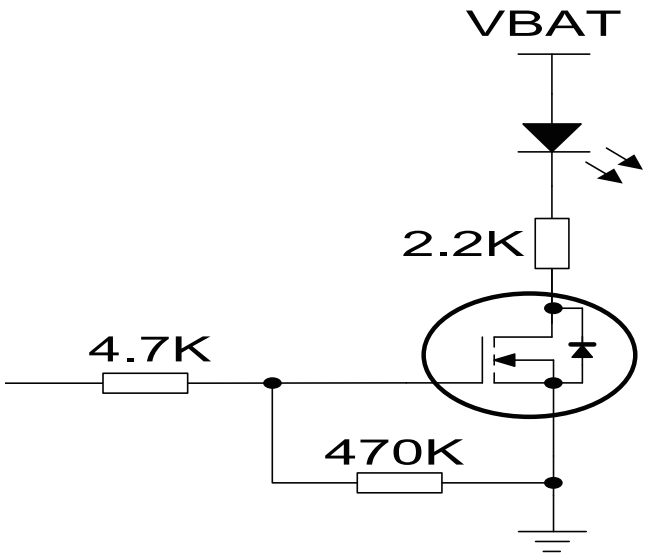


Figure 26: Reference Circuit of Network Status Indication

4.10.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It will output high level when module is powered ON successfully.

Table 21: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment

A reference circuit is shown as below.

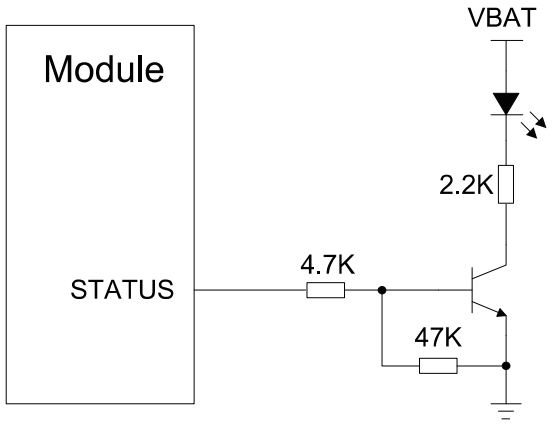


Figure 27: Reference Circuits of STATUS

NOTE

4.10.3. MAIN_RI

AT+QCFG= "risignaltype", "physical" command can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG** command. The default port is USB AT port.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 22: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC return.

The MAIN_RI behavior can be changed via **AT+QCFG="urc/ri/ring"***. Please refer to ***document [2]*** for details.

4.11. Control Signal

Table 23: Pin Definition of Control Signal

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	18	DI	Airplane mode control	1.8 V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep this pin open.

The module provides a W_DISABLE# pin to enable or disable airplane mode through hardware operation. W_DISABLE# is pulled up by default, and driving it low will set the module to airplane mode. Its control function for airplane mode is disabled by default and **AT+QCFG= "airplanecontrol", 1** can be used to enable the function.

AT+CFUN=<fun> command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- AT+CFUN=0: Minimum functionality mode (RF functions are disabled).
- AT+CFUN=1: Full functionality mode (by default).
- AT+CFUN=4: RF function is disabled (Airplane mode).

5 Antenna Interfaces

EG915U series module provides a main antenna interface, a Bluetooth/Wi-Fi Scan antenna interface. The impedance of antenna ports is 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

Table 24: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_BT/WIFI_SCAN	56	AIO	The shared interface for Bluetooth and Wi-Fi Scan	Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan can only receive but not transmit. 50 Ω impedance. If unused, keep it open.

NOTE

Only passive antennas are supported.

5.1.2. Operating Frequency

Table 25: Operating Frequency of EG915U-CN

Operating Frequency	Transmit (MHz)	Receive (MHz)

EGSM900	880-915	925-960
DCS1800	1710-1785	1805-1880
LTE-B1	1920-1980	2110-2170
LTE-B3	1710-1785	1805-1880
LTE-B5	824-849	869-894
LTE-B8	880-915	925-960
LTE-B34	2010-2025	2010-2025
LTE-B38	2570-2620	2570-2620
LTE-B39	1880-1920	1880-1920
LTE-B40	2300-2400	2300-2400
LTE-B41	2535-2675	2535-2675

Table 26: Operating Frequency of EG915U-EU

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824-849	869-894
PCS1900	1850-1910	1930-1990
EGSM900	880-915	925-960
DCS1800	1710-1785	1805-1880
LTE-B1	1920-1980	2110-2170
LTE-B3	1710-1785	1805-1880
LTE-B5	824-849	869-894
LTE-B7	2500-2570	2620-2690
LTE-B8	880-915	925-960
LTE-B20	832-862	791-821
LTE-B28	703-748	758-803

Table 27: Operating Frequency of EG915U-LA

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824-849	869-894
PCS1900	1850-1910	1930-1990
EGSM900	880-915	925-960
DCS1800	1710-1785	1805-1880
LTE-B2	1850-1910	1930-1990
LTE-B3	1710-1785	1805-1880
LTE-B4	1710-1755	2110-2155
LTE-B5	824-849	869-894
LTE-B7	2500-2570	2620-2690
LTE-B8	880-915	925-960
LTE-B28	703-748	758-803
LTE-B66	1710-1780	2110-2200

NOTE

Only EG915U-CN supports LTE-TDD.

5.1.3. Reference Design of Antenna Interface

A reference design of ANT_MAIN pin and ANT_BT/WIFI_SACN pin are shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

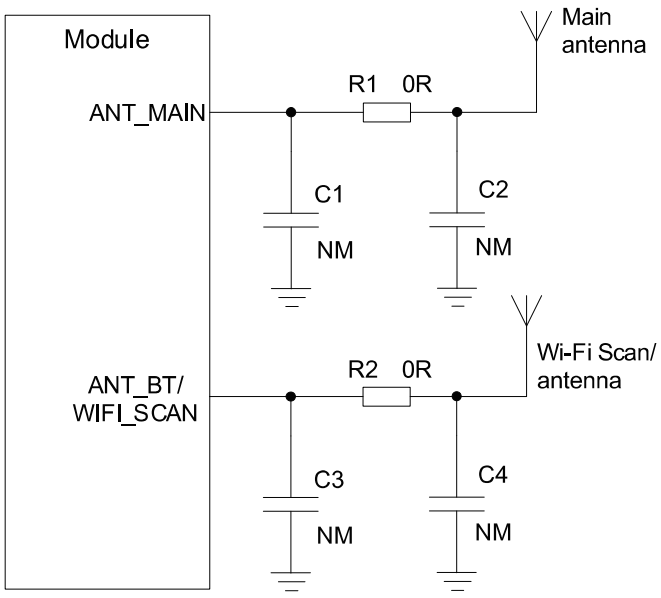


Figure 28: Reference Circuit of RF Antenna

5.1.4. Operating Frequency

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between the RF traces and the ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

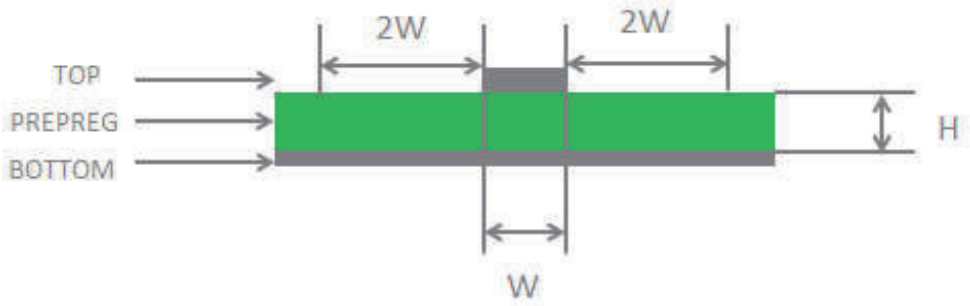


Figure 29: Microstrip Design on a 2-layer PCB

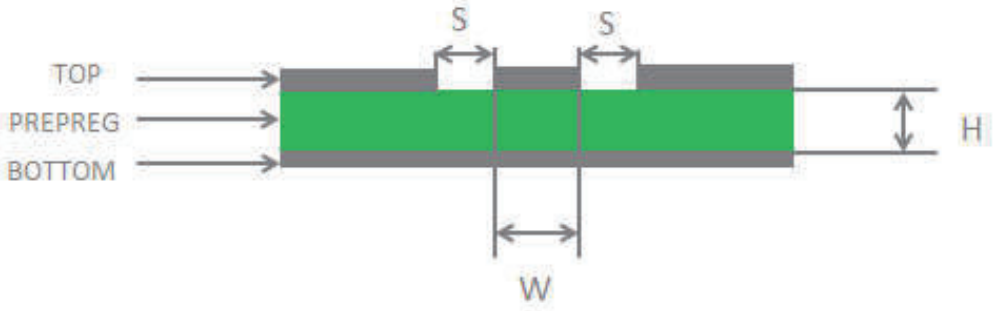


Figure 30: Coplanar Waveguide Design on a 2-layer PCB

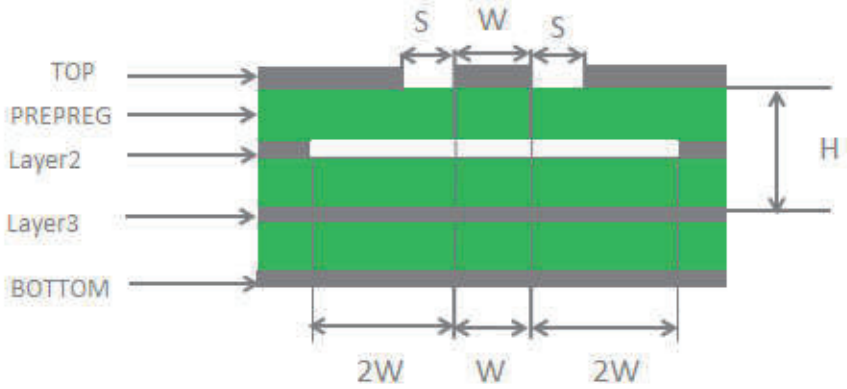


Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

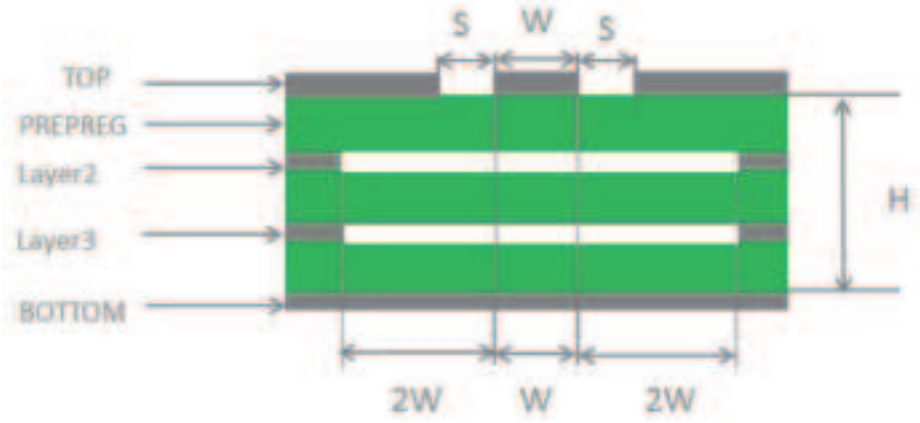


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.2. Antenna Installation

5.2.1. Antenna Design Requirement

Table 28: Requirements for Antenna Design

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < **1 dB**: LB（< 1 GHz） < **1.5 dB**: MB（1–2.3 GHz） < **2 dB**: HB（> 2.3 GHz）

5.2.2. RF Connector Recommendtion

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by *Hirose*.

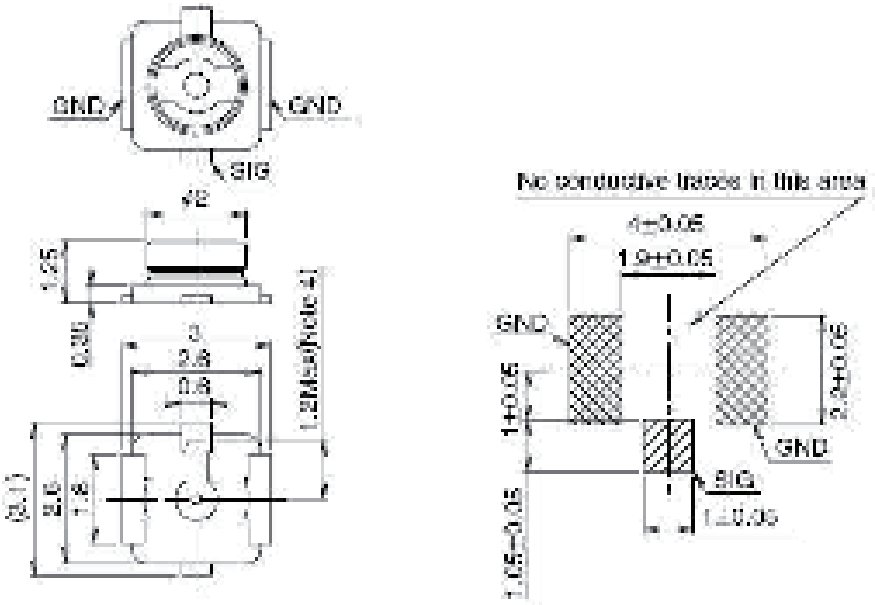


Figure 33: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

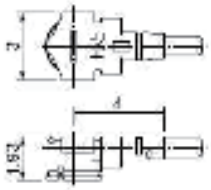
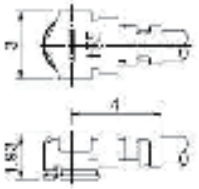
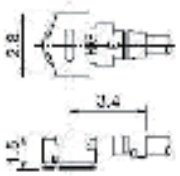
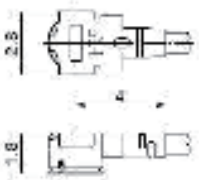
	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.6	45.5	71.7
RoHS	YES				

Figure 34: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

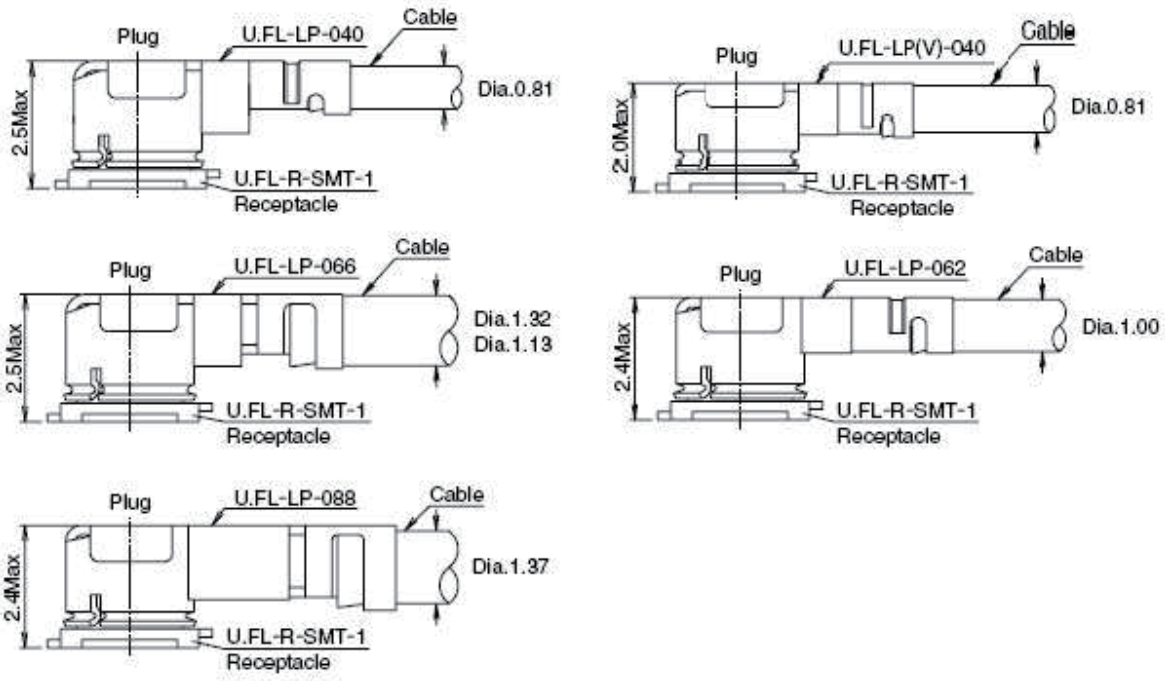


Figure 35: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 32: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	1.0	A
Peak Current of VBAT_RF	0	2.5	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT	V
Voltage at ADC1	0	VBAT	V

6.2. Power Supply Ratings

Table 29: The Module's Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM 900	-	-	400	mV

	Voltage drop during peak data rate	-	-	-	-	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM 900	-	1.7	2.5	A
USB_VBUS	USB connection detection	-	3.5	5.0	5.25	V

6.3. Operation and Storage Temperatures

Table 30: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [6]	-35	+25	+75	℃
Extended Operation Range [7]	-40	+25	+85	℃
Storage Temperature Range	-40	+25	+90	℃

6.4. Power Consumption

Table 31: EG915U-CN Current Consumption

EG915U-CN			
Description	**Conditions**	**Typ.**	**Unit**
OFF state	Power down	32	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.0	mA
	AT+CFUN=0 (USB connected)	2.2	mA
	AT+CFUN=4 (USB disconnected)	1.0	mA

[6] Within operating temperature range, the module is 3GPP compliant.
[7] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

	AT+CFUN=4 (USB connected)	2.3	mA
	EGSM @ DRX = 2 (USB disconnected)	2.0	mA
	EGSM @ DRX = 5 (USB disconnected)	1.5	mA
	EGSM @ DRX = 5 (USB connected)	2.7	mA
	EGSM @ DRX = 9 (USB disconnected)	1.3	mA
	DCS @ DRX = 2 (USB disconnected)	2.0	mA
	DCS @ DRX = 5 (USB disconnected)	1.5	mA
	DCS @ DRX = 5 (USB connected)	2.7	mA
	DCS @ DRX = 9 (USB disconnected)	1.3	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.5	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.8	mA
	LTE-FDD @ PF = 64 (USB connected)	3.0	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.4	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.2	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.5	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.8	mA
	LTE-TDD @ PF = 64 (USB connected)	3.1	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.4	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.2	mA
Idle state	EGSM @ DRX = 5 (USB disconnected)	12.2	mA
	EGSM @ DRX = 5 (USB connected)	28.5	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.5	mA
	LTE-FDD @ PF = 64 (USB connected)	29.0	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.5	mA
	LTE-TDD @ PF = 64 (USB connected)	29.0	mA
LTE data transfer	LTE-FDD B1 @ 22.93 dBm	571	mA

	LTE-FDD B3 @ 22.86 dBm	583	mA
	LTE-FDD B5 @ 23.51 dBm	527	mA
	LTE-FDD B8 @ 22.79 dBm	568	mA
	LTE-FDD B34 @ 23.32 dBm	268	mA
	LTE-FDD B38 @ 23.29 dBm	300	mA
	LTE-FDD B39 @ 23.15 dBm	241	mA
	LTE-FDD B40 @ 22.97 dBm	284	mA
	LTE-FDD B41 @ 23.06 dBm	296	mA
GPRS data transfer	GSM900 4DL/1UL @ 32.86 dBm	226	mA
	GSM900 3DL/2UL @ 30.86 dBm	343	mA
	GSM900 2DL/3UL @ 28.81 dBm	392	mA
	GSM900 1DL/4UL @ 26.63 dBm	405	mA
	DCS1800 4DL/1UL @ 30.13 dBm	160	mA
	DCS1800 3DL/2UL @ 28.12 dBm	221	mA
	DCS1800 2DL/3UL @ 26.01 dBm	249	mA
	DCS1800 1DL/4UL @ 23.94 dBm	258	mA
GSM voice call	GSM900 PCL=5 @ 32.83 dBm	245	mA
	GSM900 PCL=12 @ 18.94 dBm	90	mA
	GSM900 PCL=19 @ 6.18 dBm	63	mA
	DCS1800P CL=0 @ 30.12 dBm	176	mA
	DCS1800P CL=7 @ 15.97 dBm	75	mA
	DCS1800P CL=15 @ 0.28 dBm	57	mA
GSM voice call (Max. Current)	GSM900 PCL=5 @ 32.83 dBm	1.77	A
	GSM900 PCL=12 @ 18.94 dBm	0.44	A
	GSM900 PCL=19 @ 6.18 dBm	0.18	A
	DCS1800P CL=0 @ 30.12 dBm	1.18	A

	DCS1800P CL=7 @ 15.97 dBm	0.3	A
	DCS1800P CL=15 @ 0.28 dBm	0.15	A

Table 32: EG915U-EU Current Consumption

EG915U-EU			
Description	**Conditions**	**Typ.**	**Unit**
OFF state	Power down	43	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.01	mA
	AT+CFUN=0 (USB connected)	2.2	mA
	AT+CFUN=4 (USB disconnected)	1.02	mA
	AT+CFUN=4 (USB connected)	2.21	mA
	EGSM @ DRX = 2 (USB disconnected)	2.09	mA
	EGSM @ DRX = 5 (USB disconnected)	1.55	mA
	EGSM @ DRX = 5 (USB connected)	2.67	mA
	EGSM @ DRX = 9 (USB disconnected)	1.39	mA
	DCS @ DRX = 2 (USB disconnected)	2.1	mA
	DCS @ DRX = 5 (USB disconnected)	1.5	mA
	DCS @ DRX = 5 (USB connected)	2.78	mA
	DCS @ DRX = 9 (USB disconnected)	1.36	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.49	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.22	mA
	LTE-FDD @ PF = 64 (USB connected)	3.48	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.63	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.34	mA
Idle state	EGSM @ DRX = 5 (USB disconnected)	12.05	mA

	EGSM @ DRX = 5 (USB connected)	27.3	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.38	mA
	LTE-FDD @ PF = 64 (USB connected)	27.58	mA
LTE data transfer	LTE-FDD B1 @ 22.29 dBm	638	mA
	LTE-FDD B3 @ 22.88 dBm	617	mA
	LTE-FDD B5 @ 23.01 dBm	637	mA
	LTE-FDD B7 @ 22.95 dBm	793	mA
	LTE-FDD B8 @ 23.17 dBm	696	mA
	LTE-FDD B20 @ 23.05 dBm	516	mA
	LTE-FDD B28 @ 23.06 dBm	559	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.96 dBm	266	mA
	GSM850 3DL/2UL @ 30.7 dBm	394	mA
	GSM850 2DL/3UL @ 28.66 dBm	457	mA
	GSM850 1DL/4UL @ 26.41 dBm	464	mA
	GSM900 4DL/1UL @ 32.31 dBm	245	mA
	GSM900 3DL/2UL @ 30.7 dBm	371	mA
	GSM900 2DL/3UL @ 28.66 dBm	445	mA
	GSM900 1DL/4UL @ 26.63 dBm	452	mA
	DCS1800 4DL/1UL @ 29.84 dBm	171	mA
	DCS1800 3DL/2UL @ 27.89 dBm	242	mA
	DCS1800 2DL/3UL @ 25.85 dBm	269	mA
	DCS1800 1DL/4UL @ 23.78 dBm	279	mA
	PCS1900 4DL/1UL @ 29.68 dBm	171	mA
	PCS1900 3DL/2UL @ 27.74 dBm	247	mA
	PCS1900 2DL/3UL @ 25.66 dBm	279	mA

	PCS1900 1DL/4UL @ 23.59 dBm	295	mA
GSM voice call	GSM850 PCL=5 @ 32.82 dBm	289	mA
	GSM850 PCL=12 @ 19.08 dBm	111	mA
	GSM850 PCL=19 @ 6.12 dBm	80	mA
	GSM900 PCL=5 @ 32.34 dBm	261	mA
	GSM900 PCL=12 @ 19.06 dBm	109	mA
	GSM900 PCL=19 @ 5.39 dBm	79	mA
	DCS1800P CL=0 @ 29.89 dBm	196	mA
	DCS1800P CL=7 @ 15.96 dBm	91	mA
	DCS1800P CL=15 @ 0.95 dBm	75	mA
	PCS1900P CL=0 @ 29.66 dBm	193	mA
	PCS1900P CL=7 @ 15.59 dBm	93	mA
	PCS1900P CL=15 @ 0.58 dBm	75	mA
GSM voice call (Max. Current)	GSM850 PCL=5 @ 32.82 dBm	1.88	A
	GSM850 PCL=12 @ 19.08 dBm	0.46	A
	GSM850 PCL=19 @ 6.12 dBm	0.19	A
	GSM900 PCL=5 @ 32.34 dBm	1.72	A
	GSM900 PCL=12 @ 19.06 dBm	0.44	A
	GSM900 PCL=19 @ 5.39 dBm	0.19	A
	DCS1800P CL=0 @ 29.89 dBm	1.13	A
	DCS1800P CL=7 @ 15.96 dBm	0.30	A
	DCS1800P CL=15 @ 0.95 dBm	0.16	A
	PCS1900P CL=0 @ 29.66 dBm	1.10	A
	PCS1900P CL=7 @ 15.59 dBm	0.33	A
	PCS1900P CL=15 @ 0.58 dBm	0.15	A

Table 33: EG915U-LA Current Consumption

EG915U-LA			
Description	**Conditions**	**Typ.**	**Unit**
OFF state	Power down	40	uA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.98	mA
	AT+CFUN=0 (USB connected)	2.38	mA
	AT+CFUN=4 (USB disconnected)	1.06	mA
	AT+CFUN=4 (USB connected)	2.43	mA
	EGSM @ DRX = 2 (USB disconnected)	2.20	mA
	EGSM @ DRX = 5 (USB disconnected)	1.65	mA
	EGSM @ DRX = 5 (USB connected)	3.07	mA
	EGSM @ DRX = 9 (USB disconnected)	1.47	mA
	DCS @ DRX = 2 (USB disconnected)	2.22	mA
	DCS @ DRX = 5 (USB disconnected)	1.63	mA
	DCS @ DRX = 5 (USB connected)	3.03	mA
	DCS @ DRX = 9 (USB disconnected)	1.48	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.54	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.25	mA
	LTE-FDD @ PF = 64 (USB connected)	3.74	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.61	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.32	mA
Idle state	EGSM @ DRX = 5 (USB disconnected)	13.06	mA
	EGSM @ DRX = 5 (USB connected)	28.73	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.05	mA
	LTE-FDD @ PF = 64 (USB connected)	28.61	mA
LTE data transfer	LTE-FDD B2 @ 22.63d Bm	694	mA

	LTE-FDD B3 @ 22.88 dBm	667	mA
	LTE-FDD B4 @ 22.94d Bm	718	mA
	LTE-FDD B5 @ 23.01 dBm	622	mA
	LTE-FDD B7 @ 22.95 dBm	797	mA
	LTE-FDD B8 @ 23.17 dBm	644	mA
	LTE-FDD B28 @ 23.06 dBm	627	mA
	LTE-FDD B66 @ 22.81d Bm	725	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.96 dBm	269	mA
	GSM850 3DL/2UL @ 30.7 dBm	394	mA
	GSM850 2DL/3UL @ 28.66 dBm	463	mA
	GSM850 1DL/4UL @ 26.41 dBm	473	mA
	GSM900 4DL/1UL @ 32.31 dBm	257	mA
	GSM900 3DL/2UL @ 30.7 dBm	372	mA
	GSM900 2DL/3UL @ 28.66 dBm	456	mA
	GSM900 1DL/4UL @ 26.63 dBm	452	mA
	DCS1800 4DL/1UL @ 29.84 dBm	174	mA
	DCS1800 3DL/2UL @ 27.89 dBm	244	mA
	DCS1800 2DL/3UL @ 25.85 dBm	270	mA
	DCS1800 1DL/4UL @ 23.78 dBm	280	mA
	PCS1900 4DL/1UL @ 29.68 dBm	179	mA
	PCS1900 3DL/2UL @ 27.74 dBm	250	mA
	PCS1900 2DL/3UL @ 25.66 dBm	289	mA
	PCS1900 1DL/4UL @ 23.59 dBm	295	mA
GSM voice call	GSM850 PCL=5 @ 32.82 dBm	288	mA
	GSM850 PCL=12 @ 19.08 dBm	113	mA
	GSM850 PCL=19 @ 6.12 dBm	80	mA

	GSM900 PCL=5 @ 32.34 dBm	261	mA
	GSM900 PCL=12 @ 19.06 dBm	112	mA
	GSM900 PCL=19 @ 5.39 dBm	79	mA
	DCS1800P CL=0 @ 29.89 dBm	187	mA
	DCS1800P CL=7 @ 15.96 dBm	91	mA
	DCS1800P CL=15 @ 0.95 dBm	72	mA
	PCS1900P CL=0 @ 29.66 dBm	196	mA
	PCS1900P CL=7 @ 15.59 dBm	94	mA
	PCS1900P CL=15 @ 0.58 dBm	72	mA

6.5. Tx Power

Table 34: EG915U-CN RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD	23 dBm ±2 dB	< -39 dBm
LTE-TDD	23 dBm ±2 dB	< -39 dBm

Table 35: EG915U-EU RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm

Table 36: EG915U-LA RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

6.6. Rx Sensitivity

Table 37: EG915U-CN Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	Primary+ Diversity
EGSM900	-108.0	-102 dBm
DCS1800	-107.5	-102 dBm
LTE-FDD B1 (10 MHz)	-97.3	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99	-93.3 dBm
LTE-TDD B34 (10 MHz)	-98	-96.3 dBm
LTE-TDD B38 (10 MHz)	-97.6	-96.3 dBm
LTE-TDD B39 (10 MHz)	-98.4	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98.3	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97	-94.3 dBm

Table 38: EG915U-EU Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	Primary+ Diversity
GSM850	-108	-102 dBm
EGSM900	-106.5	-102 dBm
DCS1800	-107.5	-102 dBm
PCS1900	-107	-102 dBm
LTE-FDD B1 (10 MHz)	-97	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.3	-93.3 dBm
LTE-FDD B5 (10 MHz)	-97.4	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.1	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97	-93.3 dBm
LTE-FDD B20 (10 MHz)	-98.3	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.6	-94.8 dBm

Table 39: EG915U-LA Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	Primary+ Diversity
GSM850	-108	-102 dBm
EGSM900	-106.8	-102 dBm
DCS1800	-107.5	-102 dBm
PCS1900	-107.2	-102 dBm
LTE-FDD B2 (10 MHz)	-98.1	-94.3 dBm
LTE-FDD B3 (10 MHz)	-98.2	-93.3 dBm
LTE-FDD B4 (10 MHz)	-97.5	-96.3 dBm

LTE-FDD B5 (10 MHz)	-97.4	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.1	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97.5	-93.3 dBm
LTE-TDD B28 (10 MHz)	-99.4	-93.3 dBm
LTE-TDD B66 (10 MHz)	-97.9	-95.8 dBm

6.7. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective component to the ESD sensitive interfaces and points in the product design of the module.

The following table shows the electrostatics discharge characteristics of the module.

Table 40: Electrostatics Discharge Characteristics (25 ℃, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.2 Mechanical Dimensions

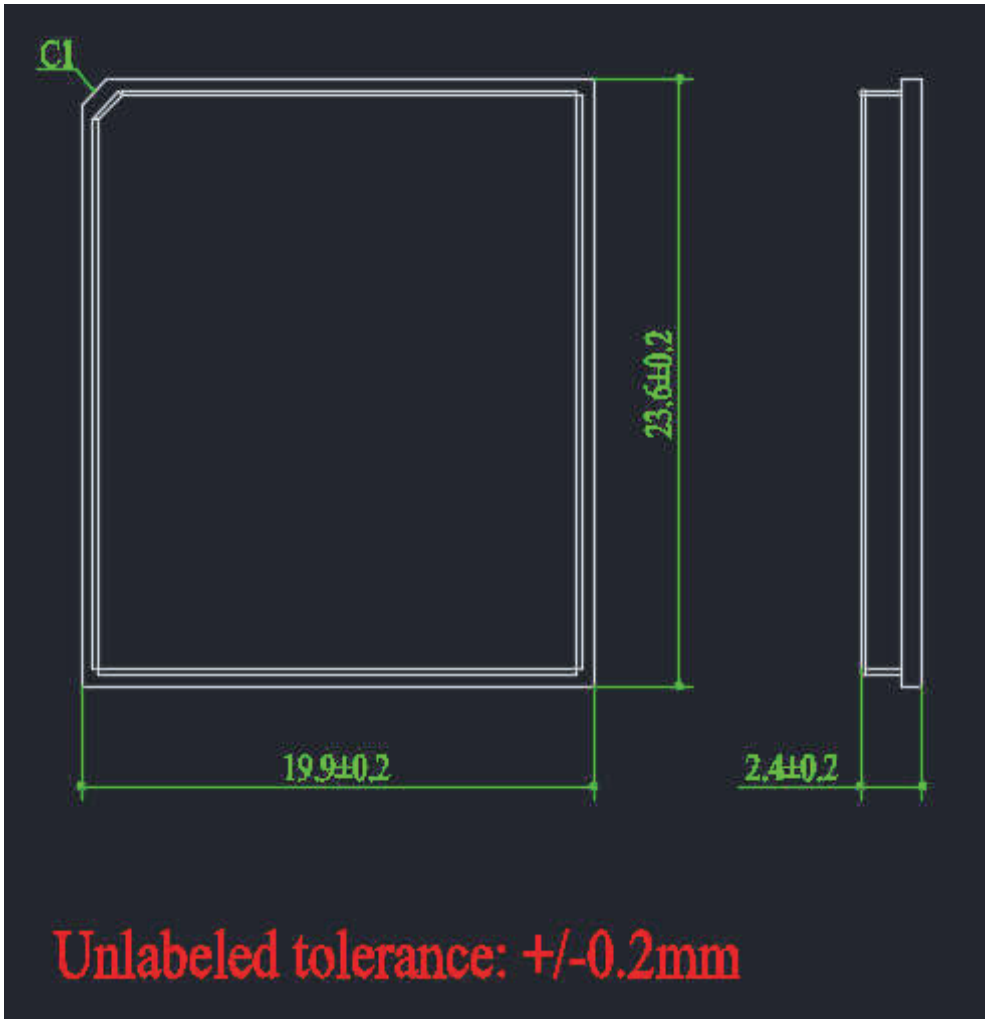


Figure 36: Module Top and Side Dimensions (Unit: mm)

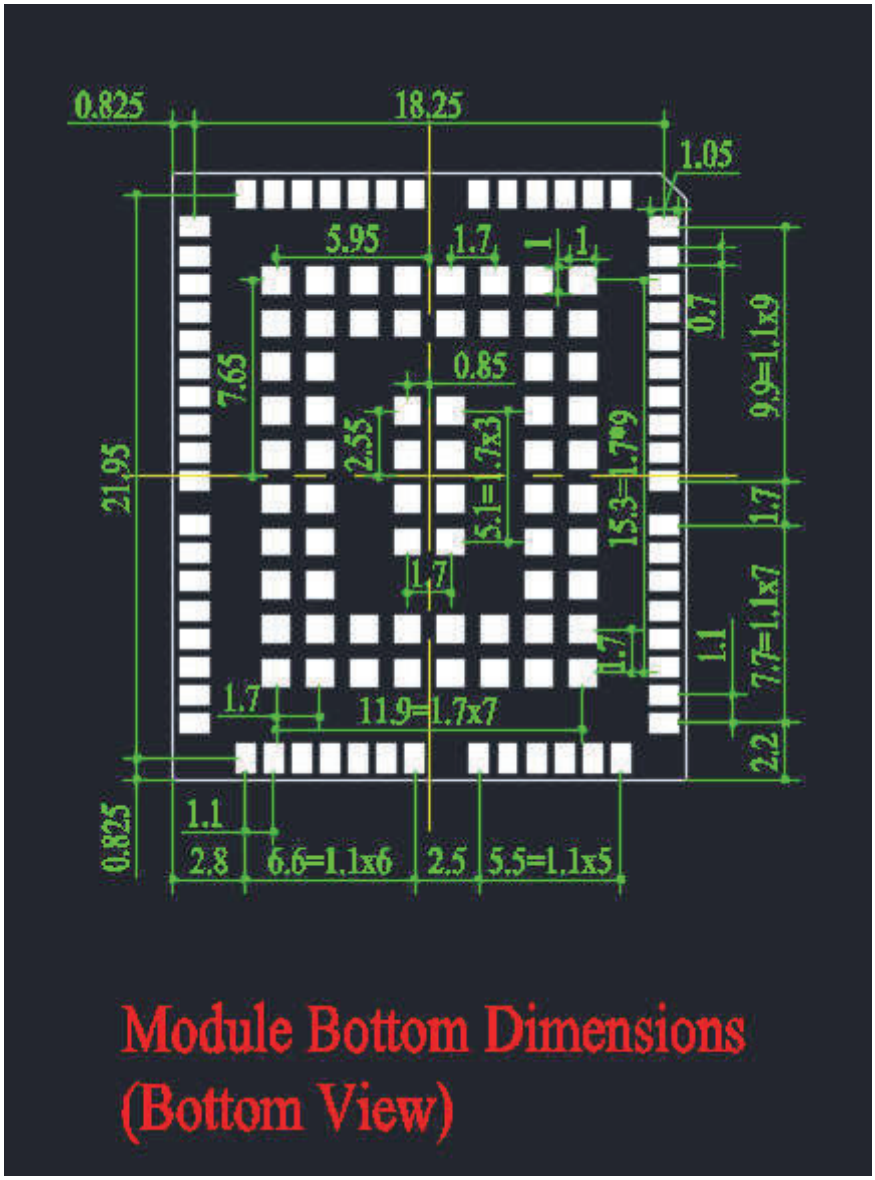


Figure 37: Module Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.3 Recommended Footprint

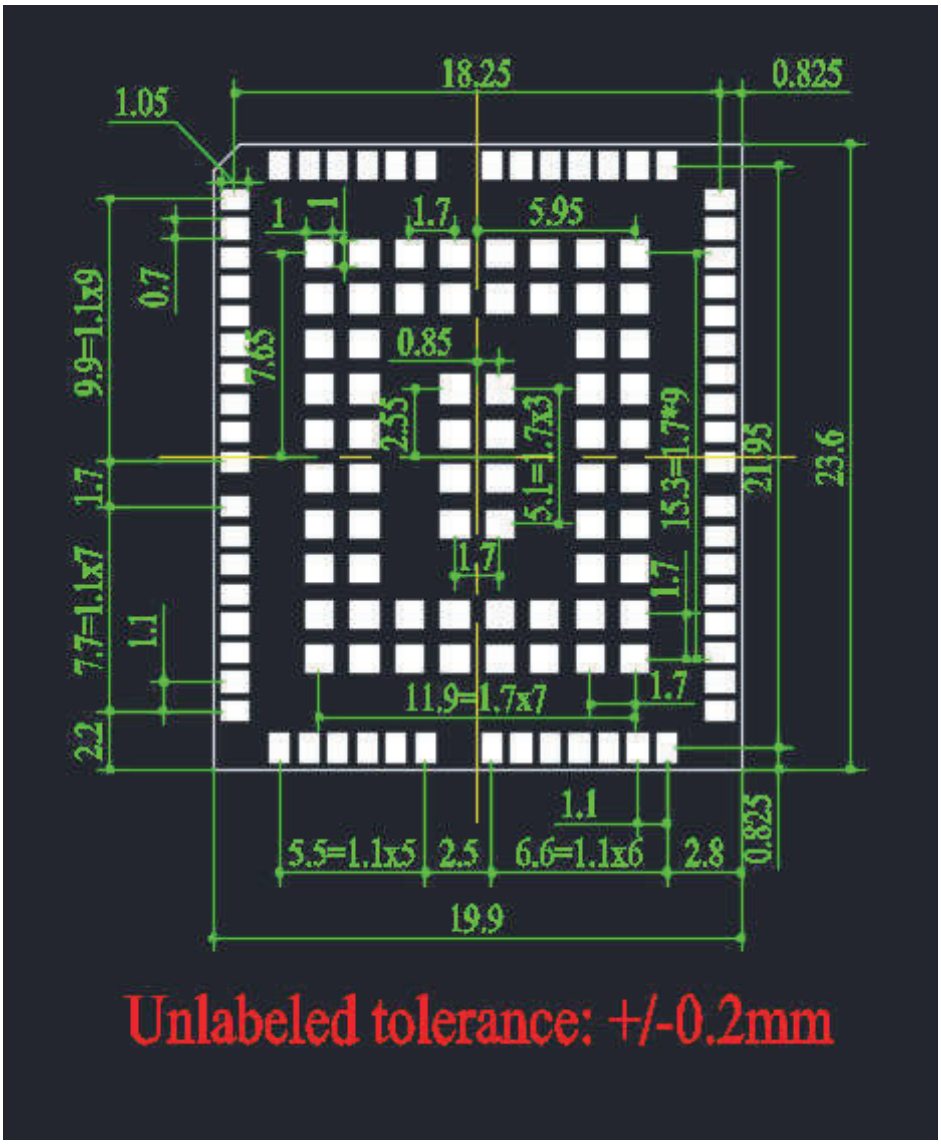


Figure 38: Recommended Footprint (TOP View)

NOTE

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the motherboard.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm

7.3 Top and Bottom Views

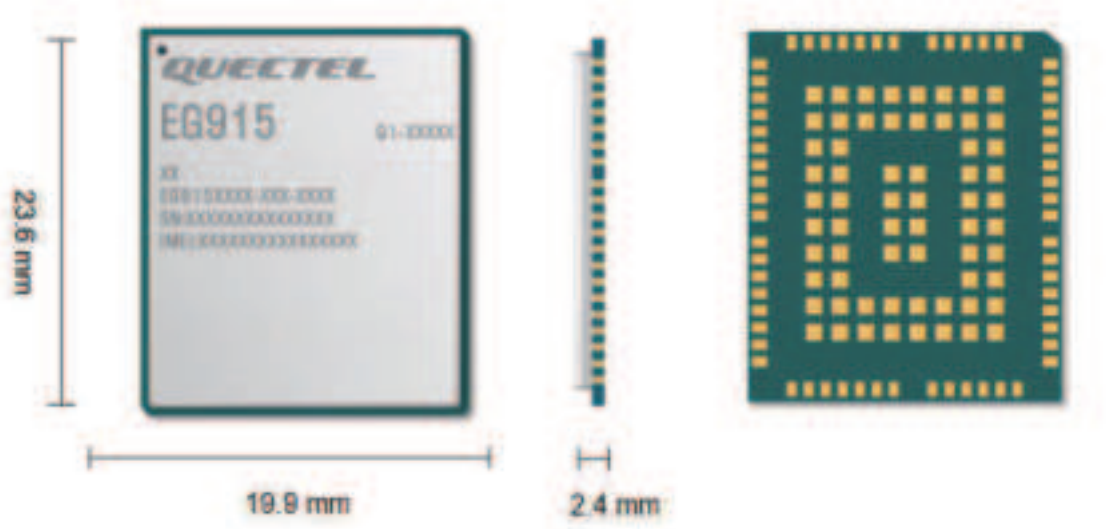


Figure 39: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1 Storage Conditions

Module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 ℃ and the relative humidity should be 35–60%.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 [8] hours in a plant where the temperature is 23 ±5 ℃ and relative humidity is below 60%. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 ℃;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[8] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.
3. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.

8.2

8.2 Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [4]***.

The peak reflow temperature should be 235–246 ℃, with 246 ℃ as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

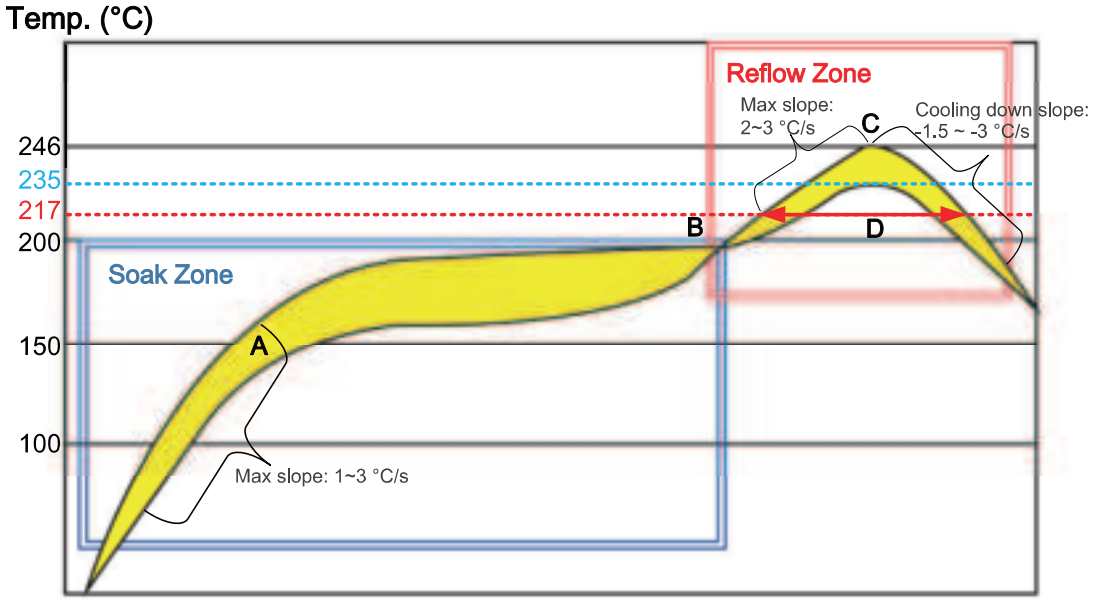


Figure 40: Recommended Reflow Soldering Thermal Profile

Table 41: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 ℃/s
Soak time (between A and B: 150 ℃ and 200 ℃)	70–120 s
Reflow Zone	
Max slope	2–3 ℃/s
Reflow time (D: over 217 ℃)	40–70 s
Max temperature	235–246 ℃
Cooling down slope	-1.5 to -3 ℃/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3 Packaging Specifications

The module is packaged in tape and reel carriers. One reel is 300 mm long and contains 250 modules.

The figures below show the package details, measured in mm.

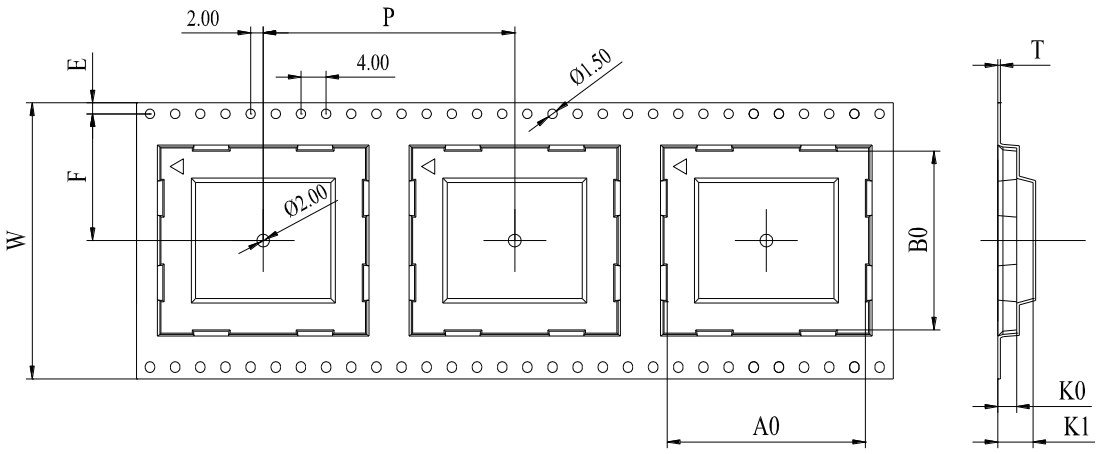


Figure 41: Tape Specifications

Table 39:Tape Size（mm）

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

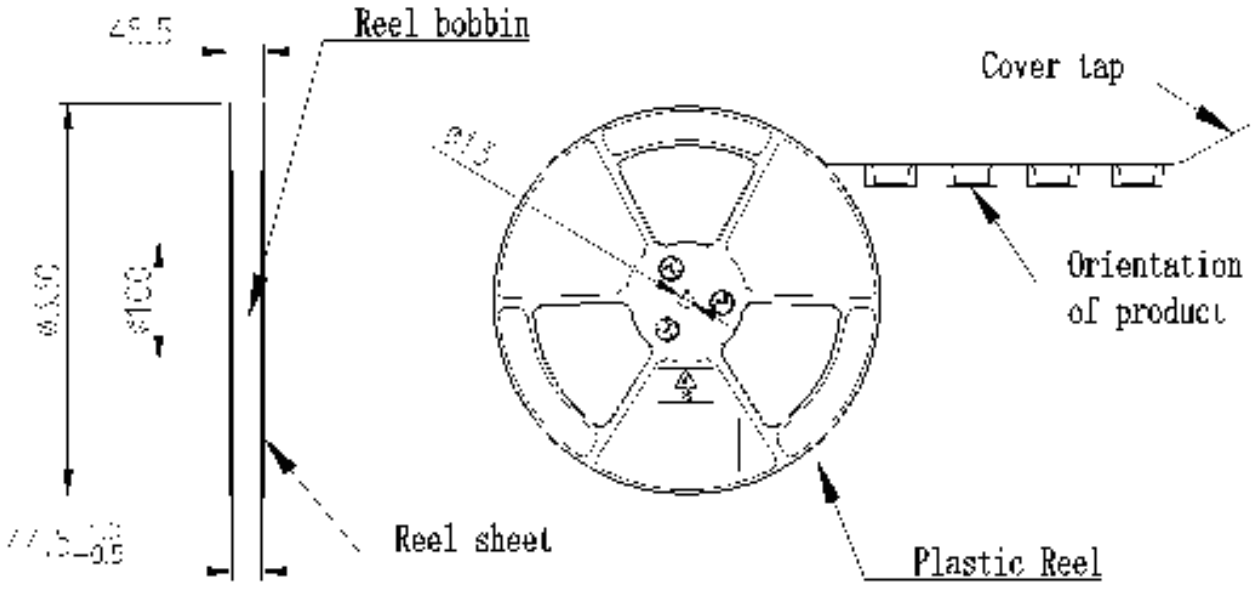


Figure 42: Reel Specifications

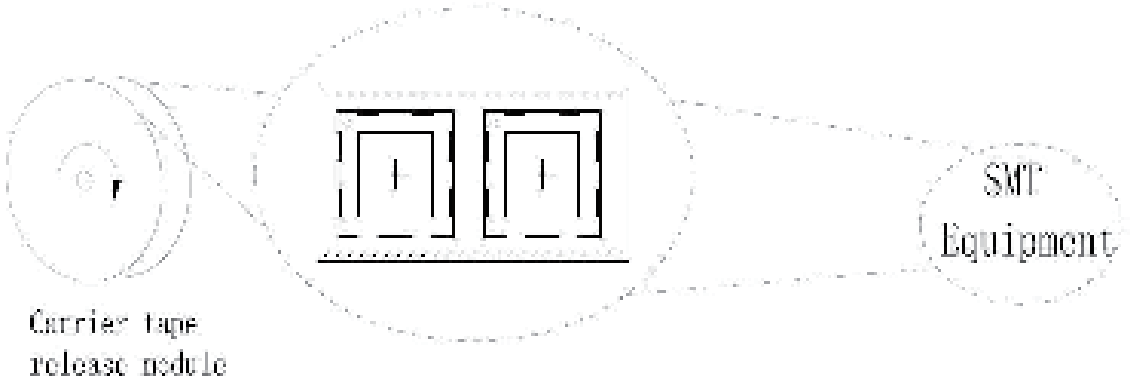
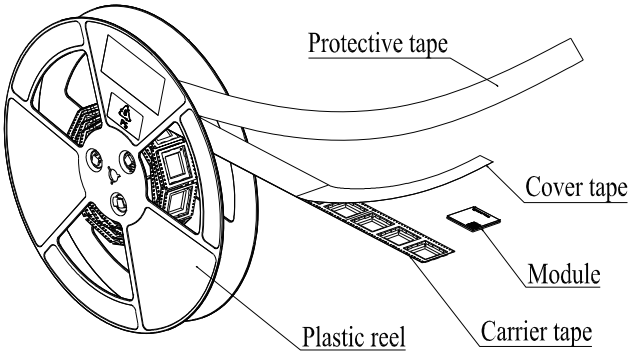


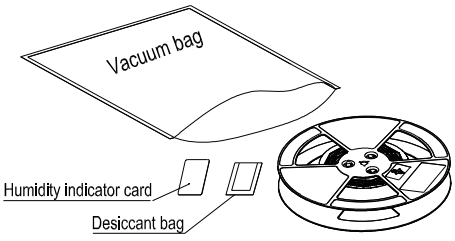
Figure 43: Tape and Reel Directions

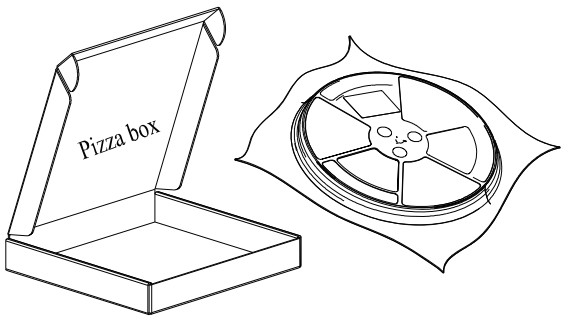
Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 cartoon box and seal it. 1 cartoon box can pack 1000 modules.

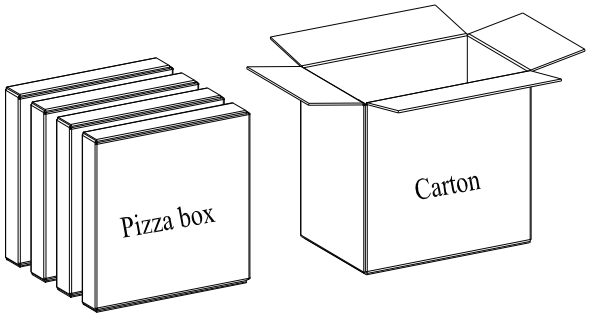


Figure 43: Packaging Process

9 Appendix References

Table 42: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EG915U-EU_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_User_Guide

Table 43: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AON	Active Optical Network
AP	Application Processor
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CS2	Commercial Sample II

CTS	Clear To Send
DAI	Digital Audio Interface
DCE	Data Communications Equipment
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FEM	Front-End Module
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access

HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inorm	Normal Current
LAA	License Assisted Access
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio

NSA	Non-Stand Alone
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mount Device

SMS	Short Message Service
SoC	System on a Chip
SPI	Serial Peripheral Interface
STB	Set Top Box
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value

$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network