



正基科技股份有限公司

SPECIFICATION

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DATE : 10.12. 2013

PRODUCT NAME : AP6234

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

AMPAK

AP6234

WiFi 11a/b/g/n +Bluetooth 4.0
SIP Module Spec Sheet

Revision History

Date	Revision Content	Revised By	Version
2012/10/18	- Initial released	Brian	1.0
2012/12/18	- Pin definition modify	Joe	1.1
2013/01/23	- Pin definition modify	Joe	1.2
2013/04/26	- Specification modify	Joe	1.3
2013/10/12	- Block Diagram modify	Brian	1.4

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1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module, with integrated dual band (2.4GHz/5GHz) IEEE 802.11 a/b/g and single-stream IEEE 802.11n MAC/baseband/radio and Bluetooth 4.0.

The integrated module provides SDIO V2.0 Host interface for Wi-Fi, high-speed UART is provided for the Bluetooth Host interface.

This compact module is a total solution for a combination of Wi-Fi dual mode + BT4.0 technologies. The module is specifically developed for mobiles, tablets or handheld wireless system devices.

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2. Features

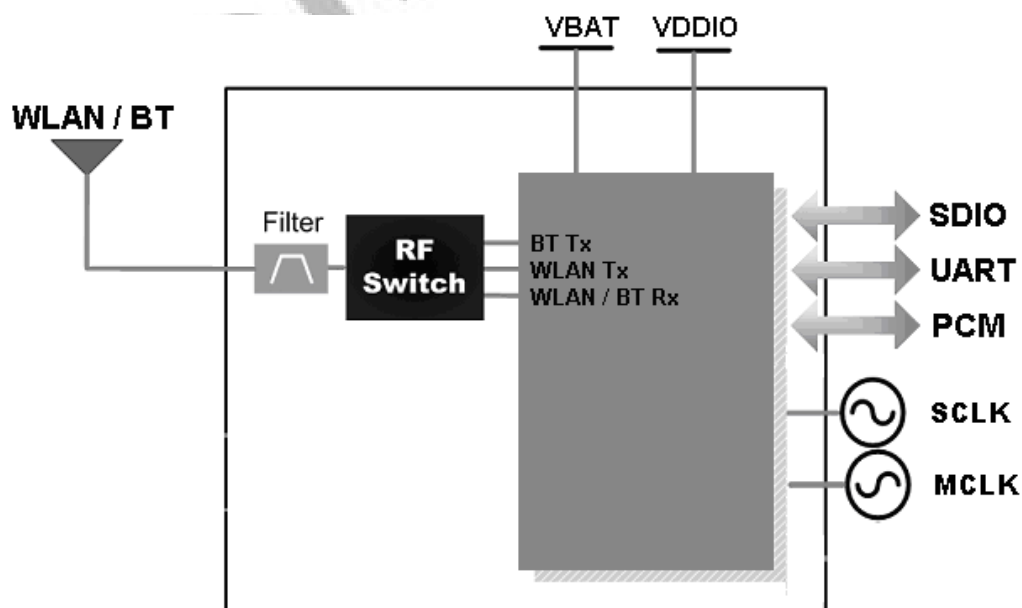
IEEE 802.11x Key Features

- Dual-band 2.4GHz/5GHz 802.11a/b/g/n.
- Single-stream IEEE 802.11n support for 20MHz and 40MHz channels provides PHY layer rates up to 150Mbps.
- WLAN host interface options: SDIO v2.0 — up to 50 MHz clock rate
- Support a single antenna shared between WLAN and Bluetooth.
- Security: WEP, WPS, WPA, WPA2, WMM, WAPI, AES,...

Bluetooth Features

- Bluetooth V4.0(BLE) Low Energy with provisions for supporting future specifications.
- Bluetooth Class1 or Class2 transmitter operation.
- BT host digital interface UART(up to 4 Mbps) with support all Bluetooth4.0 package types
- Multipoint operation with up to seven active ACL links, three active SCO and eSCO connections.
- Full support for power savings modes (standard sniff, deep sleep modes)
- ECI - enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

For module approval, the chip antenna with 3.26 dBi gain was verified in the conformity testing.

4. General Specification

4.1 General Specification

Model Name	AP6234
Product Description	Supports Wi-Fi dual mode /Bluetoothfunctionalities
Dimension	L x W x H: 12.0 x 12.0 x 1.5 (typical) mm
WiFi Interface	SDIOV2.0
BT Interface	UART/ PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.6	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.6	4.8	V
VDDIO	1.6	3.3	3.4	V

5. WiFi RF Specification

5.1 2.4GHz & 5GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11a/b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band) 5.150 GHz ~ 5.850 GHz (5.0 GHz ISM Band)
Number of Channels	2.4GHz : Ch1 ~ Ch11 5.0GHz : Please see the table ¹
Modulation	802.11a : OFDM /64-QAM, 16-QAM, QPSK, BPSK 802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM, 16-QAM, QPSK, BPSK
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -88 dBm, typical
	- MCS=1 PER @ -84 dBm, typical
	- MCS=2 PER @ -82 dBm, typical
	- MCS=3 PER @ -80 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -74dBm, typical
	- MCS=6 PER @ -72 dBm, typical
	- MCS=7 PER @ -70 dBm, typical
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 PER @ -87 dBm, typical
	- MCS=1 PER @ -83 dBm, typical
	- MCS=2 PER @ -81 dBm, typical
	- MCS=3 PER @ -79 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -76 dBm, typical
	- MCS=6 PER @ -71 dBm, typical
	- MCS=7 PER @ -70 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -89 dBm, typical
	- 9Mbps PER @ -88 dBm, typical
	- 12Mbps PER @ -86 dBm, typical

	- 18Mbps	PER @ -84 dBm, typical
	- 24Mbps	PER @ -82 dBm, typical
	- 36Mbps	PER @ -78 dBm, typical
	- 48Mbps	PER @ -75 dBm, typical
	- 54Mbps	PER @ -73 dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps	PER @ -95 dBm, typical
	- 2Mbps	PER @ -94 dBm, typical
	- 5.5Mbps	PER @ -90 dBm, typical
	- 11Mbps	PER @ -87 dBm, typical
Receive Sensitivity (11a) @10% PER	- 6Mbps	PER @ -88 dBm, typical
	- 9Mbps	PER @ -86 dBm, typical
	- 12Mbps	PER @ -84 dBm, typical
	- 18Mbps	PER @ -82 dBm, typical
	- 24Mbps	PER @ -80 dBm, typical
	- 36Mbps	PER @ -78 dBm, typical
	- 48Mbps	PER @ -75 dBm, typical
	- 54Mbps	PER @ -73 dBm, typical
Maximum Input Level	802.11b : -10 dBm	
	802.11a/g/n : -20 dBm	
Data Rate	802.11a : 6, 9, 12, 18, 24, 36, 48, 54Mbps	
	802.11b : 1, 2, 5.5, 11Mbps	
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps	
	802.11n: MCS0, MCS1, MCS2, MCS3, MCS4, MCS5, MCS6, MCS7	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

¹5GHz Channel table

Band (GHz)	Operating Channel Numbers	Channel center frequencies(MHz)
5.15GHz~5.25GHz	36	5180
	40	5200
	44	5220
	48	5240
5.25GHz~5.35GHz	52	5260
	56	5280
	60	5300
	64	5320
5.5GHz~5.7GHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620

5.725GHz~5.825GHz	128	5640
	132	5660
	136	5680
	140	5700
	149	5745
	153	5765
	157	5785
	161	5805

6. Bluetooth Specification

6.1 Bluetooth Specification

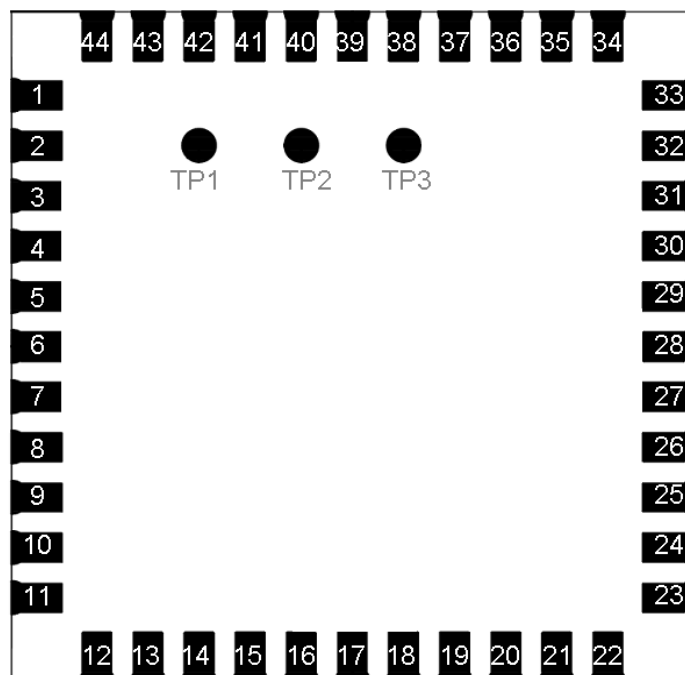
Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V4.0 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2.400 GHz ~ 2483.5 GHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
RF Specification			
	Min.	Typical.	Max.
Output Power (Class 1.5)		10 dBm	
Output Power (Class 2)		2 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

7. Pin Assignments

7.1 Pin Outline

< TOP VIEW >



7.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Floating (Don't connected to ground)
5	NC	—	Floating (Don't connected to ground)
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	NC	—	Floating (Don't connected to ground)
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	XTAL oscillator input
11	XTAL_OUT	O	XTAL oscillator output
12	WL_REG_ON	I	Internal regulators power enable/disable
13	WL_HOST_WAKE	O	WLAN to wake-up HOST

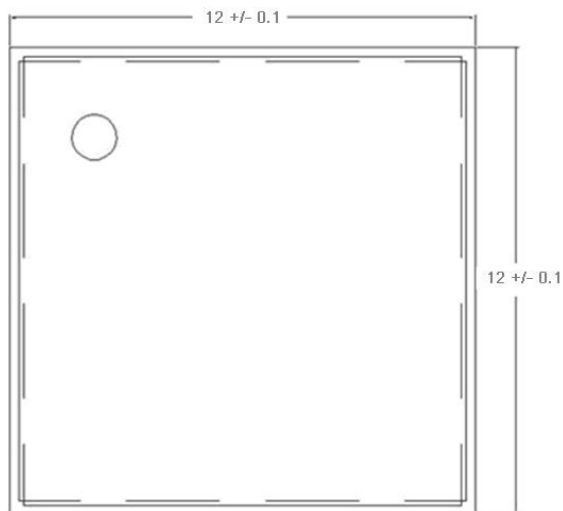
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	Low power oscillator clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	NC	—	Floating (Don't connected to ground)
30	NC	—	Floating (Don't connected to ground)
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	NC	—	Floating (Don't connected to ground)
38	NC	—	Floating (Don't connected to ground)
39	NC	—	Floating (Don't connected to ground)
40	NC	—	Floating (Don't connected to ground)
41	UART_RTS_N	O	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	UART_RXD	I	Bluetooth UART interface
44	UART_CTS_N	I	Bluetooth UART interface
45	TP1	—	Floating (Don't connected to ground)
46	TP2	—	Floating (Don't connected to ground)
47	TP3	—	Floating (Don't connected to ground)

8. Dimensions

8.1 Physical Dimensions

(Unit: mm)

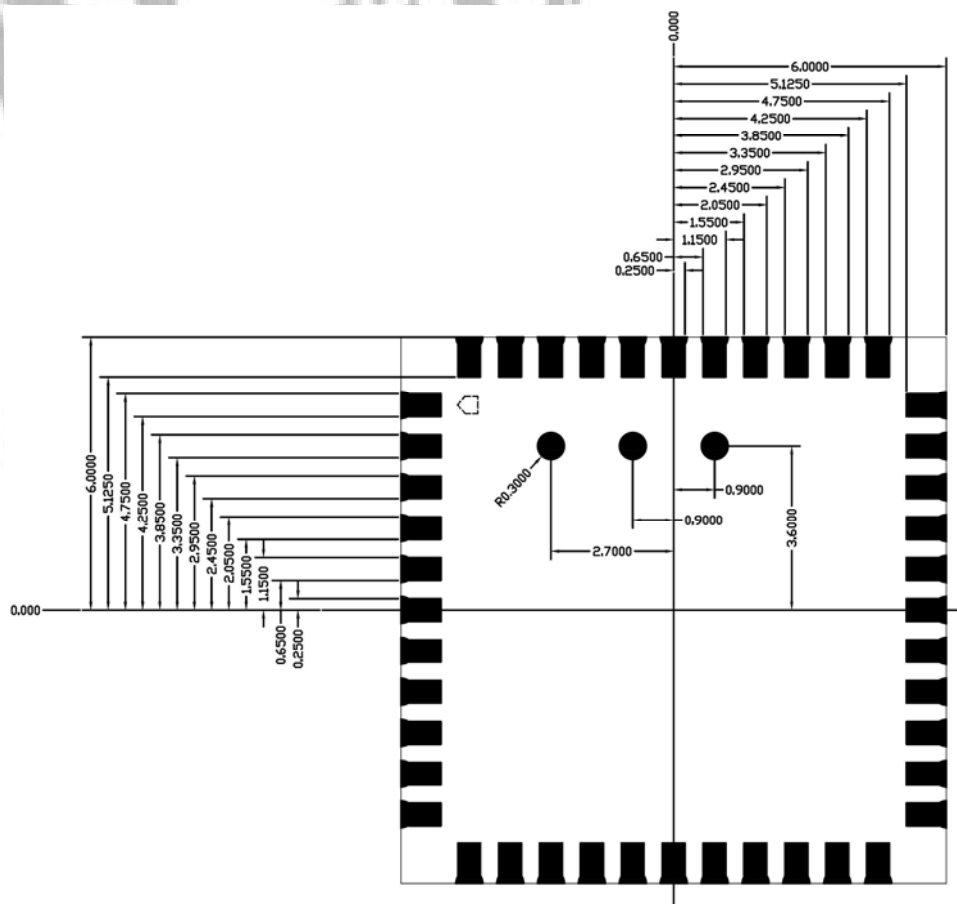
< TOP VIEW >



< Side View >



< TOP VIEW >



(Unit: mm)

Technical drawing of a rectangular building footprint, oriented horizontally. The drawing includes dimensions for the overall footprint and internal layout details.

Overall Dimensions:

- Overall width (horizontal): 6.2500
- Overall height (vertical): 6.0000

Internal Layout and Dimensions:

- Top Wall:** A series of vertical lines representing columns or structural elements. Dimensions from the left edge (0.000) to the right edge (6.2500) are: 0.2500, 0.6500, 1.1500, 1.5500, 2.0500, 2.4500, 2.9500, 3.3500, 3.8500, 4.2500, 4.7500, 5.1250, 5.6250, and 6.2500.
- Bottom Wall:** A series of vertical lines representing columns or structural elements. Dimensions from the left edge (0.000) to the right edge (6.2500) are: 0.2500, 0.6500, 1.1500, 1.5500, 2.0500, 2.4500, 2.9500, 3.3500, 3.8500, 4.2500, 4.7500, 5.1250, 5.6250, and 6.2500.
- Left Wall:** A series of horizontal lines representing columns or structural elements. Dimensions from the top edge (0.000) to the bottom edge (6.0000) are: 0.2500, 0.6500, 1.1500, 1.5500, 2.0500, 2.4500, 2.9500, 3.3500, 3.8500, 4.2500, 4.7500, 5.1250, 5.6250, and 6.0000.
- Right Wall:** A series of horizontal lines representing columns or structural elements. Dimensions from the top edge (0.000) to the bottom edge (6.0000) are: 0.2500, 0.6500, 1.1500, 1.5500, 2.0500, 2.4500, 2.9500, 3.3500, 3.8500, 4.2500, 4.7500, 5.1250, 5.6250, and 6.0000.
- Internal Features:**
 - Three circular features (possibly columns or openings) are located in the upper right quadrant. Their horizontal positions are 0.9000, 2.7000, and 3.6000 from the left edge. Their vertical positions are 0.9000, 2.7000, and 3.6000 from the top edge.
 - A dimension of 0.9000 is shown for the horizontal distance between the first and second circular features.
 - A dimension of 2.7000 is shown for the horizontal distance between the second and third circular features.
 - A dimension of 0.9000 is shown for the horizontal distance between the third circular feature and the right edge.
 - A dimension of 3.6000 is shown for the vertical distance between the first and second circular features.
 - A dimension of 0.9000 is shown for the vertical distance between the second and third circular features.
 - A dimension of 0.9000 is shown for the vertical distance between the third circular feature and the bottom edge.
 - A dimension of 0.9000 is shown for the horizontal distance between the first and second circular features.
 - A dimension of 2.7000 is shown for the horizontal distance between the second and third circular features.
 - A dimension of 0.9000 is shown for the horizontal distance between the third circular feature and the right edge.
 - A dimension of 3.6000 is shown for the vertical distance between the first and second circular features.
 - A dimension of 0.9000 is shown for the vertical distance between the second and third circular features.
 - A dimension of 0.9000 is shown for the vertical distance between the third circular feature and the bottom edge.

9. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	± 30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

9.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

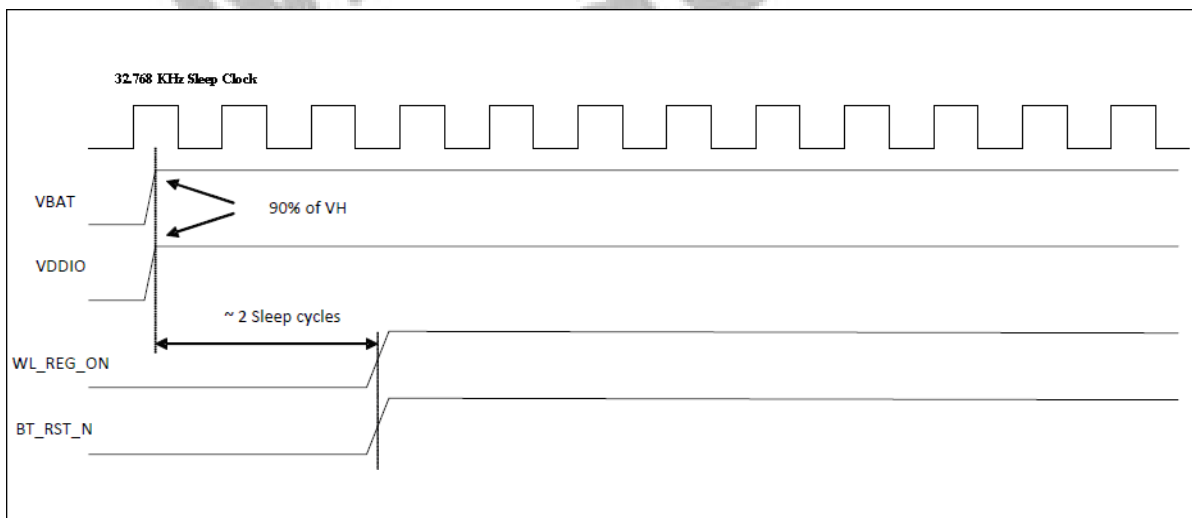
10. Host Interface Timing Diagram

10.1 Power-up Sequence Timing Diagram

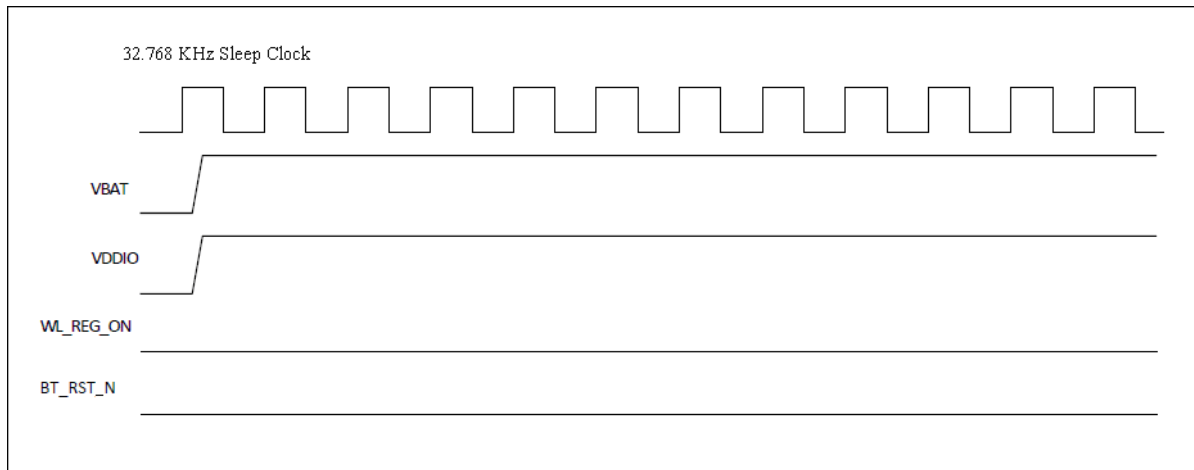
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

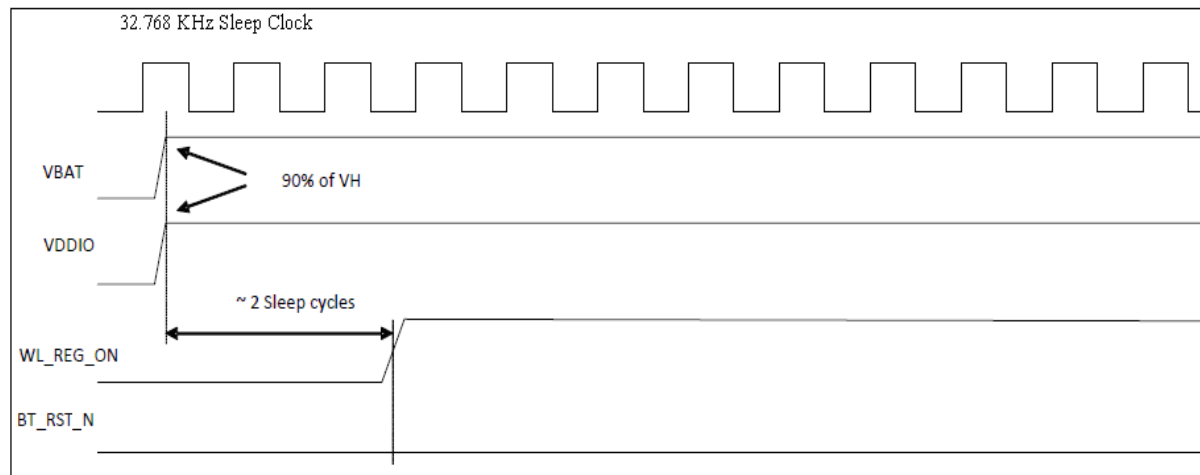
- ※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT_RST_N: Low asserting reset for Bluetooth only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



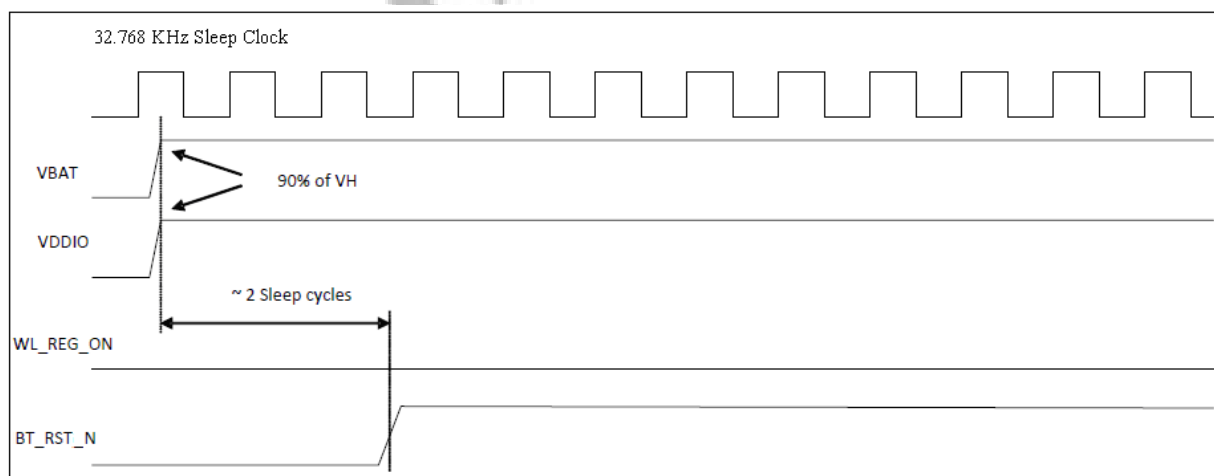
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

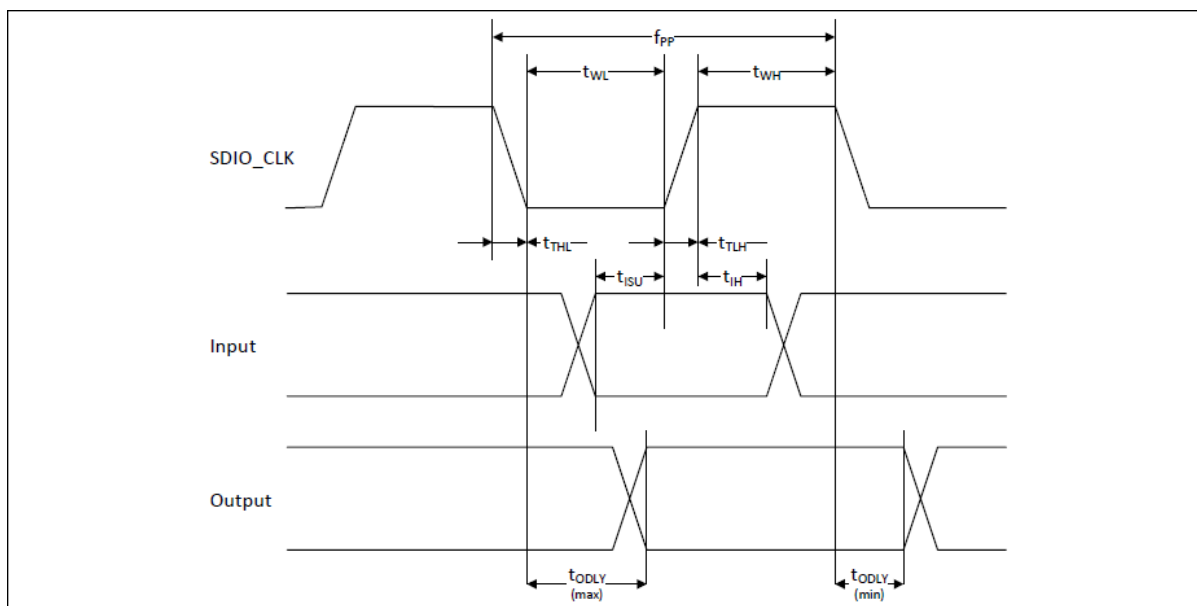


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

10.2 SDIO Default Mode Timing Diagram

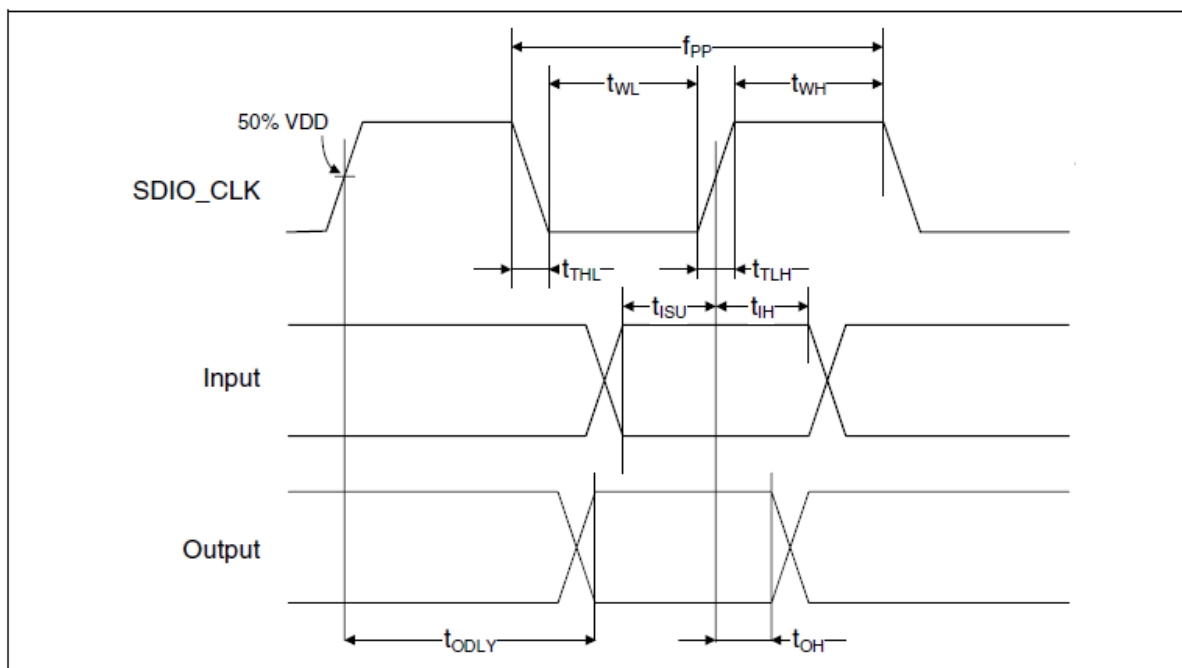


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency-Data Transfer mode	f_{PP}	0	-	25	MHz
Frequency-Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	10	-	-	ns
Clock high time	t_{WH}	10	-	-	ns
Clock rise time	t_{TLH}	-	-	10	ns
Clock low time	t_{THL}	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	-	-	ns
Input hold time	t_{IH}	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	0	-	14	ns
Output delay time - Identification mode	t_{ODLY}	0	-	50	ns

a. Timing is based on $CL \leq 40pF$ load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

10.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency-Data Transfer mode	f_{PP}	0	-	50	MHz
Frequency-Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	7	-	-	ns
Clock high time	t_{WH}	7	-	-	ns
Clock rise time	t_{TLH}	-	-	3	ns
Clock low time	t_{THL}	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6	-	-	ns
Input hold time	t_{IH}	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	-	-	14	ns
Output hold time	t_{OH}	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL $\leq$ 40pF load on CMD and Data.

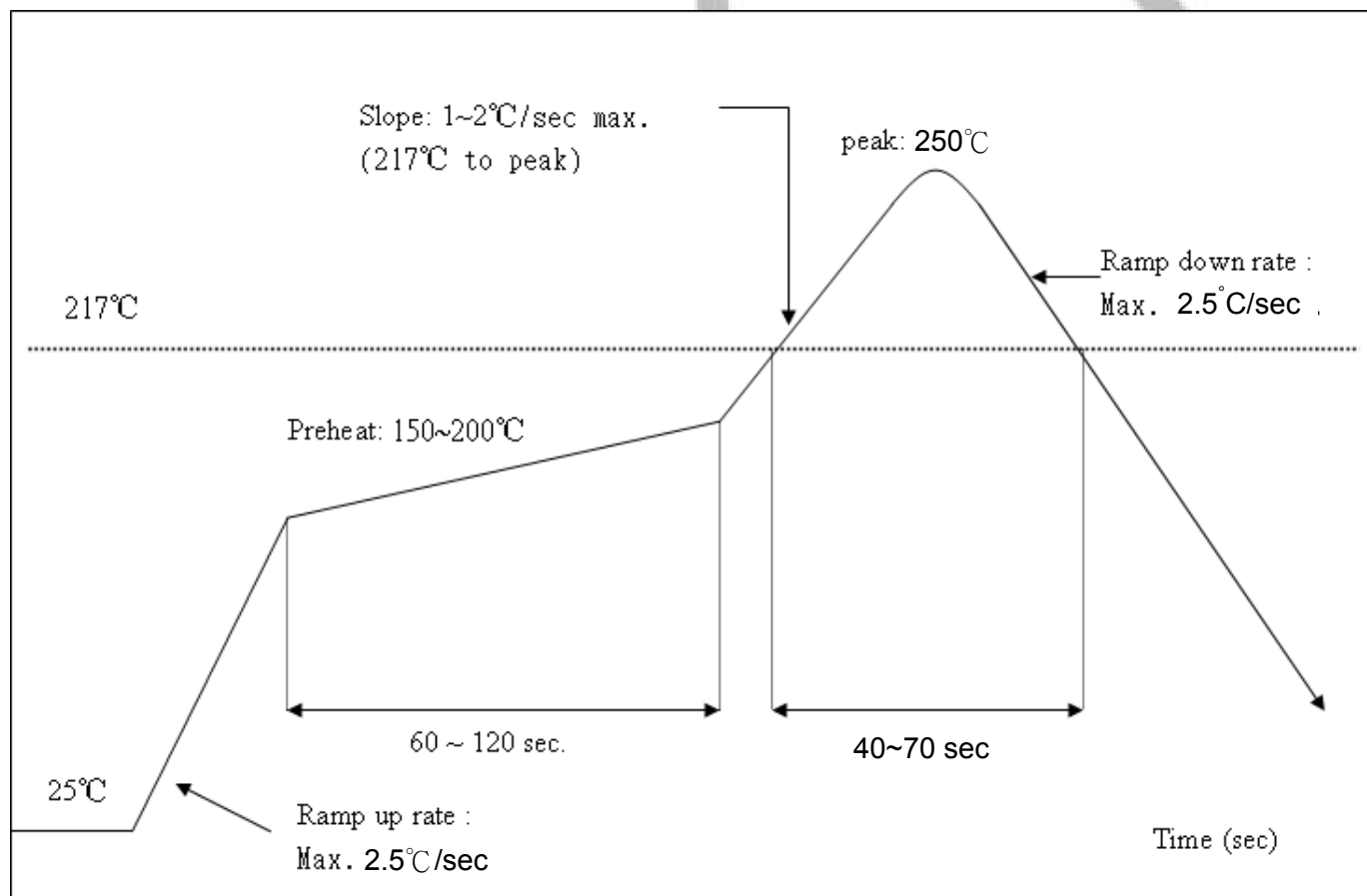
b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : $<250^{\circ}\text{C}$

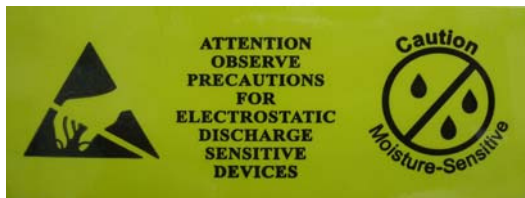
Number of Times : ≤ 2 times



12. Package Information

12.1 Label

Label A→ Anti-static and humidity notice



Label B→ MSL caution / Storage Condition

Caution		LEVEL
This bag contains MOISTURE-SENSITIVE DEVICES		☐ If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: _____ hours of factory conditions If blank, see adjacent bar code label ≤30°C/60% RH, or b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: _____ If blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

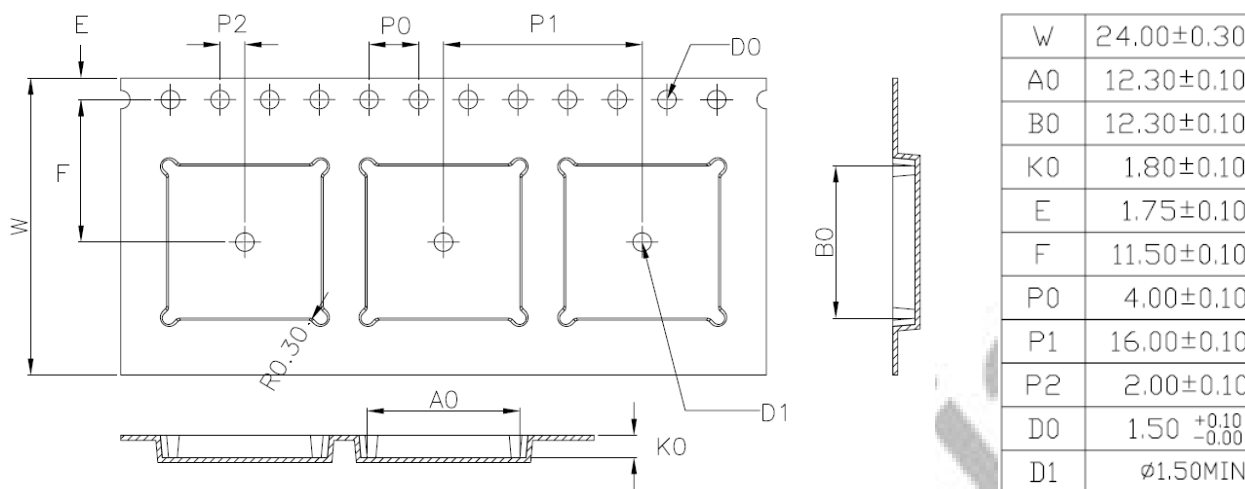
Label C→ Inner box label .

PKG S/N :	 9PKG12013100001
Model:	 XXXXXXXXXXXX
P/N :	 99P-W01-0048R
Qty :	 1500
Date Code :	 1205
Lot Code :	 T0C102B

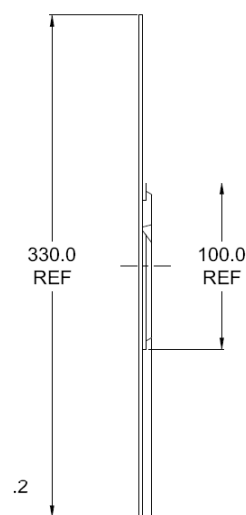
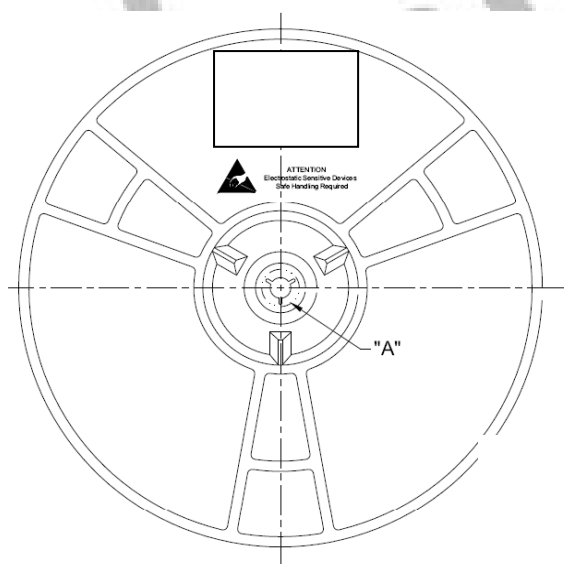
Label D→ Carton box label .

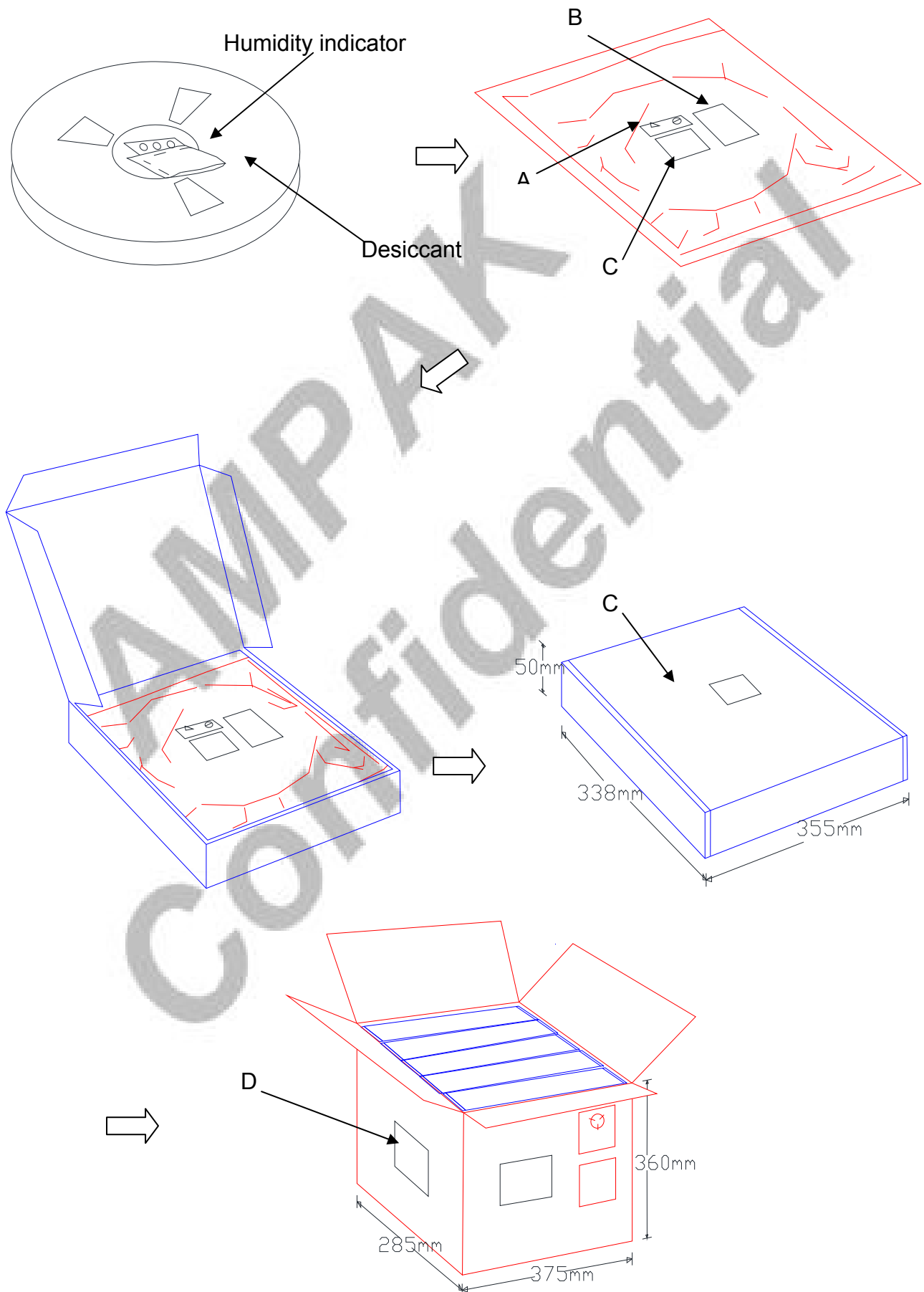
AMPAK Technology	
Model Name :	 XXXXXXXXXXXX
Part No :	 99P-W01-0048R
Quantity :	 7500 ea
Lot D/C :	 20081000033
Manufacture :	 2012/02/22

12.2 Dimension



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





12.3 MSL Level / Storage Condition

	Caution This bag contains MOISTURE-SENSITIVE DEVICES Do not open except under controlled conditions 1. Calculated shelf life in sealed bag: 12 months at $< 40^{\circ}\text{C}$ and $< 90\%$ relative humidity(RH) 2. Peak package body temperature: 225°C 240°C 250°C 260°C ☐ ☐ ☒ ☐ 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must a) Mounted within: 48 hours of factory conditions $< 30^{\circ}\text{C} / 60\% \text{ RH}$, OR b) Stored at $< 10\% \text{ RH}$ 4. Devices require bake, before mounting, if: a) Humidity Indicator Card is $> 10\%$ when read at $23 \pm 5^{\circ}\text{C}$ b) 3a or 3b not met 5. If baking is required, devices may be baked for 24 hours at $125 \pm 5^{\circ}\text{C}$ Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: See-SEAL DATE LABEL Note: Level and body temperature defined by IPC/JEDEC J-STD-020	LEVEL 4
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※NOTE : Accumulated baking time should not exceed 96hrs