

APPENDIX 6

TRANSMITTER TUNE-UP PROCEDURE

2. VCO VOLTAGE ADJUSTMENT

SELECT THE OPERATING CHANNEL ON CH 1.
CONNECT DC VOLTMETER(14) BETWEEN GROUND AND PIN 3 OF VCO MODULE.
MAKE THE SET UNDER TX MODE.
TUNE THE VCO VOLTAGE TUNING IFT L601 TO OBTAIN 2.0 V READING OF DC VOLTMETER.
CHECK THE VOLTAGE OF CHANNEL 40 WHETHER THE READING IS IN BETWEEN 2.5 TO 5.5 V DC
UNDER RX MODE.
REMOVE DC VOLTMETER .

3. TRANSMITTER ALIGNMENT

- 3-1. CONNECT THE RF VOLTMETER (13) ON THE BASE OF Q704.
TRANSMIT ON CHANNEL 19 .
ADJUST L701, L702 FOR MAXIMUM READING ON RF VOLTMETER .
REPEAT AS NEEDED.
REMOVE RF VOLTMETER .
- 3-2. WITH THE RF POWER METER READING ON RF WATTMETER (5).
REPEAT IF NEEDED.
- 3-3. REPEAT STEPS 1 AND 2 IF NEEDED.
- 3-4. OUTPUT POWER READING ON RF WATTMETER (5) SHOULD BE FROM 3.6 TO 4.0 W.
IF POWER EXCEEDS 4.0 WATTS INCREASE R711 TO REDUCE POWER AND REPEAT
ALIGNMENT AGAIN.

4. FINAL CHECK

IN TRANSMIT ON ALL 40 CHANNELS

- 4-1. OUTPUT POWER SHOULD BE FROM 3.6 TO 4.0 WATTS .
- 4-2. FREQUENCY SHOULD BE WITHIN +400 Hz OF CHANNEL CENTER FREQUENCY .
- 4-3. STRENGTH OF SPURIOUS SIGNALS AS OBSERVED ON SPECTRUM ANALYZER (10)
SHOULD BE LESS 60 dB THAN THE TRANSMITTING FREQUENCY.

TRANSMITTER TUNE-UP PROCEDURE
FCC ID: BBOHH37ST

C . SEMICONDUCTORS AND FUNCTION

REF. NO	DESCRIPTION	RX	TX	REMARK
Q101	KTC3875S	RF ATTENUATOR	×	KEC
Q102	KTC3880S	RF AMP	×	KEC
Q103	KTC3880S	1 'ST MIXER	×	KEC
Q201	KTC3880S	2 'ND MIXER	×	KEC
Q202	KTC3880S	IF AMP	×	KEC
Q203	KTC3880S	IF AMP	×	KEC
Q204	KRA1504S	A. N. L.	×	KEC
Q403	KTA1504S	×	A. L. C.	KEC
Q404	KTC3875S	×	A. L. C.	KEC
Q500	KTC3875S	LED CONTROL	LED CONTROL	KEC
Q501	KTA1504S	LED CONTROL	LED CONTROL	KEC
Q502	KTA1504S	LED CONTROL	LED CONTROL	KEC
Q503	KTA1504S	LED CONTROL	LED CONTROL	KEC
Q510	KTC3875S	CHARGE PUMP	CHARGE PUMP	KEC
Q511	KTC3875S	CHARGE PUMP	CHARGE PUMP	KEC
Q513	KTC3875S	LED CONTROL	LED CONTROL	KEC
Q550	KTC3875S	SQ CONTROL	×	KEC
Q553	KTA1266	SQ CONTROL	×	KEC
Q601	KTC3880S	BUFFER	BUFFER	KEC
Q602	KTC3875S	×	SWITCHING	KEC
Q603	KTC3880S	VCO	VCO	KEC
Q701	KTC3880S	×	DOUBLER	KEC
Q702	KTC3880S	×	PRE AMP	KEC
Q703	KTC1006	×	RF DRIVER	KEC
Q704	KTC2078	×	RF POWER AMP	KEC
Q801	KTC3875S	ST LAMP CNTR	ST LAMP CNTR	KEC
Q802	KTA1504S	EXP AMP	EXP AMP	KEC
Q900	KTC38	BATT LOW	BATT LOW	KEC
Q901	KTC3875S	BATT LOW	BATT LOW	KEC
Q902	KTC3875S	REGULATOR(9. 1V)	REGULATOR(9. 1V)	KEC
Q903	KRA102S	B+ CONTROL	×	KEC
Q904	KRA102S	×	B+ CONTROL	KEC
IC401	KIA7217AP	×	AF AMP	KEC
IC501	LC7185	PLL	PLL	SANYO
IC551	LM386	AF AMP	×	NATIONAL
IC801	TA31101AF	COMAPANER	COMAPANER	TOSHIBA

*** MANUFACTURER INFORMATION ***

- * K. E. C ----- KOREA ELECTRONICS SEMICONDUCTOR CO., LTD.
- * MOTOROLA ----- MOTOROLA SEMICONDUCTOR CO., LTD.
- * SANYO ----- SANYO SEMICONDUCTOR CO., LTD.

APPENDIX 7

CIRCUITS AND DEVICES TO STABILIZE FREQUENCY

All 40 channels of transmitting, and receiving, frequencies are provided by PLL (Phase Locked Loop) circuitry.

The purpose of the PLL is to provide a multiple number of frequencies from VCO (Voltage Controlled Oscillator) with quartz crystal accuracy and stability from on crystal oscillator reference frequency.

The reference crystal oscillator frequency is 10.240 MHz.

CIRCUITS AND DEVICES TO
STABILIZE FREQUENCY
FCC ID: BBOHH37ST

APPENDIX 7

APPENDIX 8

Circuits For Suppression Spurious Radiation

The tuning circuit between frequency synthesizer and final amp Q702 and 3-stage "PI" network C718, C719, L711, C721, L712, C725, C722, L713, C723 in the Q704 output circuit serve to suppress spurious radiation. This network serves to impedance match Q704 to the antenna and to reduce spurious content to acceptable levels in the frequency synthesizer.

Circuits For Limiting Modulation

A portion of the modulating voltage is rectified by D401 which controls Q403, Q404 attenuating the mic input to IC401. The resulting feedback loop keeps the modulation from exceeding 100 percent with inputs approximately 40 dB greater than that required to produce 50 percent modulation. The modulation attack time is about 50 mS and the release time is about 300 mS.

Circuits For Limiting Power

During factory alignment, the series resistor of tx power amp Q704 is selected to limit the available power to slightly more than 4 watts. The tuning is adjusted so that the actual power is from 3.6 to 3.9 watts. There are no other controls for adjusting the tx output power.

DEVICES AND CIRCUITS TO SUPPRESS
SPURIOUS RADIATION AND LIMIT
MODULATION

FCC ID: BBOHH37ST

APPENDIX 8

APPENDIX 9
PLL DATA SHEETS

FIFTEEN (15) PAGES FOLLOW THIS SHEET

COPY OF PLL DATA SHEETS
FCC ID: BBOHH37ST

APPENDIX 9

SANYO

LC7185-8xxx

CMOS LSI

**CB TRANSCEIVER PLL FREQUENCY SYNTHESIZER
AND CONTROLLER****Overview**

This 27MHz band, PLL frequency synthesizer LSI chip is designed specifically for CB transceivers. The internal ROM can be changed to suit the frequency specifications of various countries (hence the 8xxx designation).

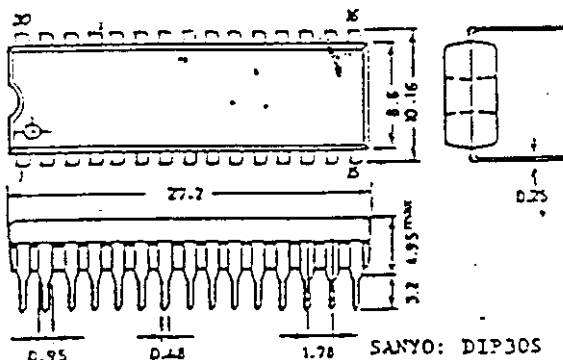
The LC7185-8xxx incorporates PLL circuitry and a controller for CB applications on a single CMOS chip. The controller handles the PLL circuitry, frequency data ROM, channel preset/recall RAM, and LED display drivers. It also supports channel scan, channel preset/recall, and emergency channel call.

Features

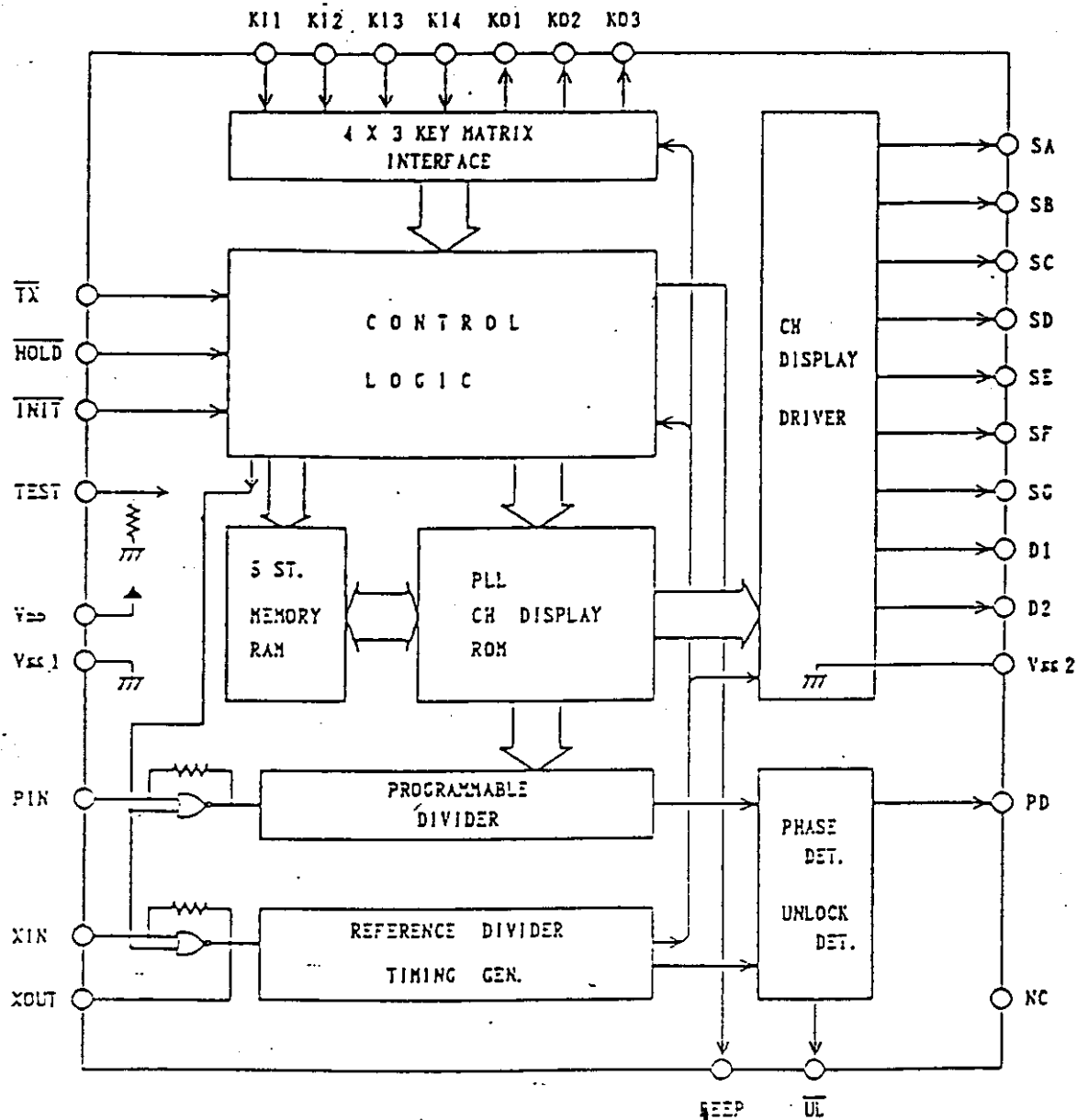
- A built-in programmable divider for the 16MHz VCO.
- Transmission is inhibited when the PLL is unlocked (digital lock monitor).
- Direct channel 9 or 19 selection (sliding switch)
- A 7-segment, 2-character LED display
- "PA" is displayed in public announcement mode.
- Output beep-tone control circuitry
- Up to 5 channel settings can be stored in memory.
- 4 x 3 key matrix implementation
- DIP30S (shrink) package

The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass-produced. The information herein is believed to be accurate and reliable. However, no responsibility is assumed by SANYO for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

Case Outline 3061-D30SNIC
(unit:mm)



Block Diagram



Pin Descriptions

TX: Transmit/receive select

HOLD: Hold mode select

INIT: Reset line

TEST: Test point (input)

VDD, VSS1, VSS2: Power supply

PIN: Programmable divider input

XIN, XOUT: Crystal oscillator input, output (e.g. 10.240MHz)

UL: Unlock detected output

PD: Charge pump output

NC: NC Pin

SA to SG: Segment drivers (for display)

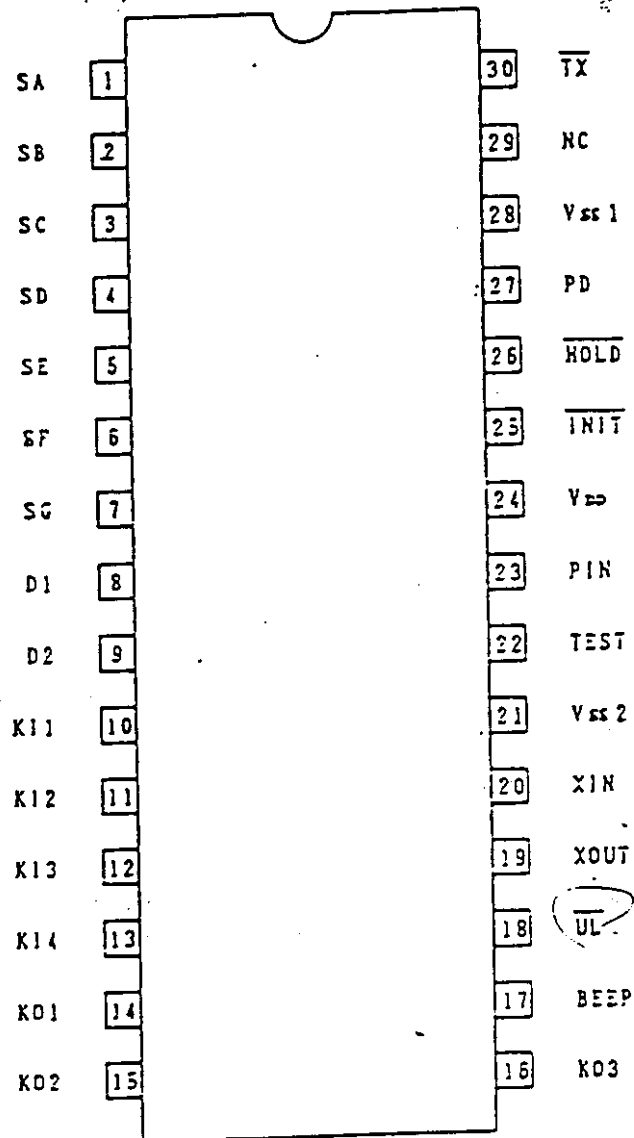
D1, D2: Digit output (for display)

K11 to 4: Key inputs

K01 to 3: Key scan outputs

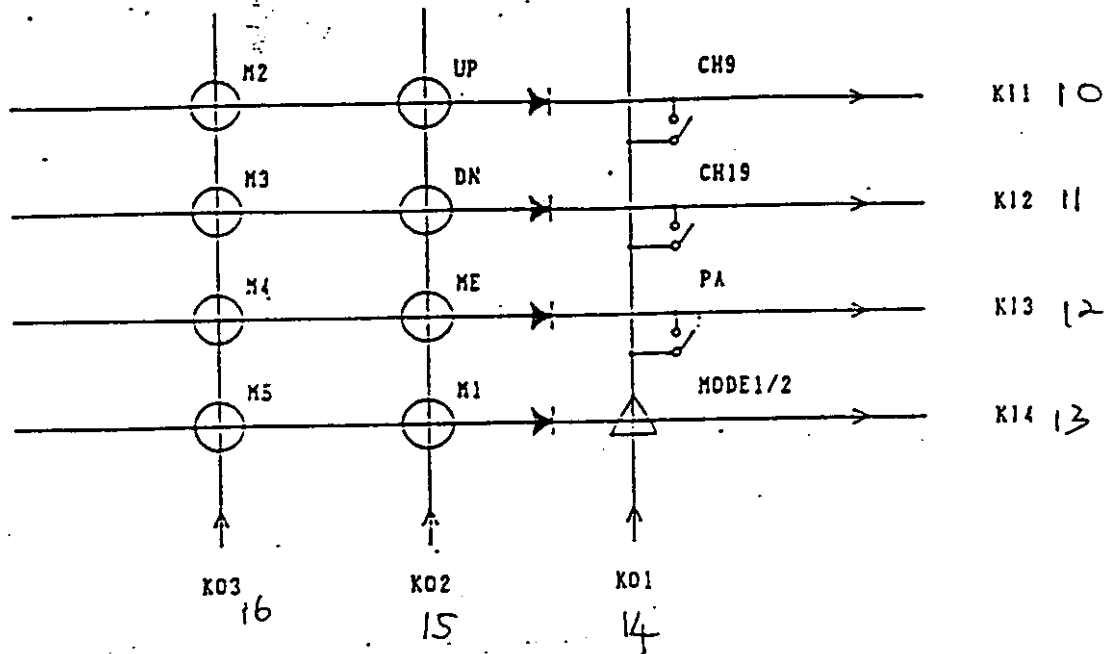
BEEP: Beep-tone control output

Pin Assignment: DIP30S (shrink) package



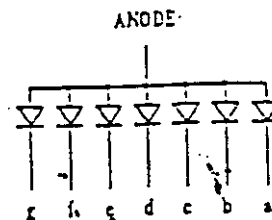
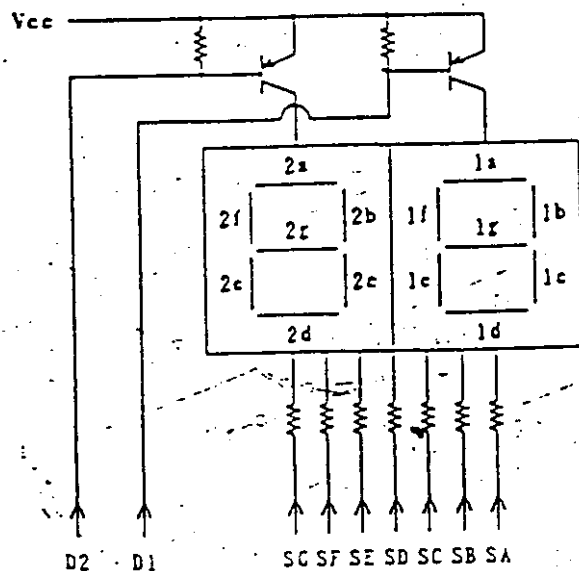
top view

Key Matrix



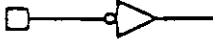
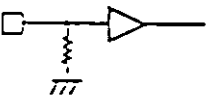
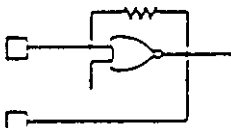
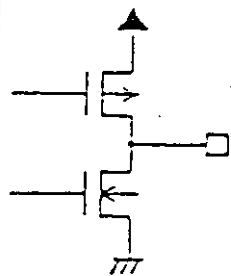
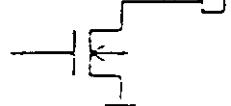
CH9: Emergency CH9 select
 CH19: Emergency CH19 select
 PA: Public announcement display
 MODE 1/2: Display mode
 UP: Channel up/scan
 DN: Channel down/scan
 ME: Channel memory enable
 M1 to M5: Channel memory recall
 UP/DN/ME/M1 to M5: Momentary switch
 CH9/CH19/PA: Sliding switch
 MODE 1/2: Diode

LED Display Configuration (Common anode/7 segment)

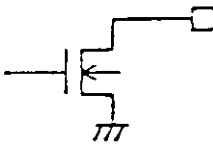
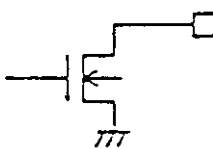
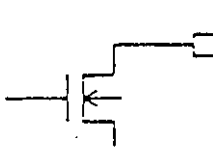
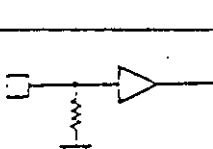
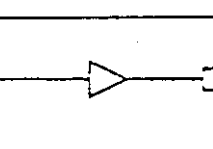


	SG	SF	SE	SD	SC	SB	SA
D1	1g	1f	1e	1d	1c	1b	1a
D2	2g	2f	2e	2d	2c	2b	2a

Pin Description

Pin Name	Pin No.	Type	Description
$\overline{\text{TX}}$	30		Transmit/receive select $\overline{\text{TX}} = "0"$... Transmit, $\overline{\text{TX}} = "1"$... Receive
$\overline{\text{HOLD}}$	26		Hold mode select $\overline{\text{HOLD}} = "0"$... Hold mode select $= "1"$... Normal mode select
$\overline{\text{INIT}}$	25		Reset line $\overline{\text{INIT}} = "0"$... Reset
TEST	22		Test point (input) Tie to ground or leave floating
V_{DD}	24		Power supply (+) Normal mode: 5.0 to 8.0V Hold mode: $\geq 3.0V$
V_{SS2}	21		Channel display LED driver Ground
PIN	23		Programmable divider input 150mVrms min Hold mode: Programmable divider is disabled.
XIN	20		Crystal oscillator Frequency: 10.24MHz
XOUT	19		Hold mode: Oscillator is disabled.
PD	27		Charge pump output from the phase comparator f_V is obtained by dividing the PIN frequency input by N (programmable divider value) f_R is the reference signal (reference divider output) $f_V > f_R$ or leading: Positive pulses $f_V < f_R$ or lagging: Negative pulses $f_V = f_R$ and phase matched: High impedance Hold mode: High impedance
V_{SS1}	28		PLL circuit and controller Ground
NC	29		No-connection
$\overline{\text{UL}}$	18		Unlock detected output Low level: See Unlock Detected Output ($\overline{\text{UL}}$) for detail. Open: Locked

Continued from preceding page.

Pin Name	Pin No.	Type	Description
BEEP	17		Beep-tone control output Open: See Beep-tone Control Output for detail. Low level: Hold mode
SA to SG	1 to 7		Segment drivers for the display (Common anode/7 segments)
D1 D2	8 9		Digit output (150Hz) for the display (Common anode/7 segments) Hold mode: Tr goes off.
KI1 to KI4	10 to 13		Key inputs Input from the key matrix
KO1 to KO3	14 to 16		Key scan output (75Hz) Output to the key matrix Hold mode: Low (scanning stops)

Operation

(1) Channel selection (up/down)

The unlock detected line (UL) is asserted (low) when the UP (or DN) key is pressed and deactivated 25ms after the key is released (see diagram below). The beep-tone control line (BEEP) is asserted (open) for 50msec after each new channel is selected (see diagram below).

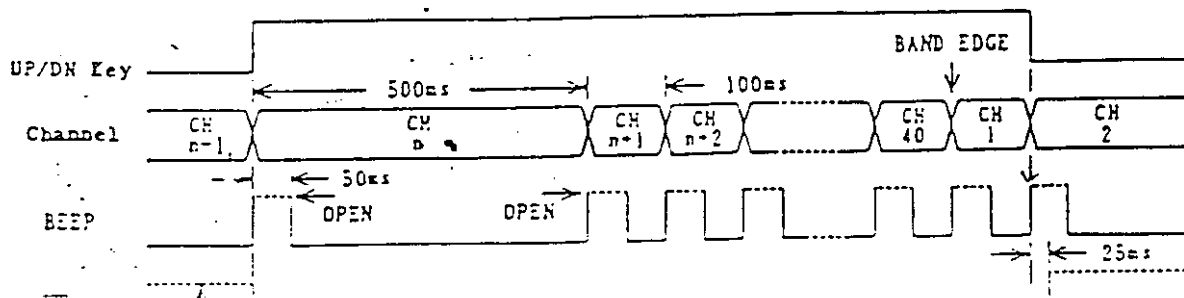
1) Manual scanning (up/down)

Pressing the UP key increments by one channel and pressing the DN key decrements by one channel.

When scanning reaches the end of the band, it automatically wraps around to the beginning.

2) Auto scanning (up/down)

Holding the UP (or DN) key down for 500msec or longer starts auto scanning. For both up and down scanning, each channel takes 100msec to scan.



(2) Selecting an emergency channel (CH9/CH19)

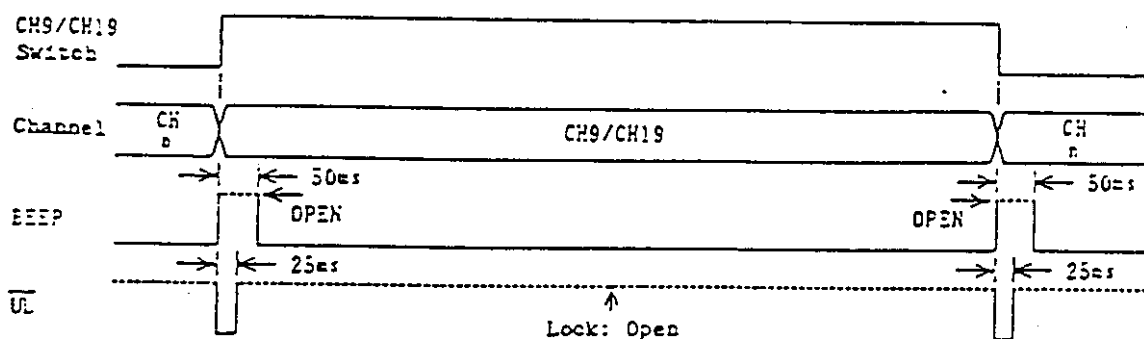
If the CH9 or CH19 switch is turned on, the LC7185 does the following:

- Stores the value of the previous channel
- Asserts the beep-tone control line for 50msec
- Disables the UP/DN, M1 to M5, and ME switches
- Causes either "9" or "19" to blink on the display
- Keep the emergency channel open until the CH9 or CH19 switch is turned off.

After the CH9 or CH19 switch is turned back off the beep-tone control line is asserted for 50msec and the LC7185 reopens the previous channel.

Note the CH9 has a higher priority over CH19. As a result, if both switches are turned on, CH9 will be opened.

As shown in the diagram, the $\overline{UL}$ line is asserted for 25ms after the CH9 or CH19 switch is turned off or on.



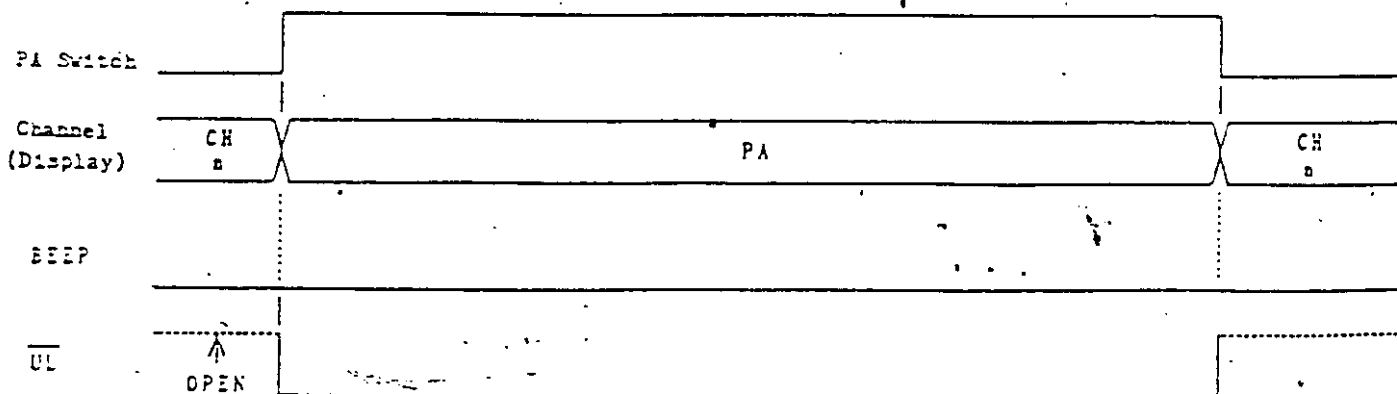
(3) Public Announcement (PA) mode

When the PA switch is turned on, the LC7185 does the following:

- Stores the value of the previous channel
- Disables all keys
- Causes "PA" to be displayed
- Stays in PA mode until the PA switch is turned off.

When the PA switch is turned back off, the LC7185 leaves PA mode and reopens the previous channel.

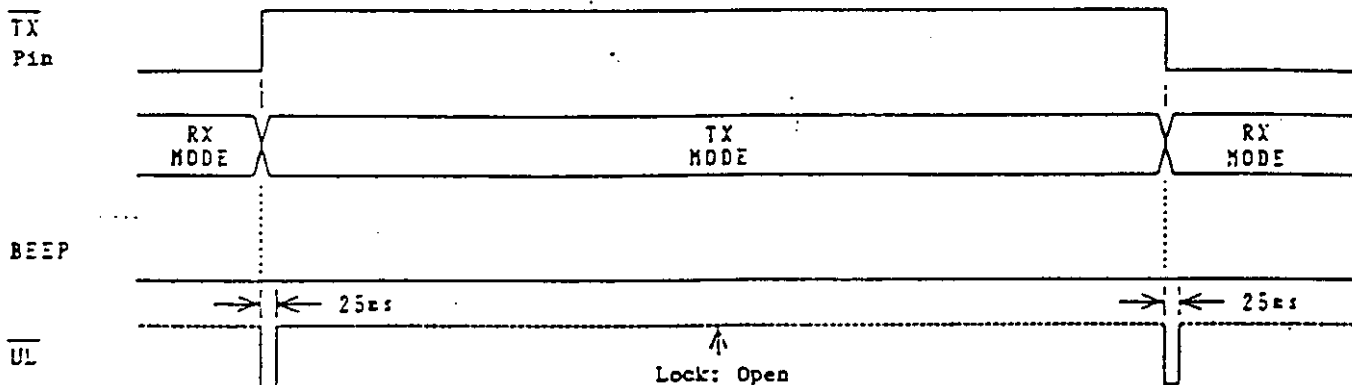
As shown in the diagram, the $\overline{UL}$ line is asserted while the PA switch is turned on.



(4) Transmit/Receive Selection

When the $\overline{\text{TX}}$ line is asserted, the LC7185 enters TX mode. The LC7185 will only leave this mode if the PA switch is pressed or the $\overline{\text{TX}}$ line is deactivated.

As shown in the diagram, the $\overline{\text{UL}}$ line is asserted for 25ms after the TX line is asserted or deactivated.



(5) Channel Preset/Recall Facility

1. The LC7185 allows up to 5 channels to be preset (assigned to M1 to M5).
 . After a reset, M1 to M5 are assigned to CE33.

2. Recalling preset channels

- . A preset channel is recalled by pressing one of the preset memory keys (M1 to M5)* to which the channel was previously assigned.
- . Presetting channel (assigning keys) are covered in the next section.
- There are two different display modes as shown below.

Mode 1 (without diode)

Each time a key is pressed (e.g. M1), the new channel is displayed.

Example: Display 21 → 15

Key

M 1

Mode 2 (with diode)

Each time a key is pressed (e.g. M1), a key mnemonic (e.g. "P1") is displayed for 400msec, then the new channel is displayed.

Example: Display 21 → P1 → 15

Key

M 1

400ms

3. Presetting channels

Presetting a channel is done in the following way. First select the channel to be preset, then hold down the ME key and press the preset memory key (M1 to M5)* to which you would like to assign the current channel.

In the following cases, a channel will not be preset:

- . 9 seconds elapse after the ME key is pressed and one of M1 to M5 is pressed.
- . Emergency channels CH9 or CH19 are currently selected
- . The TX line is asserted.
- . The PA switch is turned on (PA mode).
- . The HOLD line is asserted (hold mode).

There are two different display modes as shown below.

Mode 1 (without diode)

The current channel is displayed throughout the preset process.

Example: Display 15 → 15

Key

ME M1

Mode 2 (with diode)

When the ME key is held down, "PE" is flashed on the display. Once a preset memory key is pressed (e.g. M1), the key mnemonic (e.g. "P1") is displayed for 400msec before the current channel is redisplayed.

Example: Display 15 → PE → P1 → 15

Key

ME M1

400msec

* Note that if two or more keys are pressed at the same time, priority is assigned as follows:

M1>M2>M3>M4>M5

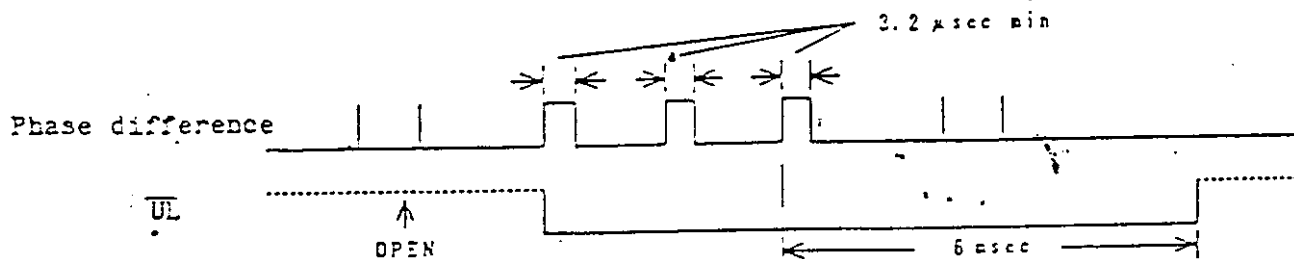
(6) Beep-tone Control Output

After each of the following events, the BEEP line is asserted for 50msec:

- . A reset (e.g. battery replacement)
- . Any key press associated with the channel memory
- . Any emergency channel switch activation
- . A new channel is selected.
- . Leaving hold mode

(7) Unlock Detected Output ($\overline{UL}$)

In the following cases, the $\overline{UL}$ line is asserted for the duration indicated.

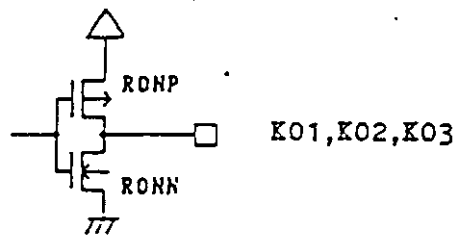


- . When the phase difference between the programmable and reference divider outputs exceeds 3.2 μ sec. The $\overline{UL}$ line is held low for 6msec after the last out-of-range phase sample is detected, as shown below.
- . After a new transmit/receive or channel selection. The $\overline{UL}$ line is asserted for 25msec.
- . While the PA switch is turned on.

(8) Key Matrix

It is normal to put diodes in series with the key scanning lines to avoid creating a short with the output lines.

But K01, K02 and K03 lines don't need diodes.

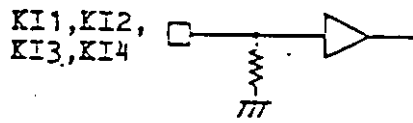


R_{ONP}, R_{ONN} : ON impedance

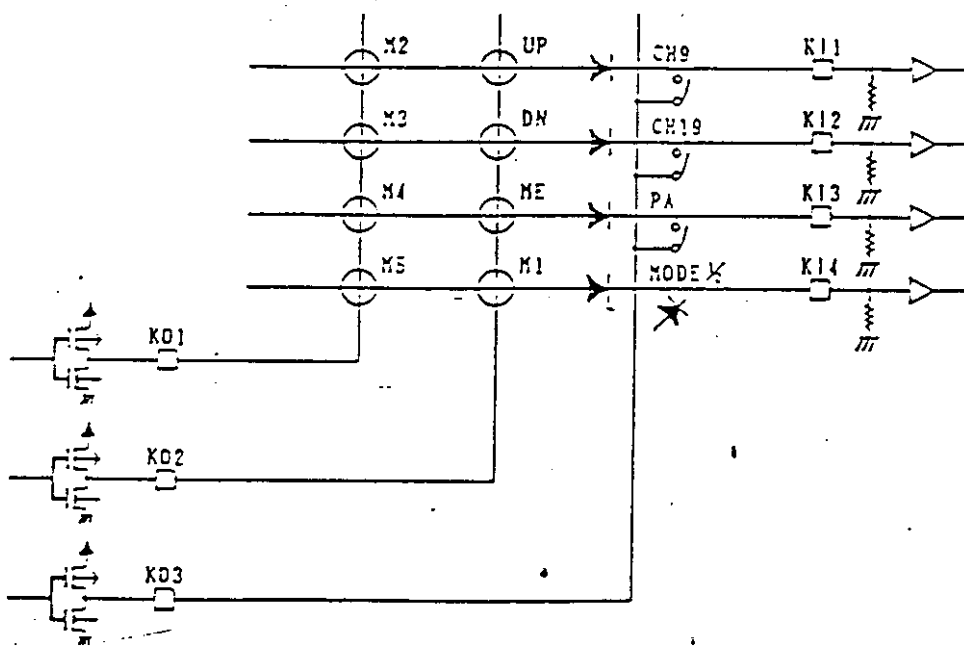
	min	typ	max	[kohm]
R_{ONP}	0.5	1.0	2.0	

R_{ONN}	30	50	70	
-----------	----	----	----	--

R_{PdN}	30	50	70	
-----------	----	----	----	--



R_{PdN} : Pull-down resistor



Hold Mode

The LC7185 enters hold mode when the $\overline{\text{HOLD}}$ line is asserted. In this mode, the channel preset/recall RAM is not affected.

(1) System status

The LC7185 will remain in hold mode until the $\overline{\text{HOLD}}$ line is deactivated or a reset occurs ($\overline{\text{INIT}}$ line is asserted). The programmable divider, crystal oscillator, and reference divider are all inhibited. Signal output levels are shown below.

PD: High impedance

UL: V_{SS} (ground)

D1, D2: High impedance

BEEP: V_{SS}

K01 to K03: V_{SS}

When the LC7185 leaves hold mode, the previously selected channel is reopened.

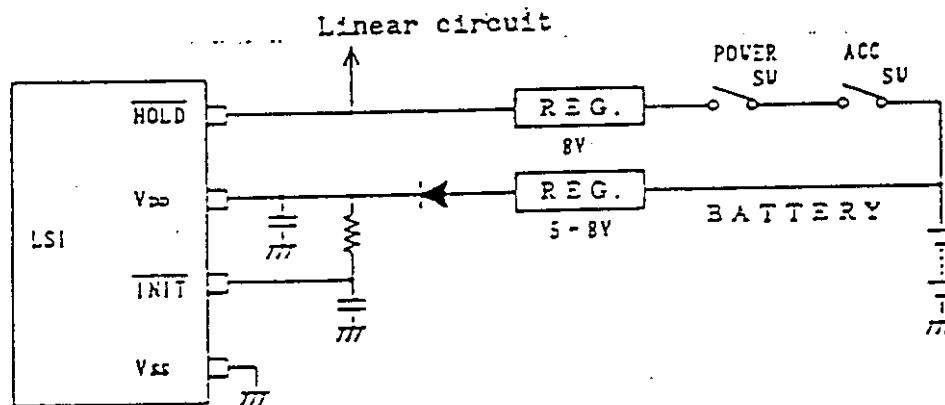
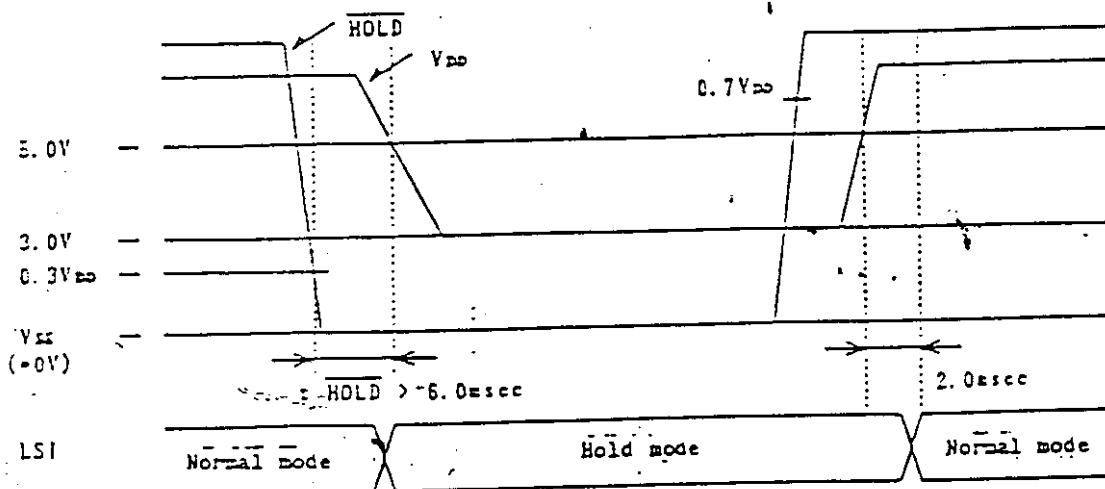
(2) Reset

To reset the chip, assert the $\overline{\text{INIT}}$ line,

Reset state:

. CH9 is selected.

. Preset memory keys are all set to CH33.

**(3) Timing Requirements for Hold Mode**

V_{DD} must remain at 5.0V or higher (crystal oscillator requirement) for 6.0msec (t_{HOLD}) after the HOLD line is asserted ($HOLD < 0.3V_{DD}$). After this V_{DD} may go as low as 3.0V.

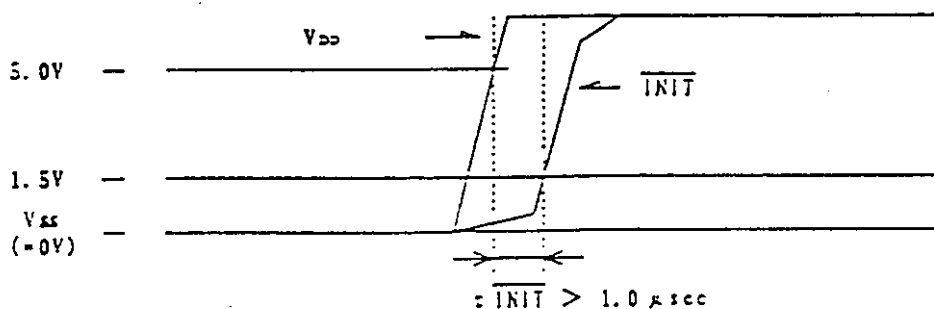
There are no constraints on timing when the chip is leaving hold mode.

The signals can be activated in one of two orders.

- 1) If HOLD is already deactivated ($> 0.7V_{DD}$), the LC7185 leaves hold mode within 2.0msec after V_{DD} rises to $> 5.0V$.
- 2) If V_{DD} is $> 5.0V$, the LC7185 enters normal mode within 2.0msec after HOLD is deactivated.

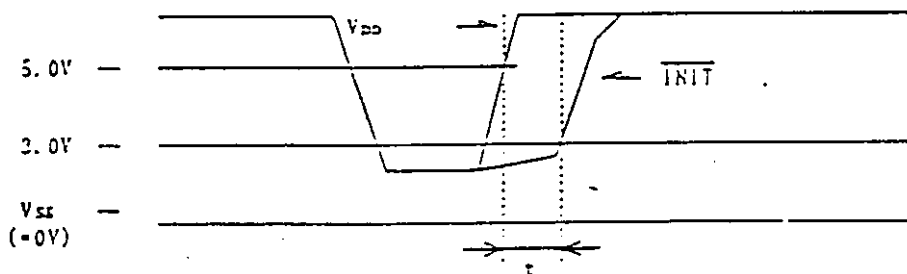
(4) Reset Timing

- 1) Reset timing (e.g. battery replacement)



Note: t_{INIT} should be greater than 1.0μsec.

- 2) Reset caused by a sudden voltage (V_{DD}) drop



Note: If V_{DD} drops momentarily down to less than 3.0V and rises up to more than 5.0V ($t > 1.0\mu\text{sec}$), a reset may be generated.

Frequency Table (U.S.A.; LC7185-8750)

CHANNEL	FREQUENCY (MHz)	RX ($\overline{TX} = 1$)		TX ($\overline{TX} = 0$)	
		N	F v c o	N	F v c o
1	26.965	6508	16.27	5393	13.4825
2	26.975	6512	16.28	5395	13.4875
3	26.985	6516	16.29	5397	13.4925
4	27.005	6524	16.31	5401	13.5025
5	27.015	6528	16.32	5403	13.5075
6	27.025	6532	16.33	5405	13.5125
7	27.035	6536	16.34	5407	13.5175
8	27.055	6544	16.36	5411	13.5275
9	27.065	6548	16.37	5413	13.5325
10	27.075	6552	16.38	5415	13.5375
11	27.085	6556	16.39	5417	13.5425
12	27.105	6564	16.41	5421	13.5525
13	27.115	6568	16.42	5423	13.5575
14	27.125	6572	16.43	5425	13.5625
15	27.135	6576	16.44	5427	13.5675
16	27.155	6584	16.46	5431	13.5775
17	27.165	6588	16.47	5433	13.5825
18	27.175	6592	16.48	5435	13.5875
19	27.185	6596	16.49	5437	13.5925
20	27.205	6604	16.51	5441	13.6025
21	27.215	6608	16.52	5443	13.6075
22	27.225	6612	16.53	5445	13.6125
23	27.255	6624	16.56	5451	13.6275
24	27.235	6616	16.54	5447	13.6175
25	27.245	6620	16.55	5449	13.6225
26	27.265	6628	16.57	5453	13.6325
27	27.275	6632	16.58	5455	13.6375
28	27.285	6636	16.59	5457	13.6425
29	27.295	6640	16.60	5459	13.6475
30	27.305	6644	16.61	5461	13.6525
31	27.315	6648	16.62	5463	13.6575
32	27.325	6652	16.63	5465	13.6625
33	27.335	6656	16.64	5467	13.6675
34	27.345	6660	16.65	5469	13.6725
35	27.355	6664	16.66	5471	13.6775
36	27.365	6668	16.67	5473	13.6825
37	27.375	6672	16.68	5475	13.6875
38	27.385	6676	16.69	5477	13.6925
39	27.395	6680	16.70	5479	13.6975
40	27.405	6684	16.71	5481	13.7025

$$V_{co} (TX) = RF \div 2$$

$$V_{co} (RX) = RF - 10.695 \text{ MHz (IF)}$$

$$CH1: V_{co} (TX) = 26.965 \div 2 = 13.4825$$

$$V_{co} (RX) = 26.965 - 10.695 = 16.27$$

Electrical Characteristics

Absolute maximum ratings at $T_a=25^\circ\text{C}$, $V_{SS}=0\text{V}$

		$V_{SS}=0\text{V}$	min	typ	max	unit
Supply Voltage	$V_{DD\max}$	V_{DD}	-0.3		9.0	V
Input Voltage	$V_{IN(1)\max}$	HOLD, TX	-0.3		15	V
	$V_{IN(2)\max}$	Input pins other than $V_{IN(1)\max}$	-0.3		$V_{DD}+0.3$	V
Output Voltage	$V_{O(1)\max}$	SA, SB, SC, SD, SE, SF, SG, D1, D2	-0.3		15	V
	$V_{O(2)\max}$	UL, BEEP	-0.3		15	V
	$V_{O(3)\max}$	PD	-0.3		$V_{DD}+0.3$	V
	$V_{O(4)\max}$	Output pins other than mentioned above	-0.3		$V_{DD}+0.3$	V
Output Current	$I_{O(1)\max}$	SA, SB, SC, SD, SE, SF, SG	0		30	mA
	$I_{O(2)\max}$	D1, D2			10	mA
	$I_{O(3)\max}$	UL	0		20	mA
	$I_{O(4)\max}$	BEEP	0		10	mA
Allowable Power Dissipation	$P_d\max$	($T_a \leq 85^\circ\text{C}$)			350	mW
Operating Temperature	T_{opg}		-40		+85	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55		+125	$^\circ\text{C}$

Allowable operating conditions at $T_a=-40$ to $+85^\circ\text{C}$, $V_{SS}=0\text{V}$

Supply Voltage	V_{DD}		5.0		8.0	V
"H"-Level Input Voltage	$V_{IH(1)}$	HOLD, TX	$0.7V_{DD}$		12	V
	$V_{IH(2)}$	INIT	3.0		V_{DD}	V
	$V_{IH(3)}$	KI1, KI2, KI3, KI4	$0.6V_{DD}$		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$	HOLD, TX	0		$0.3V_{DD}$	V
	$V_{IL(2)}$	INIT	0		1.5	V
	$V_{IL(3)}$	KI1, KI2, KI3, KI4	0		$0.4V_{DD}$	V
Output Voltage	$V_{OUT(1)}$	SA, SB, SC, SD, SE, SF, SG, D1, D2	0		13	V
	$V_{OUT(2)}$	UL, BEEP	0		8	V
Input Frequency	$f_{IN(1)}$	XIN(sine wave, capacitor coupled)	1.0	10.24	15	MHz
	$f_{IN(2)}$	PIN(sine wave, capacitor coupled)	10		30	MHz
Input Amplitude	$V_{IN(1)}$	XIN(sine wave, capacitor coupled)	0.5		1.5	Vrms
	$V_{IN(2)}$	PIN(sine wave, capacitor coupled)	0.15		1.5	Vrms
Required Oscillating Frequency	X'tal	XIN, XOUT ($C_I \leq 50\text{ohms}$)	5.0	10.24	15	MHz

Electrical characteristics at under allowable operating conditions

Internal Feedback Resistance	$R_f(1)$	XIN		1.0		Mohm
	$R_f(2)$	PIN		500		kohm
Pull-down Resistor	R_{pdN}	KI1, KI2, KI3, KI4, TEST	30	50	70	kohm
"H"-Level Input Current	$I_{IH(1)}$	HOLD, TX $V_I=12\text{V}$			5.0	μA
	$I_{IH(2)}$	INIT $V_I=V_{DD}$			5.0	μA
	$I_{IH(3)}$	XIN $V_I=V_{DD}$			20	μA
	$I_{IH(4)}$	PIN $V_I=V_{DD}$			40	μA

Continued on next page.

Continued from preceding page.

			min	typ	max	unit
"L"-Level Input Current	$I_{IL}(1)$	HOLD, TX, $V_I = V_{SS}$			5.0	μA
	$I_{IL}(2)$	INIT $V_I = V_{SS}$			5.0	μA
	$I_{IL}(3)$	XIN $V_I = V_{SS}$			2.0	μA
	$I_{IL}(4)$	PIN $V_I = V_{SS}$			4.0	μA
"H"-Level Output Voltage	$V_{OH}(1)$	KO1, KO2, K03 $I_O = 1mA$	$V_{DD} - 2.0$	$V_{DD} - 1.0$	$V_{DD} - 0.5$	V
	$V_{OH}(2)$	PD $I_O = 1mA$	$V_{DD} - 1.0$			V
"L"-Level Output Voltage	$V_{OL}(1)$	KO1, KO2, K03 $I_O = 20\mu A$	0.6	1.0	1.4	V
	$V_{OL}(2)$	PD $I_O = 0.5mA$			1.0	V
	$V_{OL}(3)$	BEEP $I_O = 2mA$			1.0	V
	$V_{OL}(4)$	SA, SB, SC, SD, SE, SF, SG $I_O = 20mA$			1.0	V
	$V_{OL}(5)$	D1, D2 $I_O = 5mA$			1.0	V
	$V_{OL}(6)$	UL $I_O = 10mA$			1.0	V
Output Leakage Current	$I_{OFF}(1)$	SA, SB, SC, SD, SE, SF, SG, D1, D2 $V_O = 13V$			5.0	μA
	$I_{OFF}(2)$	UL, BEEP $V_O = 8V$			5.0	μA
	I_{OFFH}	PD $V_O = V_{DD}$		0.01	10.0	nA
"H"-Level Tristate Leakage Current	I_{OFFL}	PD $V_O = V_{SS}$		0.01	10.0	nA
"L"-Level Tristate Leakage Current	$I_{DD}(1)$	Normal mode *1 (PLL operates)		10	15	mA
Supply Current	$I_{DD}(2)$	Hold mode $V_{DD} = 3.0V$			5	μA
		*2 (memory backup) $V_{DD} = 8.0V$			15	μA

*1 $f_{IN}(2) = 20MHz(PIN)$
 $V_{IN}(2) = 0.15V_{rms}$
 $X_{tal} = 10.240MHz$
 $\overline{TX} = \overline{HOLD} = \overline{INIT} = V_{DD}$
 Other inputs = V_{SS}
 Other outputs = open

*2 $\overline{HOLD} = V_{SS}$
 $\overline{TX} = \overline{INIT} = V_{DD}$
 Other inputs = V_{SS}
 Other outputs = open

APPENDIX 10
FINAL RF AMPLIFIER DATA SHEETS

FOUR (4) PAGES FOR KTC2078 FOLLOW THIS SHEET

FINAL RF AMP DATA SHEET
FCC ID: BBOHH37ST

APPENDIX 10

KEC

SA ELECTRONICS CO. LTD.

SEMICONDUCTOR
TECHNICAL DATA**KTC2078**

EPITAXIAL PLANAR NPN TRANSISTOR

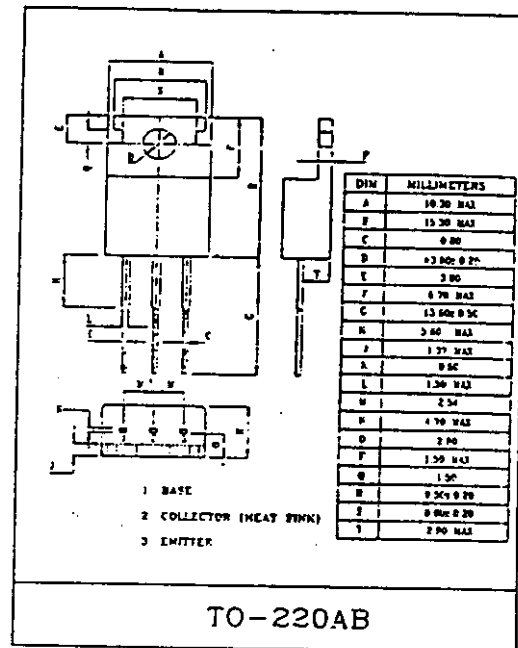
B TRANSCEIVER TX FINAL AMPLIFIER APPLICATION.
F TRANSCEIVER APPLICATION.**FEATURES**Recommended for Output Stage Application of
1M 4W Transmitter.

High Power Gain.

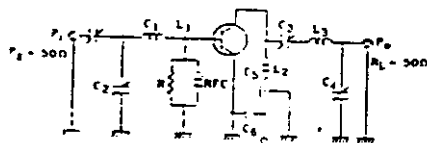
Wide Area of Safe Operation.

MAXIMUM RATINGS($T_a=25^\circ\text{C}$)

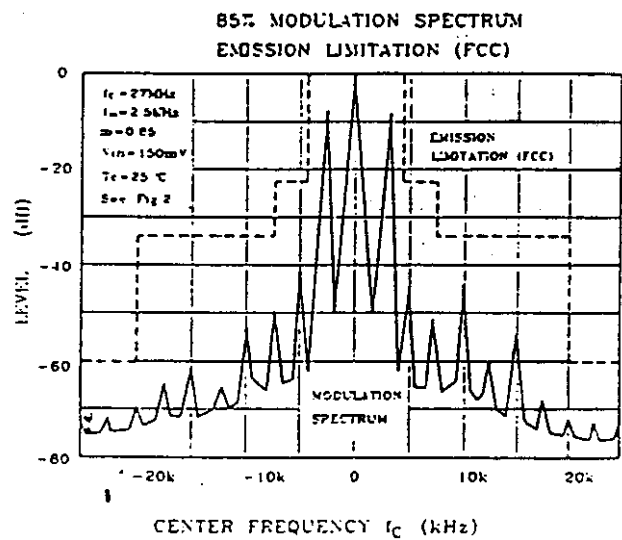
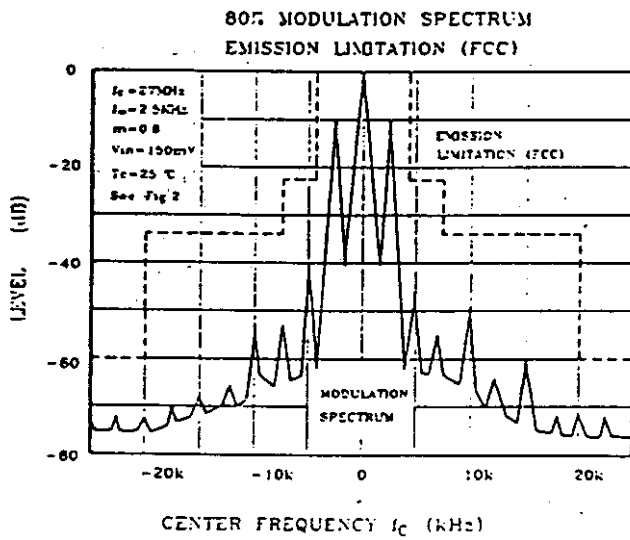
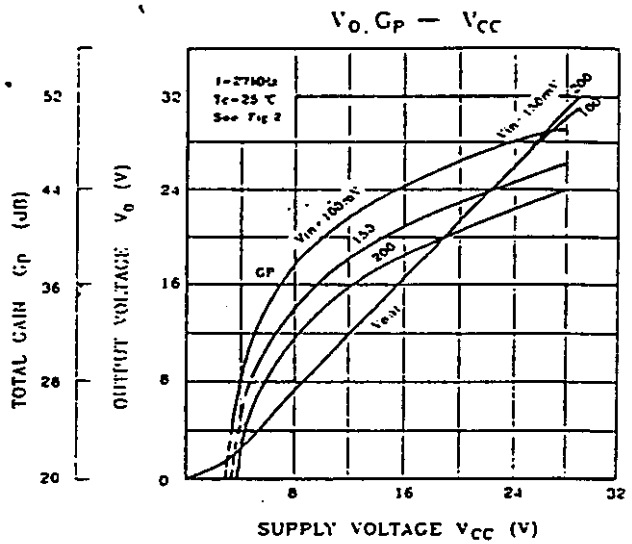
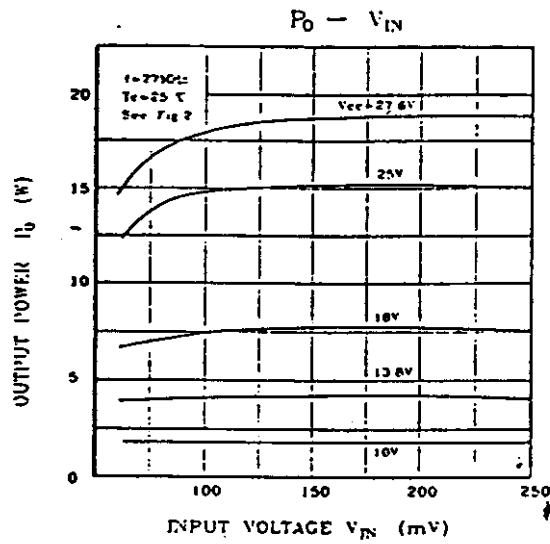
CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CB0}	80	V
Collector-Emitter Voltage ($R_{BE}=50\Omega$)	V_{CE0}	80	V
Emitter-Base Voltage	V_{EB0}	4	V
Collector Current	I_C	4	A
Emitter Current	I_E	-4	A
Collector Power Dissipation ($T_c=25^\circ\text{C}$)	P_C	10	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55-150	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ($T_a=25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	I_{CBO}	$V_{CB}=30V, I_E=0$	-	-	10	μA
Voltage	Collector-Emitter	$V_{(BR)CER}, I_C=10mA, R_{BE}=50\Omega$	80	-	-	V
	Emitter-Base	$V_{(BR)EBO}, I_E=1.0mA, I_C=0$	4	-	-	V
Current Gain	h_{FE}	$V_{CE}=5V, I_C=0.5A$	100	-	200	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=3A, I_B=0.3A$	-	-	1.5	V
Transition Frequency	f_T	$V_{CE}=5V, I_C=500mA$	100	-	-	MHz
Collector Output Capacitance	C_{ob}	$V_{CB}=10V, I_E=0, f=1MHz$	-	40	-	pF
Output Power (Fig.1)	P_o	$V_{CC}=12V, P_i=0.3W, f=27MHz$	4	-	-	W

FIG.1 P_o TEST CIRCUIT

$C_1: \sim 100pF, C_2, C_3: \sim 150pF, C_4: \sim 300pF, C_5: 1000pF$
 $C_6: 0.01\mu F, R: 250\Omega$
 $L_1: 0.8mm \phi \text{ UEW, } 7T, 8mm \text{ I.D. } L_2: 0.8mm \phi \text{ UEW, } 5T, 8mm \text{ I.D.}$
 $L_3: 0.8mm \phi \text{ UEW, } 10T, 8mm \text{ I.D. } RFC: 0.35mm \phi \text{ UEW, } 17T, 5mm \text{ I.D.}$



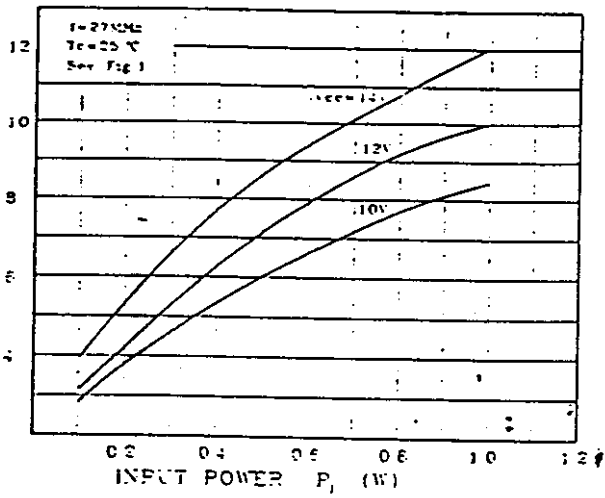
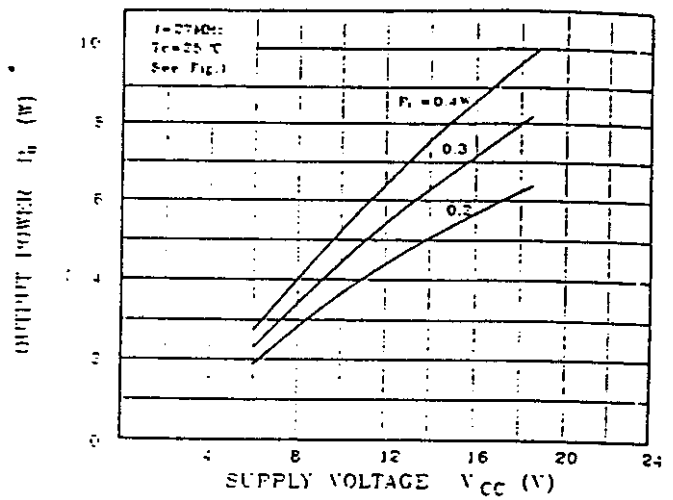
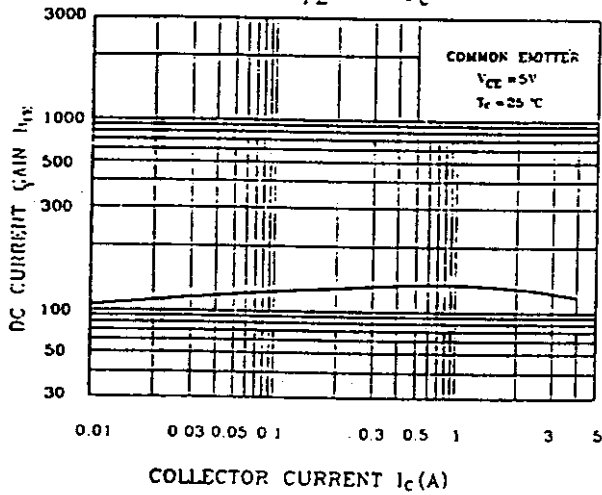
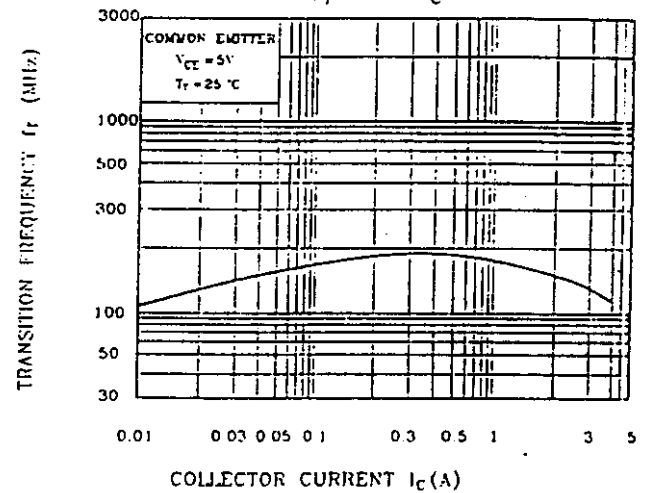
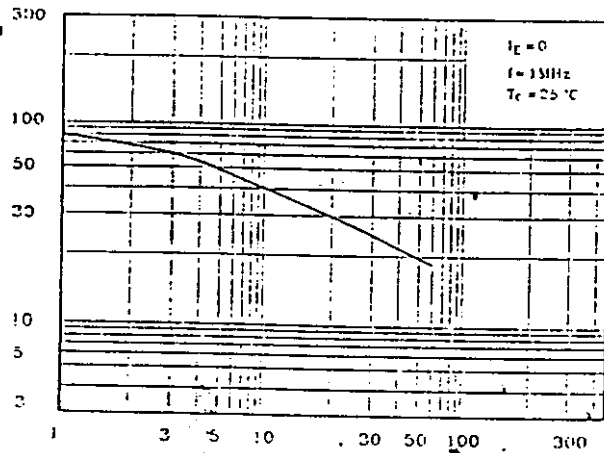
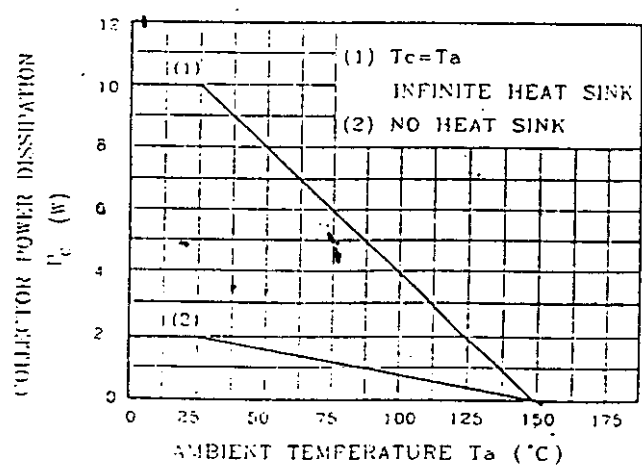
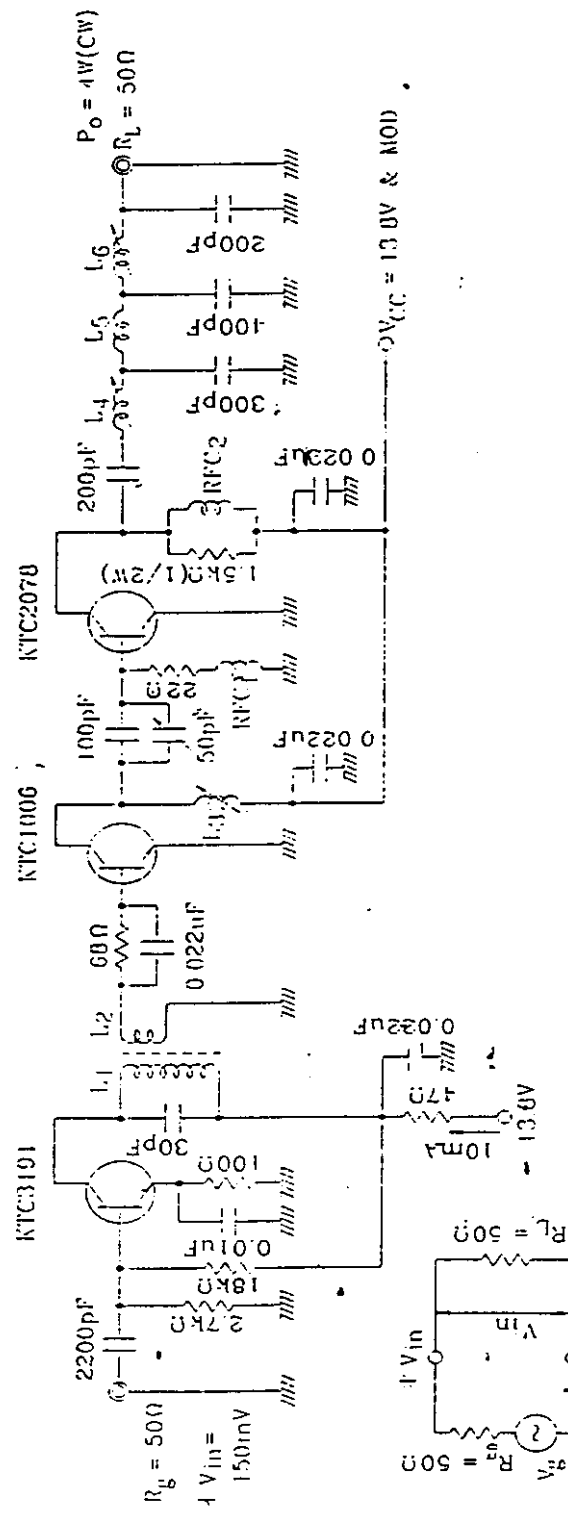
$P_o - P_i$  $P_o - V_{cc}$  $h_{FE} - I_c$  $f_T - I_c$  $C_{ob} - V_{cb}$  $P_c - T_a$ 

Fig.2 27MHz 4W OUTPUT AM TRANSCEIVER CIRCUIT



- L1 : 1.4mm ϕ BOBBIN WITH FERRITE CORE, 0.08mm ϕ UEW, 8 TURNS
 L2 : 1.4mm ϕ BOBBIN WITH FERRITE CORE, 0.08mm ϕ UEW, 2 TURNS
 L3, L6 : 0.6mm ϕ BOBBIN WITH FERRITE CORE, 0.6mm ϕ Sn PLATED COPPER WIRE 6 $\frac{1}{2}$ TURNS
 L4 : 0.6mm ϕ BOBBIN WITH FERRITE CORE, 0.6mm ϕ Sn PLATED COPPER WIRE 8 $\frac{1}{2}$ TURNS
 L5 : 0.6mm ϕ Sn PLATED COPPER WIRE, 6.5mm I.D, 0 $\frac{1}{2}$ TURNS
 RFC1 : 4.7uH, 7BA-400k (TOKO)
 RFC2 : 0.2mm ϕ UEW, 30 TURNS
 RESISTOR : 1/4W CARBON
 CAPACITOR : CERAMIC