*IP*Series

M32150-25 Mobile Radio Product Owner's Manual

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The term “IC”: before the radio certification number only signifies that Industry of Canada technical specifications were met.

Operation is subject to the following two (2) conditions: (1) this devise may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of this device.

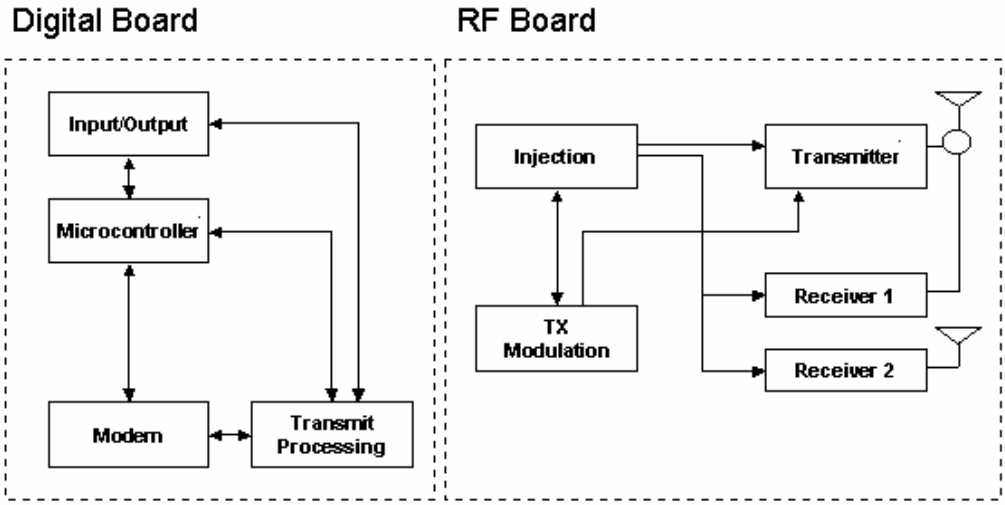
The following U.S. Patents apply to this product:

U.S. Patent numbers 5,640,695,6,018,647,6,243,393

Information contained in this document is subject to change without notice.

TABLE OF CONTENTS

General Block Diagram



General Block Diagram Definitions

For increased data security, the modem supports the Federal Government developed Digital Encryption Standard (DES) data encryption and decryption protocols. This capability requires installation of third party, Internet Protocol (IP) compliant DES encryption and decryption software on the system.

The M32150-25 mobile radio is comprised of two (2) circuit boards, the digital board and the RF board. The digital circuit board contains the following sections:

Input/Output	Circuitry associated with the radio's DB9 data connector providing all the RS232 data and handshake functions, including the necessary level changes.
Microcontroller	Manages the operation of the radio, the modem, and determines which receiver provides a better signal from a given transmission. Also provides transmit time-out protection in the event a fault causes the radio to halt in the transmit mode.
Modem	Converts serial data into an analog audio waveform for transmission and analog audio from the receiver to serial data. Within a single chip it provides forward error detection and correction, bit interleaving for more robust data communications, and third generation collision detection and correction capabilities.
Power Supply	The power supply creates the various voltages required by the digital portion of the mobile radio.

Transmit Processing — Circuitry that amplifies the analog audio signal from the modem and uses it to modulate the voltage controlled oscillator (VCO) and 10 MHz reference oscillator in the injection synthesizer section. Modulating the VCO and reference oscillator simultaneously results in a higher quality FM signal.

The RF circuit board contains the following sections:

Injection Synthesizer — Provides programmable, ultra stable signals for the radio. Synthesizer incorporates phase lock loop technology used for both receiving and transmitting.

Injection — In the receive mode, the synthesizer provides a local oscillator signal of 45 MHz above or below the selected receive channel frequency.

Transmitter — Consists of an exciter and power amplifier module. The transmitter covers the various frequency bands in segments. A different power amplifier module is required for each segment. The transmitter circuitry includes a T/R switch switching the antenna between transmitter and receiver 1 (TX/RX1).

Receiver 1/Receiver 2 — Required to support the mobile DRS; two (2) discrete receivers are tuned to the same channel and use two (2) antennas.

The receivers are double-conversion superheterodyne with a first intermediate frequency (IF) of 45 MHz and a second IF frequency of 455 KHz. Each receiver consists of bandpass filters, an RF amplifier, a MMIC mixer, crystal filters, and a one-chip IF system. The injection synthesizer provides the first local oscillator signal. Outputs from each receiver include RSSI and analog audio for the baseband routing circuitry and modem.

Power Supply — Consists of circuitry that derives the various operating voltages for the RF portion of the mobile radio.

M32150-25 Mobile Radio Section Descriptions

The M32150-25 Mobile Radio works in a frequency 150-170 MHz and requires a 1/4-wavelength antenna.

This section provides detailed descriptions of each of the sections within the M32150-25 Mobile Radio. Refer to Appendix A to view the M32150-25 Mobile Radio Circuit Board Diagram.

Microcontroller

The microcontroller (U30) is a major component of the radio as it manages the operation of the radio. It also controls the operation of the modem, and determines which receiver provides a better signal from a given transmission. It provides transmit time-out protection in the event a fault causes the radio to halt in the transmit mode. It utilizes a reduced instruction set computer (RISC) architecture which provides low power operation and a powerful instruction set. Other features include a watchdog timer, serial universal asynchronous receiver/transmitter (UART), two 8-bit timers, and 2 KB of electrically erasable programmable read only memory (EEPROM) storage.

NOTE: The EEPROM Random Access Memory (RAM) stores the setup data entered by the technician even if there is a loss of power.

Support circuitry

The support circuitry consists of the following:

- A Supervisor Control Chip (U25) provides power-on reset.
- The clock controls microcontroller operation and is generated by crystal Y3 and a Pierce oscillator circuit (inside the U30-microcontroller).
- The latch (U28) decodes low order address bits (A0-A7) from the address/data bits (AD0-AD7). It is controlled by Address Latch Enable (ALE) output of U30 and the bits are used by the modem.
- A 512Kx8 Static RAM Chip (U31) provides temporary storage of the radio's configuration data facilitating the technician with access to make changes.
- Control logic is also an important part in the microcontroller section. The RAM chip select (RAMCS*) and modem chip select (MODEMCS*) command lines are created by U26A, U27BCD, and U44ABC. These gates decode four (4) high order address bits (A11-A15). The RAM is addressed by five (5) memory addresses (MA14-MA18) bits decoded by U26D, U27A, and U24. This logic decodes port address bits (PA14-PA18) to produce memory address bits (MA14-MA18) for the RAM chip.

Input/Output

Input/output components convert serial and handshake data from the modem section to RS232 levels, and vice-versa. Chip U22 is an RS232 transmitter and receiver. It converts data in 5-volt logic form to data in +/-12-volt form, as required by the RS232 standard. A charge pump power supply on the chip converts the +5-volt DC logic power on pin 26 to the +12-volt and –12-volt levels required. Capacitors C106-C109 generate these voltages by a charge pump. These values determine the operating voltages.

Modem

The single-chip modem circuit converts parallel data to an analog audio waveform for transmission and analog audio from a receiver to parallel data. In addition to the modem functions, the chip provides forward error detection and correction (FEC), bit interleaving and Viterbi Soft Decision Algorithms for more robust data communications.

The microcontroller section controls the modem operation. Address bus, address/data bus, and control lines operate the modem chip. The modem circuitry is also run by a crystal-controlled clock, which consists of crystal Y1 and an internal Pierce oscillator.

The received audio signal is demodulated into digital data appearing on the AD0-AD07 lines when the MODEMCS* and RD* lines are low. The data goes to the microcontroller section for futher processing, and then to the input/output section for conversion to RS232 or Ethernet signal levels.

During a transmission, outgoing data appearing on the AD0-AD07 lines is converted into a 4-level FSK analog signal by the modem chip. This operation takes place when the MODEMCS* and WR* lines are low. Data from the user's MDC or VIU passes through the input/output section and microcontroller section to the AD0-AD07 bus. After processing, data passes through a root raised cosine filter and is output to TXMOD.

This modem supports 115.2 KBPS (serial port) and 19.2 KBPS (over-the-air) data transmission rates.

VLogic and Digital Ground

The VLogic and Digital Ground section consists of a pulse-width modulation (PWM) step-down DC-DC converter (U20) that provides an adjustable output. It also reduces noise in sensitive communications applications and minimizes drop out voltage.

An external Schottky diode (D2) is required as an output rectifier to pass inductor current during the second half of each cycle to prevent the slow internal diode of the N-channel MOSFET from turning on. This diode operates in pulse-frequency modulation (PFM) mode and during transition periods while the synchronous rectifier is off.

Receiver 1 Front-End

This section contains components that include several RF Bandpass filters, a low-noise amplifier, and a MMIC mixer.

Incoming signals pass through one (1) pre-selector filter (FLT7) that selectively provides a high degree of out-of-band signal rejection. A low-noise amplifier (U3) amplifies the selected signals and is followed by an image and noise reject filter (FLT8). The output from FLT8 passes through a mixer (U4). U4 is a MMIC mixer which mixes the receive injection (RXINJ1) signal from the synthesizer and the RF signal from the antenna to produce a 45 MHz IF signal. This 45 MHz signal passes through crystal filters (FLT3 and FLT4) to the Receiver 1 IF section to provide the bulk of the Receiver's selectivity.

Receiver 2 Front-End operates identical to Receiver 1 Front-End.

Receiver 1 IF

The major contributor of the IF subsystem (U33) a complete 45 MHz superheterodyne receiver chip incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps.

Incoming 45 MHz signals appearing at RX1_45MHz pass through the low-voltage high performance monolithic FM IF system. Within U33, the signals pass through a simple LC filter and are boosted by the RF amplifier. The output of the RF amplifier drives a mixer. A crystal oscillator is controlled by crystal Y4 and provides the injection frequency for the mixer. The mixer output passes through a 455 KHz ceramic filter (FL6). It is then amplified and passed through another ceramic filter (FL5) to a second gain stage. The IF output drives a quadrature detector. The phase shift elements for the detector are C123 and FL5. The RSSI detector converts the AGC voltage generated inside the chip into a DC level corresponding logarithmically to the signal strength. The Diversity Reception Controller uses BRSSI1 to select the receiver with the best quality signal.

The audio is amplified by an op amp (U19C) and delivered to the power and analog ground circuitry via the RXMOD1 output. High frequency de-emphasis is provided by a filter consisting of a resistor and a capacitor. In order to match the audio signal levels with the other circuitry, a gain control is included. A pot (R81) is necessary to adjust gain.

Receiver 2 IF operates identical to Receiver 1 IF.

Transmit Modulation

The analog circuitry in this section modulates the Transmitter. The data-bearing audio signal from the modem appears at TXMOD. The audio is amplified by op amp (U9D). The output of U9D drives two (2) amplifiers (U9B and U9C).

The transmitter uses dual-point modulation meaning the modulation is applied both to the VCO as well as the reference oscillator (VCTCXO).

The upper amplifier (U9C) has adjustable gain. The output drives op amp (U9A), which inverts the phase of the signal. Upon the start of a transmission, the modulating signal passes through to the VCTCXO reference oscillator in the synthesizer. Some makes of VCTCXO oscillators do not require the modulation signal to be inverted and a jumper block (JMP1) is provided to accommodate the oscillators.

The lower op amp (U9B) amplifies the signal from the low pass filter and applies it to the VCO via the VCOMOD output. Pot RV2 and RV5 are used to adjust maximum deviation.

Injection Synthesizer

Two dual fractional synthesizer chips (U5 and U6) are the major contributor of the receiver and transmitter injection oscillators. This device contains the key components of a phase locked loop (PLL), including a prescaler, programmable divider, and phase detector. The selected frequencies are loaded into U38 as a clocked serial bit stream via the PLL_DATA, PLL_CLOCK, and PLL_ENABLE signals.

Frequency stability is determined by a temperature-compensated crystal oscillator module (VCTCXO) (Y5) at a frequency stability of 1 PPM from –30C to +60C. This device has an input (REFMOD) that accepts transmit modulation and voltage from a RX FREQ ADJUST pot. The pot allows the receiver to be fine-tuned to the exact operating frequency.

Two (2) voltage control oscillators (VCO) are formed by integrated low-noise oscillators with buffered outputs (VCO1 and U40) and associated circuitry. The VCO's generate receiver and transmit injection signals. The output of U40 is split by a two-way power divider (U41) leading to outputs RXINJ1 and RXINJ2. A second output of U40 is returned to the synthesizer FIN input via RXFB. This completes the loop signal path.

Transmitter/TR Switch

The transmitter section consists of a driver amplifier (U11) and a final power amplifier (U35). To transmit, PA12V line is powered up. This causes power amplifier (U35) to boost the RF power to the desired level. Up to 60 watts are available from the transmitter. Harmonic suppression is provided by C82, C83, and L11.

Power and Analog Ground

These sections consist of the power supplies and transmit control circuitry. Power from the vehicle's battery appears at VBATT. Diode D1 protects the voltage regulators by clamping any transient spikes on the supply line. Such spikes typically occur while the engine is started. The supply line powers a series of voltage regulators and the transmitter control circuitry, as follows:

- Voltage regulator U46 provides 8-volt power for most other sections in the radio.
- Voltage regulator U21 powers the transmit driver and T/R switch diodes as controlled by the microcontroller.
- Voltage regulators VR1 and VR2 provide low noise 3.3-volt and 5.0-volt sources for the radio electronics.

In the transmit control circuitry, to transmit, the microcontroller makes TXKEYOUT* high. Forcing the P-channel device to conduct, applying 12-volts via PA12V to the transmitter power amplifier bias pins.

Equipment List

The following table lists the equipment required to perform the M32150-25 Mobile Radio Factory Test Procedure:

QTY	DESCRIPTION	MANUFACTURER	MODEL
2	PC's One for Mobile One for Base	Windows 9X w/ *IP*Message AVR	
1	Service Monitor – Communication Test Set	HP	HP8920B or equivalent
1	Digital multi-meter	Tektronix Fluke	77 or equivalent
1	DC power supply w/ ammeter, 13.8V, 23 Amps or more	Astron	RM35A
1	4-Channel Scope	Tektronix	TDS 460A
1	M32150-25 Mobile Radio		
1	B32150-25 Calibrated Base Station		
1	Internet Protocol Network Controller (IPNC)		
1	100 watt dummy load/attenuator	Pasternack	PE7021-40 or equivalent
2	UHF Antennas (generic mag mount)		
1	Serial cable DB9M-DB9F connector		IPMN p/n: 156-0245-020
1	IP power cable		IPMN p/n: 502-82017-52
1	3-foot RF jumper cable with type N connectors (generic)		
1	Scope test probe (generic, X1 attenuation)		
1	Ceramic tuning tool		IPMN p/n: 44010006
1 ea	#0, #1, and #2 Phillips screwdrivers (generic)		

Programming and Configuring Mobile Radio

Once the appropriate equipment for performing the factory test are gathered, perform the following steps to program and configure an M32150-25 Mobile Radio:

Step 1 Enter the following information on the ***Test Data Sheet (see Appendix B)***:
- Radio Serial number
- Date test being performed
- Tester's Name

Step 2 Program the radio to the current Firmware revision using the AVR programming utility.

Step 3 Connect a PC to the radio and launch the *IP*Message program. In the *IP*Message window, type **`factory default`**, press **[ENTER]**, and the radio displays the radio's default values.

Step 4 Enter the appropriate values for the radio's frequency band.

```
[From: 172.16.64.1] Host serial = 115200,N,8,1, timeout=200
[From: 172.16.64.1] Channel = 0
[From: 172.16.64.1]          Channel      Tx freq      Rx freq      Inj freq
[From: 172.16.64.1] Frequency= 0, 1##.000000, 1##.000000, 1##.000000
[From: 172.16.64.1] IP Address = 172.16.64.1 (VIU = 0.0.0.0, PC = 192.168.3.5)
[From: 172.16.64.1] IPNC = 172.16.112.200
[From: 172.16.64.1] netmask = 255.255.255.0
[From: 172.16.64.1] Radio Mac Address = 00:08:ce:00:00:00
[From: 172.16.64.1] Hosting framing = SLIP no status messages
[From: 172.16.64.1] channel spacing = 25000
[From: 172.16.64.1] Injection = LOW SIDE, 45 MHz
[From: 172.16.64.1] TX Power = 0
[From: 172.16.64.1] Car to car TX power = 0
[From: 172.16.64.1] serial number: undefined
[From: 172.16.64.1] TX quiet time = 5
[From: 172.16.64.1] TX sync time = 2- milliseconds
[From: 172.16.64.1] TX tail time = 5
[From: 172.16.64.1] TX delay = 0 slots
[From: 172.16.64.1] Radio data rate = 19200
[From: 172.16.64.1] Max data tx time = 60 seconds
[From: 172.16.64.1] PLL load to txkey delay = 2 milliseconds
[From: 172.16.64.1] Carrier detect delay time = 6 milliseconds
[From: 172.16.64.1] roam status times = 900 seconds
[From: 172.16.64.1] roam lost time = 60 seconds
[From: 172.16.64.1] Polarity = TX-, RX+
[From: 172.16.64.1] RSSI step = 12 (=234mV)
[From: 172.16.64.1] noise = -126dBm, -126dBm
[From: 172.16.64.1] num timeslots = 16
[From: 172.16.64.1] timeslot period = 992ms
[From: 172.16.64.1] timeslots per voice packet = 4
[From: 172.16.64.1] 06Feb2036 22:28:34 (PST), calibration=43
[From: 172.16.64.1] diversity speed = 5
[From: 172.16.64.1] receiver = 2
[From: 172.16.64.1] Receiver Hysteresis = 2
[From: 172.16.64.1] Internal GPS Port Address = 5000
[From: 172.16.64.1] Internal GPS Input Protocol = TSIP
[From: 172.16.64.1] Internal GPS Output Protocol = TSIP
[From: 172.16.64.1] 12dB SINAD = -120dBm (54 on RX0)
[From: 172.16.64.1] 12dB SINAD = -120dBm (54 on RX1)
[From: 172.16.64.1] 30dB S/N = -106dBm (72 on RX0)
[From: 172.16.64.1] 30dB S/N = -106dBm (72 on RX1)
[From: 172.16.64.1] 40dB S/N = -90dBm (114 on RX0)
[From: 172.16.64.1] 40dB S/N = -90dBm (114 on RX1)
[From: 172.16.64.1] –40dBm = (214) on RX0)
[From: 172.16.64.1] –40dBm = (214) on RX1)
[From: 172.16.64.1] PLL counter: 510.000000 MHz, N = 22200, R = 800 (400x2)
[From: 172.16.64.1] Suspend Tx = 0 seconds
[From: 172.16.64.1] DHCP Client disabled
[From: 172.16.64.1] DHCP Server disabled
[From: 172.16.64.1] diag message level = 0
[From: 172.16.64.1] TFTP options = 512 (block size), 0 (interval)
[From: 172.16.64.1] Internal GPS not found
[From: 172.16.64.1] Modem FEC = on
```

Adjustment / Alignment Procedures

Receiver Injection

Perform the following steps to adjust the receiver injection and injection frequency:

Step 1 While monitoring the receiver injection frequency at RXINJ1, adjust potentiometer **R81** for minimum frequency error of +/- 100Hz. Record this value on the ***Test Data Sheet***.

Step 2 While monitoring the 44.545 MHz 2nd injection frequency at U34 pin 4, adjust trimmer capacitor CV4 for the maximum amplitude of this injection frequency. The maximum amplitude must be between -3 to -5 dBm. Record this value on the ***Test Data Sheet***.

Receiver 1

Perform the following steps to adjust receiver 1:

Step1 Inject an on-frequency carrier signal with an amplitude of -80 dBm, modulated with a 1 kHz test tone at +/- 5.0 kHz deviation into receiver 1's antenna port.

Step 2 While monitoring the voltage at RSSI1 Test Point with a DMM, adjust trimmer capacitor CV1 to midway between the points where the oscillation stops.

Step 3 While monitoring the DC level of the recovered modulation, adjust potentiometer R82 for a reading of 2.500 VDC +/- 1 mV DC.

Step 4 While monitoring the amplitude of the recovered audio signal, adjust potentiometer R81 and R82 for a reading of 350 mV RMS and 2.500 VDC.

Step 5 Steps 3 and 4 are interactive adjustments, therefore repeat steps 3 and 4 until further adjustment is no longer required (i.e. when 350 mV RMS and 2.500 VDC are realized).

Step 6 While monitoring the recovered audio signal at TP1, verify the distortion is less than 3%, adjust CV1 if necessary to achieve less than 3% distortion. Record this value on the ***Test Data Sheet***.

Step 7 While monitoring the recovered audio signal at TP1, verify the SINAD is -118 dBm or better. Record this value on the ***Test Data Sheet***.

Receiver 2

Perform the following steps to adjust receiver 2:

Step 1 Inject an on-frequency carrier signal with an amplitude of -80 dBm, modulated with a 1 kHz test tone at +/- 5.0 kHz deviation into Receiver 2's antenna port.

Step 2 While monitoring the voltage at RSSI2 Test Point with a DMM, adjust trimmer capacitor CV4 to midway between the points where the oscillation stops.

Step 3 While monitoring the DC level of the recovered modulation, adjust potentiometer R99 for a reading of 350 mV (+/-10 mV) RMS.

Step 4 While monitoring the amplitude of the recovered audio signal, adjust potentiometer R93 for a reading of 2.500 (+/-10 mV) VDC.

Step 5 Steps 3 and 4 are interactive adjustments, therefore repeat steps 3 and 4 until further adjustment is no longer required (i.e. when 350 mV RMS and 2.500 VDC are realized).

Step 6 While monitoring the recovered audio signal at TP1, verify the distortion is less than 3%, adjust CV4 if necessary to achieve less than 3% distortion. Record this value on the ***Test Data Sheet***.

Step 7 While monitoring the recovered audio signal at TP1, verify the SINAD is -118 dBm or better. Record this value on the ***Test Data Sheet***.

Transmit Data

Perform the following steps to adjust transmit data:

Step 1 Use *IP*Message to set the transmit power to 0.

Step 2 Using the **x=2000,n** command of *IP*Message to generate transmit data messages while observing the transmitted signal on the HP RF communications test set, adjust pot RV4 for minimum frequency error while transmitting data messages.

Step 3 Turn potentiometer RV5 fully counterclockwise.

Step 4 Adjust RV2 for deviation of 4.9 kHz.

Step 5 Using calibrated base station, and monitoring the uplink received data quality on the base station's Hyperterminal screen, slowly turn RV5 clockwise until consistent data quality readings of 240 - 248 are achieved using 2000 character test messages. Data quality reading should not be less than 240 for 2000 character messages.

If unable to reach the data quality readings then ask for Technical Support. Poor data quality readings are indicative of poor group delay performance, or other defect.

Step 6 Verify transmit deviation, frequency error, and transmitting data messages quality and record this data on the ***Test Data Sheet***.

Power Setting

Perform the following steps to adjust the transmit power control:

Step 1 Attach a power attenuator to the transmit port of the radio.

Step 2 Using the **x=2000,n** command of *IP*Message, and while monitoring the transmit power level on the HP communications test set, check the level of the transmit power. Using *IP*Message set the power setting to **txpower=0**. The radio should have an output power level of approximately 1 mW. Record this value on the ***Test Data Sheet***.

Step 3 Using *IP*Message send the **txpower=** command to increase the power level settings until 60 Watts of output power is obtained. Record this value on the ***Test Data Sheet***. Note that values on the table are to plot the codes vs. power output. The 60-Watt setting can be a code not on the table. Adjust **txpower** until the code is found that does not exceed 60.0 Watts. Record this value on the ***Test Data Sheet***.

Do not to exceed 60 Watts of output power, as this may reduce the life of the amplifier.

Receive Data

Perform the following steps to verify the receive data performance:

Step 1 Using the DOS **ping** command on the PC connected to the radio, ping the network controller to generate uplink and downlink data messages. The following command will generate one Hundred 500 character messages:

```
>;Ping 192.168.3.3 -n 100 -l 500
```

Step 2 Observe the data quality readings on the *IP*Message window of the PC connected to the radio using the **V** (for Verbose) command in the *IP*Message program. With the mobile radio's antenna connected to receiver 1, verify the received data quality readings are consistently 248s. Data quality readings should also be verified at the base station using the **V** command on the Hyperterminal window.

Step 3 Verify receiver 2 data quality readings are also consistently 240 to 248s by changing the antenna from receiver 1 port to receiver 2 port. In this manner both uplink and downlink data quality can be verified. Record this data on the ***Test Data Sheet***.

Final Test

A final test **must** be performed prior to shipping the M32150-25 mobile radio to the customer. This final test will verify that the timing characteristics are correct and that both transmit and receive data quality readings are consistently high.

Perform the following steps for the final test:

Step 1 Attach the 40dB 100-Watt power attenuator to the transmit port of the radio.

Step 2 Program the radio for full power operation. The **tx power** level setting can be found in the radio's ***Test Data Sheet***.

The setting must not to exceed 60 Watts.

Step 3 Attach a digital scope to the base station as described in section the next section, ***Uplink Hardware Timing Verification***. Using the **x=2000,19** command (which will cause the radio to transmit 19 2000 character messages), verify the following:

Transmit frequency of radio is adjusted for minimum frequency error of +/- 100 Hz.

The **x=2000,19** command will generate different messages with differing DC components. Each message will slightly slew the frequency off from the center frequency). Be careful to closely monitor the variation in transmit frequency due to these different messages and ensure that on average the transit frequency error has been minimized to within +/-100 Hz. This indicates that some of these test messages will be slightly high in frequency, some messages will be slightly low in frequency, and some messages will be right on frequency.

Step 4 Verify the transmit deviation is 4.9 kHz

Step 5 Verify the timing characteristics are identical to the plots in the next section, ***Uplink Hardware Timing Verification***.

Step 6 At the base station monitor PC, verify that all the data quality readings are 240 and higher.

Step 7 Move the scope probes to monitor the timing at the mobile radio as described in ***Downlink Hardware Timing Verification***. Generate test messages by pinging the IPNC from the PC attached to the radio. The following command will cause 100 pings, 500 bytes in length to be transmitted from the mobile radio and echoed by the IPNC through the base station:

```
.>;Ping 192.168.3.3 -n 100 -l 500 -w 2000
```

Step 8 Set **CRC =1 Enable** on the radio

Step 9 Verify the timing characteristics are identical to those in ***Downlink Hardware Timing Verification***.

Step 10 Verify that both receivers on the mobile radio report data quality readings of 240 or higher (248 is typical). This can be accomplished by installing the antenna on the TX/RX1 port and verifying RX1 is selected by observing the RX1 LED on the mobile radio and installing the antenna on the RX2 port and verifying RX2 is selected by observing the RX2 LED on the mobile radio.

Step 11 Reset **CRC = 0 Disable** on the radio

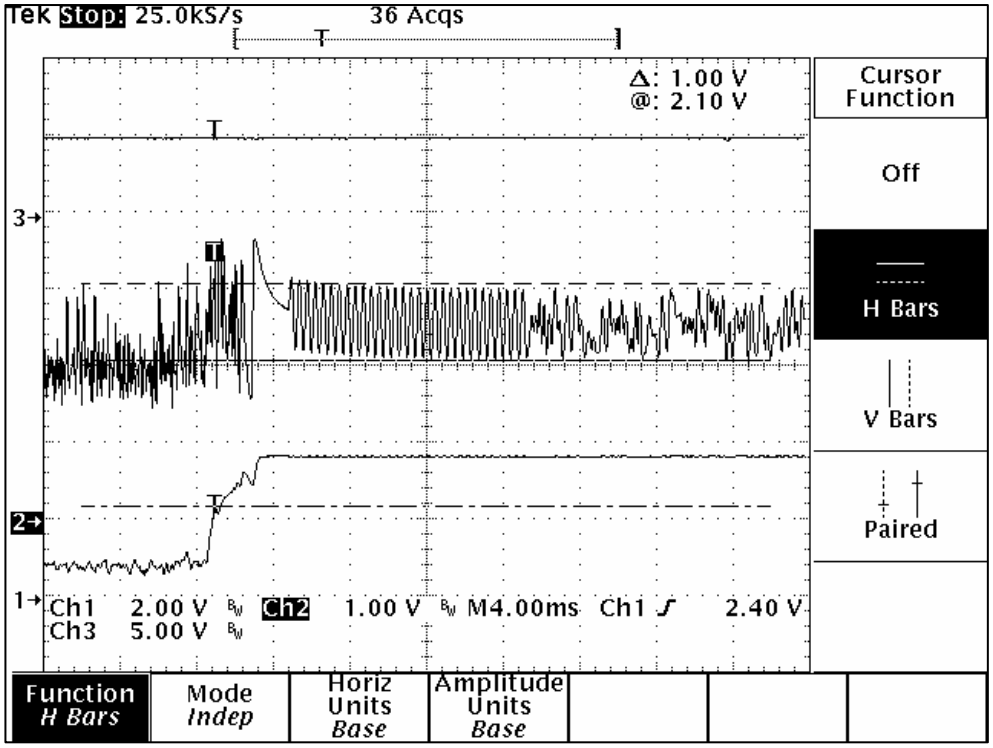
Step 12 In *IP*Message, type the **?** command to radio. Copy the radio settings and paste them into the ***Test Data File***.

Step 13 Perform a close visual inspection of the radio closely inspecting manufacturing related problems (loose screws, solder particles, etc.).

Uplink Hardware Timing Verification

Figure 2-1 below displays an oscilloscope plot of an uplink data message from the mobile to the base station. Channel 1 is connected to the base station's RSSI (XXX-12), channel 2 is connected to the base station's recovered modulation, and channel 3 is connected to the base station's modem chip select line. The scopes acquisition mode is high-resolution.

Figure 2-1: Oscilloscope Plot of an Uplink Data Message

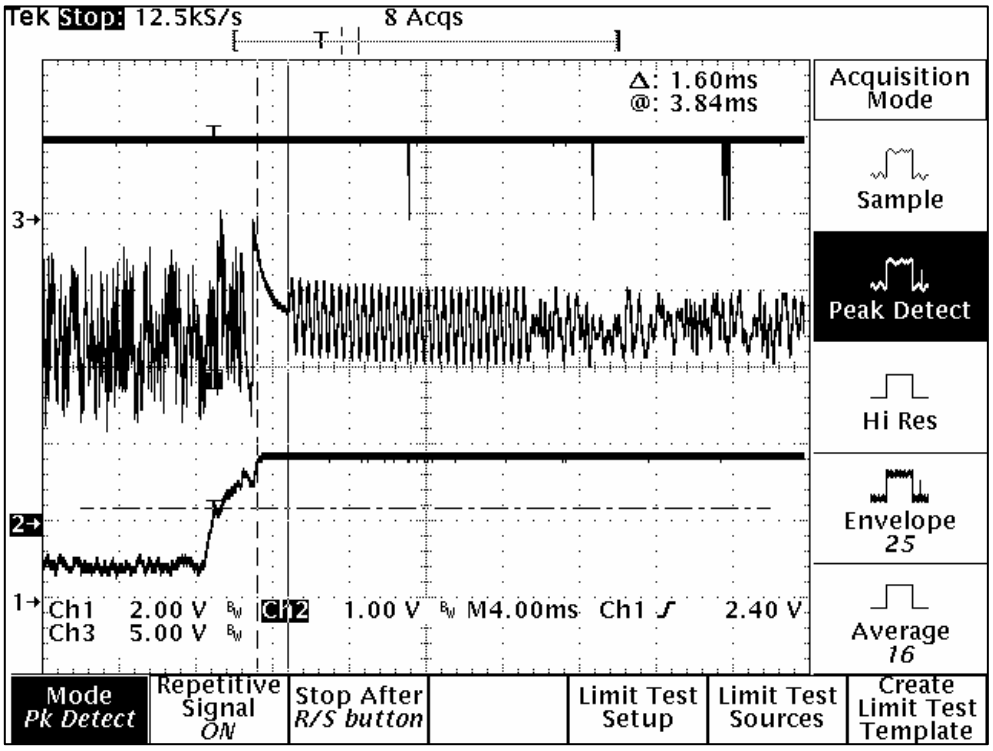


As seen in the above plot, the mobile radio's transmit carrier has ramped up to full power (channel 1) in just a few milliseconds. The recovered modulation (channel 2) is stable by this time. There follows a few milliseconds of quiet time followed by 12 milliseconds of symbol sync time.

The recovered modulation from a mobile radio should look identical to this plot. The recovered modulation signal should be approximately 1.0 Volts peak-to-peak and should be centered at approximately 2.5 VDC as is indicated in the figure above.

Figure 2-2 displays another oscilloscope plot of an up-link data message from the mobile to the base station. As in the last plot, channel 1 is connected to the base station's RSSI (J5-12), channel 2 is connected to the base station's recovered modulation test point, and channel 3 is connected to the base station's modem chip select line (U16-13). The scope's acquisition mode is now in the peak detect mode. This enables the base station's modem CS (Chip Select) line to be viewed.

Figure 2-2: Another Oscilloscope Plot of an Uplink Data Message



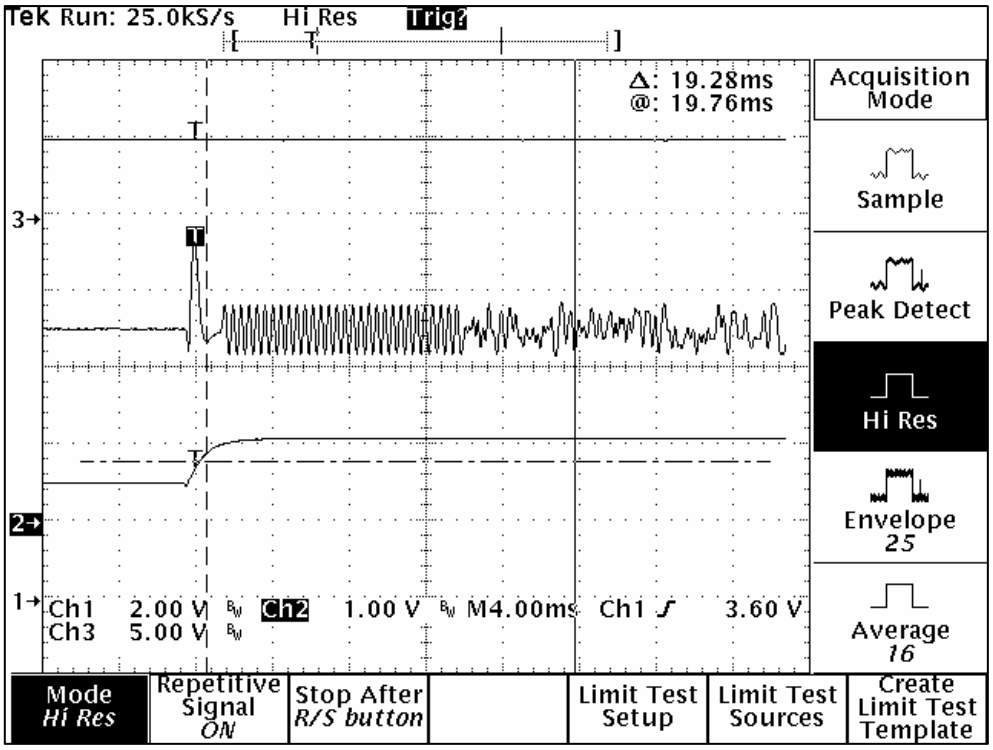
The base station's microcontroller, upon detecting a step response in the RSSI (caused by the mobile radio's transmitter coming up to power), waits a period of time equal to the programmed value of the base station's carrier detect delay time. The microcontroller then instructs the modem to search for the modem synchronization preamble. When the base station instructs the modem to look for sync tones, the modem's CS line transitions low. This can be seen in the above plot. Approximately 10 milliseconds after the mobile radio's transmitter causes a step increase in the base station's RSSI, the CS signal goes low momentarily. As can be seen, the sync tones are stable by this time and the modem quickly establishes synchronization.

Downlink Hardware Timing Verification

Figure 2-3 displays a plot of the downlink timing characteristics. Channel 1 is connected to RSSI, channel 2 is connected to recovered audio, and channel 3 is connected to the modem CS pin. The scope is in the high-resolution acquisition mode.

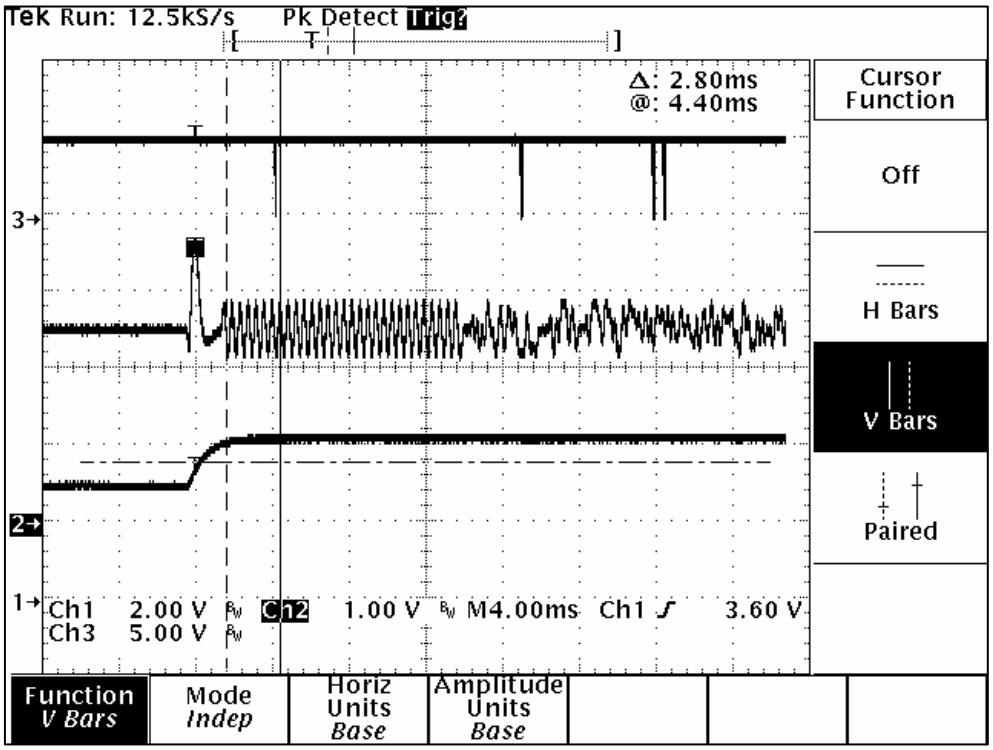
There is a very short period of quiet time (no modulation) followed by approximately 12 milliseconds of modem synchronization time (sync time).

Figure 2-3: Downlink Timing Characteristics Plot



The plot in Figure 2-4 is the same as before but now the scope is in the peak detect acquisition mode. After the mobile radio detects a step response in the RSSI (caused by a down-link transmission), the radio's microcontroller waits an amount of time equal to the programmed value of the "carrier detect delay time" then instructs the modem to look for frame sync. When the microcontroller instructs the modem to look for frame sync, it asserts the modem's CS line (active low). In this plot, the modem's CS line can be seen to transition low approximately 3 milliseconds after the base station's transmitter has come up to full power.

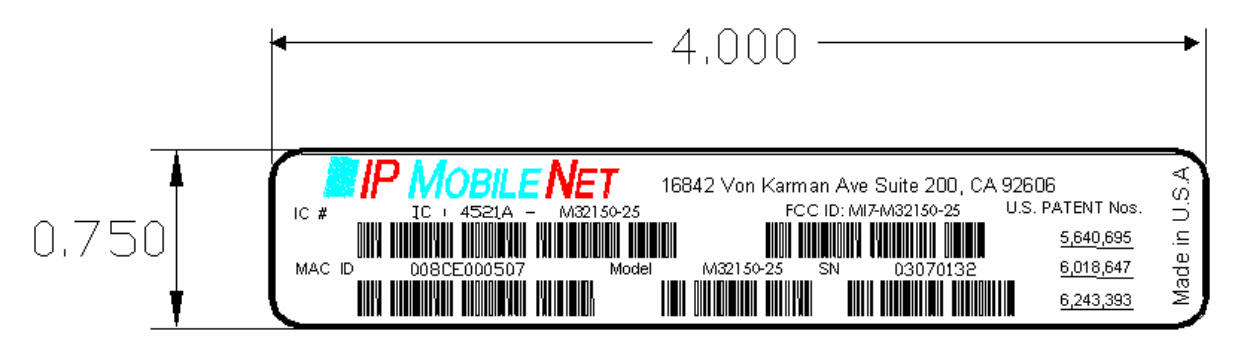
Figure 2-4: Downlink Timing Characteristics Plot in Peak Detect Acquisition Mode



The recovered modulation should be centered at approximately 2.5 VDC and should have an amplitude of approximately 800 mV peal-to-peak as indicated in the plot above.

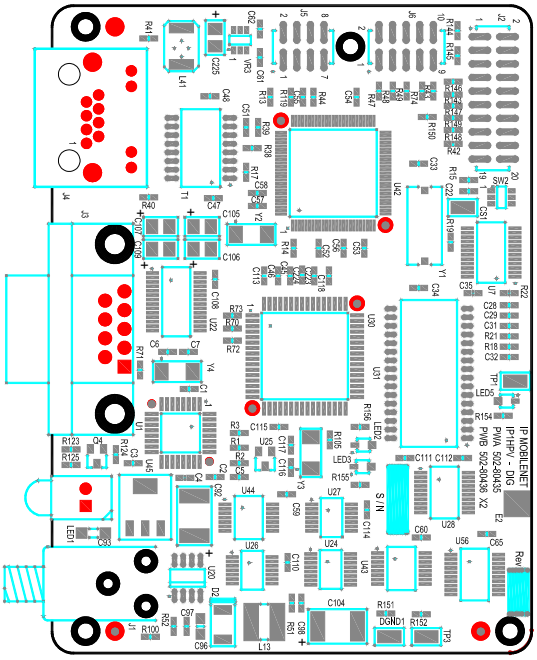
M32150-25 Mobile Radio FCC Label Placement

M32150-25 Mobile Radio FCC Label

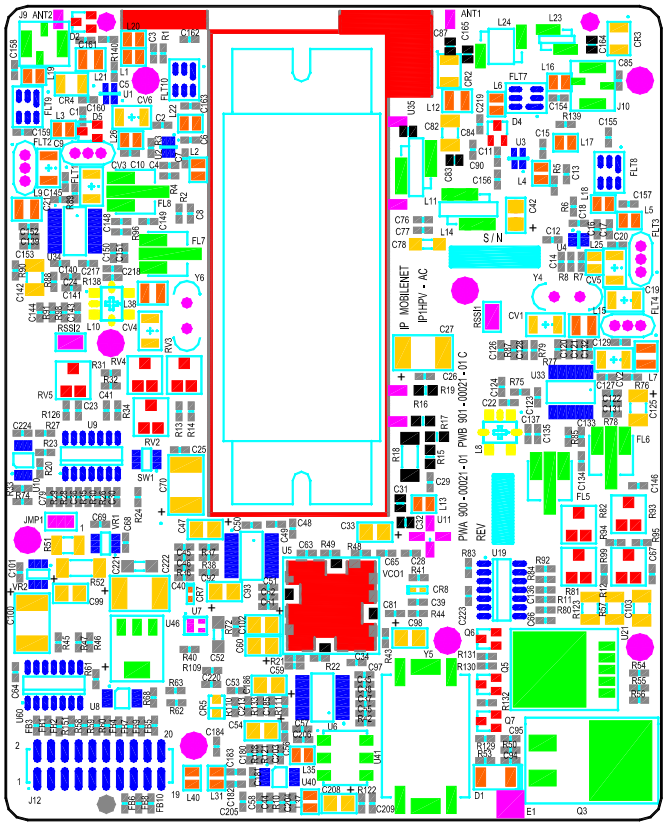


APPENDIX A: CIRCUIT BOARD DIAGRAMS

M32150-25 Mobile Radio Digital Circuit Board



M32150-25 Mobile Radio RF Circuit Board



Program and Configure Radio

Date _____

Serial Number _____

Firmware Revision _____

Tester _____

Adjustment / Alignment Procedures

Receiver Injection

Parameter	**Spec**	**Measured**
Injection Frequency Error at RXINJ1(within +/- 100 Hz of exact injection frequency)	**+/- 100 Hz**	
U34 pin 4 power level	**-3 to -5 dBm**	

Receiver 1& 2

Parameter	**Spec**	**Receiver 1 Measured**	**Receiver 2 Measured**
Audio DC Amplitude (1 kHz Test tone @ 5.0 kHz Deviation)	**2.5 VDC +/- 1mV**		
Audio AC Amplitude (1 kHz Test tone @ 5.0 kHz Deviation)	**350 mVRMS +/- 1mV**		
Distortion (1 kHz Test tone @ 5.0 kHz Deviation)	**3%<**		
SINAD 12 dB (1 kHz Test tone @ 5.0 kHz Deviation)	**-118dBm >**		

APPENDIX B: IPM1 TEST DATA SHEET

Transmit Section

Parameter	Spec	Measured
Transmit Modulation Deviation (4.9 kHz while transmitting 2000 character test message)	**4.9 kHz**	
Transmit Data Quality (While transmitting 2000 character test messages to the base station)	**240 >**	
Transmit Frequency Error (Transmitting 2000 character test message)	**+/- 100Hz**	

Transmit Power Control

Caution: Do not to exceed 40-Watts RF output power during this test.

Transmit Power Setting	Expected RF Out	RF Out Watts
0	~ 1mW	
25		
50		
75		
100		
125		
150		
175		
200		
225		
250		

Parameter	Digital Code	Measure
Maximum power output setting without exceeding 60.0Watts		

Data Quality

Parameter	Spec	Measured
Receiver 1 Data Quality (While receiving 500 character "pings" from base station, 100 pings min, no errors allowed, CRC errors enabled)	**240>**	
Receiver 2 Data Quality (While receiving 500 character "pings" from base station, 100 pings min, no errors allowed, CRC errors enabled)	**240>**	

Final Tests

Uplink Final

Parameter	Spec	Measured
Transmit Frequency Error	**+/- 100 Hz** (Transmitting 19, 2000 character test message)	
Transmit Modulation Deviation	**4.9 kHz** (while transmitting 19,2000 character test message)	
Uplink Hardware Timing Verified		
Transmit Carrier ramp up time	**2mS < X < 4mS**	
Symbol Sync time (Stable Amplitude to with in 100mV during the period)	**12ms +/- 1ms**	
Recovered modulation signal	**1 V PtoP ~**	
	2.5 VDC ~	
Verify Sync Start (RSSI to CS first going low)	**10mS +/- 0.5**	
Verify Fram Sync (From end of Sync to CS second time going low)	**4 +/- 0.1 mS**	
Transmit Data Quality (While transmitting 19, 2000 character test messages to the base station)	**240 >**	

Downlink Final

Parameter	Spec	Measured
Downlink Hardware Timing Verification		
Sync start (RSSI to CS first going low)	**3.0 +/- 0.5ms**	
Recovered Modulation Levels	**800 mV~ 2.5VDC~**	
Frame Sync (From end of Sync to CS second time going low)	**3.2 +/- 0.5 mS**	
Receiver 1 Data Quality (While receiving 500 character "pings" from base station, 100 pings min, no errors allowed, CRC errors enabled)	**240>**	
LED Receiver 1	**Lit**	
Receiver 2 Data Quality (While receiving 500 character "pings" from base station, 100 pings min, no errors allowed, CRC errors enabled)	**240>**	
LED Receiver 2	**Lit**	
Attach copy of all firmware settings	**Completed**	
Visual inspection	**Completed**	

Copy Radio Setting below