SNM909 Hardware Design Manual

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Pay attention to the following safety precautions when using or repairing any terminal or mobile phone that contains modules. The user should be informed of the following safety information on the terminal device. Otherwise, Meig will not be responsible for any consequences caused by the user not following these warning actions.

Identification	Claim
	When you are at a hospital or medical facility, observe the restrictions on using your phone. If necessary, please turn off the terminal or mobile phone, otherwise the medical device may malfunction due to radio frequency interference.
	Turn off the wireless terminal or mobile phone before boarding. To prevent interference with the communication system, wireless communication equipment is prohibited on the aircraft. Ignoring the above will violate local laws and may result in a flight accident.
	Do not use mobile terminals or mobile phones in front of flammable gases. Turn off the mobile terminal when you are near an explosion, chemical factory, fuel depot, or gas station. It is dangerous to operate a mobile terminal next to any potentially explosive electrical equipment.
	The mobile terminal receives or transmits radio frequency energy when it is turned on. It can interfere with TV, radio, computer or other electrical equipment.
	Road safety first! Do not use a handheld terminal or mobile phone while driving, please use a hands-free device. Stop before using your handheld terminal or mobile phone.
	GSM mobile terminals operate under RF signals and cellular networks, but are not guaranteed to be connected in all situations. For example, there is no credit or invalid SIM card. When in this situation and need emergency services, remember to use an emergency call. In order to be able to call and receive calls, the mobile terminal must be powered on and in a service area where the mobile signal is strong enough. Emergency calls are not allowed when certain network services or telephony features are in use, such as feature locks, keyboard locks. These functions should be removed before using an emergency call. Some networks require effective SIM card support.

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Foreword

Thank you for using the SNM909 module from Meg Smart. This product can provide data communication services. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

The company does not assume responsibility for property damage or personal injury caused by improper operation of the user. Users are requested to develop the corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety issues that mobile products should focus on.

Before the announcement, the company has the right to modify the contents of this manual according to the needs of technological development.

目录

Revision History

Date	Revision	Description	Author
2022/11/05	1.00	First version	Hardware

1 Introduction

This document describes the hardware application interface of the module, including the connection of the circuit and the RF interface. It can help users quickly understand the interface definition, electrical performance, and structural dimensions of the module. Combining this document with other application documents, users can quickly use modules to design mobile communication applications.

2 Module overview

SNM909 core board, the main chip is Qualcomm Snapdragon 600 series SDM660, the CPU is made of 14nm FinFET, built-in 64bit ARM, 8-core Kryo 260 CPU (Kryo Gold: quad high-performance cores targeting 2.2 GHz, Kryo Silver: quad low-power cores targeting 1.843 GHz). 2.2G processor, support LPDDR4/4X SDRAM memory. The support card memory is 128GB+4GB.

SNM909 provides high-speed broadband data access while providing WiFi, BT functions; Products support double 1600W 3D Camera or depth of field photography, can be widely used in police law enforcement instrument, intelligent POS cash register, logistics terminal, VR Camera, intelligent robot, video surveillance, security monitoring, vehicle equipment, intelligent information acquisition equipment, intelligent handheld terminals, drones and other products.

The physical interface of the module is a 653 pin pad, which provides the following hardware interfaces:

- 2 sets of 1.8V UART serial ports, supporting four or two wires
- LCD interface (MIPI interface)
- LCD backlight interface
- Camera interface (MIPI interface)
- flash interface
- High speed USB interface
- analog audio input interface
- Digital MIC interface
- Audio output interface
- GPIO interface
- I2C interface
- Indicates the SPI interface
- TF card interface
- Supports WiFi and Bluetooth 5.x functions.

2.1 Summary of features

Table 2.1: SNM909 features

Product characteristics	Description	
Platform	Qualcomm SDM660	
CPU	Octa-core Kryo 260 CPU	
GPU	Adreno512;650MHz	
System memory	32GB eMMC + 3GB LPDDR4X 1866Mhz可兼容64GB+4GB,128GB+8GB	
OS	Android 10.0	
Size	40*35*2.89mm	
Wi-Fi	WCN3990:IEEE 802.11b/g/n/a/ac 2.4G&5G	
Bluetooth	BT 5.x	
Display （Main/Sub）	Matrix: FULL HD: 2560*1600 60fps;	
	LCD Size: User defined	
	Interface: 1st LCM：MIPI DSI 4-lane; 2nd LCM：MIPI DSI 4-lane	
Camera (Rear/Front)	Interface:supports 3 sets of 4-Lane CSI interface	
	Camera Pixel:Rear CAM16-16Mp, Dual ISP supports up to 24MP Camera, Front CAM supports up to 16MP.	
	Video decode	4K30 8-bit: H.264/VP8/VP9 4K30 10-bit: HEVC
	Video encode	4K30 HEVC/H264/VP8/MPEG4
Input device	Keys (Power_on/off, Home, Reset, Volume +, Volume -)	
	Capacitive TP	
Reset	Support hardware reset	
Application interface	Interface name	Main function description
	VBAT	Module power input 3.5V～4.2V, Nominal value 3.8V
	SDIO *1	TF Card, support up to 128GB
	USB2.0(3.0)	Support OTG USB_BOOT (Forced USB for emergency download)
	BLSP ports	8 ports (BLSP1-8), 4-bits each, multiplexed serial interface functions
	UART*3	BLSP1-2,BLSP7-8&BLSP5 support UART，up to 4 Mbps
	I2C*9	BLSP1-8&LPI_GPIO2-3 support I2C
	SPI(master only)	SPI is only support via BLSP
	ADC*2	Support
	Charge	Support Quick Charge 4.0

	Motor	Support
	GPIO	100 GPIOs
	VCOIN	Real time clock backup battery
	射频接口	2.4G WiFi/BT antenna 5G WIFI- antenna
	Audio	1 main MIC 1 sub MIC 1 hands-free speaker (built-in 0.8W Class D power amplifier) 1 channel stereo headset (with headset MIC) 2 digital MIC signals (can support 4 digital MIC at the same time)

2.2 Block diagram

The following figure lists the main functional parts of the module:

- SDM660 -- Baseband chip
- PM660，PM660L -- Power management chip
- WCN3990-WIFI/BT Two-in-one chip
- Antenna interface
- LCD/CAM-MIPI interface
- EMCP --Memory chip
- AUDIO interface
- Serial ports, SD card interface, SIM interface, I2C interface, etc.

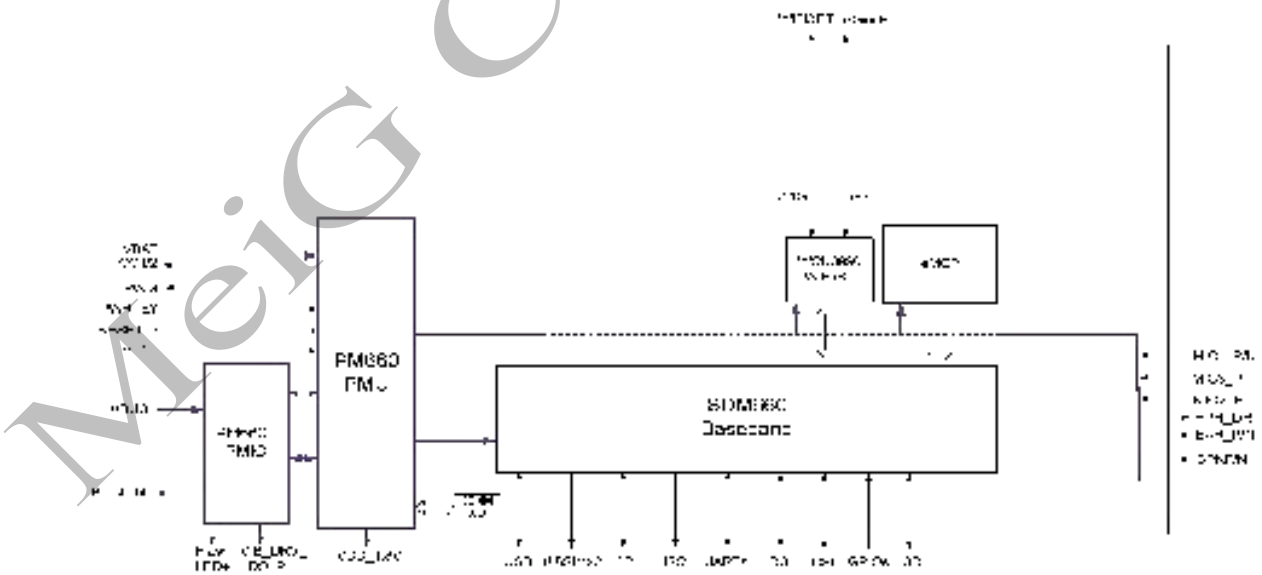

Figure 2.1: Functional block diagram of the module

3 Module Package

3.1 Pin definitions

Table 3.1: Pin description (GPIOs with '*' support INT)

PIN#	SNM_909 Pin name	GPIO Interrupt	Pad characteristics	Functional description
A1	GND		GND	GND
A5	GND		GND	GND
A7	GND		GND	GND
A8-A22	NC		NC	NC
A26	GND		GND	GND
B5	GND		GND	GND
B6	CH0_FEM_QM48858_ ANT_3		AI, AO	WLAN/BT Antenna port 0
B7	GND		GND	GND
B8	NC		NC	NC
B9	WCD_SB_DATA0	LPI_GPIO_20	DO	Module internal used. Do not connect (leave floating).
B10	CC_OUT		AO	1.8V push-pull tri-state output indicating CC1 or CC2 connection (orientation).
B11	USB_ID		AI	OTG mode enable or CC1 pin for the USB Type-C connector (userprogrammable).Requires IEC protection.
B12	BEEP_VOL1	GPIO_2	B	32 kHz clock for WiPower. When WiPower is not used,then this GPIO can be reused for other purpose.
B13	VREG_WLED		AO	WLED boost output
B14	WLED_SINK2		AI	WLED low-side current sink input, string 2
B15-B16	GND		GND	GND
B17	IBATT_SNS_M		AI	Battery minus terminal sense input. Connect this directly to the battery negative node.
B18	VBATT_SNS_P		AI	Battery plus terminal sense input. Connect this directly to the battery positive node.
B19	PM_USB_SNS		AI	USB input voltage sense pin from the external 28 V OVP.
B20	DC_EN		DO	Enable the DC_IN path from the external power multiplexer or external FET control.
B21,B22	USB_VBUS_IN		PI, PO	Input power from the selected source (USB or WiPower), or output during USB-OTG. This is a power entry node for the charger and connects to the OVP circuitry.
C5-C7	GND		GND	GND

C8	WCD_SB_CLK	LPI_GPIO_19		Module internal used. Do not connect (leave floating).
C9	WCD_RESET_N	LPI_GPIO_24		Module internal used. Do not connect (leave floating).
C10	GND		GND	GND
C11	SPKR_DRV_P		AO	Class-D speaker driver output, plus (+)
C12	UUSB_TYPEC_SEL		MV	Used for Type-C and Micro USB select
C13	WLED_SINK3		AI	WLED low-side current sink input, string 3
C14	LCD_BKL_PWM		DI	External dimming control pin PWM input, controls LED brightness.
C15	VREG_L6B_3P3_1		PO	L6B LDO regulated output
C16	VREG_BOB		PO	Regulated BOB output
C17	IBATT_SNS_P		AI	Battery plus terminal sense input. Connect this directly to the battery positive node.
C18	VBATT_SNS_M		AI	Battery voltage sense input minus. Connect to the battery negative remote sense node or connect this directly to the battery negative node.
C19	STAT_CHG		DO	Status/fault/interrupt indicator. Indicates charging, fault status, or enable for parallel charging. Multiplexed static (fault) or pulsed output (IRQ).Programmable polarity
C20	USB_EN		DO	Enable the USB path from the external 28 V OVP.
C21-C22	USB_VBUS_IN		PI, PO	Input power from the selected source (USB or WiPower), or output during USB-OTG. This is a power entry node for the charger and connects to the OVP circuitry.
D5-D7	GND		GND	GND
D8	WCD_SB_DATA1			Do not connect (leave floating). Reserved pin.
D9	WCD_INT1			Do not connect (leave floating). Reserved pin.
D10	GND		GND	GND
D11	SPKR_DRV_M		AO	Class-D speaker driver output, minus (-)
D12	CDC_IN1_P		AI	Microphone input 1, plus
D13	WLED_SINK1		AI	WLED low-side current sink input, string 1
D14	RGB_GRN		AO	RGB LED high-side current source for the green LED
D15	VREG_L6B_3P3_1		PO	L6B LDO regulated output
D16	VREG_BOB		PO	Regulated BOB output

D17	USB_CC2		AI	CC2 pin for the USB Type-C connector.
D18	PMI_HAP_OUT_P		AO	Haptics H-bridge driver output plus
D19	DC_SNS		AI	Voltage sense for DC_IN path
D20	VREG_L18A_2P85		PO	L18A LDO regulated output
D21-D22	USB_VBUS_IN		PI, PO	Input power from the selected source (USB or WiPower),or output during USB-OTG. This is a power entry node for the charger and connects to the OVP circuitry.
DD1	GND		GND	GND
AA5	DP_AUX_EN_N	GPIO_55	B-PD:nppukp	Configurable I/O
AA6	BEEP_EN	GPIO_13	B-PD:nppukp	Configurable I/O
AA7-AA12	GND		GND	GND
AA13	NFC_EN	GPIO_8	B-PD:nppukp	Configurable I/O
AA14	LCD_RST_N	GPIO_53	B-PD:nppukp	Configurable I/O
AA15	MIPI_DSI0_LANE1_N		AI, AO	MIPI display serial interface 0 lane 1– positive
AA16	MIPI_DSI0_LANE1_P		AI, AO	MIPI display serial interface 0 lane 1– negative
AA17-AA22	GND		GND	GND
DD26	GND		GND	GND
BB5	SMB_STAT	GPIO_21	B-PD:nppukp	Configurable I/O
BB6	SPI_CLK_WSA_EN2	GPIO_27	B-PD:nppukp	Configurable I/O
BB7	JTAG_TDO		DO-Z	JTAG data output
BB8	SDC2_CMD		BH-PD: nppukp	Secure digital controller 2 command
BB9	SDC2_DATA_0		BH-PD: nppukp	Secure digital controller 2 data bit 0
BB10	SDC2_DATA_1		BH-PD: nppukp	Secure digital controller 2 data bit 1
BB11	SDC2_CLK		BH-NP: dpukp	Secure digital controller 2 clock
BB12	MIPI_DSI1_LANE3_N		AI, AO	MIPI display serial interface 1 lane 3– negative
BB13	MIPI_DSI1_LANE0_N		AI, AO	MIPI display serial interface 1 lane 0– negative
BB14	MIPI_DSI1_LANE1_N		AI, AO	MIPI display serial interface 1 lane 1– negative
BB15	MIPI_DSI1_LANE2_N		AI, AO	MIPI display serial interface 1 lane 2– negative
BB16	MIPI_DSI1_CLK_N		AO	MIPI display serial interface 1 clock – negative
BB17	USB0_SS_TX_P		AO	USB super-speed 0 transmit – plus
BB18	USB1_SS_RX_M		AI	USB super-speed 1 receive – minus
BB19	USB1_SS_TX_M		AO	USB super-speed 1 transmit – minus

BB20	USB0_SS_RX_M		AI	USB super-speed 0 receive – minus
BB21	USB1_HS_DM		AI, AO	USB high-speed 1 data – minus
BB22	USB1_HS_DP		AI, AO	USB high-speed 1 data – plus
CC5	OTG_OUT_EN	GPIO_113	B-PD:nppukp	Configurable I/O
CC6	LNBBCLK1_EN			Module internal used. Do not connect (leave floating).
CC7	SDM_SWR_CLK	GPIO_24	DO	SoundWire clock
CC8	SDM_SWR_DATA	GPIO_25	B	SoundWire data
CC9	SPI_CS_N_WSA_EN1	GPIO_26	B-PD:nppukp	Configurable I/O
CC10	SDC2_DATA_3		BH-PD: nppukp	Secure digital controller 2 data bit 3
CC11	SDC2_DATA_2		BH-PD: nppukp	Secure digital controller 2 data bit 2
CC12	MIPI_DSI1_LANE3_P		AI, AO	MIPI display serial interface 1 lane 3 – positive
CC13	MIPI_DSI1_LANE0_P		AI, AO	MIPI display serial interface 1 lane 0– positive
CC14	MIPI_DSI1_LANE1_P		AI, AO	MIPI display serial interface 1 lane 1– positive
CC15	MIPI_DSI1_LANE2_P		AI, AO	MIPI display serial interface 1 lane 2– positive
CC16	MIPI_DSI1_CLK_P		AO	MIPI display serial interface 1 clock – positive
CC17	USB0_SS_TX_M		AO	USB super-speed 0 transmit – minus
CC18	USB1_SS_RX_P		AI	USB super-speed 1 receive – plus
CC19	USB1_SS_TX_P		AO	USB super-speed 1 transmit – plus
CC20	USB0_SS_RX_P		AI	USB super-speed 0 receive – plus
CC21	USB2_HS_DM		AI, AO	USB high-speed 2 data – minus
CC22	USB2_HS_DP		AI, AO	USB high-speed 2 data – plus
DD5-DD22	NC		NC	NC
L1	NC		NC	NC
L2-L5	GND		GND	GND
L6	LPI_UART_1_TX		DO	Module internal used. Do not connect (leave floating).
L7	WP_IF		B	Open Drain, single wire (half-duplex) UART between WiPower IC and BT subsystem to exchange WiPower related messages.
L8-L9	GND		GND	GND
M10	GND		GND	GND
L18	GND		GND	GND
L19	PON_OUT			Module internal used. Do not connect (leave floating).
L20	BEEP_VOL2	GPIO_11	L V	Configurable I/O
L21	QNOVO_FET_CTL	GPIO_13	L V	Qnovo FET discharge control

L22	GND		GND	GND
L23	PTT	GPIO_43	B-PD:nppukp	Configurable I/O
L24	MIPI_CSI1_LANE2_P		AI	MIPI CSI 1, differential lane 2 – plus
L25	MIPI_CSI1_LANE2_M		AI	MIPI CSI 1, differential lane 2 – minus
L26	NC		NC	NC
M1	NC		NC	NC
M2-M6	GND		GND	GND
M7	SDM660_GPIO_73	GPIO_73	B-PD:nppukp	Configurable I/O
M8	SCAN_LED_G	GPIO_61	B-PD:nppukp	Configurable I/O
M9,M10	GND		GND	GND
M18	GND		GND	GND
M19	CCI_I2C_SDA0	GPIO_36	B	Dedicated camera control interface I2C 0 serial data
M20	CCI_I2C_SCL0	GPIO_37	B	Dedicated camera control interface I2C 0 clock
M21	CAM_AVDD_EN	GPIO_51	B-PD:nppukp	Configurable I/O
M22	CAM0_MCLK	GPIO_32	DO	Camera master clock 0
M23	RESIN_N		DI	Input pad used for generating reset when held at a logic low.
M24	MIPI_CSI1_LANE3_M		AI	MIPI CSI 1, differential lane 3 – minus
M25	MIPI_CSI1_LANE3_P		AI	MIPI CSI 1, differential lane 3 – plus
M26	NC		NC	NC
N1	NC		NC	NC
N2-N9	GND		GND	GND
N18	GND		GND	GND
N19	LPI_SPI_1_CLK	LPI_GPIO_9	DO	LPI SPI 1 clock
N20	LPI_SPI_1_MISO	LPI_GPIO_11	DI	LPI SPI 1 data master in/slave out
N21	CAM_FR_STANDBY	GPIO_49	B-PD:nppukp	Configurable I/O
N22	CAM1_MCLK	GPIO_33	DO	Camera master clock 1
N23	GND_141		GND	GND
N24	MIPI_CSI1_CLK_P		AI	MIPI CSI 1, differential clock – plus
N25	MIPI_CSI1_CLK_M		AI	MIPI CSI 1, differential clock – minus
N26	NC		NC	NC
O1	NC		NC	NC
O2	GND		GND	GND
O3	BLSP_GPIO_31	GPIO_31	B	BLSP 8 bit 0; SPI, UART, or I2C
O4	BLSP_GPIO_30	GPIO_30	B	BLSP 8 bit 1; SPI, UART, or I2C

O5	BLSP_GPIO_28	GPIO_28	B	BLSP 8 bit 3; SPI, UART, or I2C
O6	GND		GND	GND
O7	SCAN_I2C_SDA	GPIO_22	B	BLSP 6 bit 1; I2C serial data
O8	SCAN_I2C_SCL	GPIO_23	B	BLSP 6 bit 0; I2C serial clock
O9	GND		GND	GND
O18	GND		GND	GND
O19	LPI_I2C_3_SDA	LPI_GPIO_2	B	LPI I2C 3 serial data
O20	LPI_SPI_1_CS1_N	LPI_GPIO_0	DO	LPI SPI 1 chip select 1
O21	GND		GND	GND
O22	CAM0_RST_N	GPIO_46	B-PD:nppukp	Configurable I/O
O23	GND		GND	GND
O24	MIPI_CSI1_LANE0_P		AI	MIPI CSI 1, differential lane 0 – plus
O25	MIPI_CSI1_LANE0_M		AI	MIPI CSI 1, differential lane 0 – minus
O26	NC		NC	NC
P2	RF_TP		AI, AO	For RF test purpose only.Do not connect (leave floating).
P3	GND		GND	GND
P4	BLSP_GPIO_29	GPIO_29	B	BLSP 8 bit 2; SPI or UART
P5-P7	GND		GND	GND
P8	LP4X_MODE			Module internal used. Do not connect (leave floating).
P9	GND		GND	GND
P18	GND		GND	GND
P19	LPI_I2C_3_SCL	LPI_GPIO_3	B	LPI I2C 3 serial clock
P20	LPI_SPI_1_MOSI	LPI_GPIO_10	DO	LPI SPI 1 data master out/slave in
P21	GND		GND	GND
P22	CAM1_RST_N	GPIO_47	B-PD:nppukp	Configurable I/O
P23-P24	GND		GND	GND
P25	SDM660_GPIO_35	GPIO_35	B-PD:nppukp	Configurable I/O
P26	NC		NC	NC
Q1	NC		NC	NC
Q2-Q4	VREG_L13A_1P8		PO	L13A LDO regulated output
Q5-Q9	GND		GND	GND
Q18-Q19	GND		GND	GND
Q20	LPI_SPI_1_CS0_N	LPI_GPIO_8	DO	LPI SPI 1 chip select
Q21-Q24	GND		GND	GND
Q25	BOOT_CONFIG_0	GPIO_96	B-PD:nppukp	Boot configuration control bit 0; Configurable I/O

Q26	NC		NC	NC
R1	NC		NC	NC
R2-R9	GND		GND	GND
R18-R24	GND		GND	GND
R25	PON_RESET_N		DIS	Reset input
R26	NC		NC	NC
S1	NC		NC	NC
S2	GND		GND	GND
S3	TS_KP_I2C_SCL	GPIO_15	DO	Touch Panel I2C Clock
S4	TS_KP_I2C_SDA	GPIO_14	B	Touch Panel I2C Data
S5-S9	GND		GND	GND
S18	GND		GND	GND
S19	LPI_SPI_2_CLK	LPI_GPIO_5	DO	LPI SPI 2 clock
S20-S22	GND		GND	GND
S23	NFC_INT_N	GPIO_40	B-PD:nppukp	Configurable I/O
S24	SCAN_BUTTON_2	GPIO_45	B-PD:nppukp	Configurable I/O
S25	BB_VOLTAGE_DET	GPIO_48	B-PD:nppukp	Configurable I/O
S26	NC		NC	NC
E1-E7	GND		GND	GND
E8	WCD_INT2			Do not connect (leave floating). Reserved pin.
E9	NC		NC	NC
E10	CDC_EAR_M		AO	Earpiece output, minus (-)
E11	CDC_MIC2_P		AI	Microphone input 2
E12	CDC_IN1_M		AI	Microphone input 1,minus
E13	KEY_VOL_UP	PM660L_GPIO_07	MV	Volume up key
E14	RGB_RED		AO	RGB LED high-side current source for the red LED
E15	FLASH_LED1		AO	Flash high-side current source for LED1.
E16	LNBBCLK3		DO	19.2 MHz baseband (low-power) XO clock buffer output
E17	VCONN_EN		DO	Digital output to toggle the external FET gate drive.
E18	VCONN_IN		AI	An external 5 V supply is applied to this pin to support Type-C powered cables.
E19	PMI_HAP_OUT_M		AO	Haptics H-bridge driver output minus
E20	VREG_L15A_UIM1		PO	L15A LDO regulated output
E21-E22	USB_VBUS_IN		PI, PO	Input power from the selected source (USB or WiPower),or output during

				USB-OTG. This is a power entry node for the charger and connects to the OVP circuitry.
E23	VREG_L17A_UIM2		PO	L17A LDO regulated output
E24	BATT_THERM_BIAS		AO	Dedicated voltage source for BATT_THERM resistor network biasing.
E25	UIM1_PRESENT	GPIO_90	DI	UIM1 presence detection
E26	NC		NC	NC
F2	CH1_FEM_QM48858_ANT_3		AI, AO	WLAN/BT Antenna port 1
F3-F8	GND		GND	GND
F9	CDC_MIC_BIAS2		AO	Microphone bias 2
F10	CDC_EAR_P		AO	Earpiece output, plus (+)
F11	CDC_HPH_R		AO	Headphone output, right channel
F12	HEADSET_DETECT		AI	Headset detection
F13	CDC_IN3_P		AI	Microphone input 3
F14	BEEP_PWM	PM660L_GPIO_06	MV	Configurable I/O
F15	FLASH_LED1		AO	Flash high-side current source for LED1.
F16	WIPWR_CHG_OK		DO	Charger request hardware output signal to the WiPower interface. Hi-Z indicates a WiPower charge request. It asserts low to indicate that charging is complete or that WiPower charging is not requested.
F17-F18	GND		GND	GND
F19	PWR_BUTTON		DI	Input pad generally connected to a keypad power-on button and when grounded, initiates the power-on sequence. Pulled up internally to 1.8 V via the dVdd regulator.
F20	USB_IN_MID		AO	Opitional power support for VCONN.
F21-F22	USB_VBUS_IN		PI, PO	Input power from the selected source (USB or WiPower),or output during USB-OTG. This is a power entry node for the charger and connects to the OVP circuitry.
F23	VREG_L11A_1P8		PO	L11A LDO regulated output
F24	UIM1_RESET	GPIO_89	DO	UIM1 reset
F25	VREG_L14A_1P8		PO	L14A LDO regulated output
F26	NC		NC	NC
G1-G8	GND		GND	GND
G9	CDC_MIC_BIAS1		AO	Microphone bias 1
G10	REAR_DVDD_EN	PM660L_GPIO_04	L V	Enable for camera LDO2

G11	HPH_GND_SENSE		AI	Headphone ground reference
G12	FRONT_DVDD_EN		L V	Enable for camera LDO1
G13	GGND_CFILT		GND	Microphone bias filter ground
G14	RGB_BLU		AO	RGB LED high-side current source for the blue LED
G15	FLASH_LED1		AO	Flash high-side current source for LED1.
G16-G17	FLASH_LED3		AO	Flash high-side current source for LED3.
G18	VBATT_PWR		PI, PO	Battery voltage node. Output is for charging, and input is for all other operations.
G19	BOOT_PWR		AO	Auxiliary 4.4 V to 5 V low dropout (LDO) output 50 mA (minimum) output supply.
G20	GND		GND	GND
G21	BATT_ID		AI	Battery ID input to the ADC and MIPI BIF interface. It can be used for missing battery detection.
G22	GND		GND	GND
G23	VREG_L16A_2P7		PO	L16A LDO regulated output
G24	UIM2_PRESENT	GPIO_86	DI	UIM2 presence detection
G25	AUX_THERM		AI	Battery temperature input to the ADC for the remote thermistor.
G26	NC		NC	NC
H1	NC		NC	NC
H2-H8	GND		GND	GND
H9	KEY_VOLUME_DOWN	PM660L_GPIO_08	L V	Configurable I/O
H10	5V_BOOST_EN	PM660L_GPIO_05	L V	Configurable I/O
H11	CDC_HPH_L		AO	Headphone output, left channel
H12	GND		GND	GND
H13	VREG_L3B_3P0_1		PO	L3B LDO regulated output
H14	VPH_PWR		PI, PO	Primary system supply node
H15-H17	FLASH_LED2		AO	Flash high-side current source for LED2.
H18-H20	VBATT_PWR		PI, PO	Battery voltage node. Output is for charging, and input is for all other operations.
H21	QI_PMA_ON		DI	Active-high input indicating when A Qi/PMA wireless input is connected.
H22-H23	GND		GND	GND
H24	BATT_THERM		AI	Battery temperature input to ADC for measuring the pack temperature.
H25	VREG_L12A_1P8		PO	L12A LDO regulated output
H26	NC		NC	NC

I1	NC		NC	NC
I2-I12	GND		GND	GND
I13	VREG_L3B_3P0_1		PO	L3B LDO regulated output
I14-I16	VPH_PWR		PI, PO	Primary system supply node
I17	UIM_BATT_ALARM	GPIO_91	DI	UIM battery alarm
I18-I20	VBATT_PWR		PI, PO	Battery voltage node. Output is for charging, and input is for all other operations.
I21	GND		GND	GND
I22	WCD_LNBBCLK2		DO	19.2 MHz baseband (low-power) XO clock buffer output
I23	GND		GND	GND
I24	BOOT_CONFIG_7	GPIO_94	B-PD:nppukp	Boot configuration control bit 7; Configurable I/O
I25	PM660_GPIO_4	PM660_GPIO_4	MV	Configurable I/O
I26	NC		NC	NC
J1	NC		NC	NC
J2-J9	GND		GND	GND
J10-J12	VREG_L5B_2P95_1		PO	L5B LDO regulated output
J13	VREG_L3B_3P0_1		PO	L3B LDO regulated output
J14-J16	VPH_PWR		PI, PO	Primary system supply node
J17	VREG_L2B_SDC2		PO	L2B LDO regulated output
J18-J20	VBATT_PWR		PI, PO	Battery voltage node. Output is for charging, and input is for all other operations.
J21	KEYPAD_LED_PWM	PM660_GPIO_3	L V	Configurable I/O
J22	GND		GND	GND
J23	TRIGGER_BUTTON	GPIO_44	B-PD:nppukp	Configurable I/O
J24	PS_HOLD		DO	Power-supply hold signal from the SDM660 device's PS_HOLD output to PMIC PM660.
J25	SCAN_POWER_2	GPIO_80	B-PD: nppukp	Configurable I/O
J26	NC		NC	NC
K1	NC		NC	NC
K2-K5	GND		GND	GND
K6	LPI_UART_1_RX		DI	Module internal used. Do not connect (leave floating)
K7-K8	GND		GND	GND
K10-K18	GND		GND	GND

K19	NFC_LNBBCLK3_EN	PM660_GPIO_12	L V	Configurable I/O
K20	VCOIN		AI, AO	Coin-cell battery/capacitor or backup battery charger supply and input.
K21	QUIET_THERM		AI	AMUX input 5 connected with AMUX channel 17;typically used for quier thermistor readings
K22	HOLSTER_DET	GPIO_52	B-PD:nppukp	Configurable I/O
K23	GND		GND	GND
K24	MIPI_CSI1_LANE1_P		AI	MIPI CSI 1, differential lane 1 – plus
K25	MIPI_CSI1_LANE1_M		AI	MIPI CSI 1, differential lane 1 – minus
K26	NC		NC	NC
T1	NC		NC	NC
T2	BB_BOOST_EN	GPIO_59	B-PD:nppukp	Configurable I/O
T3	GND		GND	GND
T4	TS_ANALOG_EN	GPIO_12	B-PD:nppukp	Configurable I/O
T5-T18	GND		GND	GND
T19	UIM2_RESET	GPIO_85	DO	UIM2 reset
T20-T22	GND		GND	GND
T23	CCI_I2C_SCL1	GPIO_39	B	Dedicated camera control interface I2C 1 clock
T24	CCI_I2C_SDA1	GPIO_38	B	Dedicated camera control interface I2C 1 serial data
T25	SDM_HAPT_PWM	GPIO_79		PWM input for haptic control
T26	NC		NC	NC
U1	NC		NC	NC
U2	SCAN_LED_R	GPIO_62	B-PD:nppukp	Configurable I/O
U3	TS_RESET_N	GPIO_66	B-PD: nppukp	Configurable I/O
U4	JTAG_TMS		DI-PU:nppdkp	JTAG mode select input,Do not connect (leave floating)
U5-U8	GND		GND	GND
U9	CAM2_MCLK	GPIO_34	DO	Camera master clock 2
U10	SMB_PWR_BLSP2_I2C_SDA	GPIO_6	B	PM3003A I2C serial data
U11	SMB_PWR_BLSP2_I2C_SCL	GPIO_7	DO	PM3003A I2C serial clock
U12	GND		GND	GND
U13	MIPI_CSI0_LANE0_P		AI	MIPI CSI 0, differential lane 0 – plus
U14	MIPI_CSI0_LANE0_M		AI	MIPI CSI 0, differential lane 0 – minus
U15-U16	GND		GND	GND
U17	NFC_ESE_PWR_REQ	GPIO_20	B-PD: nppukp	Configurable I/O

U18-U22	GND		GND	GND
U23	BOOT_CONFIG_6	GPIO_65	B-PD:nppukp	Boot configuration control bit 6; Configurable I/O
U24	GND		GND	GND
U25	BOOT_CONFIG_2	GPIO_98	B-PD:nppukp	Boot configuration control bit 2; Configurable I/O
U26	NC		NC	NC
V1	NC		NC	NC
V2	I2C_DAT_BATT	GPIO_10	B	Battery I2C serial data
V3	EMERGENCY_INT	GPIO_72	B-PD: nppukp	Configurable I/O
V4	JTAG_SRST_N		DI-PU	JTAG reset for debug,Do not connect (leave floating)
V5-V6	GND		GND	GND
V7	RESOUT_N		DO	Reset output
V8	GND		GND	GND
V9	SCAN_BUTTON_1	GPIO_42	B-PD: nppukp	Configurable I/O
V10	LPI_GPIO_29	LPI_GPIO_29	DI	LPI DMIC 2 data
V11	LPI_GPIO_28	LPI_GPIO_28	DO	LPI DMIC 2 clock
V12	GND		GND	GND
V13	MIPI_CSI0_LANE3_P		AI	MIPI CSI 0, differential lane 3 – plus
V14	MIPI_CSI0_LANE3_M		AI	MIPI CSI 0, differential lane 3 – minus
V15	SD_CARD_DET	GPIO_54	DI	Secure digital card detection
V16	HALL_INT_N	GPIO_75	B-PD: nppukp	Configurable I/O
V17	ESE_BLSP1_SPI_MISO	GPIO_1	DI	BLSP 1 bit 2; SPI master in/slave out
V18	MIPI_CSI2_LANE3_M		AI	MIPI CSI 2, differential lane 3 – minus
V19	MIPI_CSI2_LANE2_P		AI	MIPI CSI 2, differential lane 2 – plus
V20	MIPI_CSI2_LANE1_P		AI	MIPI CSI 2, differential lane 1 – plus
V21	MIPI_CSI2_LANE0_P		AI	MIPI CSI 2, differential lane 0 – plus
V22	MIPI_CSI2_CLK_P		AI	MIPI CSI 2, differential clock – plus
V23	GND		GND	GND
V24	BOOT_CONFIG_10	GPIO_92	B-PD:nppukp Boot	configuration control bit 10; Configurable I/O
V25	BOOT_CONFIG_11	GPIO_93	B-PD:nppukp Boot	configuration control bit 11; Configurable I/O
V26	NC		NC	NC
W1	NC		NC	NC
W2	I2C_CLK_BATT	GPIO_11	B	Battery I2C serial clock
W3	ACCL_GYRO_DRDY_INT	GPIO_68	B-PD: nppukp	Configurable I/O

W4	JTAG_TRST_N		DI-PD: nppukp	JTAG reset,Do not connect (leave floating)
W5-W8	GND		GND	GND
W9	CAM_AFVDD_EN	GPIO_50	B-PD: nppukp	Configurable I/O
W10	LPI_SPI_2_MISO	LPI_GPIO_7	DI	LPI SPI 2 master in/slave o
W11	LPI_GPIO_26	LPI_GPIO_26	DO	LPI DMIC 1 clock
W12	GND		GND	GND
W13	MIPI_CSI0_CLK_P		AI	MIPI CSI 0, differential clock – plus
W14	MIPI_CSI0_CLK_M		AI	MIPI CSI 0, differential clock – minus
W15	MIPI_DSI0_LANE0_P		AI, AO	MIPI display serial interface 0 lane 0– positive
W16	MIPI_DSI0_LANE0_N		AI, AO	MIPI display serial interface 0 lane 0– negative
W17	UIM1_DATA	GPIO_87	B	UIM1 data
W18	MIPI_CSI2_LANE3_P		AI	MIPI CSI 2, differential lane 3 – plus
W19	MIPI_CSI2_LANE2_M		AI	MIPI CSI 2, differential lane 2 – minus
W20	MIPI_CSI2_LANE1_M		AI	MIPI CSI 2, differential lane 1 – minus
W21	MIPI_CSI2_LANE0_M		AI	MIPI CSI 2, differential lane 0 – minus
W22	MIPI_CSI2_CLK_M		AI	MIPI CSI 2, differential clock – minus
W23	GND		GND	GND
W24	UIM2_DATA	GPIO_83	B	UIM2 data
W25	UIM2_CLK	GPIO_84	B	UIM2 clock
W26	NC		NC	NC
X1	NC		NC	NC
X2	TS_INT_N	GPIO_67	B-PD: nppukp	Configurable I/O
X3	MAG_INT_N	GPIO_70	B-PD: nppukp	Configurable I/O
X4	JTAG_TDI		DI-PU:nppdkp	JTAG data input,Do not connect (leave floating)
X5	ESE_BLSP1_SPI_CLK	GPIO_3	DO	BLSP 1 bit 0; SPI clock
X6	ESE_BLSP1_SPI_CS_N	GPIO_2	DO	BLSP 1 bit 1; SPI chip select
X7-X8	GND		GND	GND
X9	LPI_SPI_2_CS_N	LPI_GPIO_4	DO	LPI SPI 2 chip select
X10	LPI_GPIO_17	LPI_GPIO_17	B-PD: nppukp	LPI bit 17
X11	LPI_GPIO_27	LPI_GPIO_27	DI	LPI DMIC 1 data
X12	GND		GND	GND
X13	MIPI_CSI0_LANE2_P		AI	MIPI CSI 0, differential lane 2 – plus
X14	MIPI_CSI0_LANE2_M		AI	MIPI CSI 0, differential lane 2 – minus

X15	MIPI_DSI0_LANE3_P		AI, AO	MIPI display serial interface 0 lane 3– positive
X16	MIPI_DSI0_LANE3_N		AI, AO	MIPI display serial interface 0 lane 3– negative
X17	UIM1_CLK	GPIO_88	B	UIM1 clock
X18	PRESURE_SENSOR_INT	GPIO_74	B-PD: nppukp	Configurable I/O
X19	GND		GND	GND
X20	FORCED_USB_BOOT	GPIO_57	DI	Force USB boot
X21	EDP_AUX_N		AI, AO	DisplayPort auxiliary channel – negative
X22-X25	GND		GND	GND
X26	NC		NC	NC
Y1	NC		NC	NC
Y2	DBG_BLSP2_UART_TX	GPIO_4	DO	Debug Serial UART transmit
Y3	ACCL_GYRO_EVENT_INT	GPIO_69	B-PD: nppukp	Configurable I/O
Y4	JTAG_TCK		DI-PU	JTAG clock input,Do not connect (leave floating)
Y5	BLSP_SPI_CS1_N(8)	GPIO_64	B-PD: nppukp	Configurable I/O
Y6	ESE_BLSP1_SPI_MOSI	GPIO_0	DO	BLSP 1 bit 3; SPI master out/slave in
Y7-Y8	GND		GND	GND
Y9	LPI_SPI_2_MOSI	LPI_GPIO_6	DO	LPI SPI 2 master out/slave in
Y10	LPI_SPI_1_CS2_N	LPI_GPIO_16		LPI SPI 1 chip select 2
Y11	LPI_UART_2_RX	LPI_GPIO_15		LPI UART 2 receive
Y12	GND		GND	GND
Y13	MIPI_CSI0_LANE1_P		AI	MIPI CSI 0, differential lane 1 – plus
Y14	MIPI_CSI0_LANE1_M		AI	MIPI CSI 0, differential lane 1 – minus
Y15	MIPI_DSI0_LANE2_P		AI, AO	MIPI display serial interface 0 lane 2– positive
Y16	MIPI_DSI0_LANE2_N		AI, AO	MIPI display serial interface 0 lane 2– negative
Y17	GND		GND	GND
Y18	KYPD_INT	GPIO_9	B-PD: nppukp	Configurable I/O
Y19-Y20	GND		GND	GND
Y21	EDP_AUX_P		AI, AO	DisplayPort auxiliary channel – positive
Y22-Y24	GND		GND	GND
Y25	BOOT_CONFIG_8	GPIO_95	B-PD:nppukp	Boot configuration control bit 8; Configurable I/O
Y26	NC		NC	NC
Z1	NC		NC	NC

Z2	DBG_BLSP2_UART_RX	GPIO_5	DI	Debug Serial UART receive
Z3	ALPS_INT_N	GPIO_71	B-PD: nppukp	Configurable I/O
Z4	BOOT_CONFIG_3	GPIO_60	B-PD:nppukp	Boot configuration control bit 3; Configurable I/O
Z5	DP_USBC_ORIEN	GPIO_56	B-PD:nppukp	Configurable I/O
Z6	SCAN_POWER_1	GPIO_63	B-PD: nppukp	Configurable I/O
Z7-Z8	GND		GND	GND
Z9	CBL_PWR_N			Alternate input pad, which can be used to initiate the power-on sequence when grounded;pulled up internally to 1.8V via the dVdd regulator.
Z10	GND		GND	GND
Z11	LPI_UART_2_TX	LPI_GPIO_14	DO	LPI UART 2 transmit
Z12	GND		GND	GND
Z13	NFC_DWL_REQ	GPIO_77	B-PD: nppukp	Configurable I/O
Z14	FREE/SPI_CS2_N(8)	GPIO_76	B-PD: nppukp	Configurable I/O
Z15	MIPI_DSI0_CLK_N		AO	MIPI display serial interface 0 clock – negative
Z16	MIPI_DSI0_CLK_P		AO	MIPI display serial interface 0 clock – negative
Z17-Z23	GND		GND	GND
Z24	USB_PHY_PS	GPIO_58	DI	USB PHY port select
Z25	BOOT_CONFIG_1	GPIO_97	B-PD:nppukp	Boot configuration control bit 1; Configurable I/O
Z26	NC		NC	NC

B：Bidirectionaldigital with CMOS input

H：High-voltage tolerant

NP：pdpukp=defaultno-pull with programmable options following the colon (:)

PD：nppukp=defaultpulldown with programmable options following the colon (:)

PU：nppdkp=defaultpullup with programmable options following the colon (:)

KP：nppdpu=defaultkeeper with programmable options following the colon (:)

3.2 Mechanical Dimensions

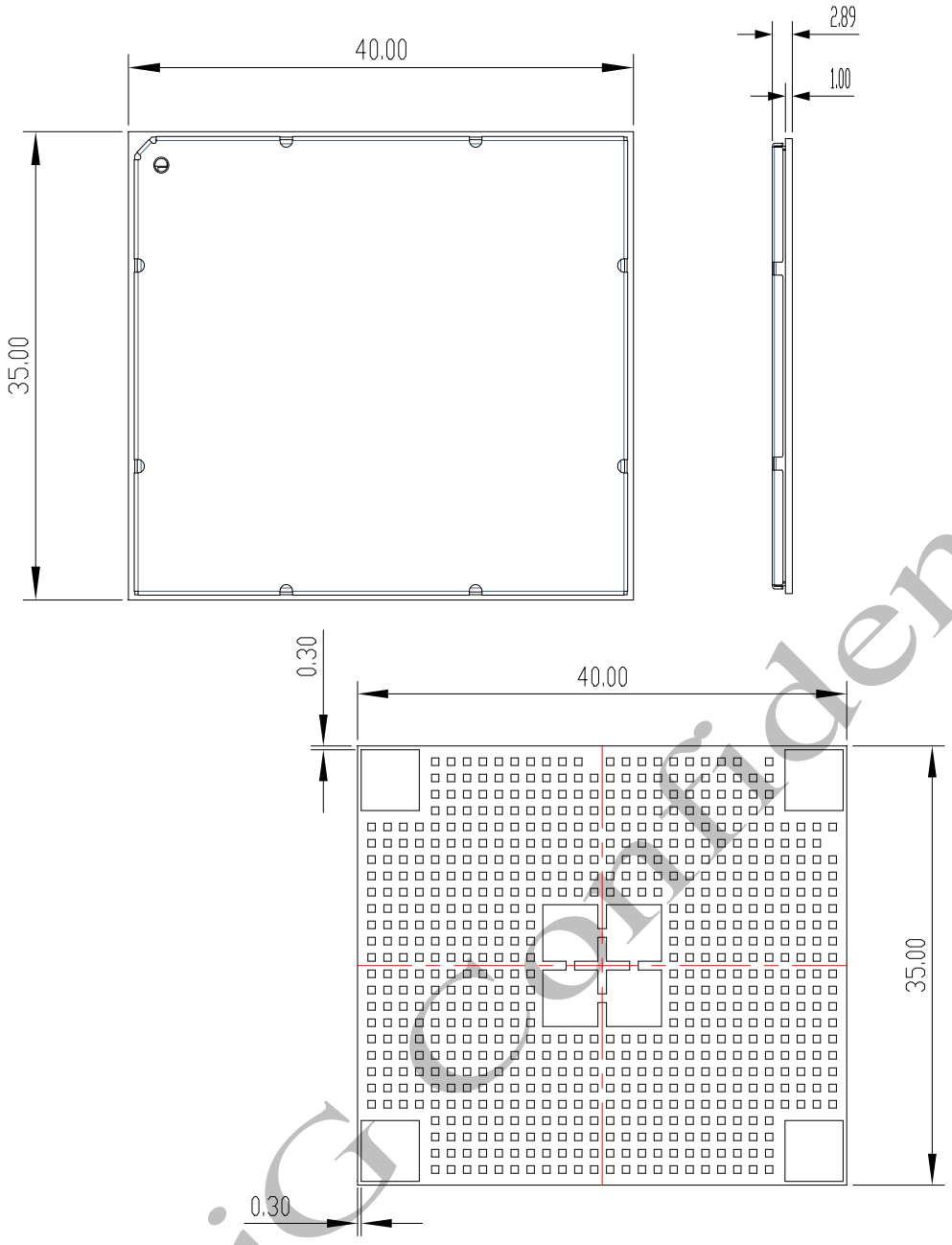

Figure 3.1: Module 3D size (unit: mm)

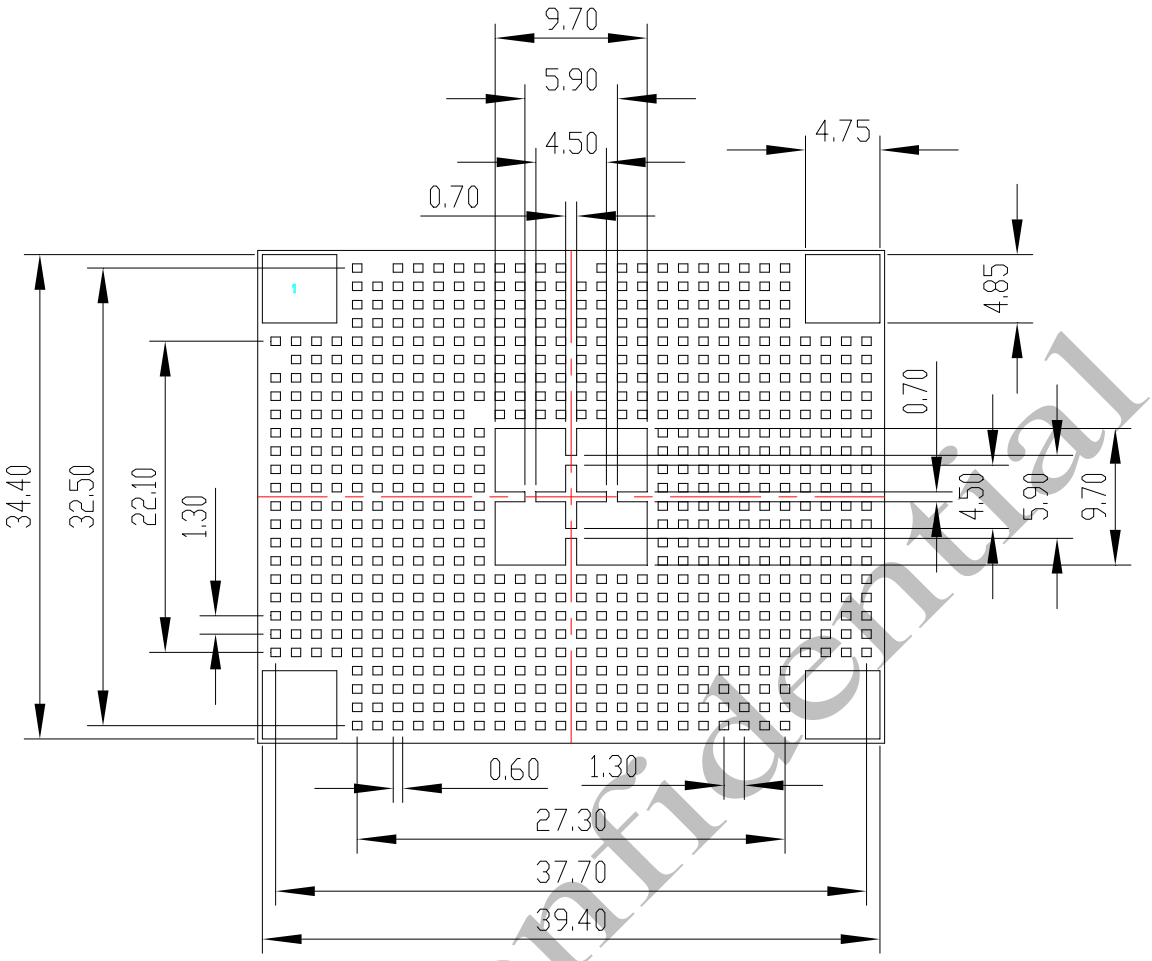

Figure 3.2: Recommended PCB package size (unit: mm)

4 Interface application

4.1 Power Supply

In the case of a battery device, the voltage input range of the module VBAT is 3.5V to 4.2V, and the recommended voltage is 3.8V. In the GSM band, when the module is transmitting at maximum power, the peak current can reach up to 4A, resulting in a large voltage drop on VBAT.

It is recommended to use a large capacitor regulator close to VBAT. It is recommended to use two 47uF ceramic capacitors. Parallel 33PF and 10PF capacitors can effectively remove high frequency interference. To prevent damage to the chip due to ESD and surge, it is recommended to use a suitable TVS tube and a 5.1V/500mW Zener diode at the VBAT pin of the module. For PCB layout, the capacitors and diodes should be as close as possible to the VBAT pin of the module. The user can directly power the module with a 3.8V lithium-ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

In addition, in addition to VBAT, also pay attention to VBATT_SNS_P/M,IBATT_SNS_P/M used to connect the battery power detection PIN, missing or wrong connection may cause the module to fail to start, see the specific circuit reference design.

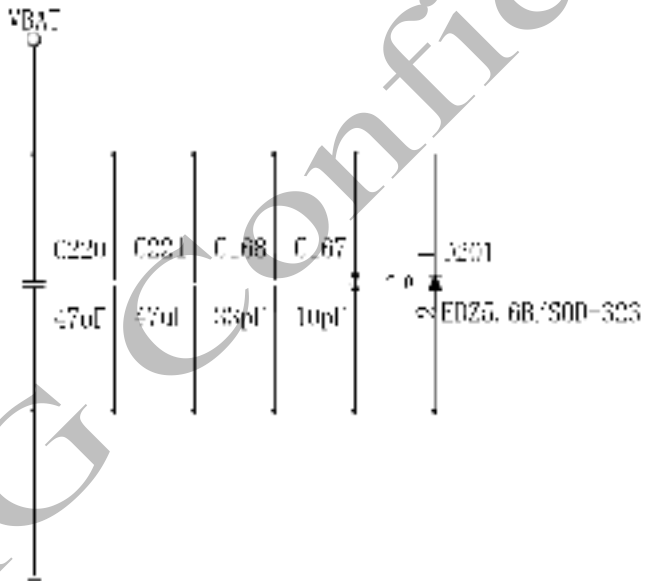

Figure 4.1: VBAT input reference circuit

If it is a DC power supply device, the DC input voltage is 4.5V-17V. The recommended circuit that can be powered by DC-DC is shown below:

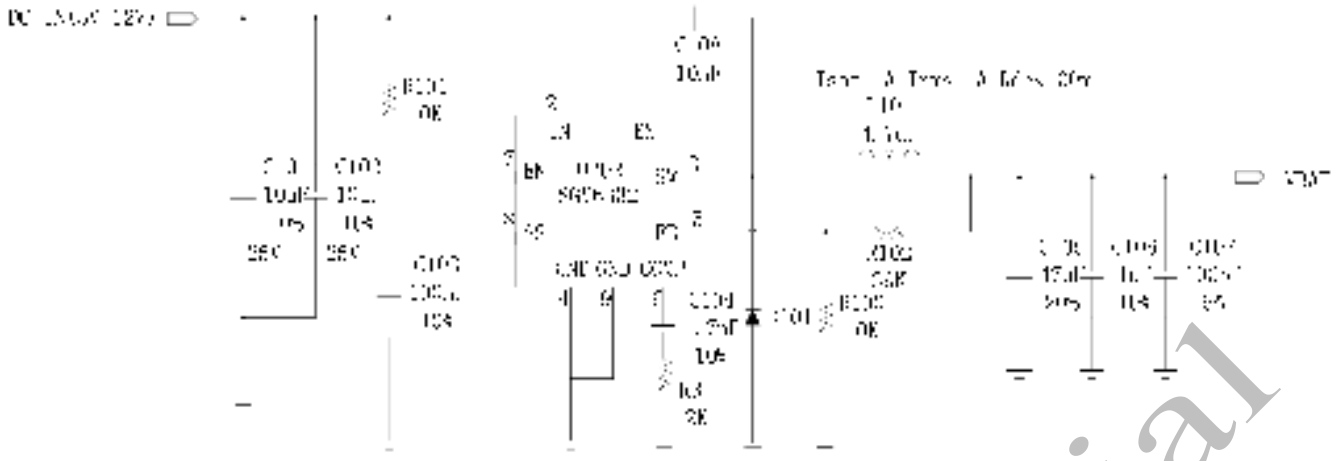

Figure 4.2: DC-DC power supply circuit

Note:If the user does not use battery power supply, please connect a 10K resistor to the H24 pin of the module (BATT_THERM) to GND to prevent the software from determining the abnormal battery temperature after the module is powered on, resulting in shutdown. The connection diagram is as follows:

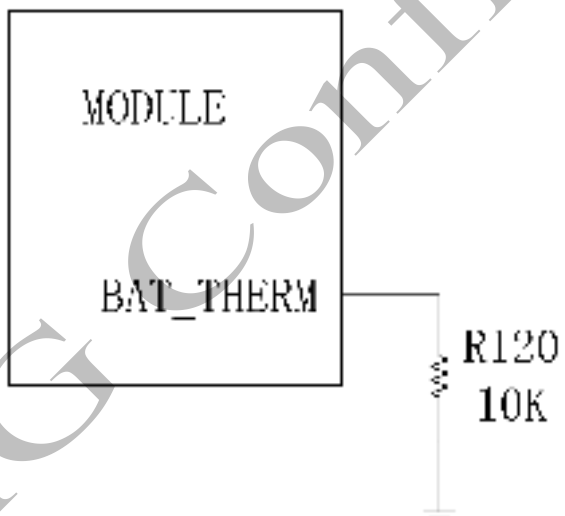

Figure 4.3: Connection diagram when not powered by battery

4.1.1 Power Pin

The VBAT pin (G18、H18、H19、H20、I18、I19、I20、J18、J19、J20) is used for power input. In the user's design, pay special attention to the design of the power supply section to ensure that the VBAT does not fall below 3.5V even when the module consumes 4A. If the voltage drops below 3.5V, the module may shut down. The PCB layout from the VBAT pin to the power supply should be wide enough to reduce the voltage drop in the transmit burst mode.

Figure 4.4: VBAT lowest voltage drop

4.1.2 Power PCB layout

Power routing should not only consider the VBAT, but also the return GND of the power supply. The line of the VBAT positive electrode must be short and thick, and the line must first pass through the large capacitor, Zener diode and then to the power supply PIN of the module. There are several pads exposed to copper at the bottom of the module. Ensure that the GND path from these exposed areas to the power supply is the shortest and most unobtainable. This ensures that the current path of the entire power supply is shortest and the interference is minimal.

4.2 Power on and off

Do not turn on the module when the module's temperature and voltage limits are exceeded. In extreme cases, such operations can cause permanent damage to the module.

4.2.1.模块开机

The user can power on the module by pulling the PWRKEY pin (F19) low. The pull-down time is at least 3 seconds. This pin has been pulled up to 1.8V in the module. The recommended circuit is as follows; or the CBL_PWR_N pin (Z9) is pulled low. CBL_PWR_N can be powered on by 10K pull-down resistor to GND. It does not need to release this signal after booting.

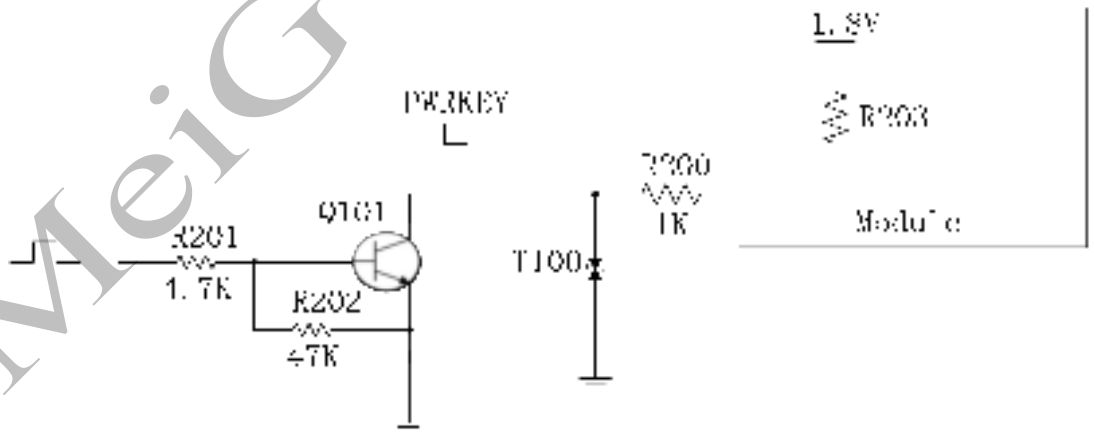

Figure 4.5: Using an external signal to drive the module to boot

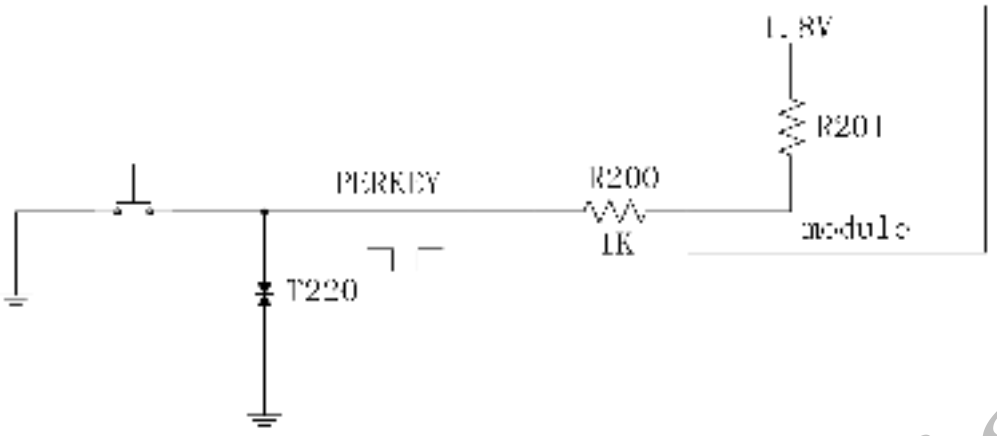

Figure 4.5: Booting with the button circuit

The following figure is the boot timing description:

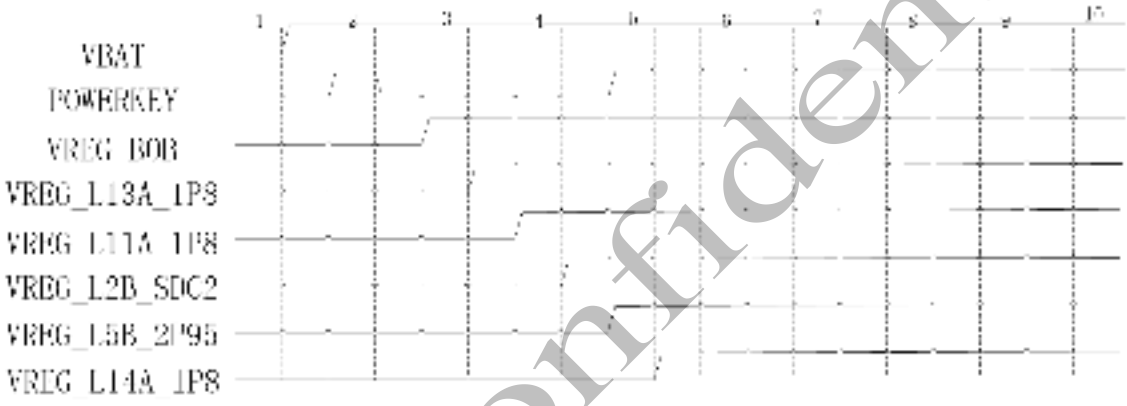

Figure 4.7: Using PWRKEY boot timing diagram

4.2.2 Module Shutdown

用户可以使用 PERKEY 引脚关机，通过把 PERKEY 信号拉低至少 3 秒用来关机。关机电路可以参考开机电路的设计。模块检测到关机动作以后，屏幕会有提示窗弹出，确认是否执行关机动作。

4.2.3 Module Reset

The SNM909 module supports a reset function that allows the user to quickly restart the module by pulling the RESET_N pin (M23) of the module low. The recommended circuit is as follows:

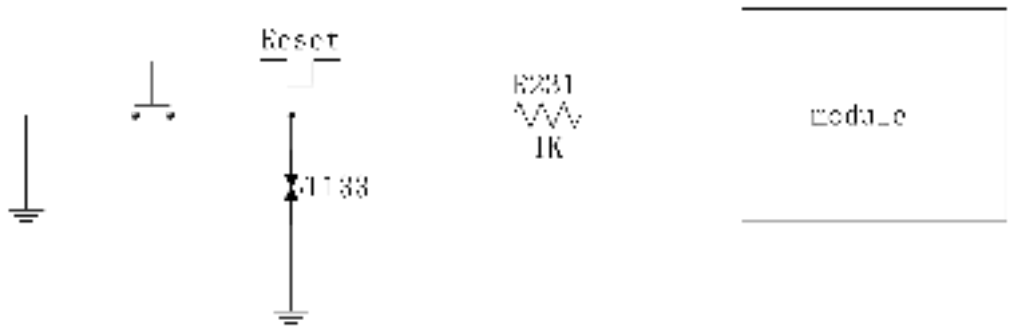

Figure 4.8: Reset using the key circuit

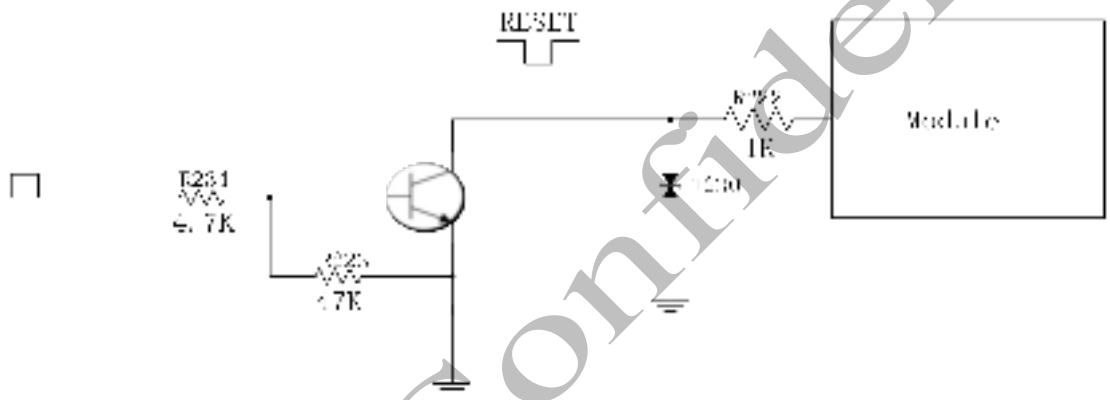

Figure 4.9: Reset Module Using External Signal

When the pin is high, the voltage is typically 1.8V. Therefore, for users with a level of 3V or 3.3V, it is not possible to directly use the GPIO of the MCU to drive the pin. An isolation circuit is required. The hardware parameters of the RESET can refer to the following table:

Table4.1: RESET Hardware Parameters

Pin	Description	Minimum	Typical	Maximum	Unit
RESET	Input high level	1	-	-	V
	Input low level	-	-	0.65	V
	Pull down effective time	11.2		-	s

4.3.VCOIN 电源

When the VBAT is disconnected, the user needs to save the real-time clock, so the VCOIN pin cannot be suspended, and the external capacitor or battery should be connected. When the external capacitor is connected, the recommended value is 100uF, which can maintain the real-time clock for 1 minute. RTC power supply using a large external capacitor or battery to power RTC inside the module reference design circuit is as follows:

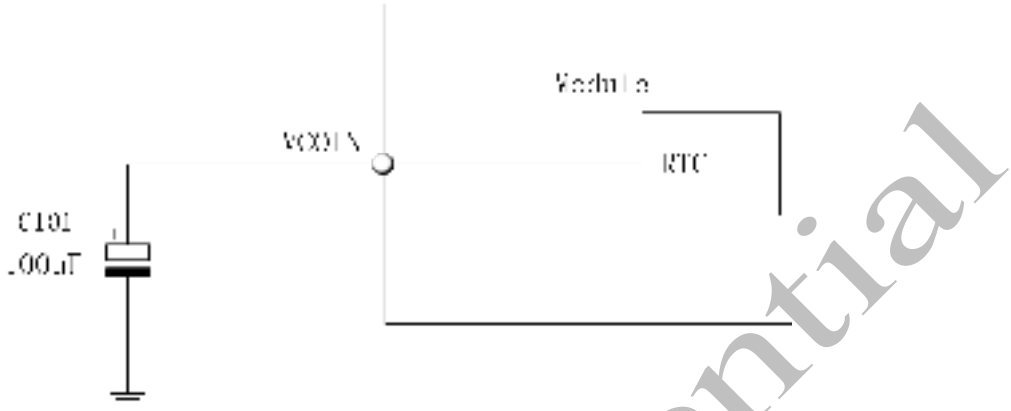

Figure 4.10: External Capacitor Powering the RTC

Rechargeable battery powered:

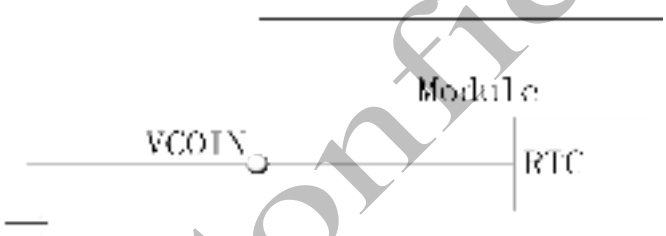

Figure 4.11: Rechargeable battery to power the RTC

Note: VCOIN power input voltage range is 2.1-3.25V, typical value is 3.0V.

4.4 Power Output

The SNM909 has multiple power outputs. For SD card, SIM card, sensor, touch panel, external LDO power supply, etc. In application, it is recommended to add parallel 33PF and 10PF capacitors to each power supply to effectively remove high frequency interference.

Table 4.2: Power Description

Signal	Default Voltage(V)	Drive Current(mA)
VREG_L13A_1P8	1.8	100
VREG_L11A_1P8	1.8	100
VREG_L3B_3P0	3.0	300
VPH_PWR	3.8	600
VREG_L5B_2P95	2.95	400

VREG_L2B_SDC2	2.95	50
VREG_L15A_UIM1	1.8/2.95	100
VREG_L17A_UIM2	1.8/2.95	100
VREG_L14A_1P8	1.8	100
VREG_BOB	3.3	300

4.5 Serial Port

The SNM909 provides three serial ports for communication. There should be three groups of I2C interfaces that can be multiplexed into hardware flow control. Note that no pull resistance can be added when the I2C interface is multiplexed into UART_RTS/CTS.

Table 4.3: UART Pin Description

Name	Pin	Direction	Function
DBG_BLSP2_UART_TX	Y2	O	UART 数据发送
DBG_BLSP2_UART_RX	Z2	I	UART 数据接收
SMB_PWR_BLSP2_I2C_SDA	U10	I	I2C serial data
SMB_PWR_BLSP2_I2C_SCL	U11	O	I2C serial clock
BLSP_GPIO_29	P4	I	UART 数据接收
BLSP_GPIO_28	O5	O	UART 数据发送
BLSP_GPIO_30	O4	I	UART 清除发送（CTS）
BLSP_GPIO_31	O3	O	UART 请求发送（RTS）
ESE_BLSP1_SPI_MISO	V17	I	UART 数据接收
ESE_BLSP1_SPI_MOSI	Y6	O	UART 数据发送
ESE_BLSP1_SPI_CS_N	X6	I	UART 清除发送（CTS）
ESE_BLSP1_SPI_CLK	X5	O	UART 请求发送（RTS）

The serial port connection can be referred to the following connection:

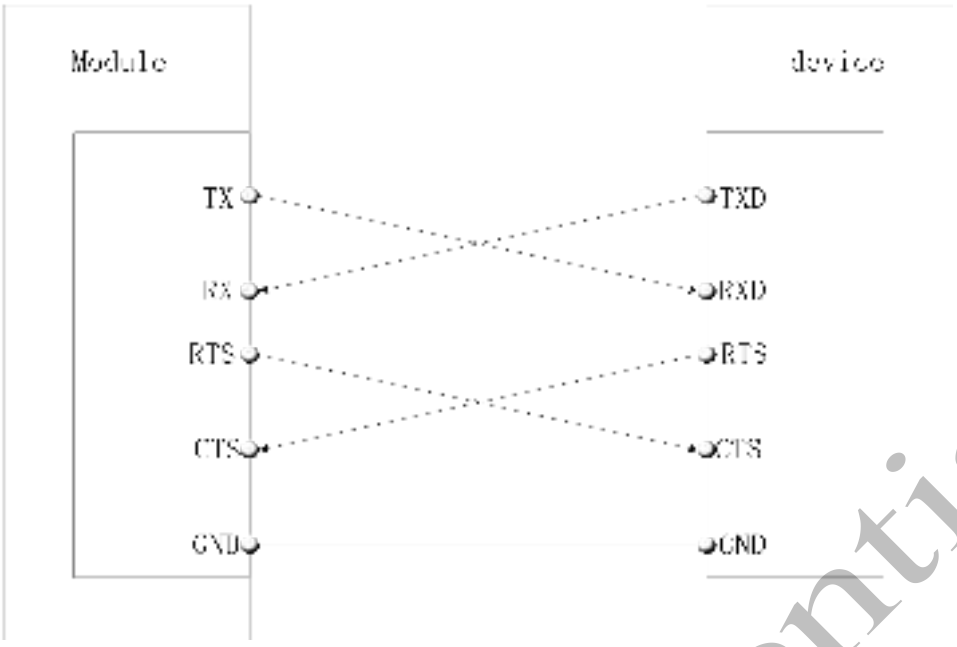

Figure 4.12: Serial Port Connection Diagram

When the serial level used by the user does not match the module, in addition to adding the level shifting IC, the following figure can also be used to achieve level matching. Only the matching circuits on TX and RX are listed here. Other low speed signals can refer to these two circuits.

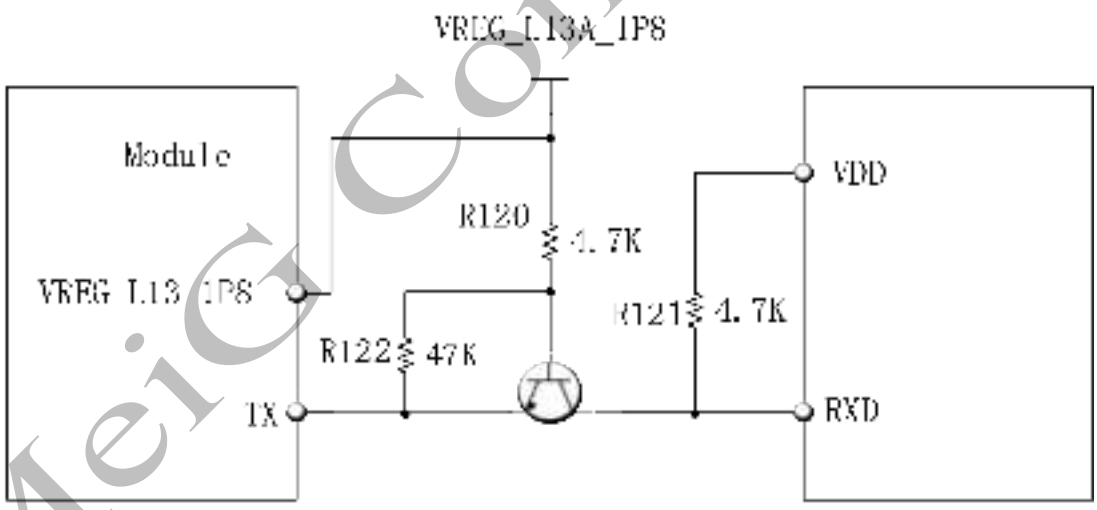

Figure 4.13: TX Connection Diagram

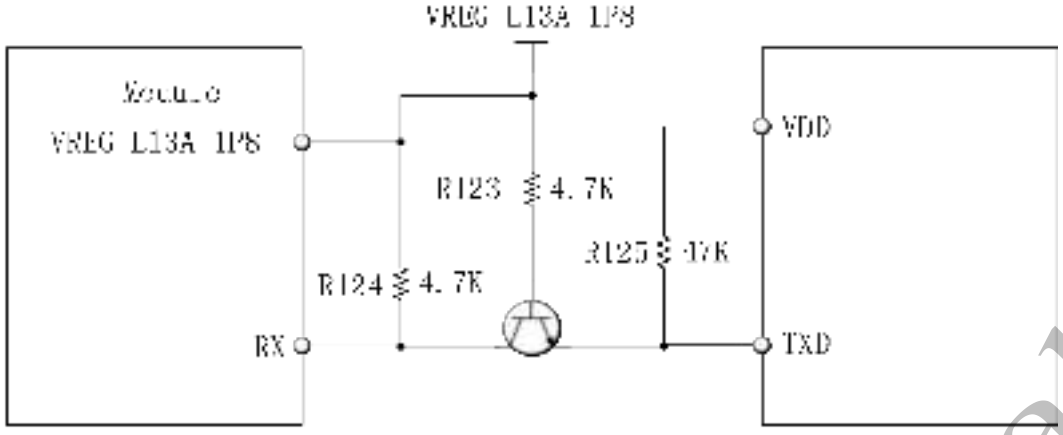

Figure 4.14: RX Connection Diagram

Note: When using Figures 4.14, 4.15 for level isolation, it is recommended that VREG_L13A_1P8 be used as the pull-up supply. The VREG_L11A_1P8 enters the low power consumption mode when it is hibernated and is not recommended.

Table 4.4: Serial Port Hardware Parameters

Description	Minimum	Maximum	Unit
输入低电平	-	0.63	V
输入高电平	1.17	-	V
输出低电平	-	0.45	V
输出高电平	1.35	-	V

Note:

1. The serial port of the module is a CMOS interface, and the RS232 signal cannot be directly connected. If necessary, please use the RS232 conversion chip.
2. If the 1.8V output of the module cannot meet the high-level range of the user terminal, please add a level shifting circuit.

4.6 MIPI Interface

The SNM909 supports the Moble Industry Processor Interface(MIPI) interface for Camera and LCD. The module supports a maximum display of FULL HD(2560*1600), among which the MIPI interface Main Camera supports a maximum of 24MP, and the Front Camera supports 16MP.

MIPI is a high-speed signal line, in the Layout stage, please strictly follow the impedance and length requirements of the line, control the difference pair within the group, the group equal length, the total length as short as possible.

4.6.1 LCD Interface

The SNM909 module supports the MIPI interface of two sets of LCD displays, supports dual-screen display, and

has the identification signal of compatible screens. The resolution of the screen can be supported up to 2560*1600. The signal interface is shown in the following table. In Layout, the MIPI signal line should strictly control the differential 85±15 ohm impedance and the equal length of signal lines within and between groups.

The MIPI interface of the module is the 1.2V power domain. When users need to design compatible screen, they can use the LCD_ID pin or ADC pin of the module. The LCD 2.8V power supply needs to be generated by an external LDO, and the input power of the LDO can use VREG_BOB.

Table 4.5: Screen interface definition

Main display interface			
MIPI_DSI0_CLK_N	Z15	O	MIPI_LCD clock
MIPI_DSI0_CLK_P	Z16	O	
MIPI_DSI0_LANE0_N	W16	O	MIPI_LCD data
MIPI_DSI0_LANE0_P	W15	O	
MIPI_DSI0_LANE1_N	AA15	O	
MIPI_DSI0_LANE1_P	AA16	O	
MIPI_DSI0_LANE3_N	X16	O	
MIPI_DSI0_LANE3_P	X15	O	
MIPI_DSI0_LANE2_N	Y16	O	
MIPI_DSI0_LANE2_P	Y15	O	
LCD_RST_N	AA14	I/O	LCD reset
CAM_FR_STANDBY	N21	I/O	LCD_ID
BB_BOOST_EN	T2	I/O	LCD frame sync signal
WLED_SINK1	D13	AI	LCD series backlight negative 1
WLED_SINK2	B14	AI	LCD series backlight negative 2
VREG_WLED	B13	PO	LCD series backlight positive electrode
VREG_L11A_1P8	F23	PO	1.8V power

Sub display interface			
MIPI_DSI1_CLK_N	BB16	O	MIPI_LCD clock
MIPI_DSI1_CLK_P	CC16	O	
MIPI_DSI1_LANE0_N	BB13	O	MIPI_LCD data
MIPI_DSI1_LANE0_P	CC13	O	
MIPI_DSI1_LANE1_N	BB14	O	
MIPI_DSI1_LANE1_P	CC14	O	
MIPI_DSI1_LANE2_N	BB15	O	
MIPI_DSI1_LANE2_P	CC5	O	
MIPI_DSI1_LANE3_N	BB12	O	

MIPI_DSI1_LANE3_P	CC12	O	
SDM660_GPIO_73	M7	I/O	LCD reset
CAM_AVDD_EN	M21	I/O	LCD frame sync signal
BEEP_PWM	F14	O	LCD backlight PW
VREG_L11A_1P8	F23	PO	1.8V power

LCD_ID of the module, this pin is internally GPIO. When used as LCD_ID, please confirm the internal circuit of LCD. If the internal divider of the LCD uses resistor divider, please pay attention to the voltage to meet the high or low range of GPIO.

MIPI is a high-speed signal line. To avoid EMI interference, it is recommended to place a common-mode inductor near the LCD side.

There are two groups of MIPI signals in this module. The MIPI signal connection method of the main screen is as follows:

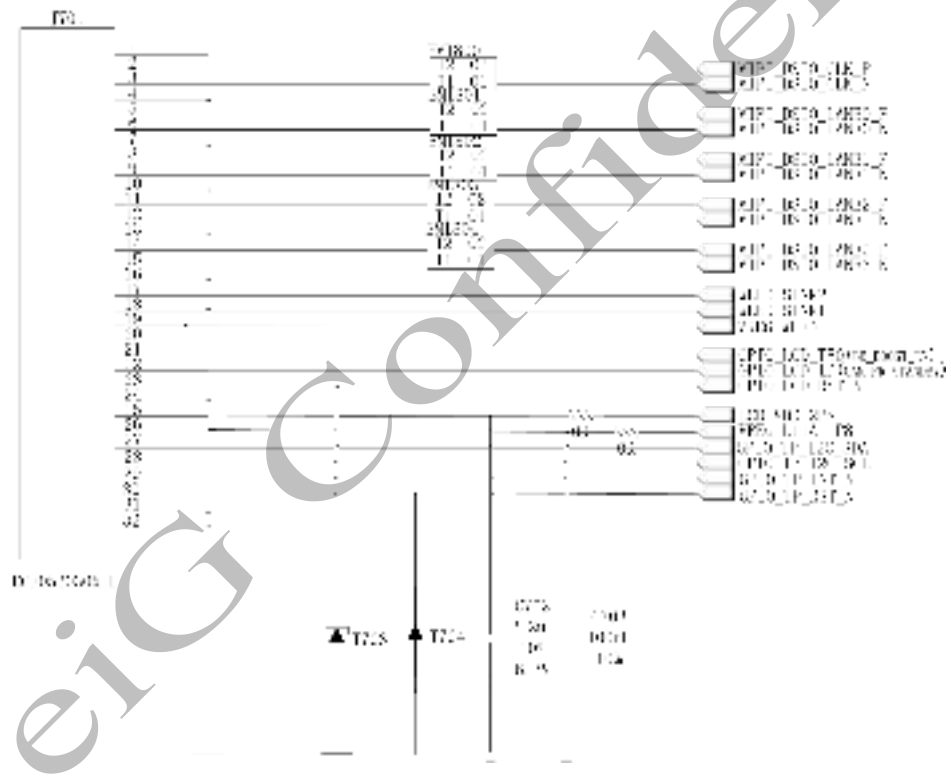

Figure 4.15: Main LCD interface circuit

LDO_2P8 must be generated by an external 2.8V LDO, and the LDO circuit can be seen in FIG. 4.16. In the design of the main and secondary screens, it is recommended to use two 2.8V Ldos to supply power to the main and secondary screens respectively.

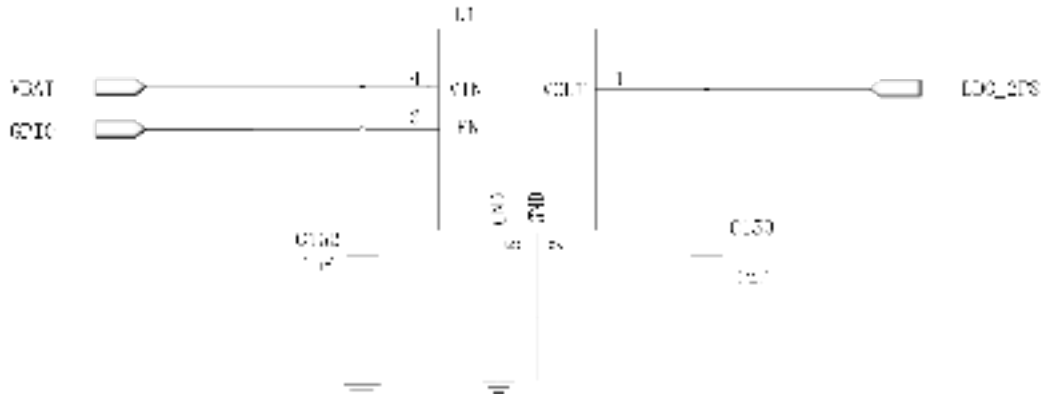

Figure 4.16: LCD 2.8V LDO reference circuit

SNM909 module comes with backlight driver output, customers can directly use this function to drive LCM backlight, SNM909 backlight driver features are as follows:

- uses common anode drive mode, VREG_WLED as common anode output, the output voltage can be configured up to 28V:
- WLED_SINK A total of two channels, each supporting a maximum of 30mA perfusion current, 2 channels in series can light 16 LED:
- The software adjusts the backlight brightness by configuring the current of WLED_SINK.

In the main and secondary screen design, the main screen can directly use the SNM909 internal backlight circuit VREG_WLED, WLED_SINK1, WLED_SINK2, up to 2 strings of 8 lights each, a total of 16 lights; The backlight driver circuit of the secondary screen can be referred to Figure 4.18. The brightness of the backlight can be adjusted through the PM660L_PWM of the module, and the modulation mode is PWM mode.

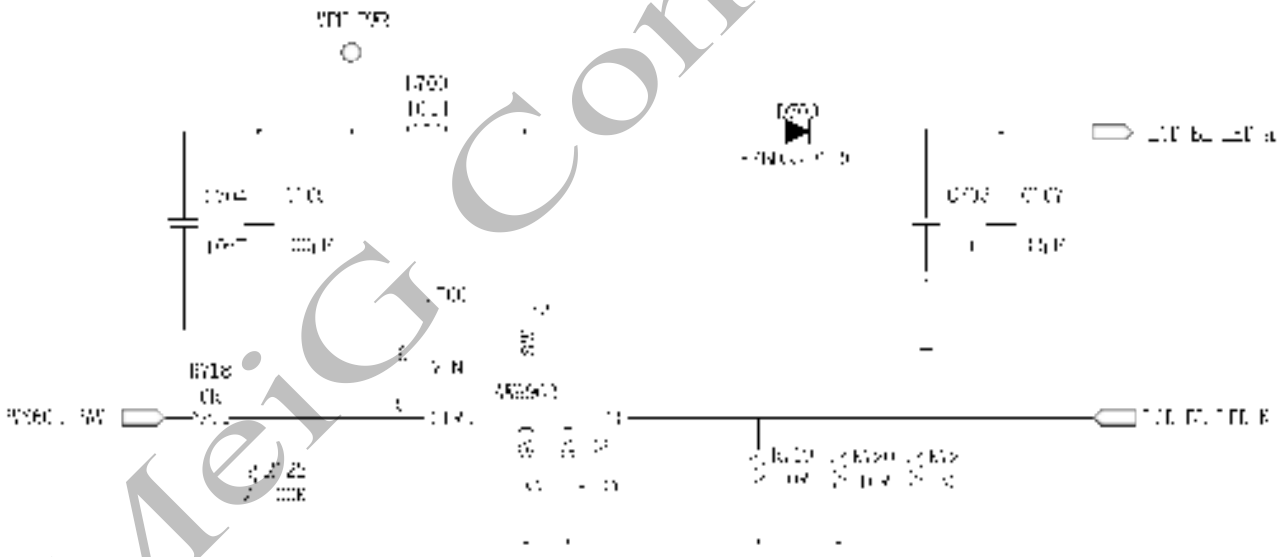

图 4.17：背光驱动示意图

Note: The backlight circuit should be based on the LCD backlight circuit to select the chip, the user should carefully read the LCD document to select the correct driver chip. The reference circuit provided in this document is a series-type PWM dimming backlight driver circuit; if it is a series-type one-line dimming backlight driver circuit, it needs to be controlled by GPIO.

4.6.2 MIPI Camera Interface

SNM909 module supports MIPI Camera interface, the main camera is CSI0 interface, supports four groups of data lines, can support a maximum of 24M pixels. The front camera is a CSI2 interface, supports four groups of data lines, and can support 16M pixels. There is also a set of CSI1 interface, which can do double 16M double camera design with the main camera, or as a dual camera design of depth of field; Can also be used as MIPI interface scan head design. The module does not provide the power required by the Camera, including AVDD-2.8V, AFVDD-2.8V (focusing motor power supply) and DVDD-1.2V(CAM nuclear voltage), which require external LDO generation.

Table 4.6: MIPI Camera Interface Definition

CSI0 interface			
Name	Pin	Input/output	Description
MIPI_CSI0_DCLK_M	W14	O	Camera0 MIPI clock
MIPI_CSI0_DCLK_P	W13	O	
MIPI_CSI0_LANE0_M	U14	I	Camera0 MIPI data
MIPI_CSI0_LANE0_P	U13	I	
MIPI_CSI0_LANE1_M	Y14	I	
MIPI_CSI0_LANE1_P	Y13	I	
MIPI_CSI0_LANE2_M	X14	I	
MIPI_CSI0_LANE2_P	X13	I	
MIPI_CSI0_LANE3_M	V14	I	
MIPI_CSI0_LANE3_P	V13	I	
CAM0_MCLK	M22	I/O	Camera0 main clock
CAM0_RST_N	O22	I/O	Camera0 reset
TRIGGER_BUTTON	J23	I/O	Camera0 sleep
CCI_I2C_SDA0	M19	I/O	I2C data
CCI_I2C_SCL0	M20	I/O	I2C clock
VREG_L11A_1P8	F23	PO	1.8V IOVDD

CSI2 interface			
Name	Pin	Input/output	Description
MIPI_CSI2_CLK_P	V22	O	Camera2 clock
MIPI_CSI2_CLK_M	W22	O	
MIPI_CSI2_LANE0_P	V21	I	Camera2 data
MIPI_CSI2_LANE0_M	W21	I	
MIPI_CSI2_LANE1_P	V20	I	
MIPI_CSI2_LANE1_M	W20	I	
MIPI_CSI2_LANE2_P	V19	I	
MIPI_CSI2_LANE2_M	W19	I	
MIPI_CSI2_LANE3_P	W18	I	
MIPI_CSI2_LANE3_M	V18	I	

CAM1_MCLK	N22	I/O	Camera2 main clock
BB_VOLTAGE_DET	S25	I/O	Camera2 reset
DP_AUX_EN_N	AA5	I/O	Camera2 sleep
CCI_I2C_SDA1	T24	I/O	I2C data
CCI_I2C_SCL1	T23	I/O	I2C clock
VREG_L11A_1P8	F23	PO	1.8V IOVDD

CSI1 interface			
Name	Pin	Input/output	Description
MIPI_CSI1_CLK_M	N25	O	Camera1 MIPI clock
MIPI_CSI1_CLK_P	N24	O	
MIPI_CSI1_LANE0_M	O25	I	Camera1 MIPI data
MIPI_CSI1_LANE0_P	O24	I	
MIPI_CSI1_LANE1_M	K25	I	
MIPI_CSI1_LANE1_P	K24	I	
MIPI_CSI1_LANE2_M	L25	I	
MIPI_CSI1_LANE2_P	L24	I	
MIPI_CSI1_LANE3_M	M24	I	
MIPI_CSI1_LANE3_P	M25	I	
CAM2_MCLK	U9	I/O	Camera1 main clock
CAM1_RST_N	P22	I/O	Camera1 reset
CAM_AFVDD_EN	W9	I/O	Camera1 sleep
CCI_I2C_SDA1	T24	I/O	I2C data
CCI_I2C_SCL1	T23	I/O	I2C clock
VREG_L11A_1P8	F23	PO	1.8V IOVDD

The MIPI interface has a high rate. The user should control the impedance by 85($\pm$ 15) ohms during the routing. Please pay attention to the length of the trace. It is not recommended to add a small capacitor on the MIPI signal line. This may affect the rising edge of the MIPI data. This in turn causes the MIPI data to be invalid.

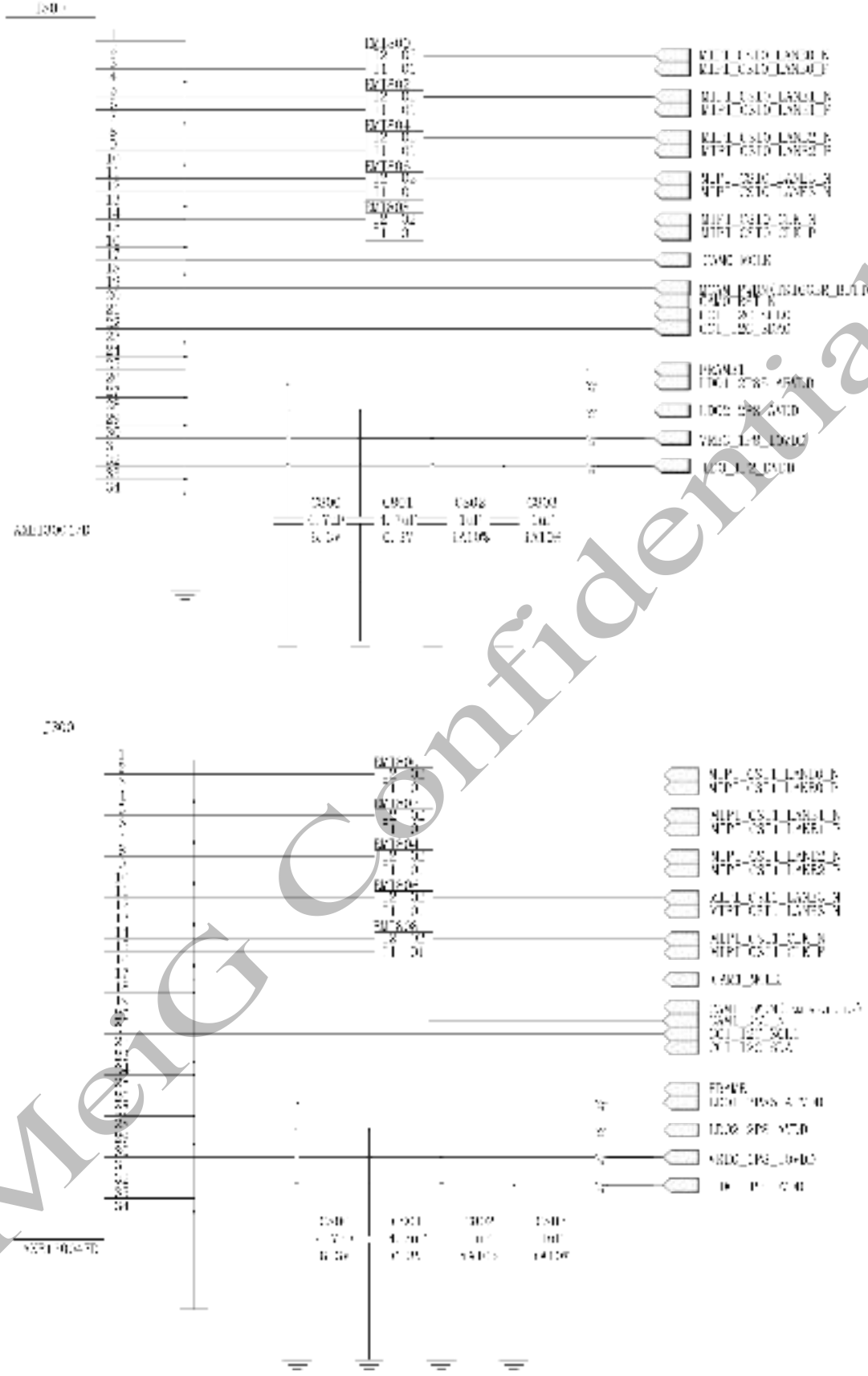

Figure 4.18: MIPI Camera reference circuit

The power supply required by the Camera, including AVDD-2.8V, AFVDD-2.8V(focusing motor power supply) and DVDD-1.2V(CAM nuclear voltage), can be designed with reference to the following LDO circuit

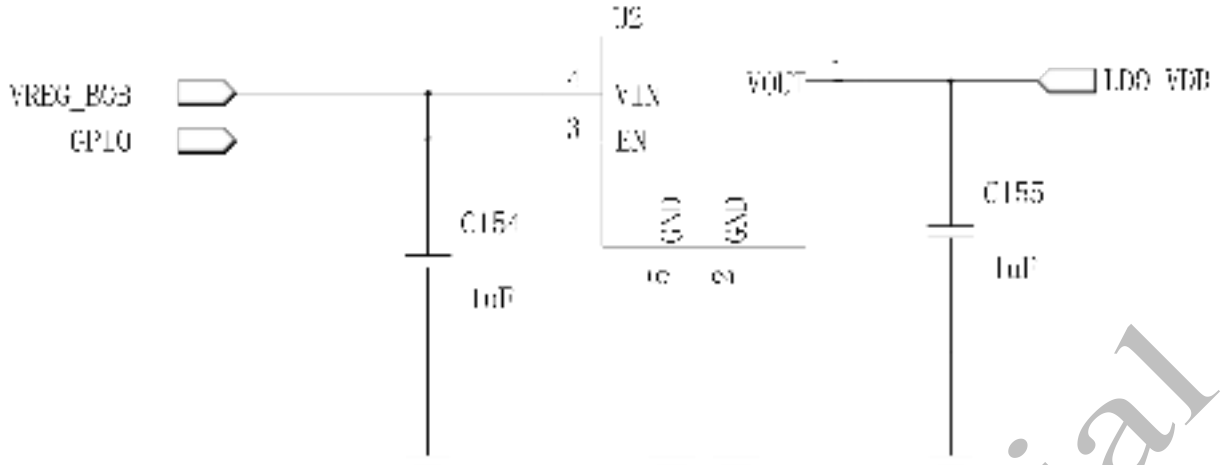

Figure 4.19: Camera power reference circuit

4.6.3 MIPI PCB layout

MIPI is a high-speed signal line, users must pay attention to the protection of the layout stage, so that it is away from the signal line is easy to be interfered with, it must be done up and down the left and right packet GND processing, the alignment for the differential pair of ways to do the 85 (± 15) ohm differential impedance matching, in order to ensure the consistency of the impedance as far as possible do not cross the different GND plane.

MIPI interface in the selection of ESD devices, please select a small capacitance TVS, it is recommended that the parasitic capacitance is less than 1pF.

The MIPI alignment requirements are as follows:：

- The total length of the alignment should not exceed 200mm.
- 85 ohm differential impedance control with ±15 ohm error is required.
- Differential line length error within the group is controlled within 0.7mm.
- The length error between groups is controlled within 1.4mm.

4.7 Capacitive Touch Interface

The module provides a set of I2C interfaces that can be used to connect the capacitive touch screen. The default interface pins of the capacitive touch screen are defined in the table below. The 2.8V power supply required by the capacitive screen needs to be generated by an external LDO.

Table 4.7: Capacitive Touch Interface Definitions

Name	Pin	Input/Output	Description
GPIO14_TS_KP_I2C_SDA	S4	I/O	The I2C interface for capacitive touch must be pulled up to VREG_L11A_1P8
GPIO15_TS_KP_I2C_SCL	S3	I/O	
GPIO67_TS_INT_N	X2	I	Interrupt
GPIO66_TS_RESET_N	U3	O	Reset
VREG_L11A_1P8	F23	PO	1.8V power

Note: The interface definition of the capacitive touch can be adjusted by software, and the user can change the GPIO

and I2C according to the design needs.

4.8 Audio Interface

The module provides three analog audio inputs, MIC_IN1_P/M is used to connect the main microphone; MIC_IN2_P is used to connect the headset microphone, and MIC_IN3_P is used to connect the noise-canceling microphone. The module also provides three analog audio outputs (HPH_L/R, REC_P/N, SPK_P/N). The audio pin pin is defined as follows:

Table 4.8: Audio Pin Definitions

Name	Pin	Input/ Output	Description
CDC_IN1_M	E12	I	Main_MIC_N, shorted to GND
CDC_IN1_P	D12	I	Main_MIC_P
CDC_MIC2_P	E11	I	HS_MIC_P
GND_MIC	G13	I	HS_MIC_N/NR_MIC_N
CDC_IN3_P	F13	I	NR_MIC_P
CDC_MIC_BIAS1	G9	O	Main_MIC_BIAS
CDC_MIC_BIAS2	F9	O	HS_MIC_BIAS
CDC_HPH_R	F11	O	Headphone right track
CDC_HPH_L	H11	O	Headphone left track
HEADSET_DETECT	F12	I	Headphone hot-plug detect
HPH_GND_SENSE	G11	I	Reference GND
CDC_EAR_M	E10	O	Receiver output negative
CDC_EAR_P	F10	O	Receiver output positive
SPKR_DRV_M	D11	O	PA (0.8W) output negative
SPKR_DRV_P	C11	O	PA (0.8W) output positive

Users are advised to use the following circuit according to the actual application to get better sound effects.

4.8.1 Receiver Interface Circuit

The receiver interface circuit places the following devices near the REC end, and the B302 and B303 can be changed to magnetic beads according to the actual effect.

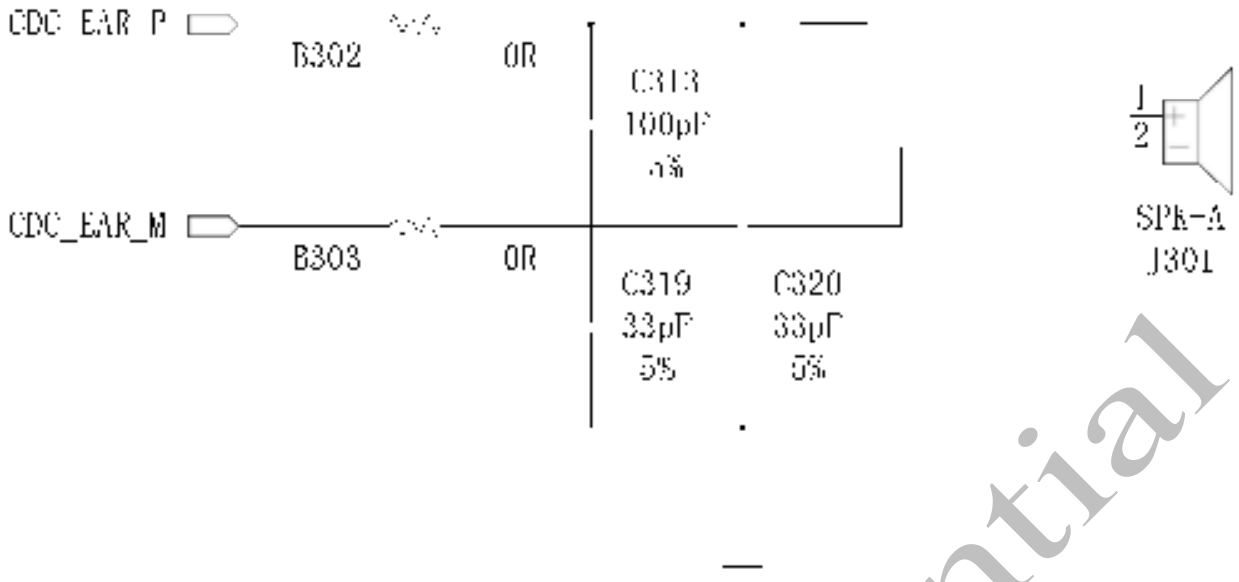

Figure 4.20: Receiver interface circuit

4.8.2 Microphone receiving Circuit

On the right is the MEMS microphone interface circuit, which has more BIAS power supply than the electret MIC. The negative signal of the main MIC must be designed with a 0R to ground resistance near the MIC. As shown in Figure R301.

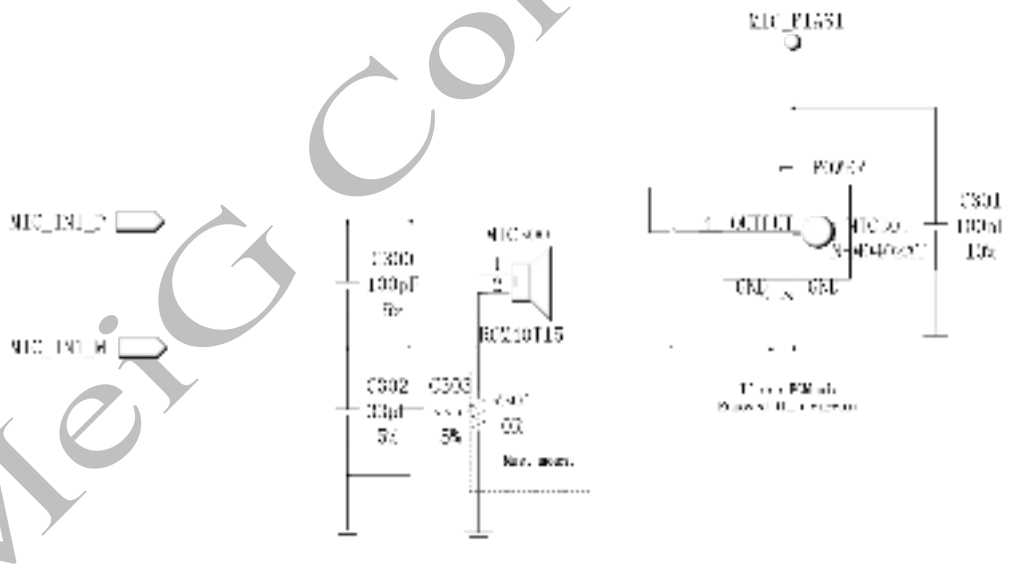

Figure 4.21: Differential interface circuit for microphone

4.8.3 Headphone Interface Circuit

The module integrates a stereo headphone jack. Users are advised to reserve ESD devices during the design phase to prevent ESD damage. The HS_DET pin of the module can be set as an interrupt. In software, this pin is the earphone

interrupt by default. The user can use this pin to detect the plugging and unplugging of the earphone.

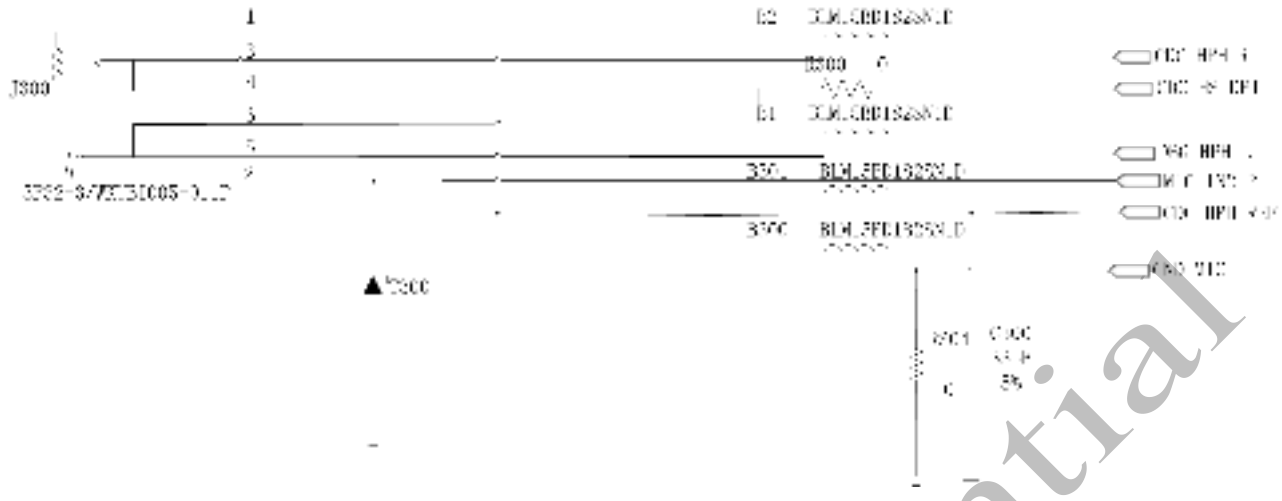

Figure 4.22: Headphone interface circuit

Note:

1.The earphone holder in Figure 4.22 is normally closed. If the user is using the normally open mode earphone holder, please modify the detection circuit according to the actual pin and modify the software accordingly.

2.We recommend that the headphone detection pin HS_DET and HPH_L form a detection circuit (the connection method in the above figure), because HPH_L has a pull-down resistor inside the chip, which can ensure that HS_DET is low when connected with HPH_L, if the user will HS_DET and HPH_R To connect, please reserve a 1K pull-down resistor on HPH_R.

3.The standard of the headphone interface is the European standard OMPT. If you need to design the American standard CTIA interface, you need to swap the GND and MIC signals for the network. If you want to be compatible with both headset standards, you need an external dedicated chip, such as the TI-TS3A226AE.

4.8.4 Speaker interface circuit

The module is integrated with a Class-D audio power amplifier, the output power is 0.8W, and the output signal is SPKR_DRV_P/SPKR_DRV_M.

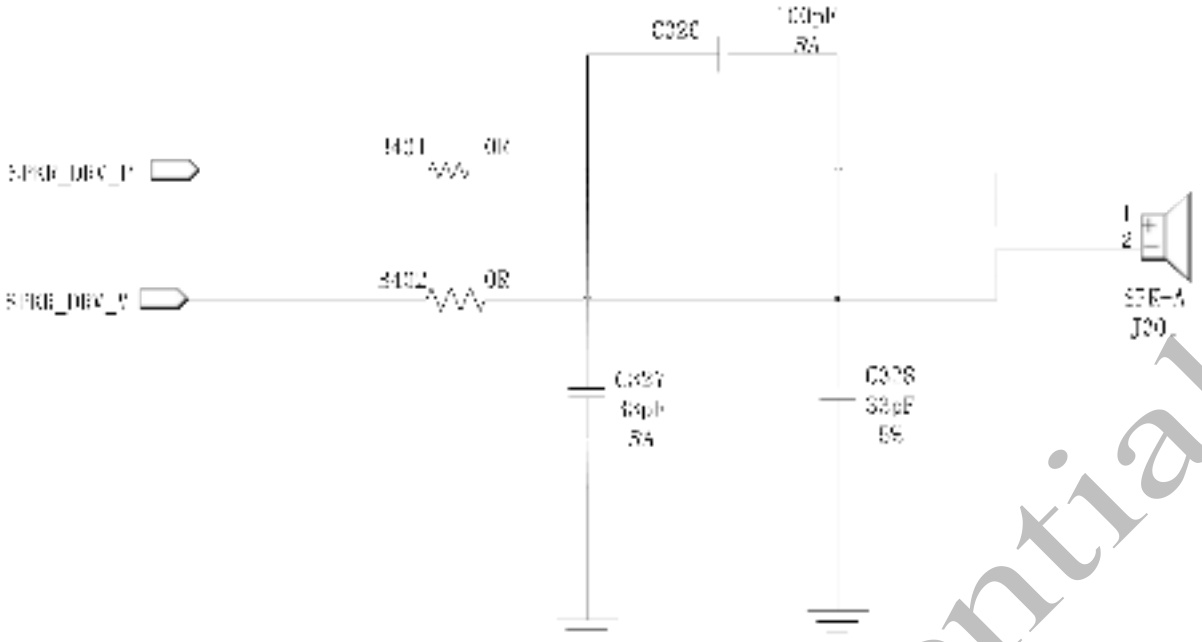

Figure 4.23: Recommended circuit with internal audio amplifier

It is also possible to add an external audio power amplifier, using CDC_HPH_R as a single-ended input signal, the reference circuit is shown below.

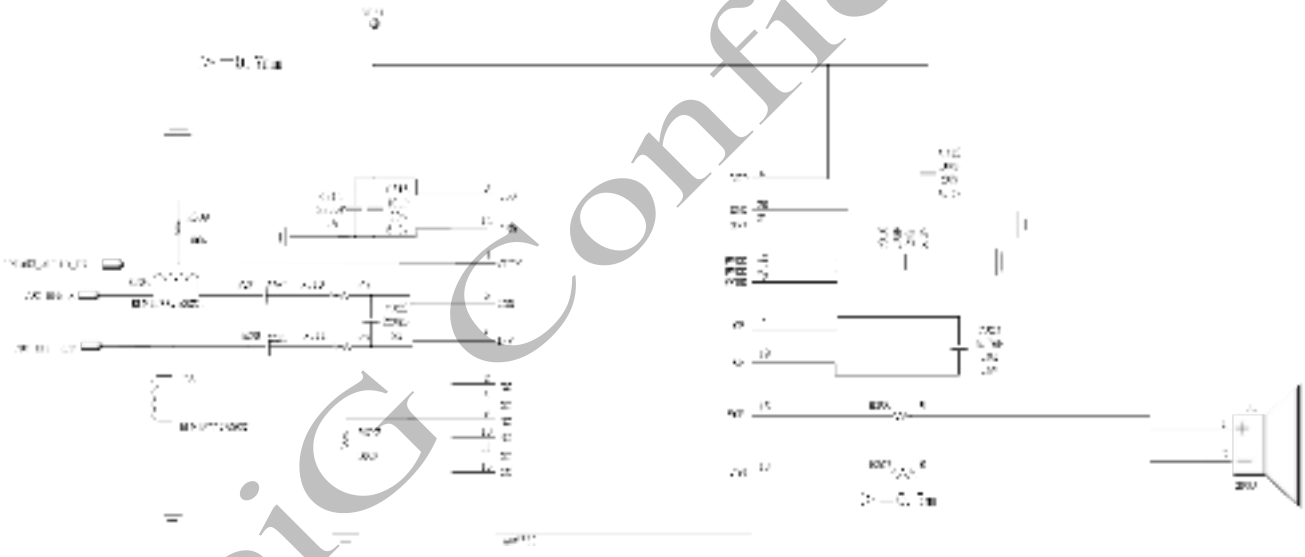

Figure 4.24: Recommended circuit with external audio amplifier

4.9 USB Interface

SNM909 supports one USB 2.0 interface, one USB 3.0 interface, and must control 90 ohm differential impedance in Layout, and control the external cable length. It should be noted that the SNM909 module must be controlled by hardware to switch the TYPE-C, MIRCO USB interface. The required pins for the switching circuit are shown in the following table:

Table 4.9: USB interface switch pin definition

Name	Pin	Input/ Output	Description
CC_OUT	B10	O	Type-c or Micro USB switch
USB_PHY_PS	Z24	I	Type-c or Micro USB switch

UUSB_TYPEC_SEL	C12	I	Type-c or Micro USB switch
VPH_PWR	H14、I14、I15、I16、J14、J15、J16	I/O	System power input and output, typical value 3.8V

The switching circuit can be designed as follows: When switch 1,2 is on, USB_PHY_PS is directly connected to CC_OUT; when UUSB_TYPEC_SEL is pulled up to VPH_PWR through 10K resistance, it switches to TYPE-C interface; when switch 3,4 is on, USB_PHY_PS is on. UUSB_TYPEC_SEL switches to MIRCO USB interface when running through 10K resistance.

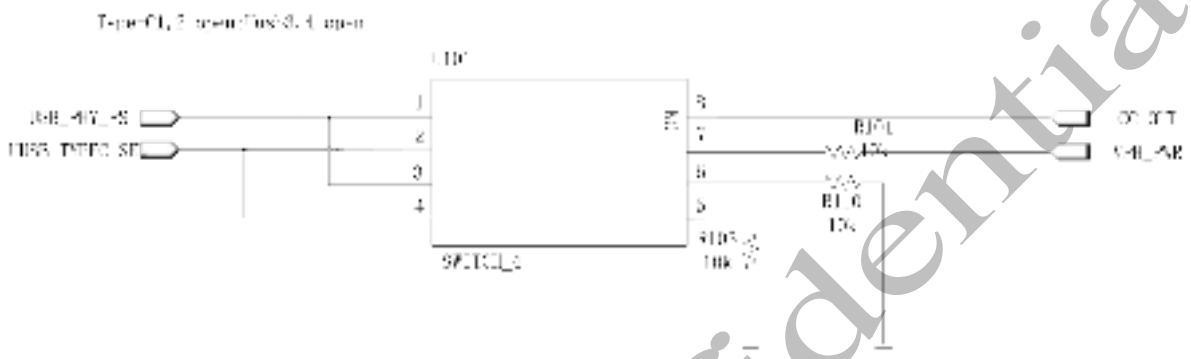

Figure 4.25: USB interface type switching reference circuit

The module also supports OTG function and can output 5V/1.5A current.

The voltage input range during charging is as follows:

Table 4.10: VBUS input range

Name	Description	Minimum	Typical	Maximum	Unit
VBUS	Input range	3.6	-	5.8	V

The USB plug-in detection of the module is realized by the VBUS and DP/DM data lines. When the USB cable is inserted, the VBUS voltage is detected first, and then the DM/DP pull-up state is detected to determine whether the USB data line or the charger is inserted. Therefore, if you need to use the USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is a high-speed mode. It is recommended to connect a common-mode inductor to the side of the USB connector to effectively suppress EMI interference. At the same time, the USB interface is an external interface. The DM/DP must add a TVS tube to prevent static damage caused by plugging and unplugging the data cable. When selecting the TVS, the user should pay attention to the load capacitance of less than 1pf. VBUS also needs to increase the TVS tube. If there is anti-surge demand, it is also necessary to increase the anti-surge tube. The connection diagram is as follows:

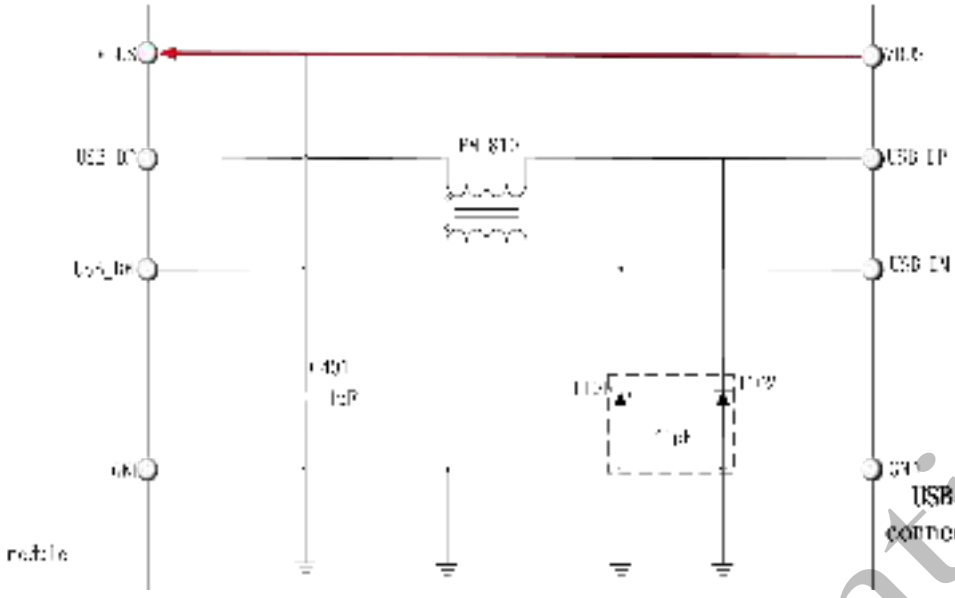

Figure 4.26: USB Connection Diagram

4.9.1 USB OTG

The SNM909 module can provide USB OTG function. The pins used in this function are as follows:

Table4.11: USB- OTG pin description

Pin name	Pin	Description
USB_VBUS_IN	B21、B22、C21、C22、D21、D22、E21、E22、F21、F22	5V charging input /OTG output power supply.
USB1_HS_DM	BB21	USB3.0 DM
USB1_HS_DP	BB22	USB3.0 DP
USB_ID	B11	USB ID

USBOTG的推荐电路图如下图：

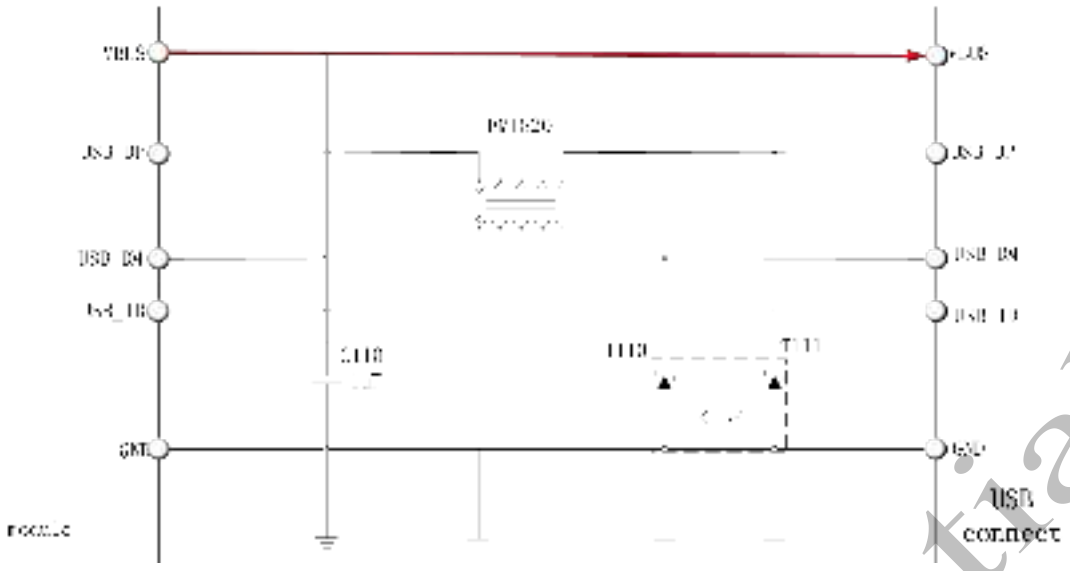

Figure 4.27: USB-OTG connection diagram

4.10.1 USB PCB layout

The module supports high-speed USB interface, the user suggests to add a common mode inductor in the schematic design stage, which can effectively suppress EMI interference, if the user needs to increase electrostatic protection, please be sure to choose the TVS tube with parasitic capacitance less than 1pF. Please refer to the following precautions in Layout:

- The common mode inductor should be close to the USB connector.
- Required to control 90 ohm differential impedance, error ±10%.
- The difference line length error is controlled within 6mm.
- If the USB has a charging function, make sure that the VBUS cable is as wide as possible.
- If there is a test point, try to avoid the cable bifurcation, and put the test point on the path of the cable.

4.10 Charging Interface

The SNM909 module integrates 3A charging scheme. This manual only describes the internal charging scheme. The SDM660 platform uses Qualcomm PM660 internal integrated charging chip by default, which is switching mode and has the characteristics of high efficiency. It integrates 15bit battery voltage detection ADC and 15bit current detection ADC internally, and the maximum charging current can reach 3A.

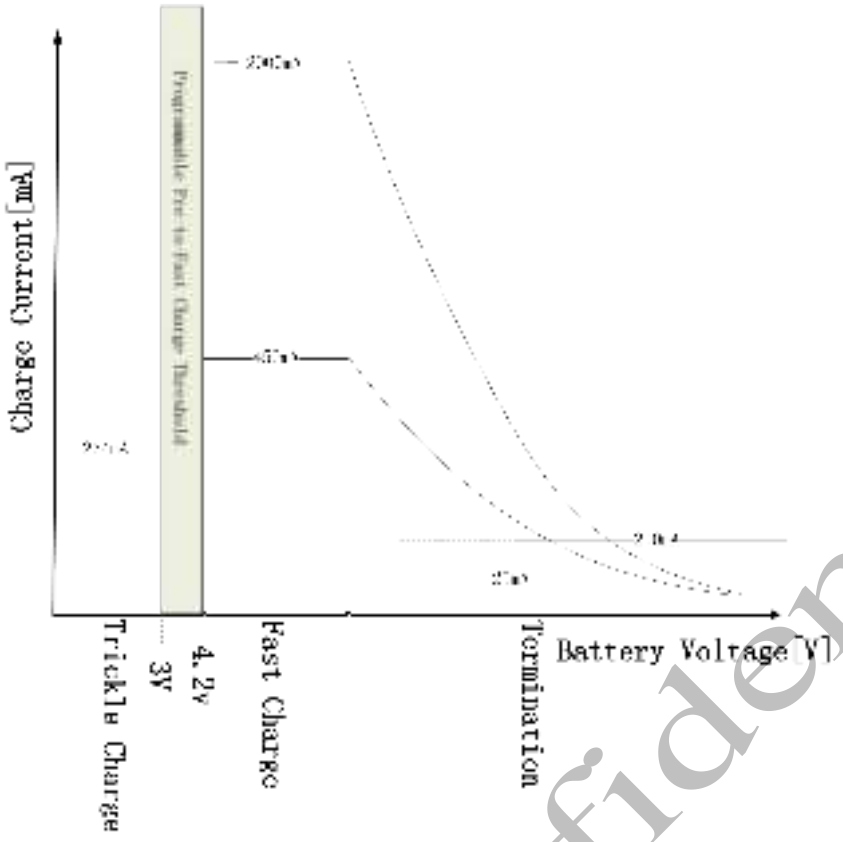

Figure 4.28: Charging diagram

4.10.1 Charging Detection

When the VBUS pin voltage is higher than 3.6V, a hardware interrupt will be generated inside the module. The software determines whether the charger is inserted or the USB data cable is inserted by judging the status of USB_DP/USB_DM.

4.10.2 Charge Control

The SNM909 module can charge the over-discharged battery. The charging process includes trickle charge, pre-charge, constant current, and constant-voltage charge. When the VBAT voltage is lower than 3V, the module is pre-charged; when VBAT is between 3.4V and 4.2V, it is charged by the constant current plus constant voltage method optimized for the lithium battery. At present, the software's charge cut-off voltage is 4.2V, and the back-off voltage is 4.05V.

4.10.3 BAT_CON_TEM

The SNM909 module has a battery temperature detection function, which can be implemented by the user through BATT_THERM (H24). This requires a 10KΩ thermistor (negative temperature coefficient) to be integrated into the battery and connected to the BAT_THERM pin. During the charging process, the software will read the voltage of

the BAT_THERM pin to determine whether the battery temperature is too high. If the temperature is found to be too high or too low, the charging will be stopped immediately to prevent battery damage. The battery charging connection diagram is shown in the following figure:

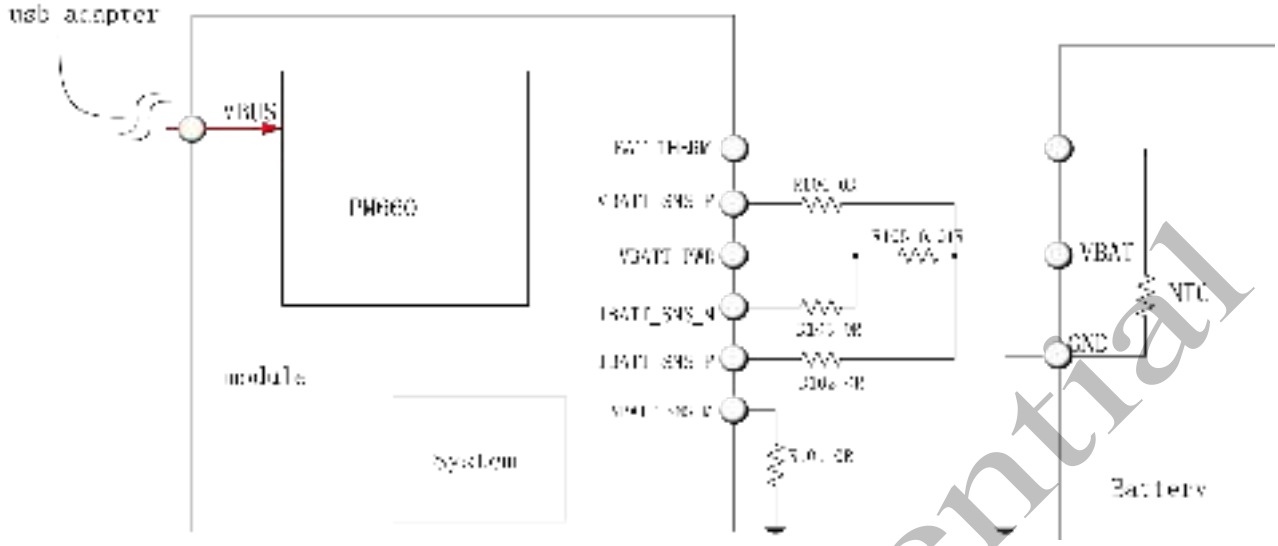

Figure 4.29: Charging circuit connection diagram

4.11 UIM Card Interface

4.11.1 UIM card interface circuit

TheSNM909 can support two SIM cards at the same time to achieve dual card dual standby. Support SIM card hot swap, can automatically recognize 1.8V and 3.0V cards. The figure below is the SIM recommended interface circuit. In order to protect the SIM card, it is recommended to use TVS devices for electrostatic protection. The device of the peripheral circuit of the SIM card should be close to the SIM card holder.

The reference circuit is as follows:

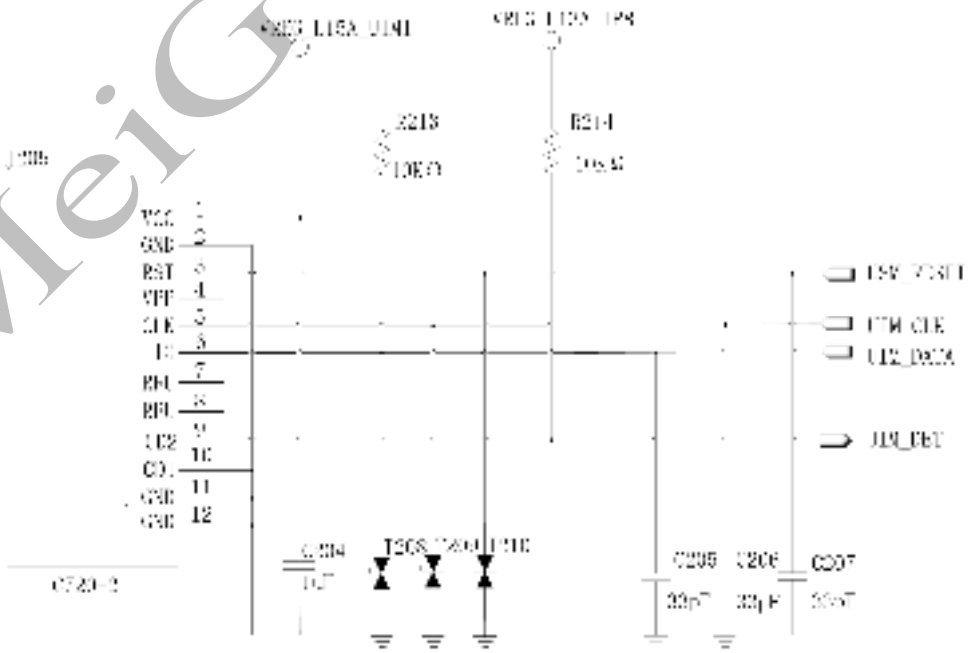

Figure 4.30: UIM card interface circuit

4.11.2 UIM card PCB layout

The SIM card area is large, and there is no anti-EMI interference device itself, it is easy to be interfered with, so in the layout, first ensure that the SIM card is far away from the antenna and the antenna extension line inside the product, as close to the module as possible, and pay attention to protect the SIM_CLK signal when the PCB is running. Keep SIM_DATA, SIM_RST, and SIM_VDD signals of the SIM card away from the power supply and away from high-speed signal cables. If it is not handled well, it is easy to cause the situation of not recognizing the card or dropping the card, so please follow the following principles when designing:

- In the PCB layout stage, be sure to keep the SIM card seat away from the GSM antenna;
- SIM card cable should be far away from RF cable, VBAT and high-speed signal cable, and SIM card cable should not be too long;
- The GND of the SIM card seat should maintain good connectivity with that of the module, so that the GND of the two is equal potential.
- To prevent SIM_CLK from interfering with other signals, you are advised to protect SIM_CLK.
- It is recommended to place a 100nF capacitor near the SIM card seat on the SIM_VDD signal cable.
- Place TVS near the SIM card seat, the parasitic capacitance of the TVS should not be greater than 50pF, and the 51Ω resistance in series between the module can enhance ESD protection;
- Add 22pf ground capacitance to the SIM card signal cable to prevent RF interference.
- Strong current passes through the VBAT backflow path. Therefore, avoid the backflow path of the SIM card as much as possible.

4.12 SD Card Interface

The SNM909 supports an SD card interface with a maximum support of 128GB
The reference circuit is as follows:

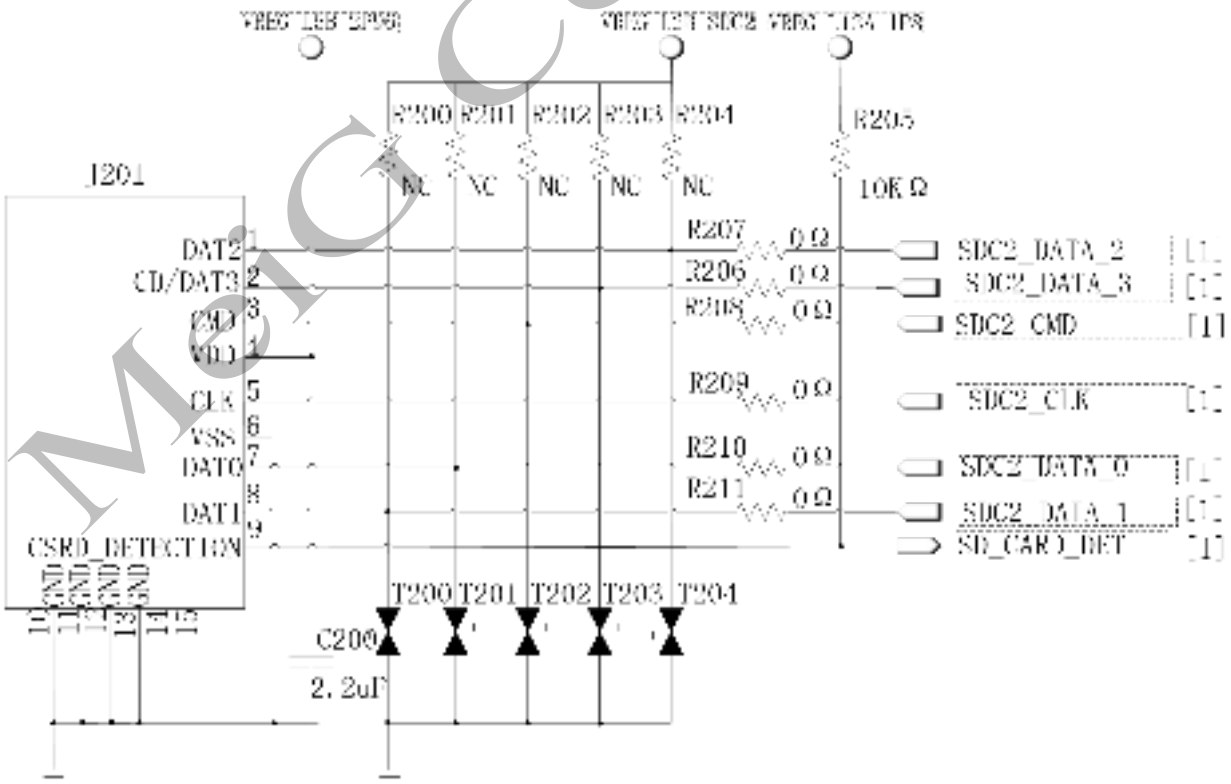

Figure 4.31: SD card interface circuit

4.13 I2C Bus Interface

The SNM909 module supports hardware I2C bus interface and two camera dedicated CCI interfaces. Pin definitions and default functions are as follows:

Table 4.12: I2C interface pin description

Name	Pin	Default function
CCI_I2C_SDA0	M19	Camera I2C
CCI_I2C_SCL0	M20	
LPI_I2C_3_SDA	O19	Sensor I2C(Default)
LPI_I2C_3_SCL	P19	
SMB_PWR_BLSP2_I2C_SDA	U10	General I2C
SMB_PWR_BLSP2_I2C_SCL	U11	
I2C_DAT_BATT	V2	General I2C
I2C_CLK_BATT	W2	
ESE_BLSP1_SPI_CS_N	X6	General I2C
ESE_BLSP1_SPI_CLK	X5	
CCI_I2C_SDA1	T24	Camera I2C
CCI_I2C_SCL1	T23	
GPIO14_TS_KP_I2C_SDA	S4	General I2C, default for TP I2C
GPIO15_TS_KP_I2C_SCL	S3	
BLSP_GPIO_30	O4	General I2C
BLSP_GPIO_31	O3	
GPIO22_SCAN_I2C_SDA	O7	General I2C
GPIO23_SCAN_I2C_SCL	O8	

Note: Connect the 2.2KΩ pull-up resistor to 1.8V when used as an I2C bus interface, see Table 3.1- I2C interface.

4.14 Analog to Digital Converter (ADC)

The SNM909 module is powered by a power management chip with one ADC: QUIET_THERM (K21)
The ADC signal has a 16bit resolution, and its performance parameters are as follows:

Table 4.13: ADC performance parameters

Description	Minimum	Typical	Maximum	Unit
Input Voltage Range	-	1.8	-	V
ADC Resolution	-	-	15	bits
Analog Input Bandwidth	-	500	-	kHz

4.15 PWM

The LCD_BKL_PWM(C14) pin can be used to adjust the backlight of the LCD, and adjust the backlight brightness by adjusting the duty cycle.

4.16 Motor

The SNM909 supports the motor function, which can be implemented by PMI_HAP_OUT_M (E19) and PMI_HAP_OUT_P (D18).

4.17 Antenna Interface

The module provides two antenna interfaces for WiFi/BT_5G and WiFi/BT_2.4G antennas. In order to ensure that the user's product has good wireless performance, the antenna selected by the user should meet the requirements that the input impedance in the operating frequency band is 50 ohms and the standing wave coefficient is less than 2.

4.17.1 Wi-Fi/BT antenna

The module provides the Wi-Fi/BT antenna pin RF_WIFI/BT. The antenna on the user's motherboard should be connected to the antenna pin of the module using a 50ohm microstrip line or strip line.

To facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

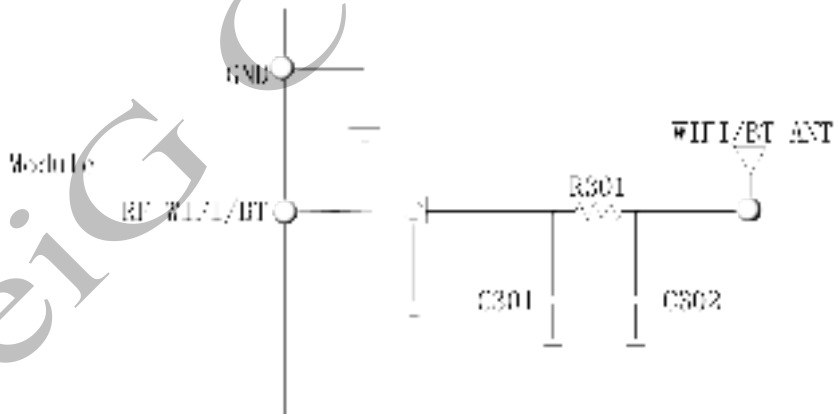

Figure 4.37: WiFi/BT antenna interface connection circuit

Note: In the figure, R301, C300, and C301 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R301 defaults to 0R, C300 and C301 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

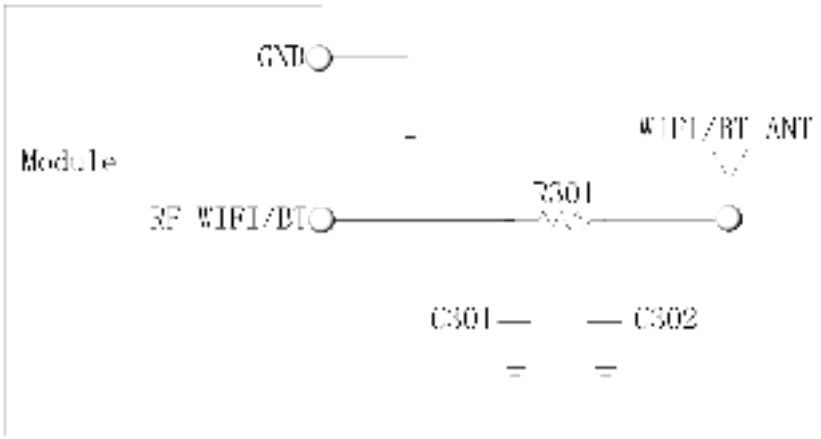

Figure 4.38: WIFI_BT antenna interface simplified connection circuit

在上图中，R301 默认贴 0R，C301 和 C302 默认不贴。

4.17.2 Antenna PCB layout

Note when placing components and RF wiring:

- The RF test head is used to test the conducted RF performance and should be placed as close as possible to the antenna pin of the module.
- The antenna matching circuit should be placed near the antenna end;
- The connection between the antenna pin of the module and the antenna matching circuit must be controlled by 50 ohm impedance;
- The device and cable between the antenna pin of the module and the antenna connector must be away from high-speed signal lines and strong interference sources, and avoid crossing or parallel with any signal lines in the adjacent layer.
- The length of the RF line between the antenna pin of the module and the antenna connector should be as short as possible, and the situation of traversing the entire PCB board should be absolutely avoided.
- If the antenna is connected by a coaxial RF line, care should be taken to avoid the coaxial RF line across the SIM card, power circuit and high-speed digital circuit, so as to minimize the impact between each other.

5 Electrical, Reliability

5.1 Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits can cause permanent damage to the module.

Table 5.1: Absolute Maximum

Parameter	Minimum	Typical	Maximum	Unit
VBAT	--0.5	-	6	V
VBUS	--0.3	-	12	V
Peak current	-	-	3	A

5.2 Working Temperature

The table below shows the operating temperature range of the module:

Table 5.2: Module Operating Temperature

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-35	-	75	℃
Storage temperature	-40	-	90	℃

5.3 Working Voltage

Table 5.3: Module Operating Voltage

Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.55	4.0	4.4	V
VBUS	3.6	5	10	V
Hardware shutdown voltage	2.9		-	V

5.4 Digital Interface Features

Table 5.4: Digital Interface Features (1.8V)

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{IH}	Input high level voltage	1.17	1.8	2.1	V
V_{IL}	Input low level voltage	-0.3	0	0.63	V
V_{OH}	Output high level voltage	1.35	-	1.8	V
V_{OL}	Output low level voltage	0	-	0.45	V

5.5 SIM_VDD Feature

Table 5.5: SIM_VDD Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
V_O	Output voltage	1.65	1.8	1.95	V
		-	2.95	-	
I_O	Output current	-	-	55	mA

5.6 PWRKEY Feature

Table 5.6: PWRKEY Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
PWRKEY	High level	1.4	-	-	V
	Low level	-	-	0.6	V
	Effective time	3000			ms

5.7 VCOIN Feature Current consumption（VBAT=3.8V）

Table 5.7: VCOIN Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
$VCOIN_{-IN}$	VCOIN input voltage	2.1	3.0	3.25	V
$VCOIN_{-OUT}$	VCOIN Output voltage	-	3.0	-	V

5.8 Current consumption（VBAT=3.8V）

Table 5.8: Current consumption

Parameter	Description	condition	Minimum	Typical	Maximum	Unit
VBAT	Supply voltage	The voltage must be between the maximum and minimum values	3.5	3.8	4.2	V
Ivbat	Average current	Shutdown mode	-	-	65	uA
Imax	Peak current	Power control at maximum output power	-	-	3	A

5.9 Electrostatic Protection

The module is not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling and operating modules.

5.10 WIFI Main RF Performance

The table below lists the main RF performance under WIFI conduction.

Table 5.13: Main RF performance parameters under WIFI conduction

Transmission performance				
	802.11B	802.11G	802.11N	
Transmit power (minimum rate)	18	17	16	dBm
Transmit power (maximum rate)	17	15	13	dBm
EVM (maximum rate)	20%	-27	-30	dB
Receiving performance				
Receiving sensitivity	802.11B	802.11G	802.11N	
Minimum rate	-92	-91	-90	dBm
Maximum rate	-89	-72	-70	dBm

Transmission performance				
	802.11A	802.11AC		
Transmit power (minimum rate)	17	17		dBm
Transmit power (maximum rate)	15	14		dBm
EVM (maximum rate)	20%	-27		dB
Receiving performance				

Receiving sensitivity	802.11A	802.11AC		
Minimum rate	-90	-90		dBm
Maximum rate	-77	-70		dBm

5.11 BT Main RF Performance

The table below lists the main RF performance under BT conduction.

Table 5.14: Main RF performance parameters under BT conduction

Transmission performance				
Transmit power	DH5	2DH5	3DH5	
	10	6	6	dBm
Receiving performance				
Receiving sensitivity	DH5	2DH5	3DH5	
	-94.5	-94.5	-86	dBm

5.12. Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to XXXX that they wish to change
the antenna trace design. In this case, a Class II permissive change application is required to be filed
by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it
must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: 2APJ4-SNM909”
The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	Band	Gain(dBi))
Glue Stick Antenna	2400~2483.5MHz	0.95
	5150~5250MHz	6.84
	5250~5350MHz	7.17
	5470~5725MHz	6.5
	5725~5850MHz	5.47
	/	/
	/	/
	/	/
	/	/
	/	/

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product
(including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following twoconditions:

(1) This device may not cause harmful interference.

(2) this device must accept any interference received, including interference that may cause undesired operation. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, 15.247 and 15.407

requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed

on the grant, and that the host product manufacturer is responsible for compliance toany other FCC

rules that apply to the host not covered by the modular transmitter grant of certification.

If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that

the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions:

(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This equipment should be installed and operated with minimum distance 20 cm between the radiator &your body.

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

In order to avoid the possibility of exceeding the IC radio frequency exposure limits, human proximity to the antenna shall not be less than 20cm (8 inches) during normal operation.

Afin d'éviter la possibilité de dépasser les limites d'exposition aux fréquences radio de la IC CNR102, la proximité humaine à l'antenne ne doit pas être inférieure à 20 cm (8 pouces) pendant le fonctionnement normal.

CE Statement

Hereby, [MeiG Smart Technology Co., Ltd] declares that the radio equipment type [SNM909] is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet

address: https://www.meigsmart.com/.

The device is restricted to indoor use only when operating in the 5250 to 5350 MHz frequency range.

	AT	BE	BG	HR	CY	CZ	DK
	EE	FI	FR	DE	EL	HU	IE
	IT	LV	LT	LU	MT	NL	PL
	PT	RO	SK	SI	ES	SE	UK(NI)

The device could be used with a separation distance of 20cm to the human body.

This radio equipment operates with the following frequency bands and maximum radio-frequency power：

BT (2400-2483.5MHz): 8.70 dBm

WIFI 2.4G(2400-2483.5MHz): 17.90 dBm

WIFI 5G (5150-5725MHz): 16.85 dBm

WIFI 5G (57250-5850MHz): 13.88 dBm

6 Production

6.1 Top and Bottom Views of The Module

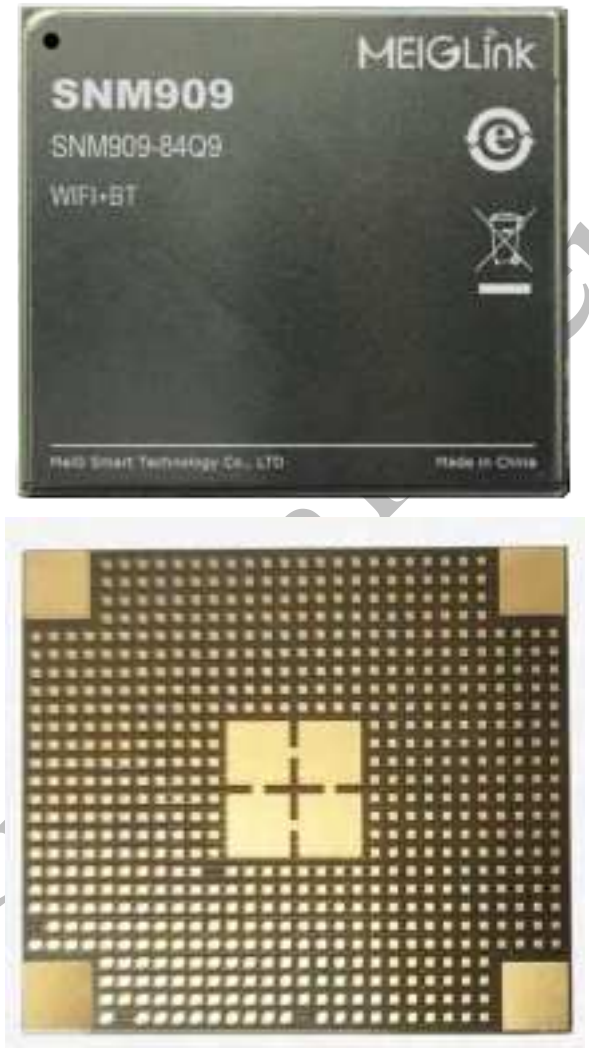

Figure 6.1: Module top and bottom views

6.2 Humidity Sensitivity (MSL)

The SNM909 module meets moisture sensitivity level 3. The dry package is subjected to the J-STD-020C specification in accordance with the IPC/JEDEC standard under ambient conditions of temperature <30 ℃ and relative humidity <60%. Under ambient conditions of temperature <40 ℃ and relative humidity <90%, the shelf life is at least 6 months without unpacking. After unpacking, The table below lists the shelf life of the modules for different moisture sensitivity levels.

Table6.1: Humidity sensitivity level distinction

Grade	Factory environment≦+30℃/60%RH
1	Indefinite quality in the environment≦+30℃/85% RH Under conditions
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Use it after forced baking. After baking, the module must be patched within the time limit specified on the label.

After unpacking, the SMT patch should be taken within 168 hours under ambient conditions of <30℃ and relative humidity <60%. If the above conditions are not met, baking is required. Note: Oxidation risk: Baking SMD packages can cause metal oxidation and, if excessive, can cause solderability problems during board assembly. The temperature and time of the SMD package are baked, thus limiting solderability considerations. The accumulation of baking time should be no more than 96 hours at temperatures above 90°C and as high as 125°C.

6.3 Baking Requirements

Due to the humidity sensitivity of the module, the SNM909 should be thoroughly baked prior to reflow soldering, otherwise the module may cause permanent damage during reflow soldering. The SNM909 should be baked for 192 hours in a cryogenic vessel at 40°C +5°C/-0°C and a relative humidity of less than 5%, or in a high temperature vessel at 80°C±5°C.Bake for 72 hours. Users should note that the tray is not resistant to high temperatures. The user should take the module out of the tray for baking, otherwise the tray may be damaged by high temperature.

Table 6.2: Baking requirements

Baking temperature	Humidity	Baking time
40°C±5°C	<5%	192 小时
120°C±5°C	<5%	4 小时

7 Appendix

7.1 Related Documents

Table 7.1: Related documents

Serial number	File name	Comment
[1]	GSM 07.07：	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10：	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05：	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)
[4]	GSM 11.14：	Digital cellular telecommunications system (Phase 2+);Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11：	Digital cellular telecommunications system (Phase 2+);Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38：	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2)；Mobile Station (MS) conformance specification；Part 1：Conformance specification
[8]	AN_Serial Port	AN_Serial Port

Figure 7.1: Module recommended soldering furnace temperature curve

7.2 Terms and Explanations

Table 7.2: Terms and explanations

Terms	Explanations
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service

TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
Phone book abbreviation	Explanations
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

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