Product Specification

Model:FLC5330XSA-A

Jiangsu Fulian Communication Technology Co., Ltd.

Approval	Review	Draft	Version	Date
			V1.2	2025.03.05

I.Version Update Log

Date	Version	Update Content
2024-10-08	V1.0	Initial document
2025-03-05	V1.2	Updated modulation modes; supplemented 11AX transmit power and receive sensitivity

II. Product Overview

The FLC5330XSA-A module integrates the TR5330 chip, featuring a highly integrated 2.4GHz Wi-Fi and BLE Combo chip with IEEE802.11b/g/n/ax baseband and RF circuits, including PA, LNA, RF balun, antenna switch, and power management modules. It supports 802.11n (20MHz/40MHz bandwidth) and 802.11ax (20MHz bandwidth), delivering a maximum physical layer rate of 150Mbps and extended coverage.

Wi-Fi baseband implements OFDMA, OFDM technologies, and is backward compatible with DSSS, CCK. Supports IEEE802.11b/g/n data rates and IEEE802.11ax MCS0–MCS9 rates.

Supports BLE 1MHz/2MHz bandwidth, BLE 4.0/4.1/4.2/5.0/5.1/5.2/5.4 protocols, BLE Mesh, and gateway functions with a maximum air interface rate of 2Mbps.

The FLC5330XSA-A adopts a stamp-hole package design (21×23mm), laser-etched shield cover for aesthetics and traceability, optimized matching and RF performance. Applications include smart home, smart city, healthcare, security, and IoT.

III. Key Features

WiFi

- 2.4GHz band (Channel 1–14) Wi-Fi Station.
- PHY supports IEEE 802.11b/g/n/ax.
- MAC supports IEEE802.11d/e/i/k/v/w.
- Supports 802.11n (20MHz/40MHz) and 802.11ax (20MHz).
- Max rate: 150Mbps@HT40 MCS7, 114.7Mbps@HE20 MCS9.
- Integrated PA/LNA, TX/RX switch, balun.
- Supports STA, SoftAP (max 8 STA), and P2P modes.

BLE

- Supports BLE 4.0/4.1/4.2/5.0/5.1/5.2/5.4.
- Rates: 125Kbps, 500Kbps, 1Mbps, 2Mbps.
- High power output: 8 dBm±2dBm.

CPU

- - 32-bit CPU, max 240MHz.
- Internal SRAM, ROM.
- Laser-etched shield cover, stamp-hole design (19-pin).
- Standard 3.3V supply (3.0–3.6V).
- Operating temperature: 0–70°C.
- Tape-and-reel packaging.

IV. Detailed Parameters

Table 4-1: Detailed Parameter Table

Parameter Name	Description
Module Model	FLC5330XSA-A
Module Type	WLAN 802.11b/g/n/ax SDIO 1T1R Module
Main Chip	TR5330S
Standard	802.11 b/g/n/ax
Rate	150Mbps@HT40 MCS7 114.7Mbps@HE20 MCS9
Modulation	CCK/DSSS/DBPSK/DQPSK/OFDM/16QAM/64QAM/256QAM, GFSK
Frequency Band	2.4–2.4835 GHz
Transmit Power	802.11b@11Mbps: 16dBm±2dB 802.11ax@MCS9: 14dBm±2dB
Receive Sensitivity	11ax HE20 MCS9 (PER<10%): <-66dBm±2dB
OS Support	Windows/Linux/Mac/Android/Win CE
Security	WEP, TKIP, AES, WPA/WPA2
Interface	SDIO 1.1/2.0
Power Supply	DC 3.3V (3.0–3.6V)
Operating Temp	0–+70°C
Storage Temp	-20–125°C
Humidity	5%–90%
Dimensions	21×23×2.4mm (±0.2mm)

V. Hardware Block Diagram

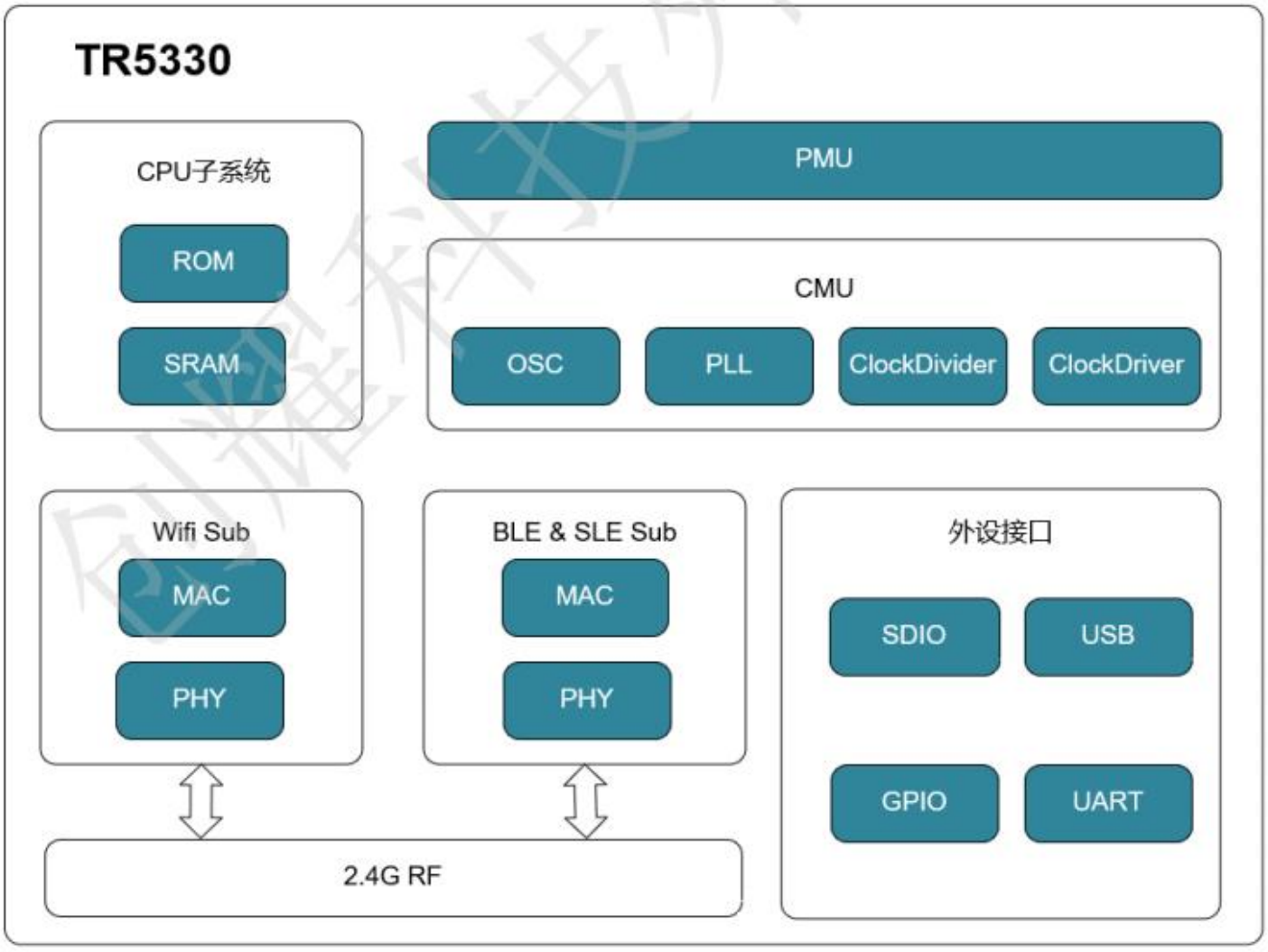

Figure 5-1 Hardware diagram of the FLC5330XSA-A

VI. Module Dimensions (Unit: mm)

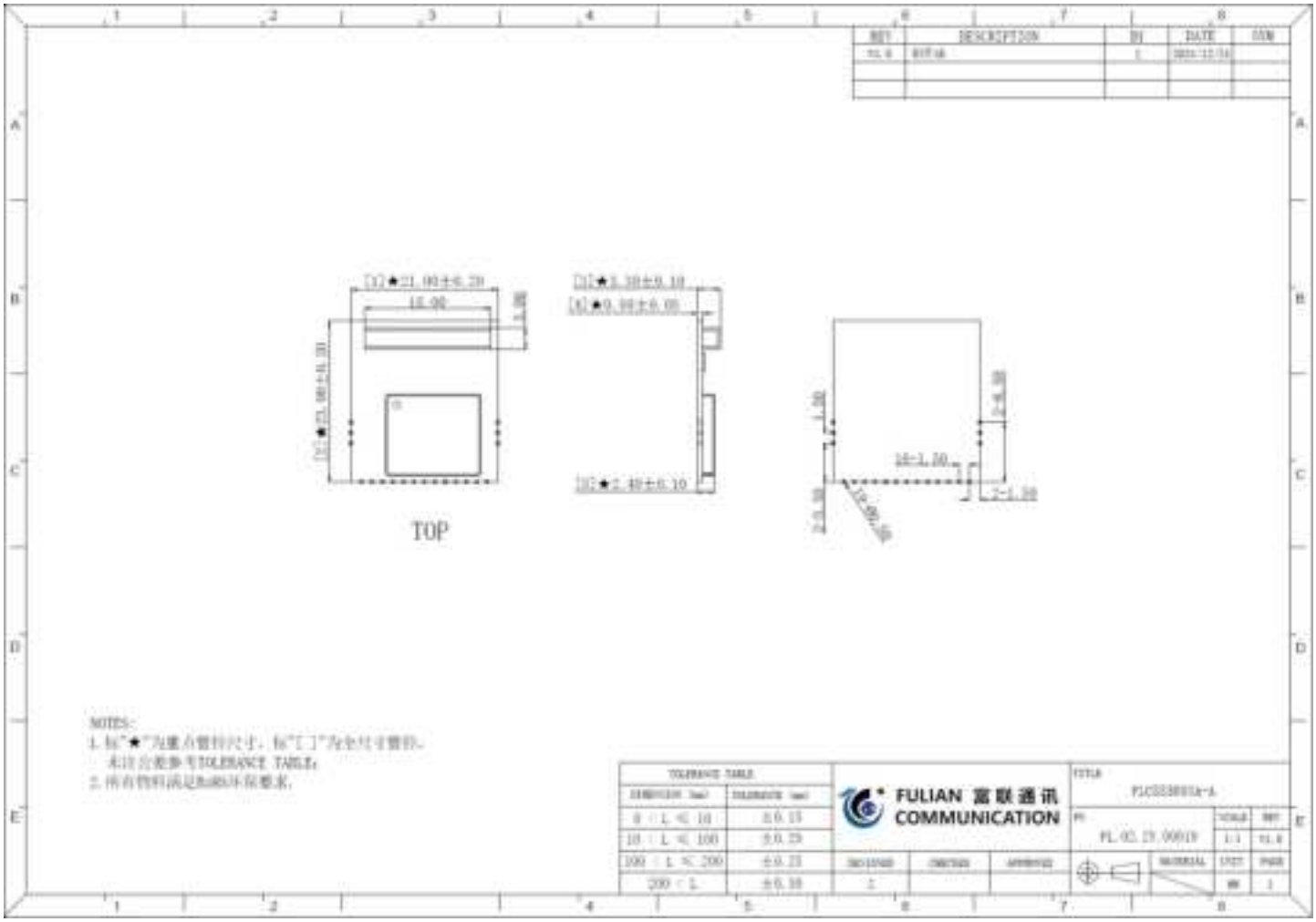

Figure 6-1 Dimensions of the FLC5330XSA-A

VII. Module Pin Definitions

Table 7-1: Pin Mapping Table

Pin No.	Pin Name	Description
1–3	GND	Ground
4	VBAT	3.3V Power
5	NC	Not Connected
6	VDDIO	IO Supply (1.8–3.3V, Max 3.6V)
7	GND	Ground
8	CHIP_EN	Chip Enable
9	INT/GPIO0	WL_DEV_WAKE_HOST
10	SD_D2	SD_D2
11	SD_D3	SD_D3

12	SD_CMD	SD_CMD
13	SD_CLK	SD_CLK
14	SD_D0	SD_D0
15	SD_D1	SD_D1
16-19	GND	GND

VIII. Electrical Parameters

8.1 Power Supply

Table 8-1 Power supply parameters

Symbol	Description	Condition	Detail			
			Min	Typ	Max	Unit
VBAT	Power Voltage	DC	3.0	3.3	3.6	V
VDDIO	IO Supply Voltage	DC	1.7	1.8/3.3	3.6	V

8.2 3.3V Digital IO Pin DC Parameters

Table 8-2 3.3V digital IO pin DC parameters

Symbol	Description	Condition	Detail			
			Min	Typ	Max	Unit
VIH	High-Level Input	DC	2.0	3.3	3.6	V
VIL	Low-Level Input	DC	0	0	0.9	V
VOH	High-Level Output	DC	2.97	-	3.3	V
VOL	Low-Level Output	DC	0	-	0.33	V

IX. Interface Timing Diagrams

9.1 Power-Up/Power-Down Timing

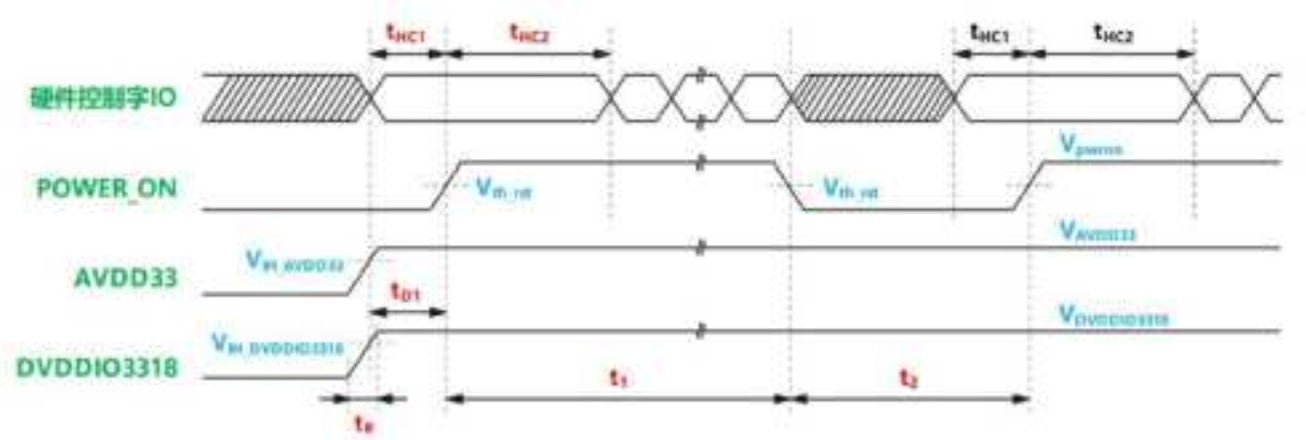

Figure 9-1 Power-on sequence

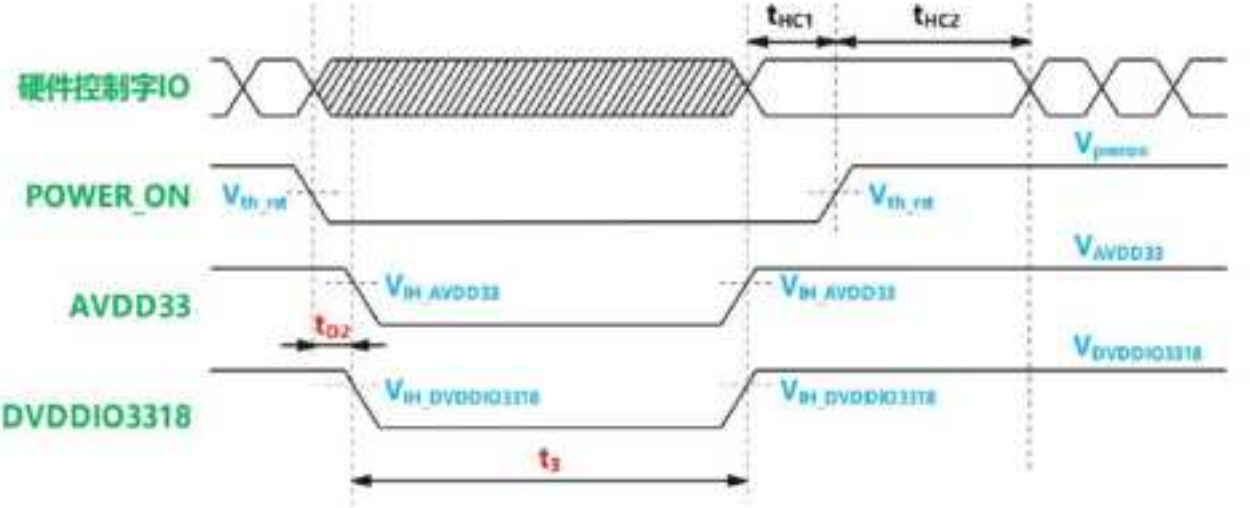

Figure 9-2 Power-off sequence

Timing Parameters

Table 9-1 Time parameters

No	**Parameters**	**Description**	**Min**	**Max**	**Unit**
t_1	POWER_ON High Duration		20	-	ms
t_2	Clock Low Time	Default	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	Default	10	-	ns
		HS	7	-	ns
T_{ISU}	Input build time	Default	5	-	ns
		HS	6	-	ns
T_{IH}	Input hold time	Default	5	-	ns
		HS	2	-	ns

T_{ODLY}	Output delay time	Default	-	14	ns
		HS	-	14	ns

Voltage parameter description

Table 9-2 Voltage parameters

No	**Parameters**	**Description**	**Min**	**Max**	**Unit**
t_1	High level duration of the POWER ON after power-on	-	20	-	ms
t_2	Clock low time	Default	10	-	ns
		HS	7	-	ns
T_{WH}	Clock high level time	Default	10	-	ns
		HS	7	-	ns
T_{ISU}	Input build time	Default	5	-	ns
		HS	6	-	ns
T_{IH}	Input hold time	Default	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output delay time	Default	-	14	ns
		HS	-	14	ns

9.2 SDIO Port Timing Diagram

SDIO supports 3 SDIO working modes：

- Default speed mode（DS）

  The interface clock frequency is up to 25MHz, including 1bit and 4bit modes.

- High speed modes（HS）

  The maximum clock frequency of the interface is 50MHz.

- SDR12，SDR25 modes

The maximum frequency of the interface clock is 25MHz and 50MHz respectively.

Default speed mode

The Default speed mode is the default mode after the SDIO is powered on. To ensure compatibility with various HOST devices, this mode requires a low working rate and only supports 25MHz.

Table 9-3 Clock parameters in Default speed mode (DVDDIO=3.3V)

Parameter	Symbol	Min	Max	Unit	Remarks
Clock CLK （All value are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	25	MHz	C_{CARD}≤10pF
Clock frequency Identification Mode	f_{OD}	-	400	KHz	C_{CARD}≤10pF
Clock low time	t_{WL}	10	-	ns	C_{CARD}≤10pF
Clock high time	t_{WH}	10	-	ns	C_{CARD}≤10pF
Clock rise time	t_{TLH}	-	10	ns	C_{CARD}≤10pF
Clock fall time	t_{THL}	-	10	ns	C_{CARD}≤10pF

The data required by the SDIO interface is stable time before clock sampling, and tIH is the holding time, that is, the time for the data required by the SDIO interface to maintain the original level after clock sampling in this mode.

Input mode timing diagram: tISU is the establishment time, that is, the stable time of the data required by the SDIO interface before clock sampling in this mode; tIH is the hold time, that is, the time of the data required by the SDIO interface to maintain the original level after clock sampling in this mode

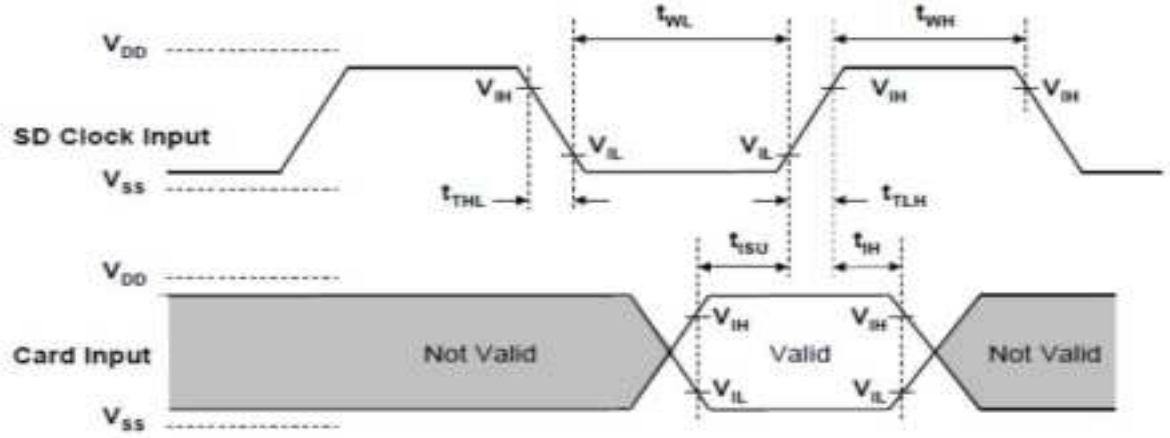

Figure 9-3 Timing diagram of the Default speed input mode

Output mode timing diagram and constraints:

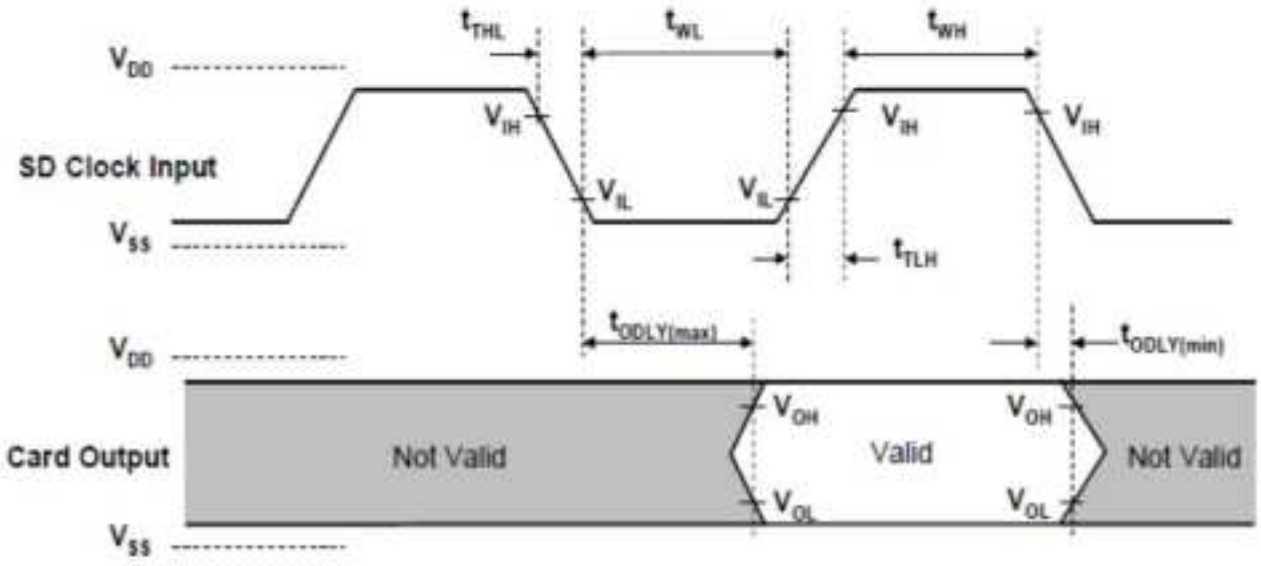

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Figure 9-4 Timing diagram of Default speed output mode

Table 9-4 Timing constraints on the Default speed mode

Parameter	Symbol	Min	Max	Unit	Remarks
Inputs CMD,DAT （referred to CLK)					
Input set-up time	t_{ISU}	5	-	ns	C_{CARD}≤10pF
Input hold time	t_{IH}	5	-	ns	C_{CARD}≤10pF
Outputs CMD,DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	C_L≤40pF
Output Delay time during Identification Mode	t_{ODLY}	-	50	ns	C_L≤40pF

Note: Tclk indicates the period of the SDIO CLOCK

High speed mode

High speed mode Indicates the mode switching mode that the SDIO enters after being powered on and initialized to use a higher rate. This mode requires a higher working rate than the default speed mode, and its clock supports 50MHz. The time sequence of input data in High speed mode is shown in the following figure, where tISU is the establishment time, that is, the stable time before the clock sampling required by the SDIO interface in this mode; tIH is the hold time, that is, the time when the data required by the SDIO interface in this mode remains at the original level after the clock sampling.

High speed mode Input timing:

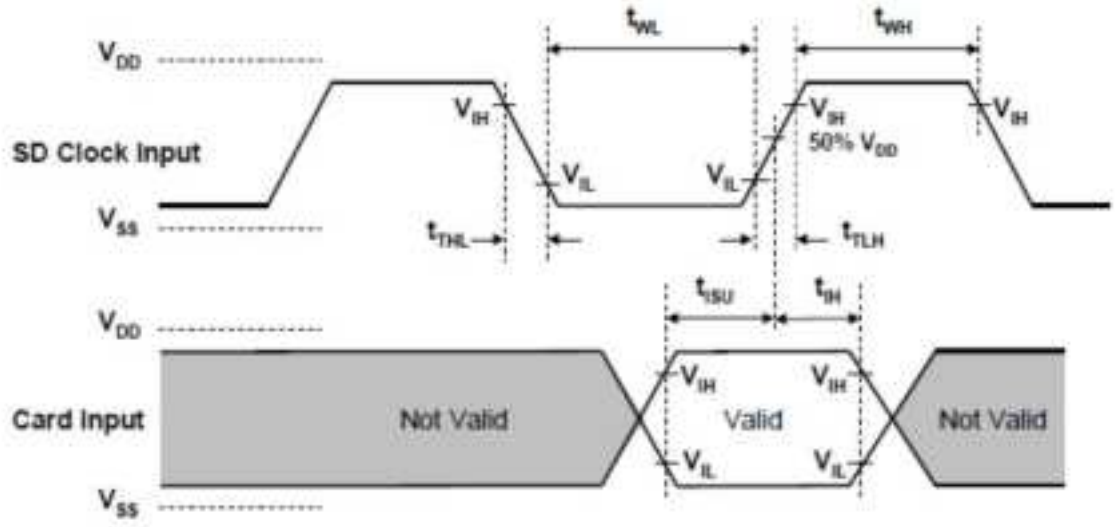


Figure 9-5 Timing diagram of input in High speed mode

Clock parameter table：

Table 9-5 Clock parameters in High speed mode (DVDDIO=3.3V)

Parameter	Symbol	Min	Max	Unit	Remarks
Clock CLK (All value are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	C_{CARD}≤10pF
Clock low time	t_{WL}	7	-	ns	C_{CARD}≤10pF
Clock high time	t_{WH}	7	-	ns	C_{CARD}≤10pF
Clock rise time	t_{TLH}	-	3	ns	C_{CARD}≤10pF
Clock fall time	t_{THL}	-	3	ns	C_{CARD}≤10pF

The output data sequence of High speed mode is shown in the figure below. Where, tODLY (max) is the maximum time delay for the output data to appear on the interface with respect to the rising edge of the clock, and tOH is the minimum time delay

for the output data to appear on the interface with respect to the rising edge of the clock.

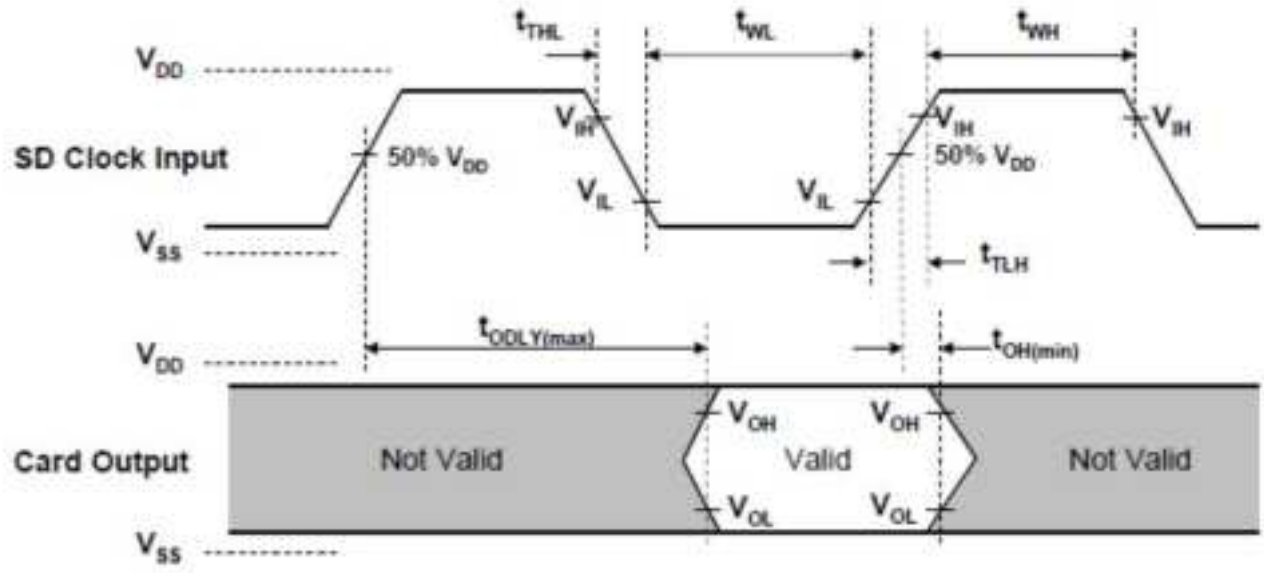


Figure 9-6 Output sequence in High speed mode

Table 9-6 Timing constraints for High speed mode (DVDDIO=3.3V)

Parameter	Symbol	Min	Max	Unit	Remarks
Inputs CMD, DAT （referred to CLK）					
Input set-up time	t_{ISU}	6	-	ns	$C_{CARD} \leq 10pF$
Input hold time	t_{IH}	2	-	ns	$C_{CARD} \leq 10pF$
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	$C_L \leq 40pF$
Output Hold time	t_{OH}	2.5	-	ns	$C_L \leq 15pF$
Total System Capacitance for each line	C_L	-	40	pF	1 card

Note: High speed mode data signal timing, its output data and input data are based on the rising edge of the clock as a reference.

SDR12 and SDR25 modes

The maximum clock frequency in SDR12 mode is 25MHz, and the maximum clock frequency in SDR25 mode is 50MHz.

Table 9-7 Clock parameters in SDR12 and SDR25 modes

Parameter	Min	Max	Unit	Remarks
t_{CLK}	20.0	-	ns	50 MHz(Max.)，V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	C_{CARD}=10pF。Any clock frequency, tCR, tCF maximum should be less than 10ns.
Clock Duty	30	70	%	-

SDR12, SDR25 mode input timing:

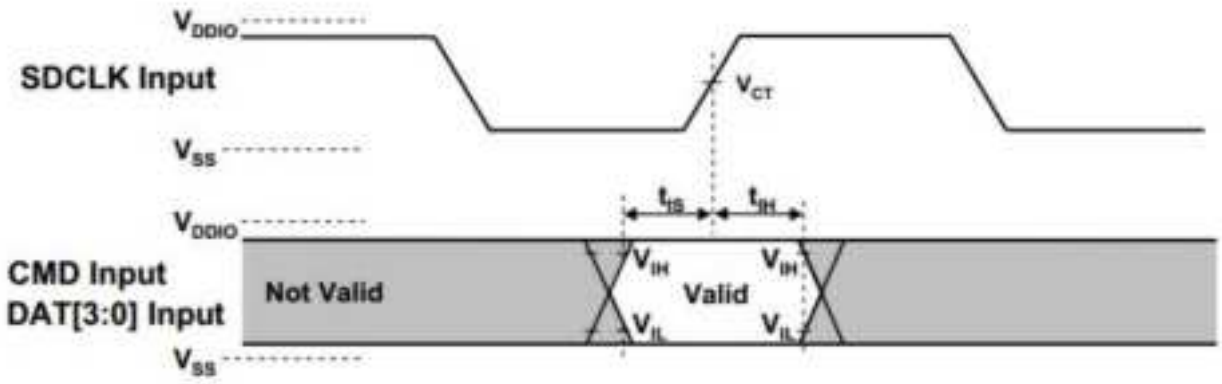


Figure 9-7 Timing diagram of input in SDR12 and SDR25 mode

SDR12, SDR25 mode input timing constraint table：

Table 9-8 Constraints on the input sequence of SDR12 and SDR25 modes

Symbol	Min	Max	Unit	Remarks
t_{IS}	3	-	ns	C_{CARD}≤10pF，V_{CT}=0.975V
t_{IH}	0.8	-	ns	C_{CARD}≤5pF，V_{CT}=0.975V

SDR12, SDR25 mode output sequence：

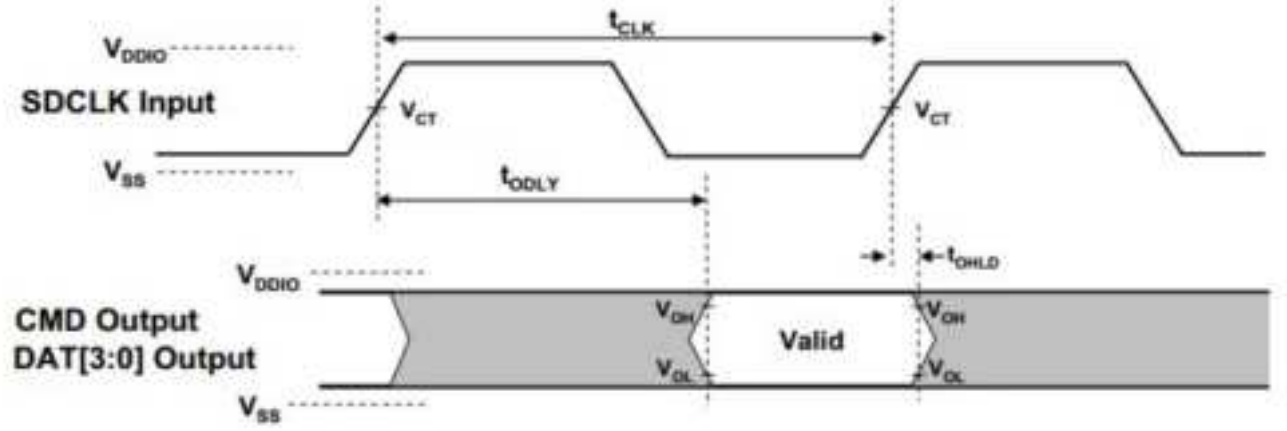


Figure 9-8 Output sequence of SDR12 and SDR25 modes

SDR12，SDR25 模式输出时序约束表：

Table 9-9 Constraints on the output sequence of SDR12 and SDR25 modes

Symbol	Min	Max	Unit	Remarks
t_{ODLY}	-	14	ns	t_{CLK}≥20.0ns，C_L=40pF，using driver Type B
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY}（min.），CL=15pF

X. Radio frequency indicators：

1. Test indicators of BLE TX/RX

Sort	Index	Concrete item	Index value
TX	Output Power	Output Power（dBm	8±2
	CarrieFreq offset&drift （LE1M&LE2M）	Freq offset（kHz）	≤150
		Initial freq drift（kHz	≤23
	Modulation characteristic（LE1M）	△f1avg（kHz）	225≤x≤275
		△f2avg（kHz）	＞185
		△f2avg/△f1avg	≥0.8
	Modulation characteristic（LE2M）	△f1avg（kHz）	450≤x≤550
		△f2avg（kHz）	＞370
		△f2avg/△f1avg	≥0.8
	In-band Spurious Emission（LE1M）	±2M offset（dBm)	≤-20
		≥3MHz offset（dBm	≤-30
		≤-3MHz offset（dBm	≤-30
	In-band Spurious Emission （LE2M）	±4M offset（dBm）	≤-20
		≥6MHz offset（dBm	≤-30
		≤-6MHz offset（dBm	≤-30
RX	Sensitiviy	LE1M（dBm）	≤-70
		LE2M（dBm）	≤-70

2. SLE TX/RX test indicators

Sort	Index	Concrete item	Index value
TX	Output Power	GFSK 1M/2M/4M （dBm）	8±2
		QPSK（dBm）	8±2
		8PSK（dBm）	8±2
	CarrierFreq ffset&drift	Freq offset（kHz）	≤150
		Initial freq drift（kHz）	≤23
	Modulation characteristic （GFSK 4M）	△f1avg（kHz）	900≤x≤1100
		△f2avg（kHz）	＞740
		△f2avg/△f1avg	≥0.8
	TX EVM（QPSK	RMS EVM	≤13%
		99% EVM	≤28%
		Peak EVM	≤32%
	In-band Spurious Emission（GF SK 4M）	±7M offset（dBm）	≤-20
		≥10MHz offset（dBm）	≤-30
		≤-10MHz offset（dBm）	≤-30
	In-bandSpur ious EmissionPS K 2M	|Δf|=2MHz	≤-26
		2.5MHz≤|Δf|≤5.5MHz	≤-20
		|Δf|>5.5MHz	≤-35
	In-band Spurious Emission PSK 4M	|Δf|=4MHz	≤-26
		3.5MHz≤|Δf|≤7.5MHz	≤-20
		|Δf|>7.5MHz	≤-35
RX	Sensitiviy	SLE 4M GFSK（dBm）	-67
		SLE 2M QPSK（dBm）	-70
		SLE 4M QPSK（dBm）	-67

3. WiFi TX/RX test indicators

Agreement	Speed	Power（dBm	EVM	Sensitivity
11b	1M	20.00	≤-15	-98.00
	2M	20.00	≤-15	-95.00
	5.5M	20.00	≤-15	-92.00
	11M	20.00	≤-15	-89.00
11g2g20	6Mbps	19.00	≤-7	-94.00
	9Mbps	19.00	≤-10	-92.00
	12Mbps	19.00	≤-12	-91.00
	18Mbps	19.00	≤-15	-89.00
	24Mbps	18.00	≤-18	-86.00
	36Mbps	18.00	≤-21	-62.00
	48Mbps	17.00	≤-25	-78.00
	54Mbps	16.00	≤-27	-76.00
11n2g20	MCS0	19.00	≤-7	-94.00
	MCS1	19.00	≤-12	-90.00
	MCS2	19.00	≤-15	-88.00
	MCS3	19.00	≤-18	-85.00
	MCS4	18.00	≤-21	-81.00
	MCS5	17.00	≤-24	-77.00
	MCS6	16.00	≤-27	-75.00
	MCS7	15.00	≤-29	-74.00
11n2g40	MCS0	19.00	≤-7	-91.00

	MCS1	19.00	≤-12	-87.00
	MCS2	19.00	≤-15	-85.00
	MCS3	19.00	≤-18	-82.00
	MCS4	18.00	≤-21	-79.00
	MCS5	17.00	≤-24	-75.00
	MCS6	16.00	≤-27	-72.00
	MCS7	15.00	≤-29	-71.00
11ax2g20	MCS0	19.00	≤-7	-95.00
	MCS1	19.00	≤-12	-91.00
	MCS2	19.00	≤-15	-89.00
	MCS3	19.00	≤-18	-86.00
	MCS4	18.00	≤-21	-82.00
	MCS5	17.00	≤-24	-78.00
	MCS6	16.00	≤-27	-77.00
	MCS7	15.00	≤-29	-75.00
	MCS8	14.00	≤-32	-72.00
	MCS9	14.00	≤-34	-69.00

XI. Reflow Soldering Temperature Profile

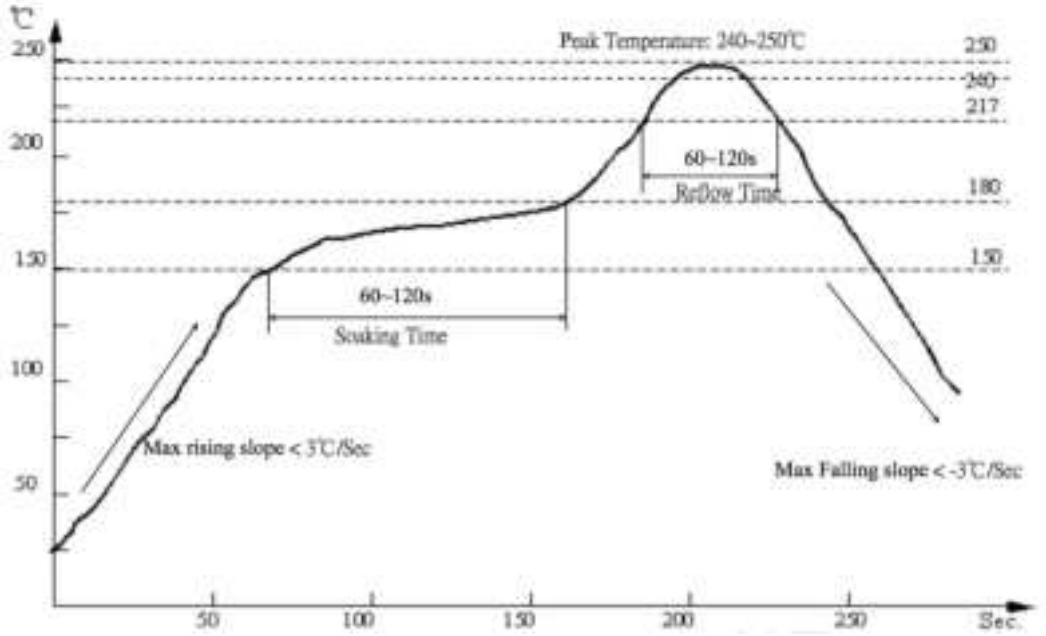


Figure 10-1 FLC5330XSA-A reflow soldering temperature diagram

XII. Packaging & Storage

It is shipped by coil packaging, which is convenient for customers to SMT, built-in humidity card and desiccant, electrostatic bag vacuum, and carton packaging, and the coil and the outer box are pasted with factory notes and the inspection of the warehouse two-dimensional code, which is easy to track and cross goods.

Figure 11-1 Packaging of FLC5330XSA-A

Announcements

- The operators at all stations must wear electrostatic gloves during the whole process of production.
- The copper needs to be removed from the bottom plate corresponding to the red area in Figure 2. The larger the area, the less the impact on the antenna and the better the performance.
- During operation, ensure that the bottom surface of the module is protected from water or dirt;
- If the unpacking time exceeds 3 months, it is prohibited to use SMT process to weld this batch of modules, because PCB metal-sinking process, the pad oxidation is serious after 3 months, the SMT patch is very likely to lead to false welding, welding failure, and our company will not be responsible for all kinds of problems caused by this;
- Before installing the SMT, protect the module with ESD discharge.
- Please apply the SMT patch according to the reflow soldering curve, the peak temperature is 245℃, the reflow soldering temperature curve is shown in the figure.
- In order to ensure the qualified rate of reflow soldering, 10% of the first SMT products should be selected for visual inspection and AOI detection to ensure the reasonableness of furnace temperature control, device adsorption method and placement method; After mass production, it is recommended to extract 5-10 pieces per hour for visual inspection and AOI testing.

Storage conditions and ESD prevention

Figure 11-2 FLC5330XSA-A storage conditions and ESD prevention instructions

Sales and technical support information

If you need to consult or purchase this product, please call Jiangsu Fu Unicom Communication Technology Co., LTD during office hours.

Office hours: Monday to Saturday, 8:00 am to 12:00 PM, 13:00 PM to 17:00 PM

postcode：212310

phone： 0511-80760088

Email: sales@fulian-link.com

Address: Fulianxun Industrial Park, Lanling Road, Economic and Technological Development Zone, Danyang City, Jiangsu Province

FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This modular has been tested and found to comply with part 15 requirements for Modular Approval.
FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01r01

2.2 List of applicable FCC rules

CFR 47 FCC Part 15 Subpart C and Subpart F has been investigated. It is applicable to the modular transmitter

2.3 Specific Operational Use Conditions - Antenna Placement Within the Host Platform

The module is tested for standalone mobile RF exposure use condition.
The antenna must be installed such that 20cm is maintained between the antenna and users,
The transmitter module may not be co-located with any other transmitter or antenna.
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

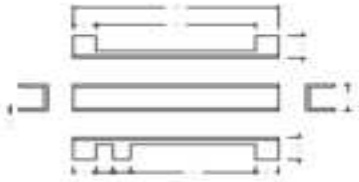
2.4 Limited Module Procedures

Not Applicable.

2.5 Trace Antenna Designs

Metal Antenna specification
Below is Metal antenna specification
You can see antenna size is 18(L)mm*3.0(W)mm*2.5(T)mm From below specification.

Antenna Dimensions



2.6 RF Exposure Considerations

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should beinstalled and operated with minimum distance 20cm between the radiator & your body.

2.7 Antenna Type and Gain

The following antennas have been certified for use with this module.
Only antennas of the same type with equal or lower gain may also be used with this module.
Other types of antennas and/or higher gain antennas may require the additional authorization for operation.
Antenna Specification list below:

Antenna Type	Antenna Model No.	Maximum Antenna Gain(dBi)	Frequency Range(MHz)
Metal antenna	FLC5330XSA-A	3.1	2400-2500

2.8 End Product Labelling Compliance Information

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily removed. If not, a second label must be placed on the outside of the final device that contains the following text: " Contains FCC ID: 2AXS5-FLC5330XSA-A" . The FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on Test Modes and Additional Testing Requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) class II permissive change re-evaluation or new FCC authorization.
Host manufacturer installed this modular with single modular approval should perform the test of radiated emission and spurious emission according to FCC part 15C, 15.209, 15.207 requirement, only if the test result comply with FCC part 15C, 15.209, 15.207 requirement, then the host can be sold legally.

2.10 Additional testing, Part 15 Subpart B Disclaimer

This transmitter modular us tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B rules requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rules requirements if applicable. As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this modular installed.

2.11 Manual Information to The End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user' s manual of the end product which integrates this module.
The host integrator must follow the integration instructions provided in this document and ensure that the composite system end product complies with the requirements by a technical assessment or evaluation to the rules and to KDB Publication 996369.
The host integrator installing this module into their product must ensure that the final composite product complies with the requirements by a technical assessment or evaluation to the rules, including the transmitter operation and should refer to guidance in KDB Publication 996369.

OEM/Host Manufacturer Responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and RF Exposure essential requirements of the FCC rules.

2.12 How to Make Changes - Important Note

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.