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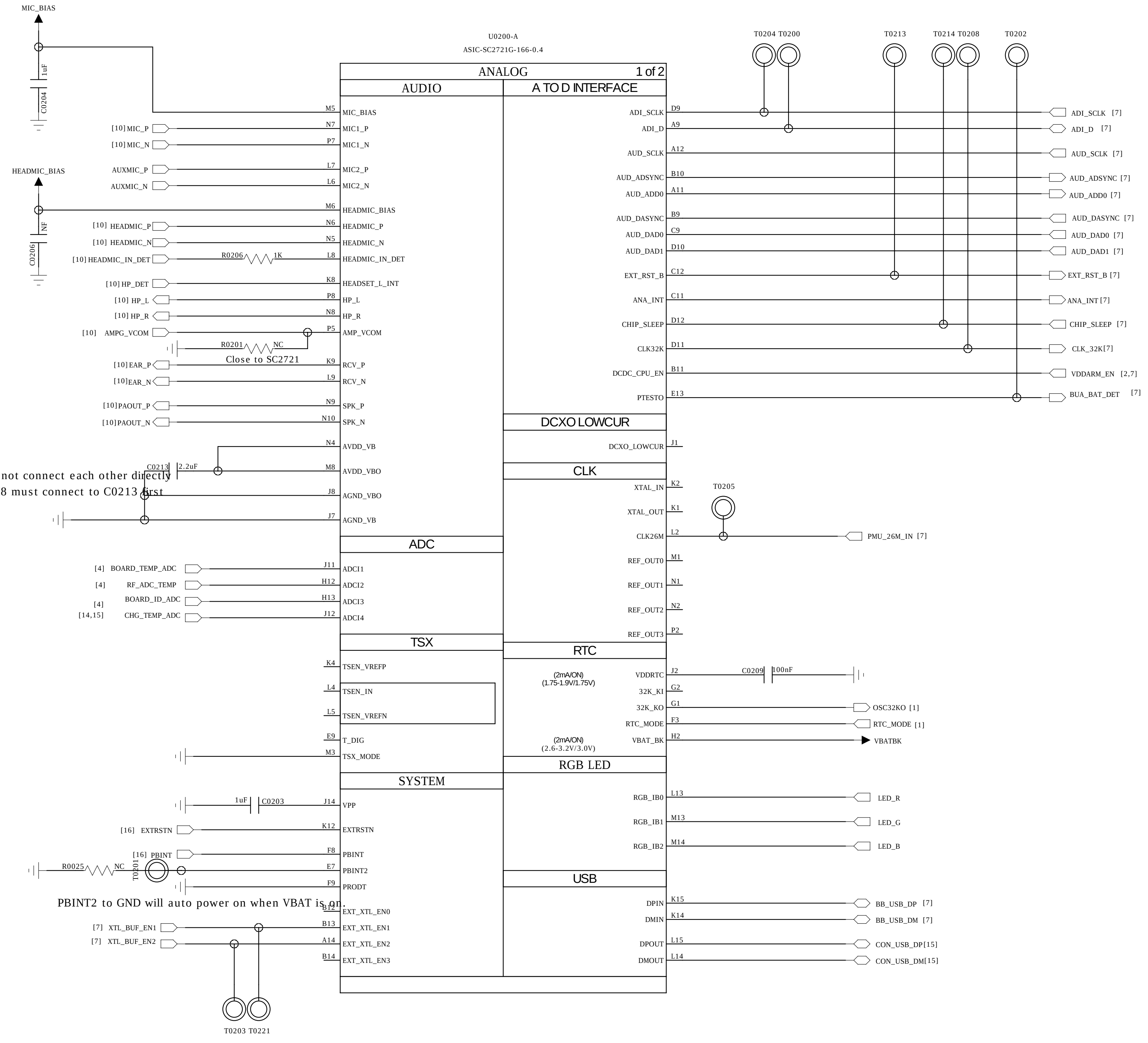
D

# PMU_ANALOG

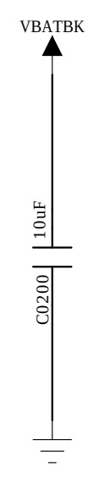


Close to SC2721

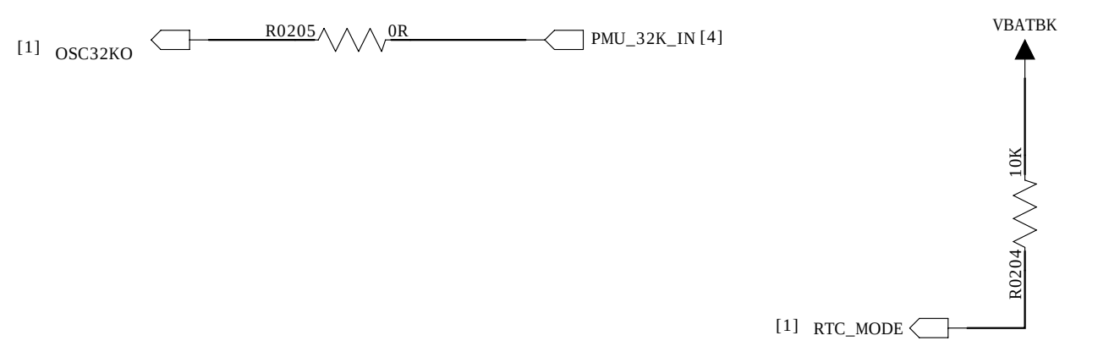
N4 and M8 can not connect each other directly
N4 and M8 must connect to C0213 first

PBINT2 to GND will auto power on when VBAT is on.

# BKBT



# RTC



| RTC MODE | |
|---|---|
| HIGH | 32K-LESS |
| LOW | 32K Crystal |

| RTC Mode | Type | R0202 | R0205 | X0200 | C0201 | C0202 | R0203 | R0204 | |
|---|---|---|---|---|---|---|---|---|---|
| 32K Crystal | Option | 0R | NF | Crystal | 8.2pF | 8.2pF | 0R | NF | |
| 32K-less | Default | NF | 0R | NF | NF | NF | NF | 10K | |

Note:32K-less only use in TSX mode,32K crystal is only use in TCXO mode.

C

B

A

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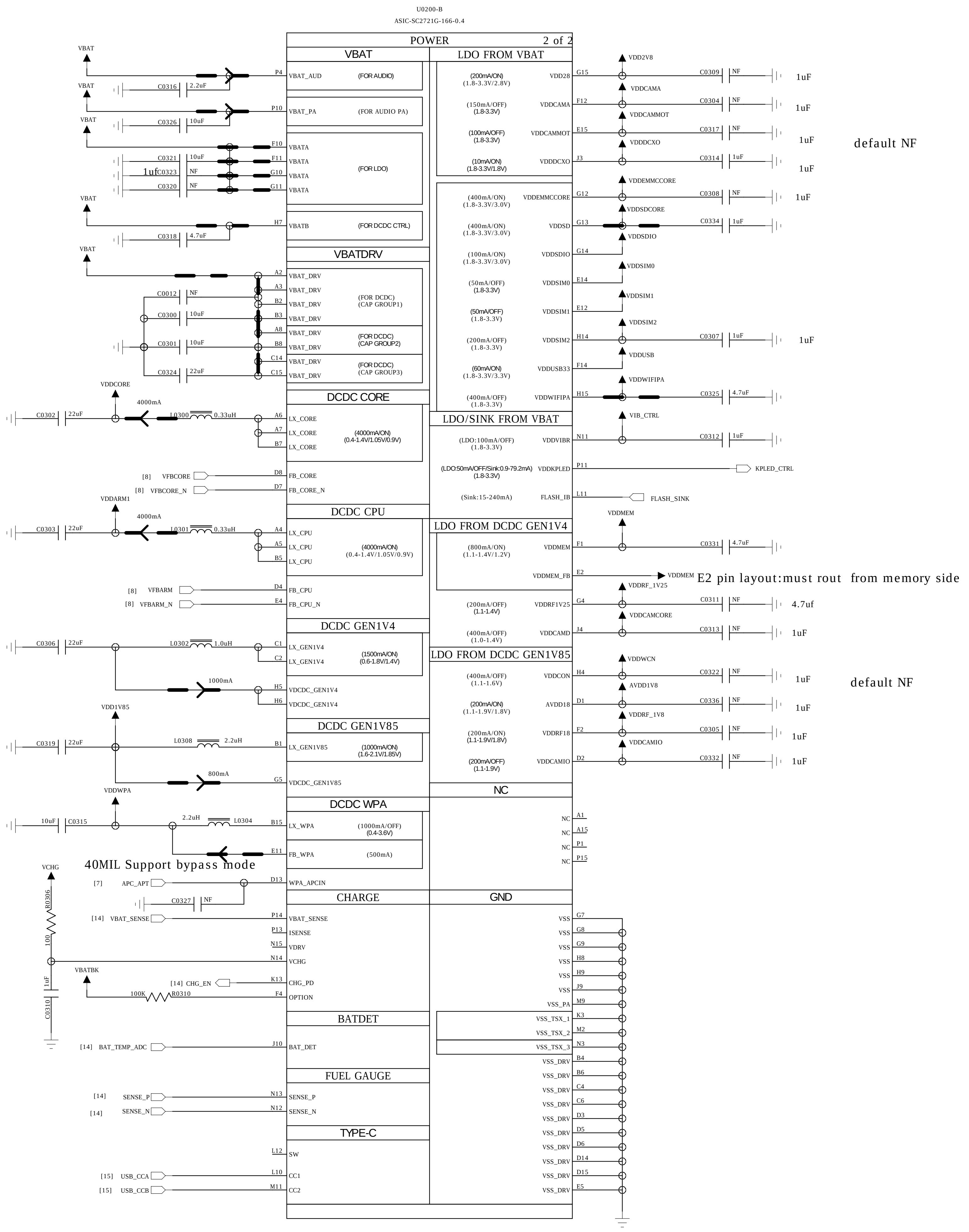
# PMU_POWER

| INPUT | Description |
|---|---|
| VBAT_AUD | VBAT power input for audio |
| VBAT_PA | VBAT power input for audio speaker PA |
| VBATA | VBAT power input for LDO |
| VBATB | VBAT power input for KP_LED,VIB,VBATBK,Flash LED |
| VBATC | VBAT power input for LDO |
| VBAT_DRV | VBAT power input for DCDC |



default NF

E2 pin layout:must rout from memory side

default NF

40MIL Support bypass mode

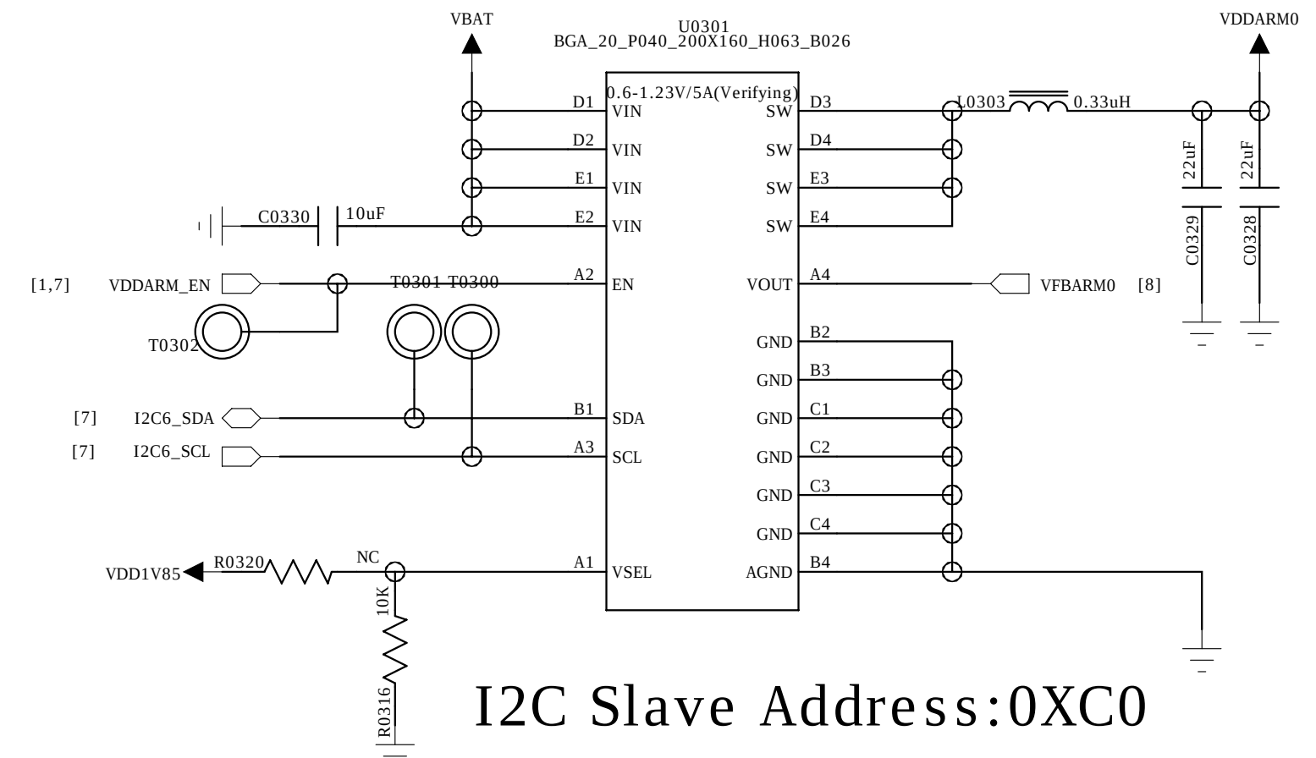
## SC2721 DCDC output

| Input Power | Power Name | Output Voltage (V) | Output Current | Default Voltage | Default |
|---|---|---|---|---|---|
| VBAT | DCDCCPU | 0.4-1.4/1.05/0.9 | 4000mA | 0.9V | ON |
| | DCDCCORE | 0.4-1.4/1.05/0.9 | 4000mA | 0.9V | ON |
| | DCDCGEN1V4 | 0.6-1.8 | 1500mA | 1.4V | ON |
| | DCDCGEN1V85 | 1.6-2.1 | 1000mA | 1.85V | ON |
| | DCDCWPA | 0.4-3.6 | 1000mA | | OFF |

## SC2721 LDO output

| Input Power | Power Name | Output Voltage (V) | Output Current | Default Voltage | Default |
|---|---|---|---|---|---|
| LDO from VBAT | VDDCAMA | 1.8-3.3 | 150mA | 2.8V | OFF |
| | VDDCAMMOT | 1.8-3.3 | 100mA | 2.8V | OFF |
| | VDDSIM0 | 1.8-3.3 | 50mA | 1.8V | OFF |
| | VDDSIM1 | 1.8-3.3 | 50mA | 1.8V | OFF |
| | VDDSIM2 | 1.8-3.3 | 200mA | 1.8V | OFF |
| | VDD28 | 1.8-3.3 | 200mA | 2.8V | ON |
| | VDDEMMCCORE | 1.8-3.3 | 400mA | 3.0V | ON |
| | VDDSDCORE | 1.8-3.3 | 400mA | 3.0V | ON |
| | VDDSDIO | 1.8-3.3 | 100mA | 3.0V | ON |
| | VBATBK | 2.6-3.2 | 2mA | 3.0V | ON |
| | VDDVIB | 1.8-3.3 | 100mA | 3.3V | OFF |
| | VDDKPLED | 1.8-3.3 | LDO:50mA/Sink:0.9-79.2mA | | |
| | VDDWIFIPA | 1.8-3.3 | 400mA | 3.3V | OFF |
| | VDDDCXO | 1.8-3.3 | 10mA | 1.8V | ON |
| | VDDUSB33 | 1.8-3.3 | 60mA | 3.3V | ON |
| LDO from DCDC GEN1V4 | VDDCAMD | 1.0-1.4 | 400mA | | OFF |
| | VDDRF1V25 | 1.1-1.4 | 200mA | | OFF |
| | VDD_MEM | 1.1-1.4 | 800mA | 1.2V | ON |
| LDO from DCDC GEN1V85 | VDDCAMIO | 1.1-1.9 | 200mA | | OFF |
| | AVDD18 | 1.1-1.9 | 200mA | 1.8V | ON |
| | VDDRF18 | 1.1-1.9 | 200mA | 1.8V | ON |
| | VDD_CON | 1.1-1.6 | 400mA | | OFF |

## EXT DCDC ARM



I2C Slave Address:0XC0
I2C-Compatible Interface Up to 3.4Mbps

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# V1.0 CHANGED 0825

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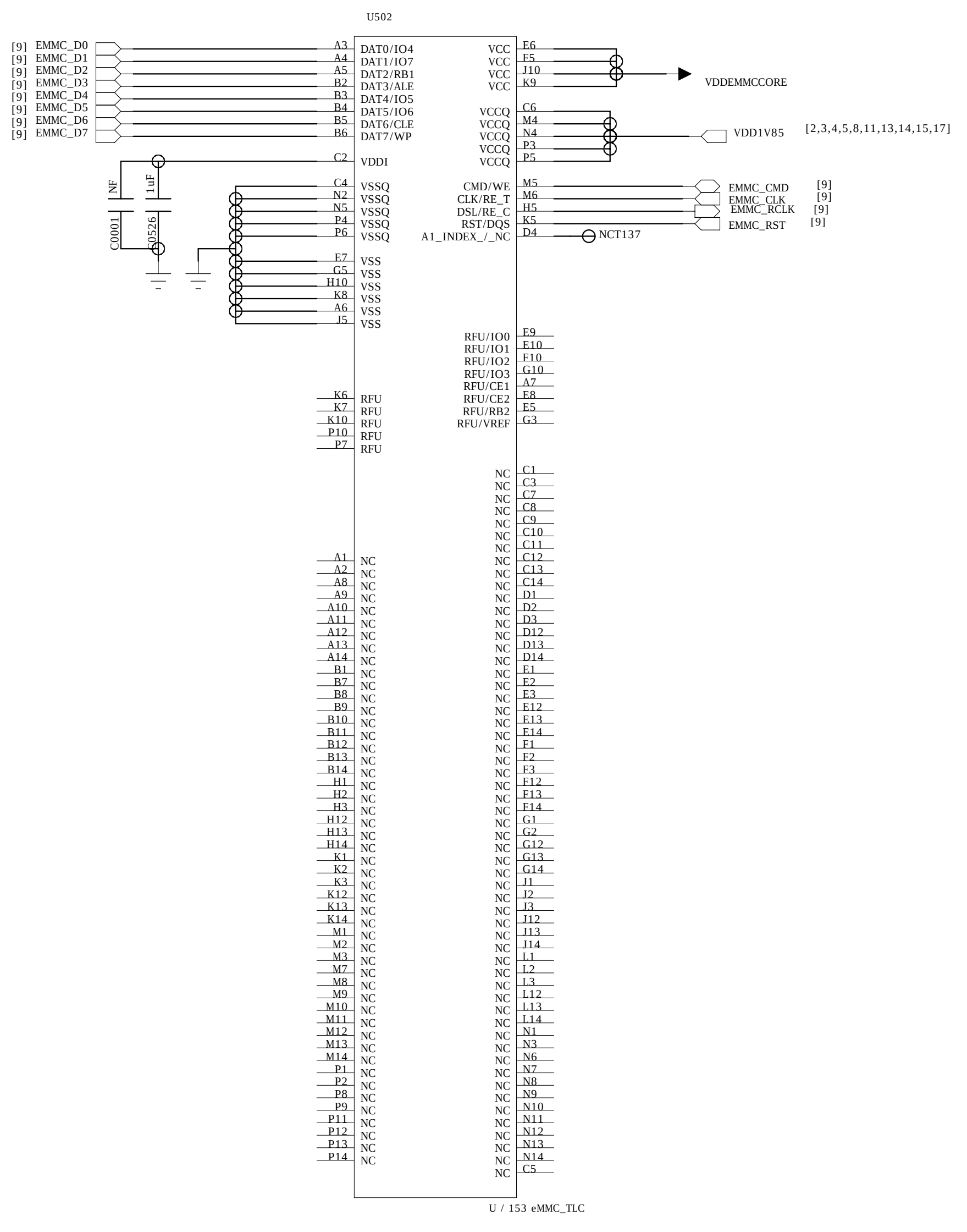
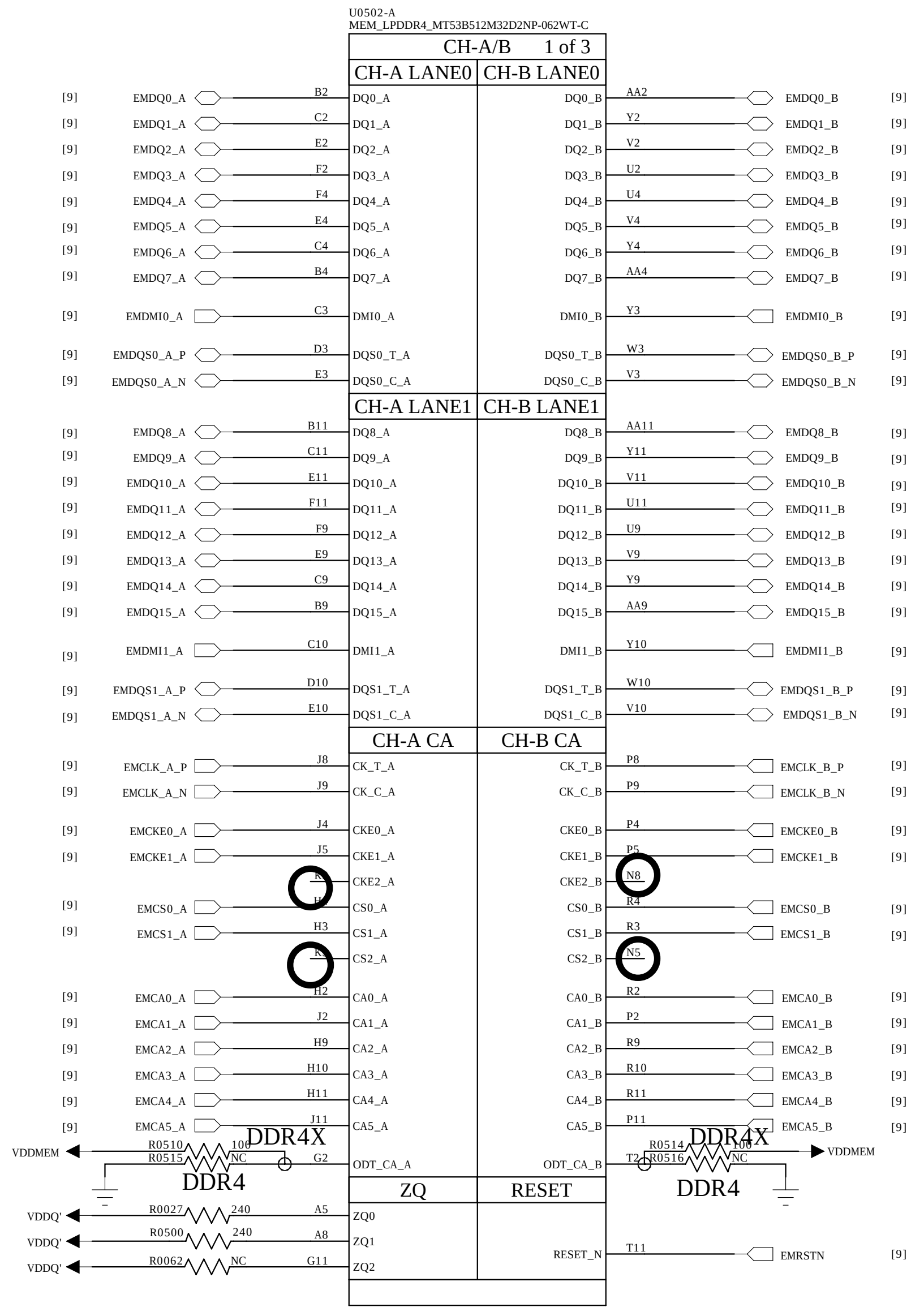
## eMMC+LPDDR3

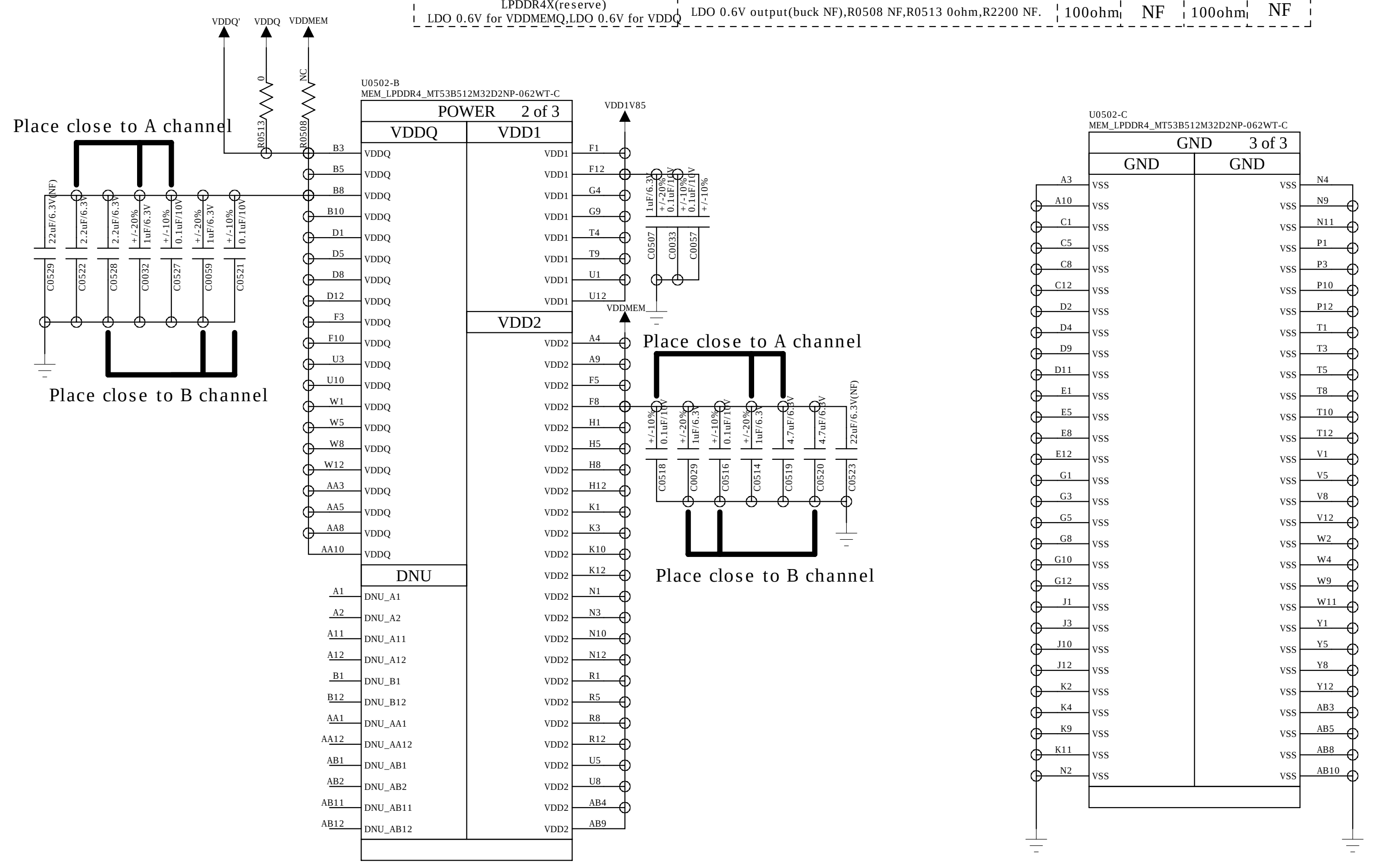


## Discrete LPDDR4(default)/Discrete LPDDR4X(backup)

Please refer to QVL table to select LPDDR4(X) was verified by us.

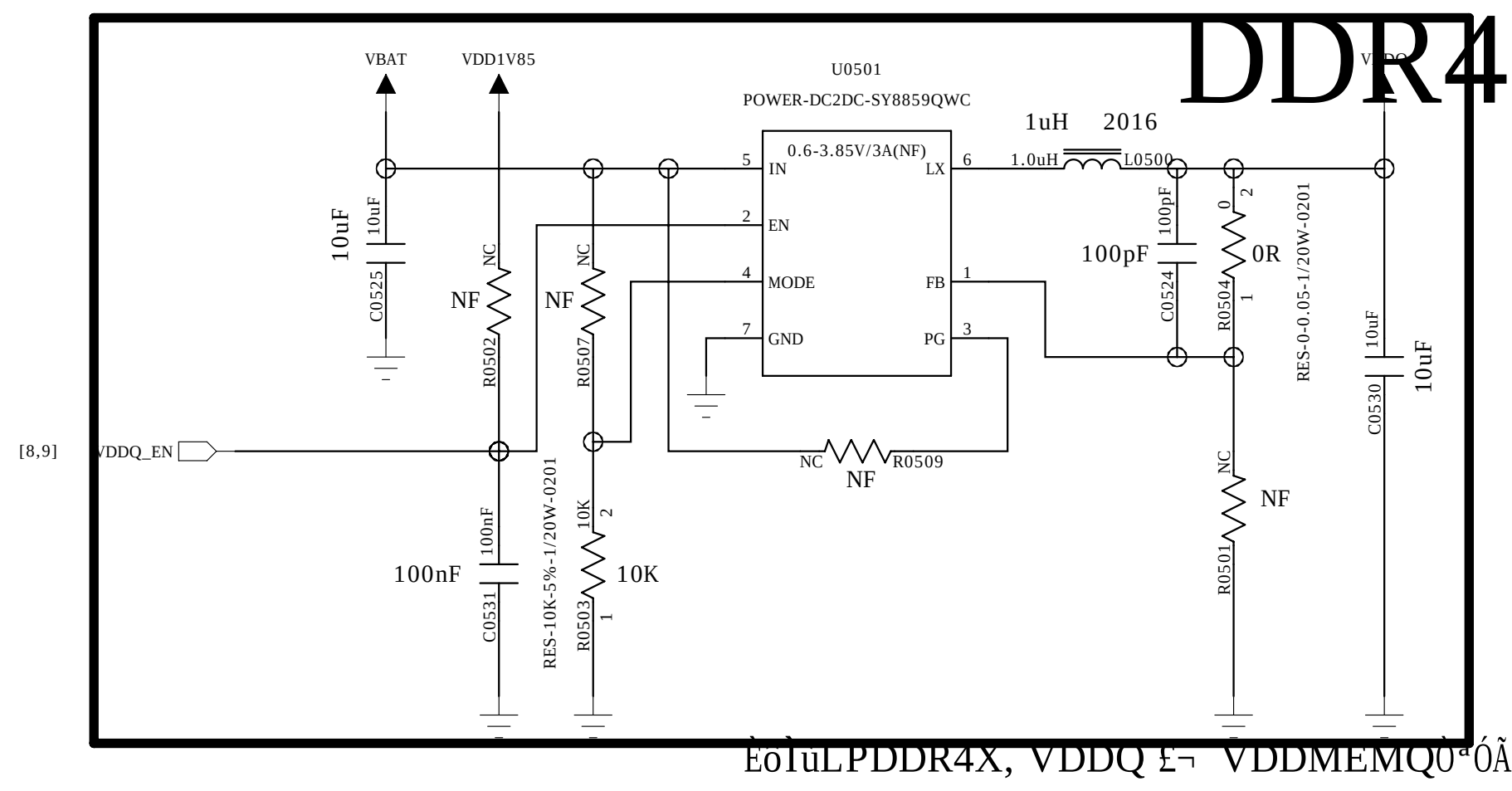
| Memory VDDQ&BB VDDMEMQ power source selection | | ODT pull high or pull low | | | |
|---|---|---|---|---|---|
| | | R0510 | R0515 | R0514 | R0516 |
| LPDDR4(default)<br>LDO 0.9V for VDDMEMQ,PMIC 1.1V for VDDQ | LDO 0.9V output(buck NF),R0508 0ohm,R0513 NF,R2200 NF. | NF | 100ohm | NF | 100ohm |
| LPDDR4(reserve)<br>BUCK 0.9V for VDDMEMQ,PMIC 1.1V for VDDQ | BUCK 0.9V output(LDO NF),R0508 0ohm,R0513 NF,R2200 NF. | NF | 100ohm | NF | 100ohm |
| LPDDR4(reserve)<br>PMIC 1.1V for VDDMEMQ,PMIC 1.1V for VDDQ | BUCK&LDO NF,R0508 0ohm,R0513 NF,R2200 0ohm.<br>Just reserve for this solution. | NF | 100ohm | NF | 100ohm |
| LPDDR4X(default)<br>BUCK 0.6V for VDDMEMQ,BUCK 0.6V for VDDQ | BUCK 0.6V output(LDO NF),R0508 NF,R0513 0ohm,R2200 NF. | 100ohm | NF | 100ohm | NF |
| LPDDR4X(reserve)<br>LDO 0.6V for VDDMEMQ,LDO 0.6V for VDDQ | LDO 0.6V output(buck NF),R0508 NF,R0513 0ohm,R2200 NF. | 100ohm | NF | 100ohm | NF |





## Buck default for VDDQ of LPDDR4X

DDR4È«²¿²»Ìù



ÈôÌùLPDDR4X, VDDQ £¬ VDDMEMQÒªÓÃ BUCK 0.6v ¹©µç

BUCK 0.6V output for BB VDDMEMQ and Memory VDDQ(LPDDR4X Default):

| C0525 | R0518 | R0502 | C0531 | R0507 | R0503 | R0509 | L0500 | C0524 | C0530 | R0504 | R0501 | U0501 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10UF | 0ohm | NF | 0.1UF | NF | 10K | NF | 1uH | 100pF | 10uF | 0ohm | NF | BUCK IC |

BUCK 0.9V output for BB VDDMEMQ(LPDDR4 reserve):

| C0525 | R0518 | R0502 | C0531 | R0507 | R0503 | R0509 | L0500 | C0524 | C0530 | R0504 | R0501 | U0501 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10UF | 0ohm | NF | 0.1UF | NF | 10K | NF | 1uH | 100pF | 10uF | 60K 1% | 120K 1% | BUCK IC |

R0504 value is half of R0501 to set output voltage as 0.9V.

²Î¿¼SPM:

SPM_SC9863A_SCH_V0.1.1_discrete_LPDDR4(X)_0201.sch

4X£¬0.6V¾ÍÓÃDCDC

# Discrete to EMCP£º

1£¬memory¸ÄÎª254ball EMCP£¬pinmux¶ÔÓ¦µ÷Õû
2£¬VDDQµçÔ´µ÷Õû£¬Ôö¼Ó0.6V DCDC£¬É¾³ý0.9VLDO
3£¬memoryÍâÎ§µçÈÝÎ¢µ÷
4£¬ODT¸ÄÎªÉÏÀ100Å·
5£¬Board ID0¸ÄÎªÉÏÀ£¬Óë·ÖÀëÊ½ÏÂÀ¿ÉÒÔÇø·Ö£¬Èí¼þ×ö×ÔÊÊÓ¦

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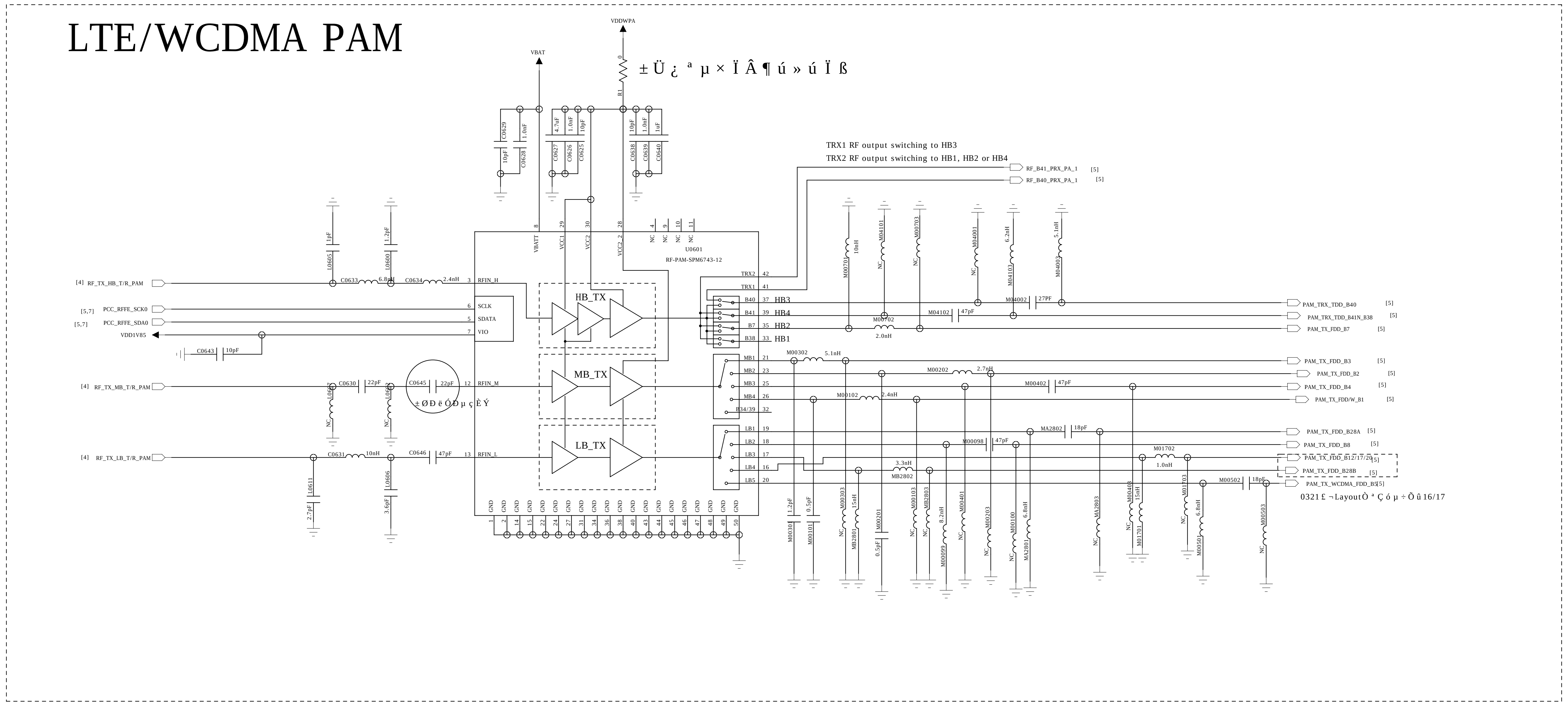
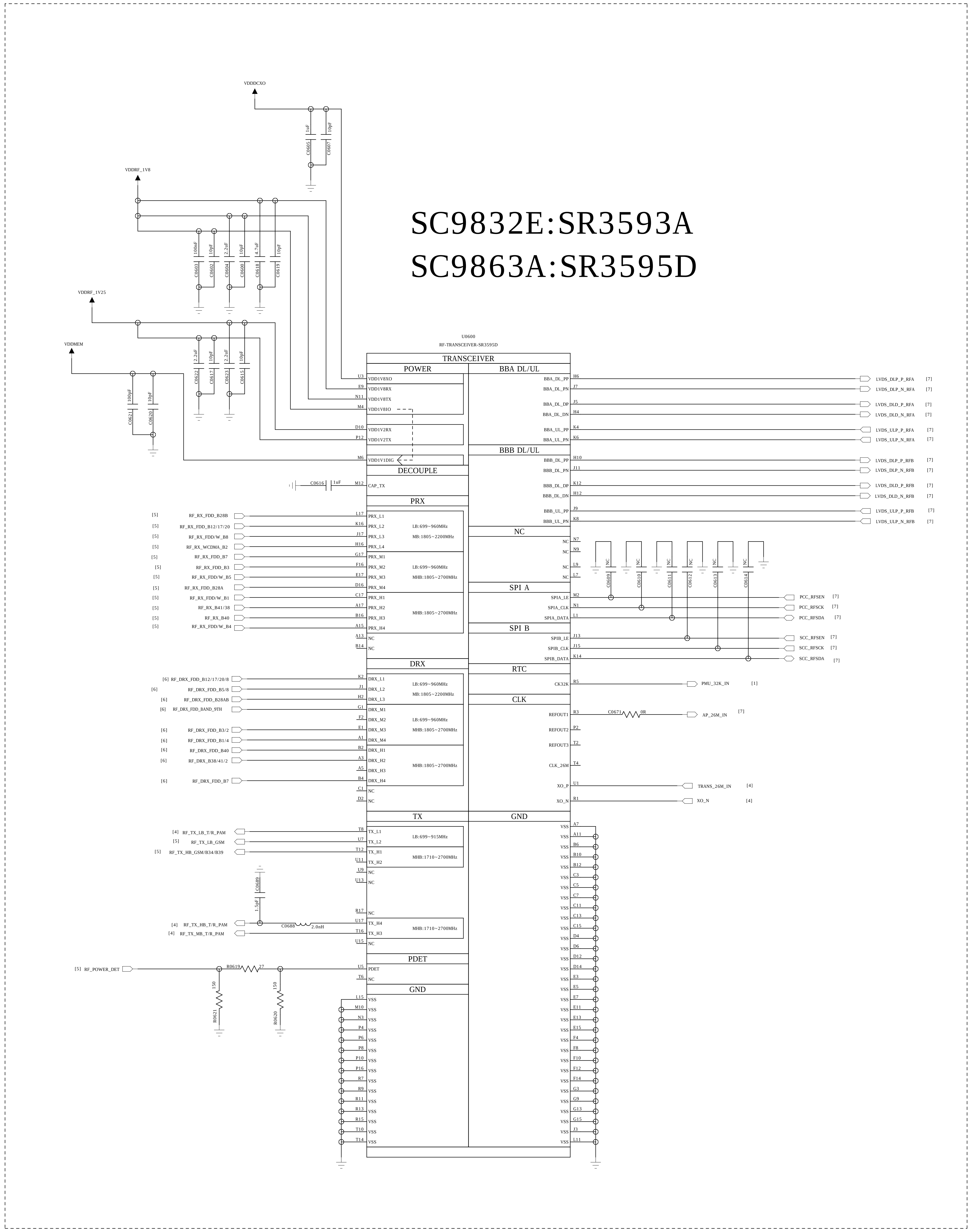
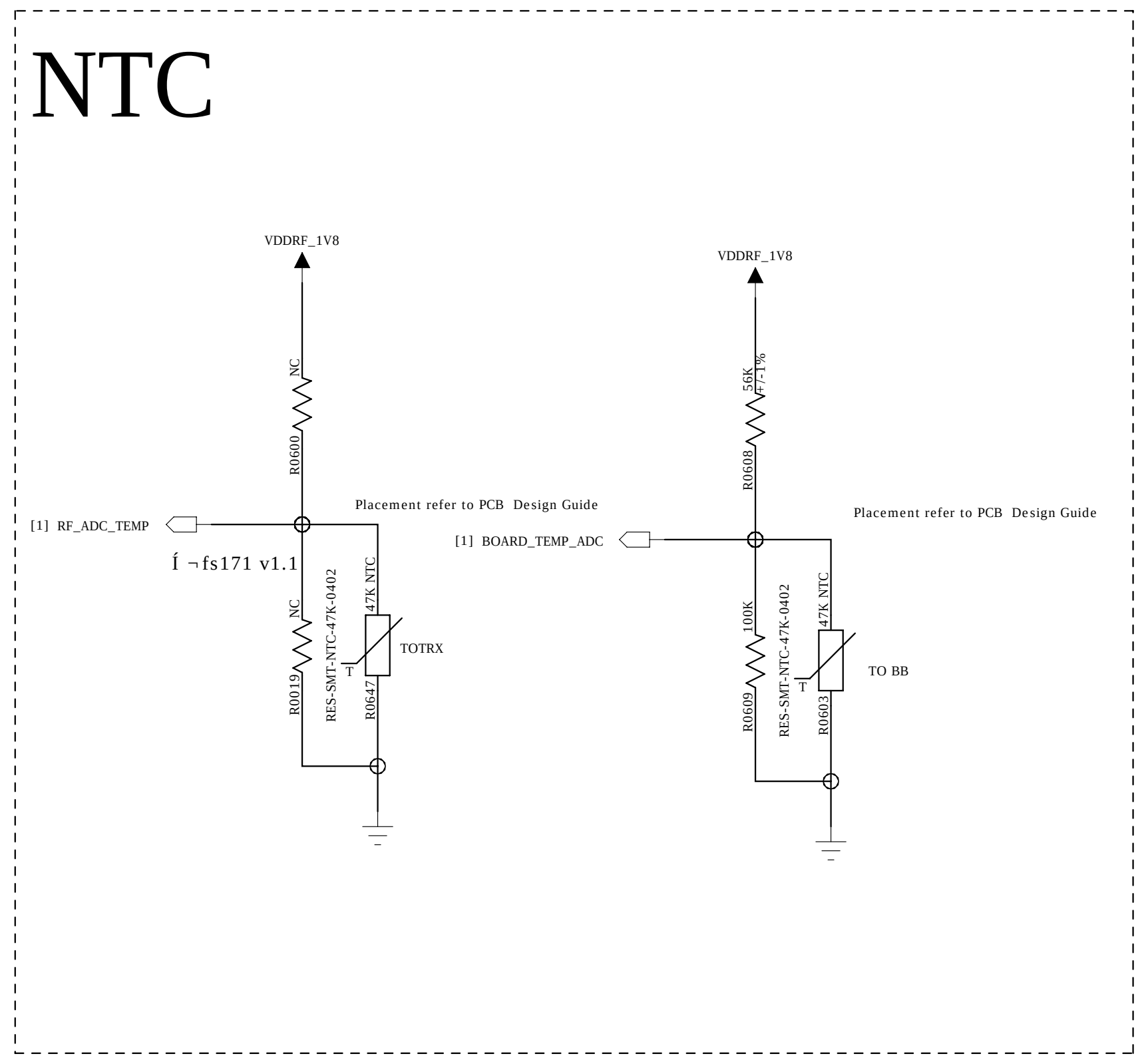
# LTE/WCDMA PAM



# SC9832E:SR3593A
# SC9863A:SR3595D



# NTC

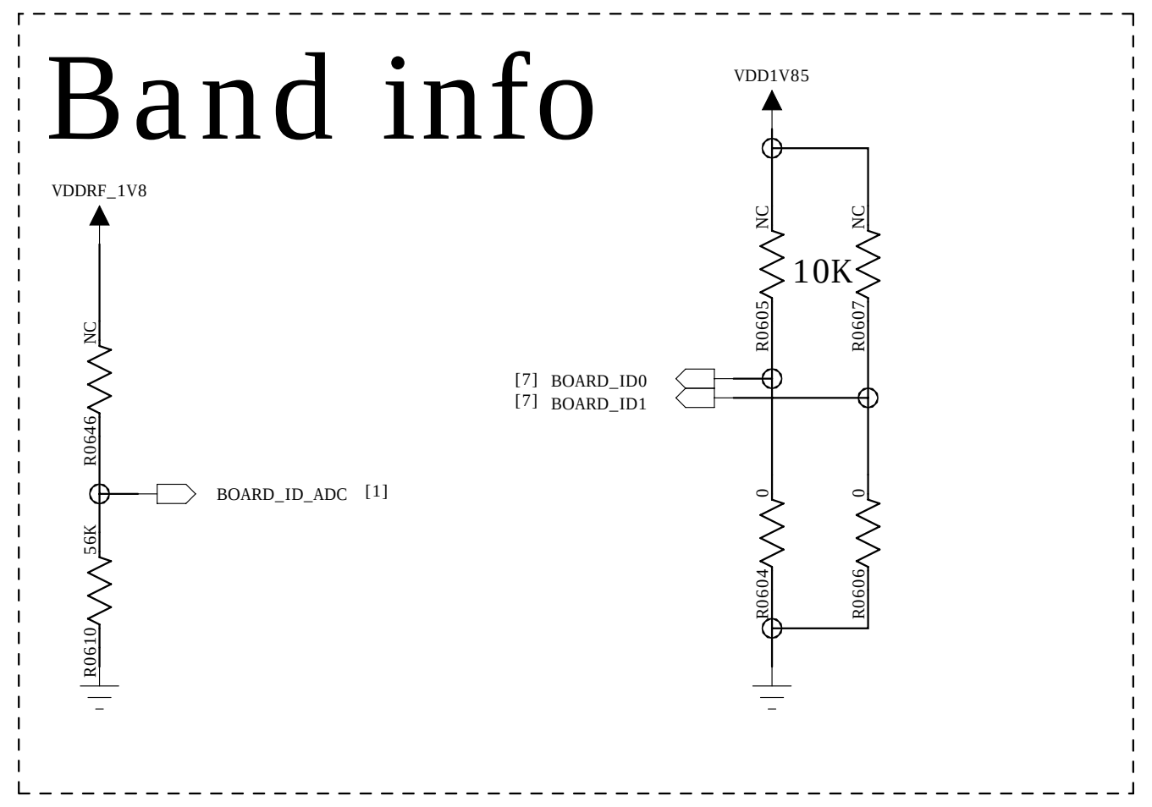


| Clock Mode | BoardID0 |
|---|---|
| TSX | 0 |
| TCXO +32K | 1 |

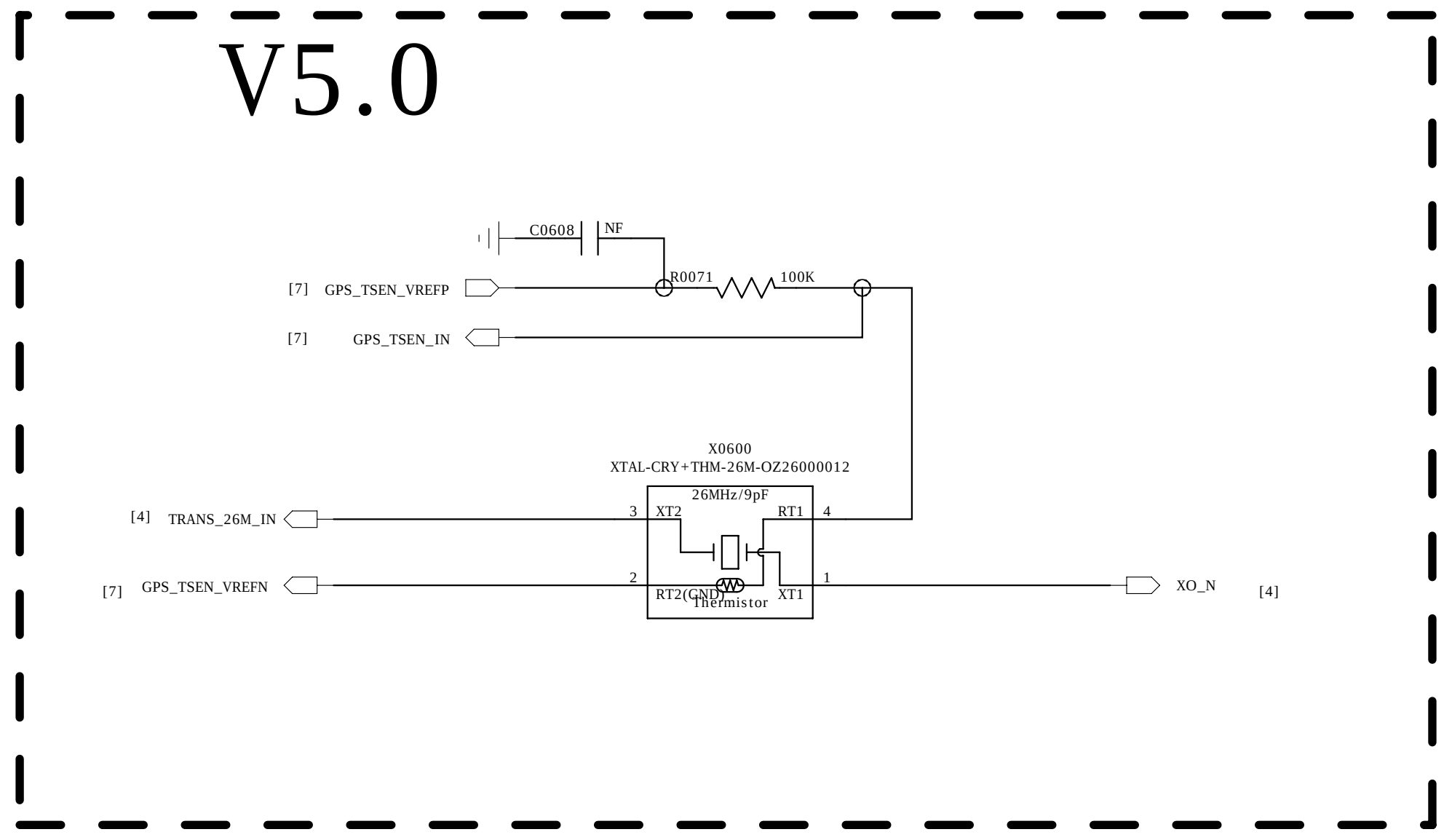
| LPDDR Type | BoardID1 |
|---|---|
| LPDDR3 | 0 |
| LPDDR4X | 1 |

BoardID2 Backup

# Band info



# V5.0



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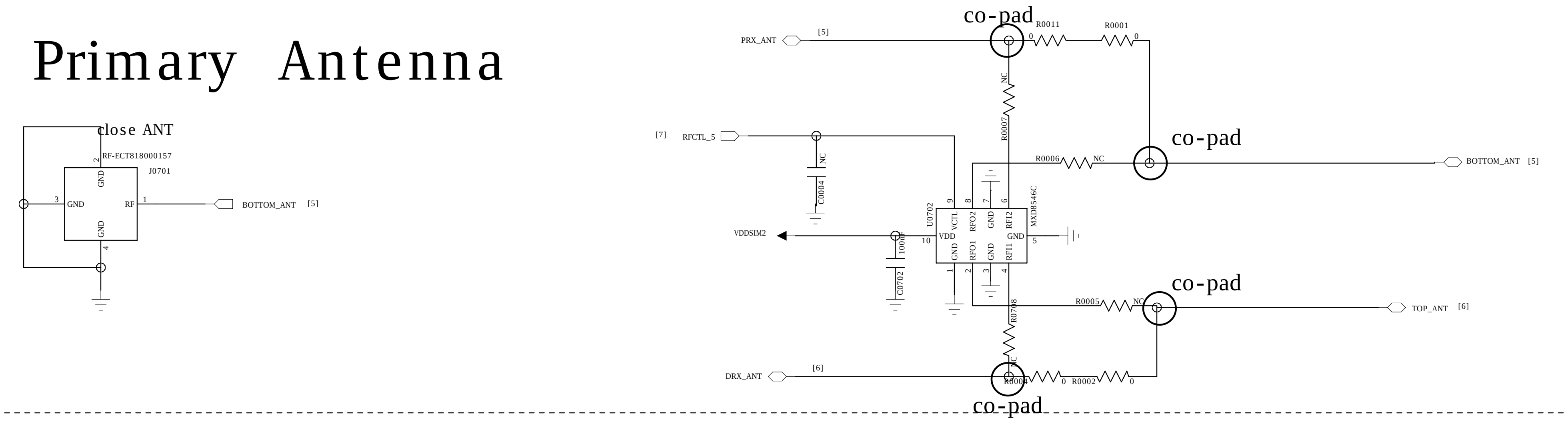
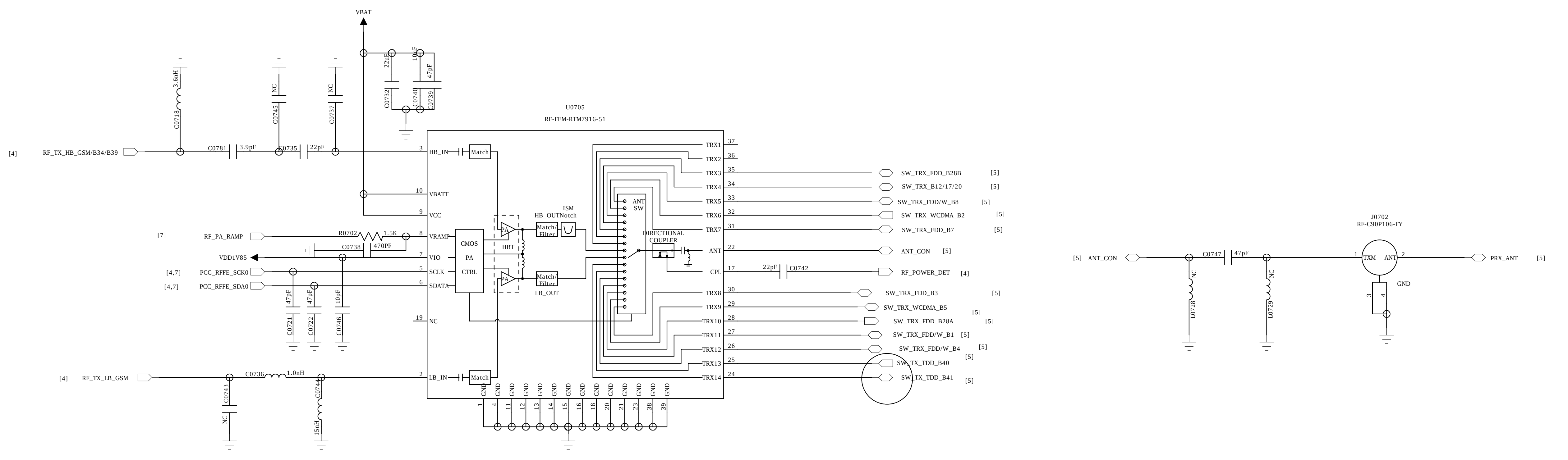
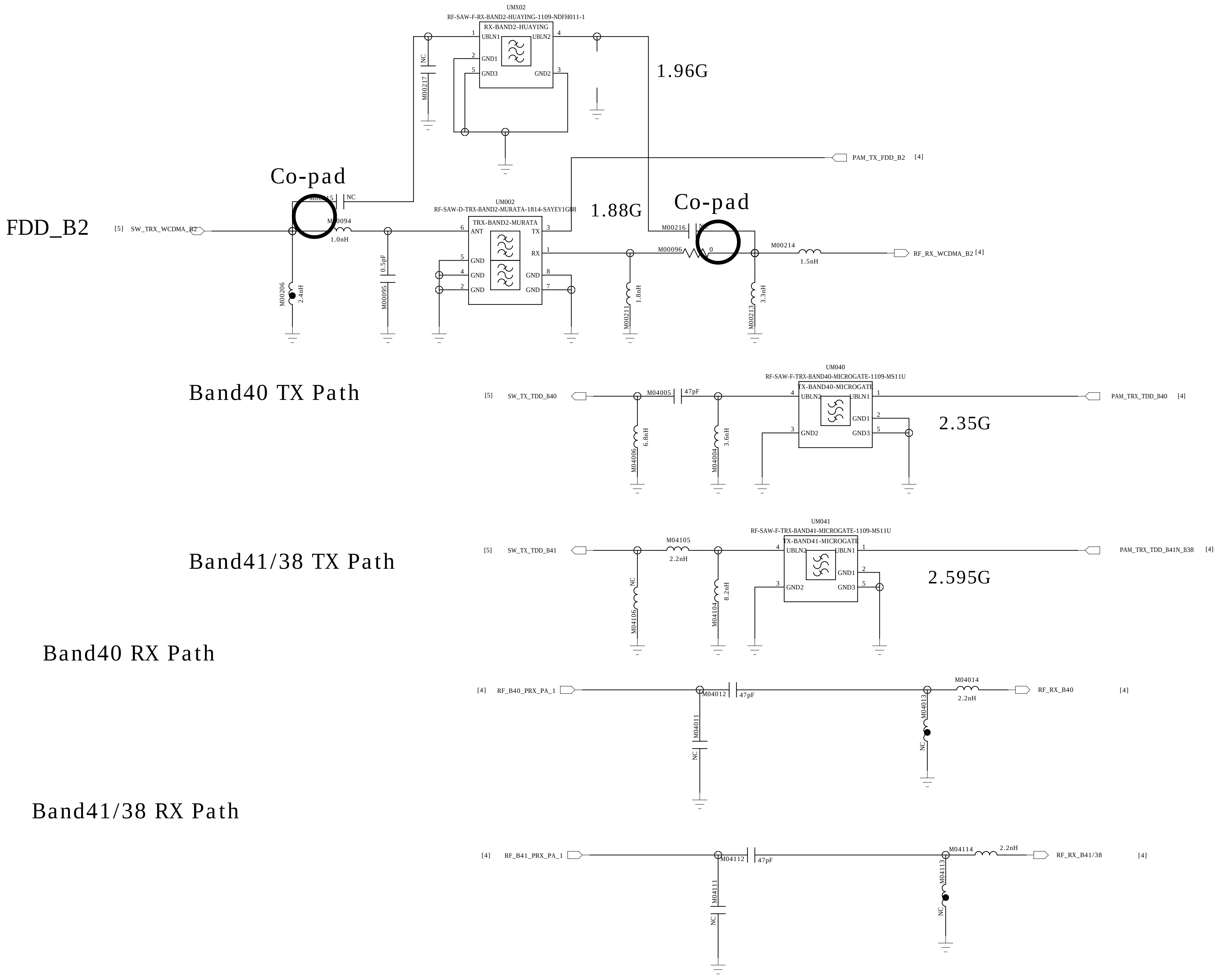
# Primary Antenna



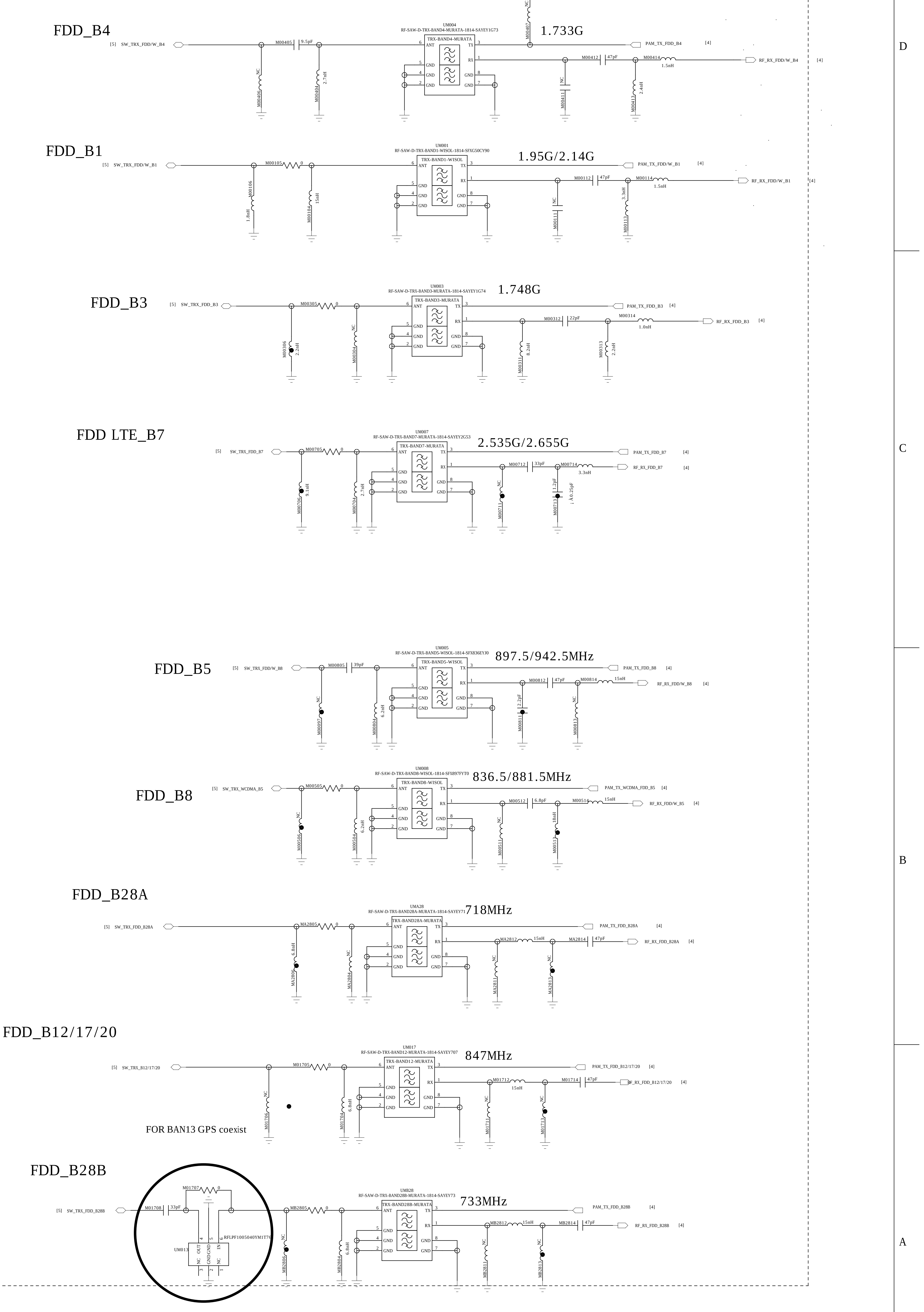
# TDS/TDD B34_B39/GSM PA + Switch



# TDD LTE Parts



# PRIMARY TRX Path



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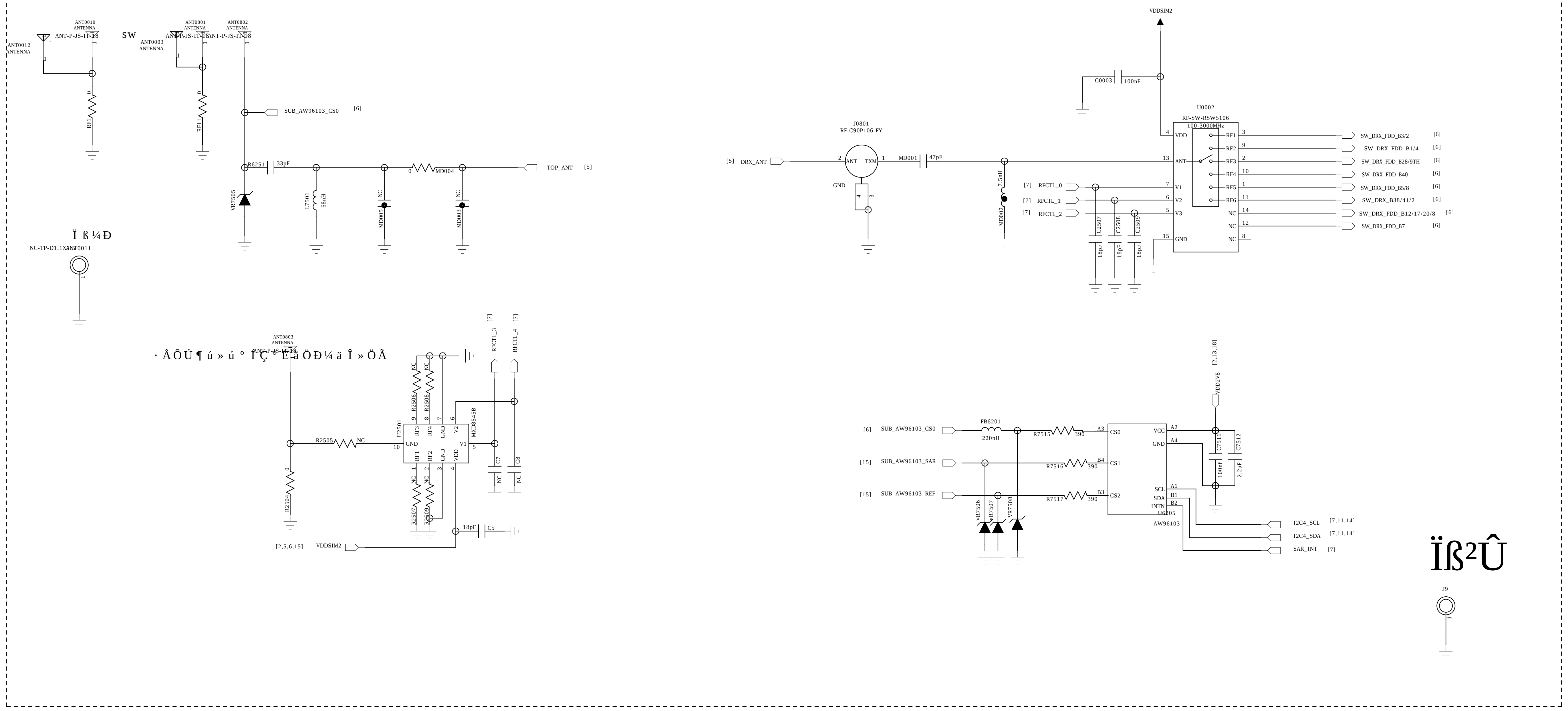
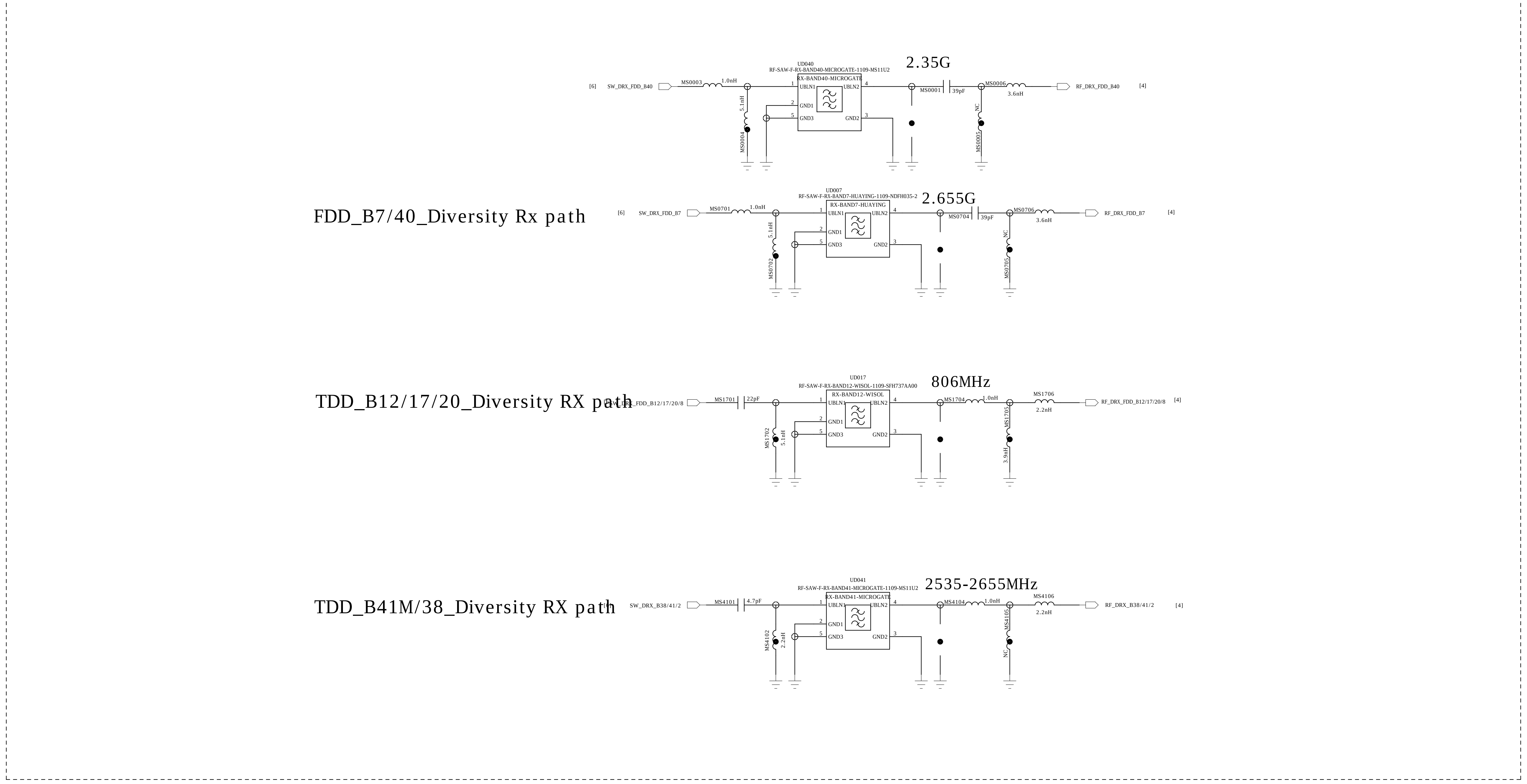
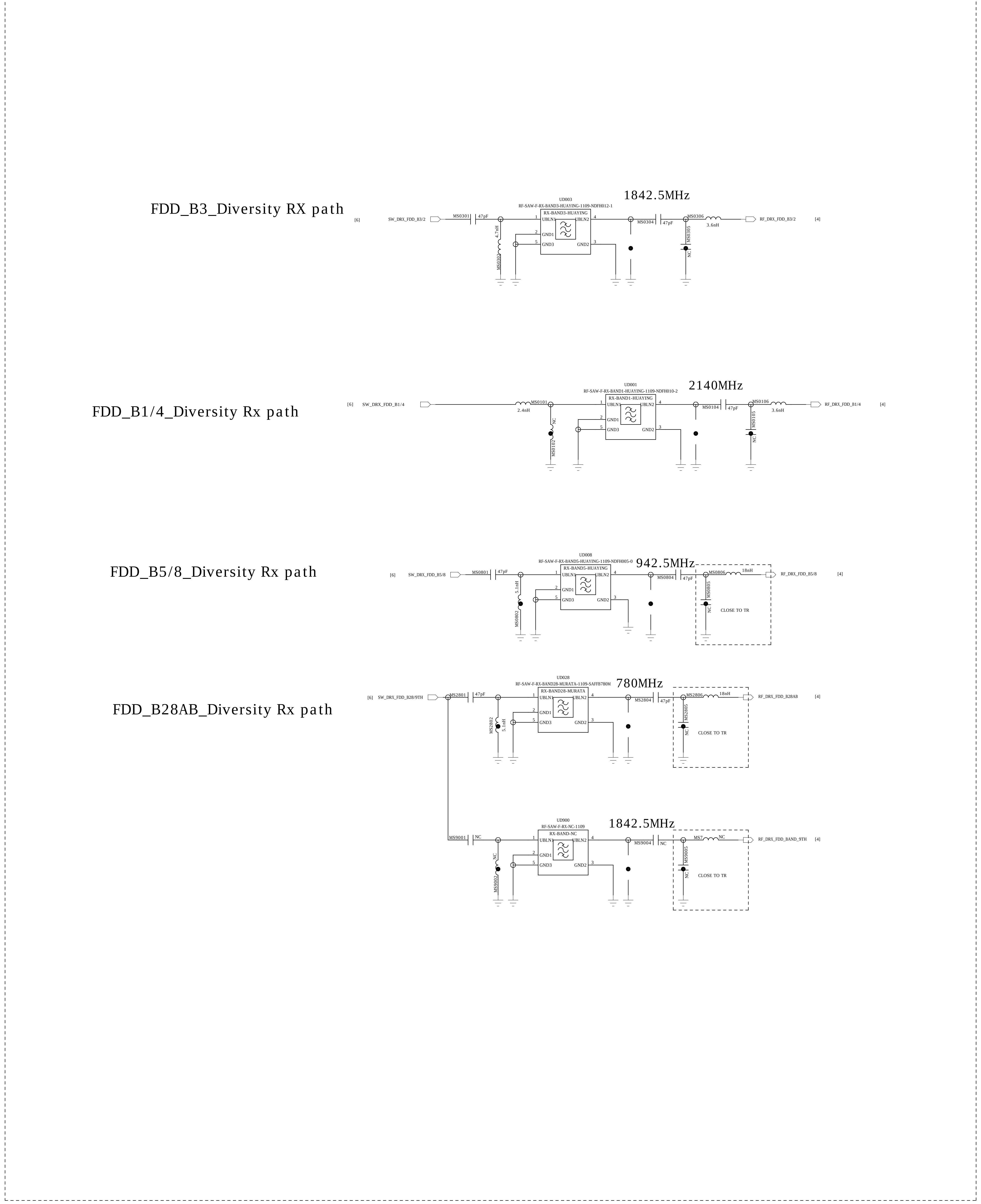
# Diversity LTE LMB Path



# Diversity HB Antenna



# Diversity LTE RX Path



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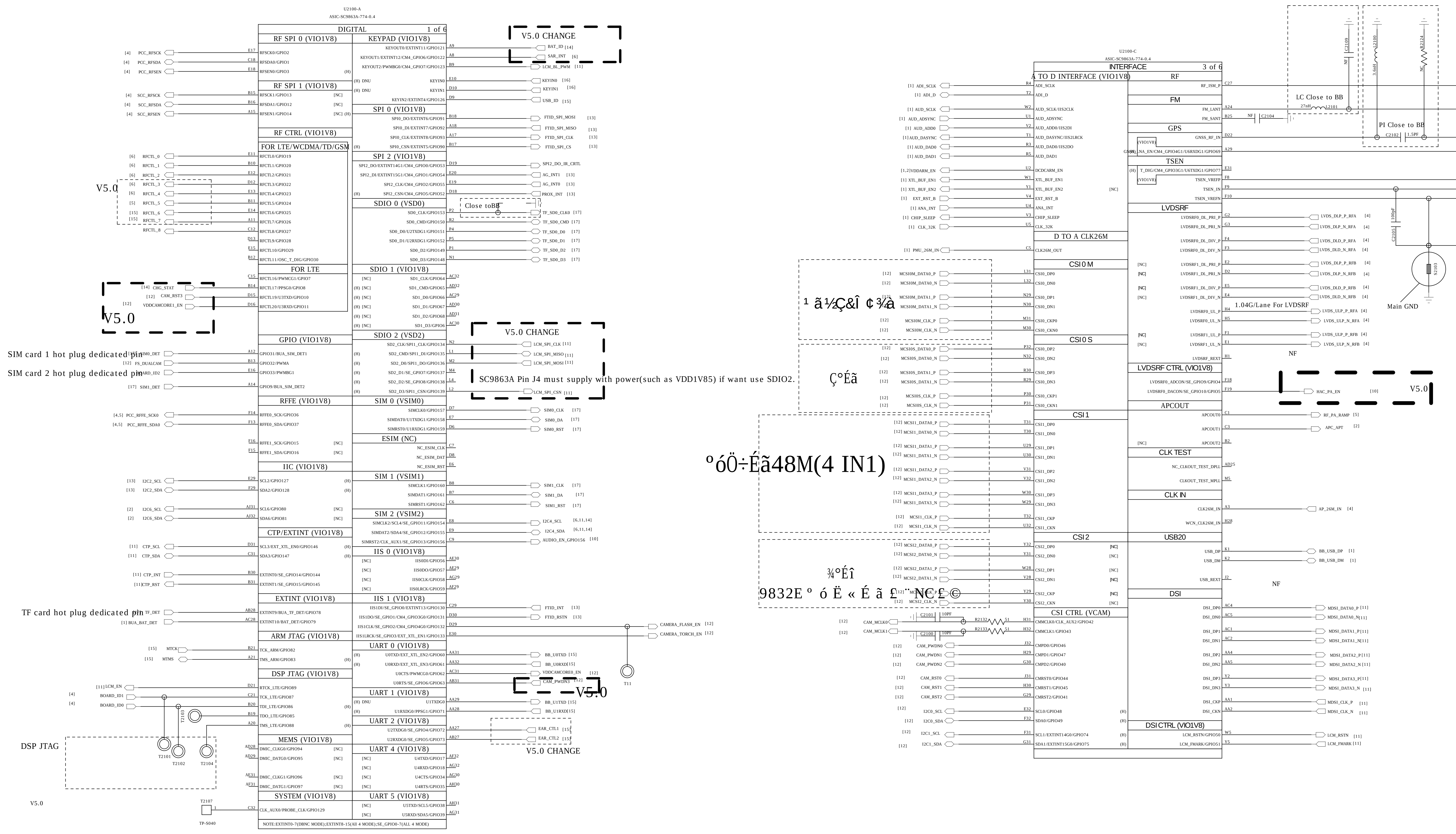
# DIGITAL



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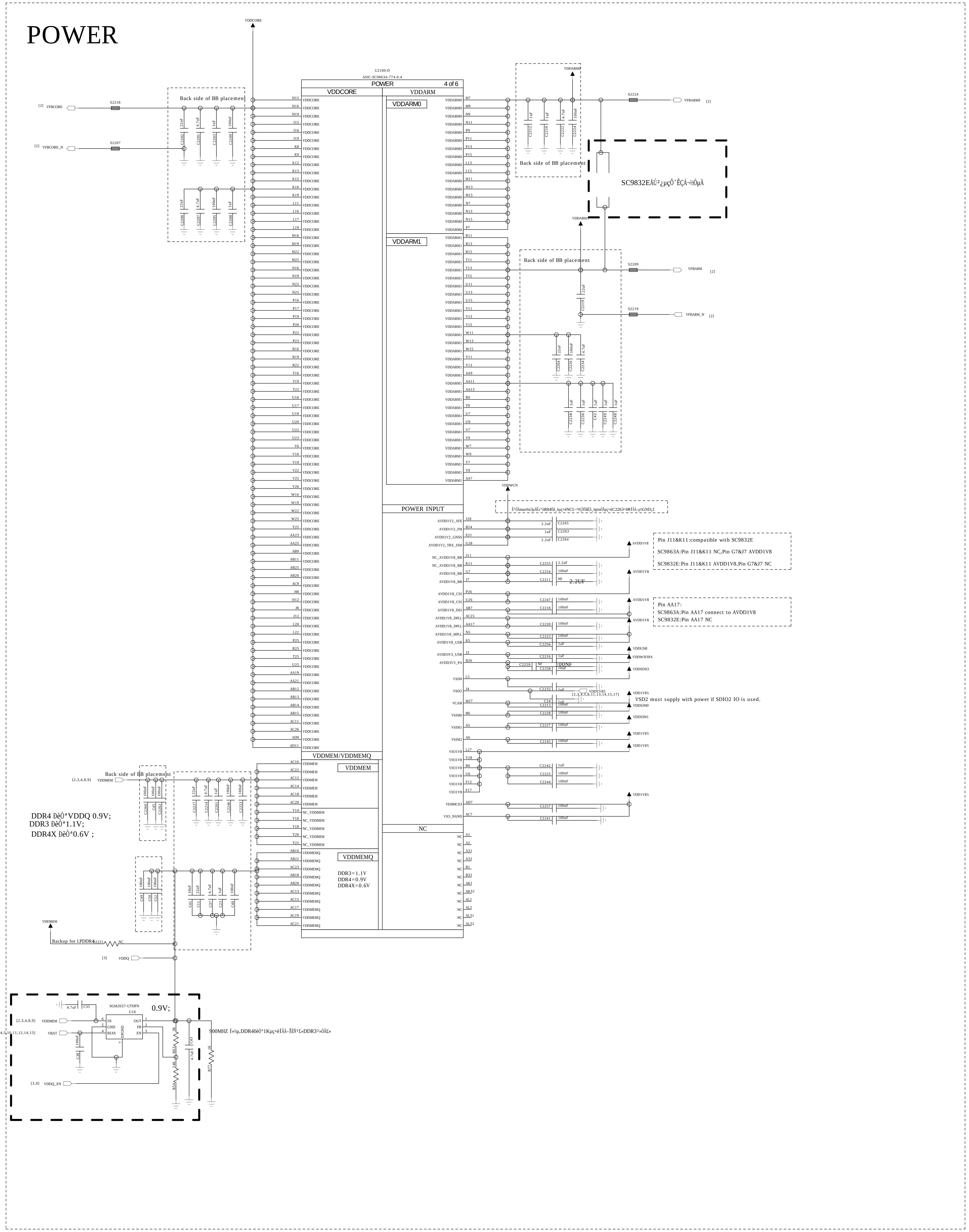

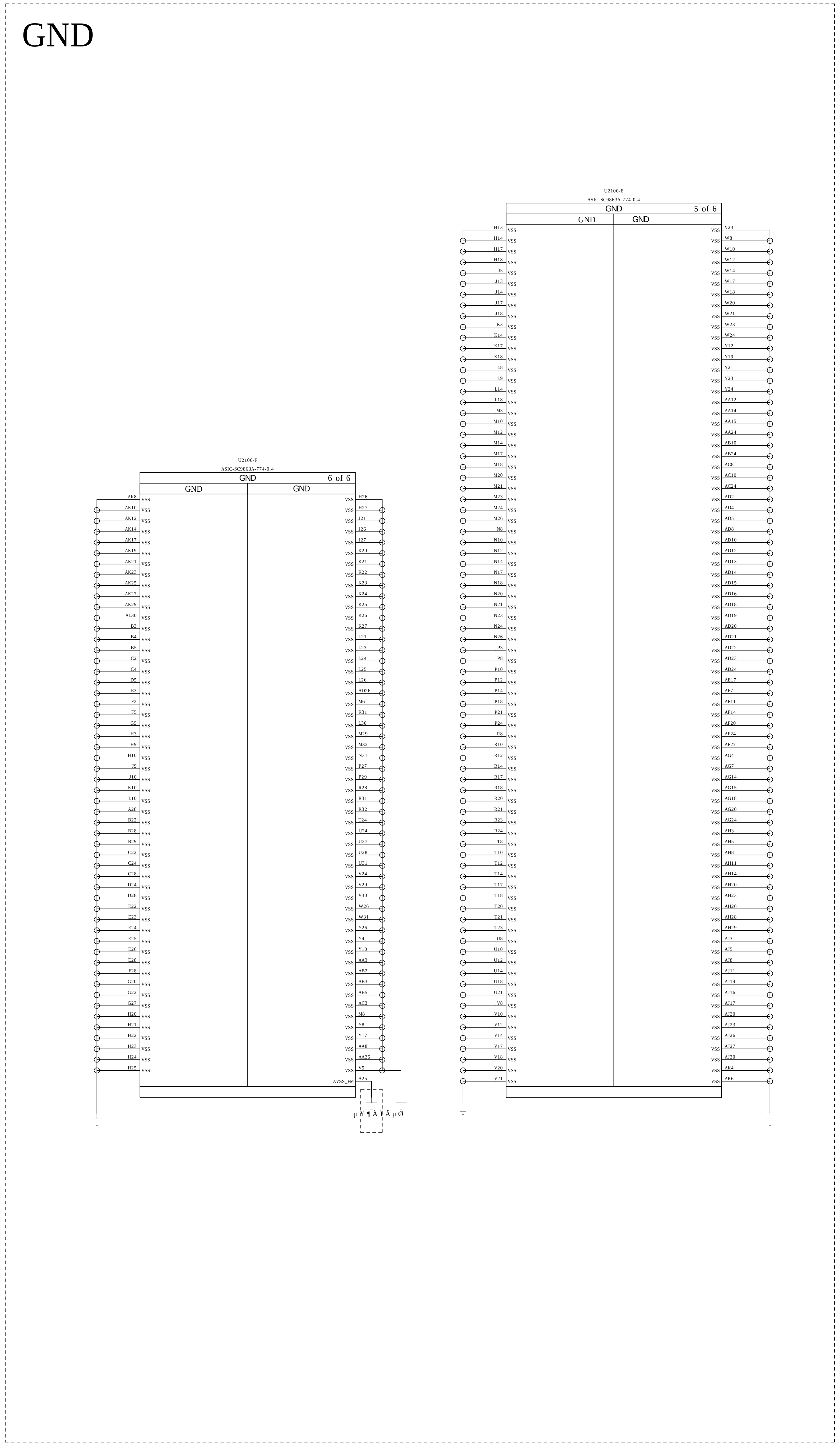

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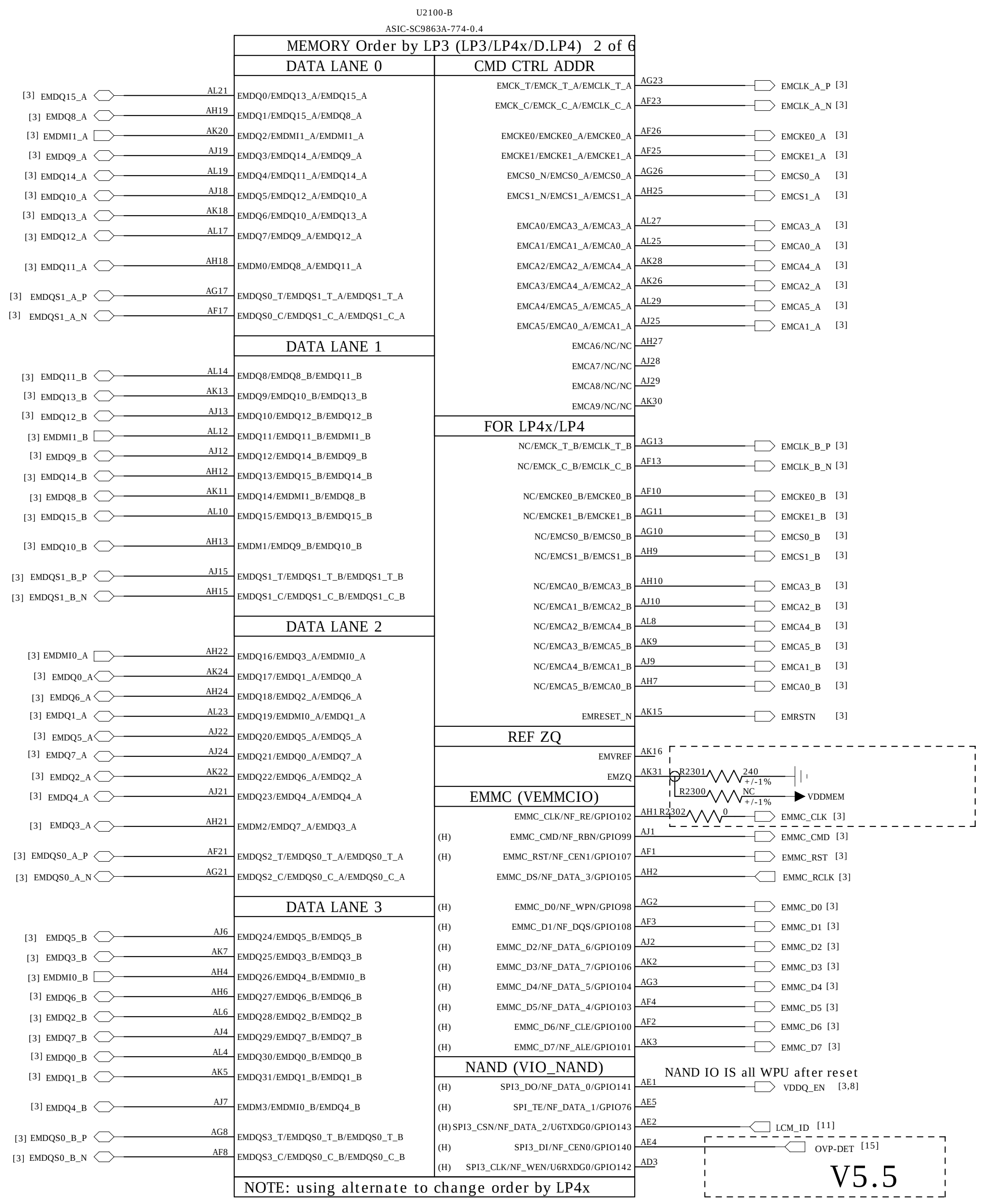
# V5.5 CHANGE to ddr4 0616

## MEMORY


U2100-B
ASIC-SC9863A-774-0.4
MEMORY Order by LP3 (LP3/LP4x/D.LP4) 2 of 6
DATA LANE 0
[3] EMDQ15_A AL21 EMDQ0/EMDQ13_A/EMDQ15_A
[3] EMDQ8_A AH19 EMDQ1/EMDQ15_A/EMDQ8_A
[3] EMDMI1_A AK20 EMDQ2/EMDMI1_A/EMDMI1_A
[3] EMDQ9_A AJ19 EMDQ3/EMDQ14_A/EMDQ9_A
[3] EMDQ14_A AL19 EMDQ4/EMDQ11_A/EMDQ14_A
[3] EMDQ10_A AJ18 EMDQ5/EMDQ12_A/EMDQ10_A
[3] EMDQ13_A AK18 EMDQ6/EMDQ10_A/EMDQ13_A
[3] EMDQ12_A AL17 EMDQ7/EMDQ9_A/EMDQ12_A
[3] EMDQ11_A AH18 EMDM0/EMDQ8_A/EMDQ11_A
[3] EMDQS1_A_P AG17 EMDQS0_T/EMDQS1_T_A/EMDQS1_T_A
[3] EMDQS1_A_N AF17 EMDQS0_C/EMDQS1_C_A/EMDQS1_C_A
DATA LANE 1
[3] EMDQ11_B AL14 EMDQ8/EMDQ8_B/EMDQ11_B
[3] EMDQ13_B AK13 EMDQ9/EMDQ10_B/EMDQ13_B
[3] EMDQ12_B AJ13 EMDQ10/EMDQ12_B/EMDQ12_B
[3] EMDMI1_B AL12 EMDQ11/EMDQ11_B/EMDMI1_B
[3] EMDQ9_B AJ12 EMDQ12/EMDQ14_B/EMDQ9_B
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[3] EMDQ8_B AK11 EMDQ14/EMDMI1_B/EMDQ8_B
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[3] EMDQ10_B AH13 EMDM1/EMDQ9_B/EMDQ10_B
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[3] EMDQS1_B_N AH15 EMDQS1_C/EMDQS1_C_B/EMDQS1_C_B
DATA LANE 2
[3] EMDMI0_A AH22 EMDQ16/EMDQ3_A/EMDMI0_A
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[3] EMDQ6_A AH24 EMDQ18/EMDQ2_A/EMDQ6_A
[3] EMDQ1_A AL23 EMDQ19/EMDMI0_A/EMDQ1_A
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[3] EMDQ7_A AJ24 EMDQ21/EMDQ0_A/EMDQ7_A
[3] EMDQ2_A AK22 EMDQ22/EMDQ6_A/EMDQ2_A
[3] EMDQ4_A AJ21 EMDQ23/EMDQ4_A/EMDQ4_A
[3] EMDQ3_A AH21 EMDM2/EMDQ7_A/EMDQ3_A
[3] EMDQS0_A_P AF21 EMDQS2_T/EMDQS0_T_A/EMDQS0_T_A
[3] EMDQS0_A_N AG21 EMDQS2_C/EMDQS0_C_A/EMDQS0_C_A
DATA LANE 3
[3] EMDQ5_B AJ6 EMDQ24/EMDQ5_B/EMDQ5_B
[3] EMDQ3_B AK7 EMDQ25/EMDQ3_B/EMDQ3_B
[3] EMDMI0_B AH4 EMDQ26/EMDQ4_B/EMDMI0_B
[3] EMDQ6_B AH6 EMDQ27/EMDQ6_B/EMDQ6_B
[3] EMDQ2_B AL6 EMDQ28/EMDQ2_B/EMDQ2_B
[3] EMDQ7_B AJ4 EMDQ29/EMDQ7_B/EMDQ7_B
[3] EMDQ0_B AL4 EMDQ30/EMDQ0_B/EMDQ0_B
[3] EMDQ1_B AK5 EMDQ31/EMDQ1_B/EMDQ1_B
[3] EMDQ4_B AJ7 EMDM3/EMDMI0_B/EMDQ4_B
[3] EMDQS0_B_P AG8 EMDQS3_T/EMDQS0_T_B/EMDQS0_T_B
[3] EMDQS0_B_N AF8 EMDQS3_C/EMDQS0_C_B/EMDQS0_C_B
CMD CTRL ADDR
EMCK_T/EMCK_T_A/EMCLK_T_A AG23 EMCLK_A_P [3]
EMCK_C/EMCK_C_A/EMCLK_C_A AF23 EMCLK_A_N [3]
EMCKE0/EMCKE0_A/EMCKE0_A AF26 EMCKE0_A [3]
EMCKE1/EMCKE1_A/EMCKE1_A AF25 EMCKE1_A [3]
EMCS0_N/EMCS0_A/EMCS0_A AG26 EMCS0_A [3]
EMCS1_N/EMCS1_A/EMCS1_A AH25 EMCS1_A [3]
EMCA0/EMCA3_A/EMCA3_A AL27 EMCA3_A [3]
EMCA1/EMCA1_A/EMCA0_A AL25 EMCA0_A [3]
EMCA2/EMCA2_A/EMCA4_A AK28 EMCA4_A [3]
EMCA3/EMCA4_A/EMCA2_A AK26 EMCA2_A [3]
EMCA4/EMCA5_A/EMCA5_A AL29 EMCA5_A [3]
EMCA5/EMCA0_A/EMCA1_A AJ25 EMCA1_A [3]
EMCA6/NC/NC AH27
EMCA7/NC/NC AJ28
EMCA8/NC/NC AJ29
EMCA9/NC/NC AK30
FOR LP4x/LP4
NC/EMCK_T_B/EMCLK_T_B AG13 EMCLK_B_P [3]
NC/EMCK_C_B/EMCLK_C_B AF13 EMCLK_B_N [3]
NC/EMCKE0_B/EMCKE0_B AF10 EMCKE0_B [3]
NC/EMCKE1_B/EMCKE1_B AG11 EMCKE1_B [3]
NC/EMCS0_B/EMCS0_B AG10 EMCS0_B [3]
NC/EMCS1_B/EMCS1_B AH9 EMCS1_B [3]
NC/EMCA0_B/EMCA3_B AH10 EMCA3_B [3]
NC/EMCA1_B/EMCA2_B AJ10 EMCA2_B [3]
NC/EMCA2_B/EMCA4_B AL8 EMCA4_B [3]
NC/EMCA3_B/EMCA5_B AK9 EMCA5_B [3]
NC/EMCA4_B/EMCA1_B AJ9 EMCA1_B [3]
NC/EMCA5_B/EMCA0_B AH7 EMCA0_B [3]
EMRESET_N AK15 EMRSTN [3]
REF ZQ
EMVREF AK16
EMZQ AK31
R2301 240 +/-1%
R2300 NC +/-1%
VDDMEM
EMMC (VEMMCIO)
EMMC_CLK/NF_RE/GPIO102 AH1 R2302 0 EMMC_CLK [3]
(H) EMMC_CMD/NF_RBN/GPIO99 AJ1 EMMC_CMD [3]
(H) EMMC_RST/NF_CEN1/GPIO107 AF1 EMMC_RST [3]
EMMC_DS/NF_DATA_3/GPIO105 AH2 EMMC_RCLK [3]
(H) EMMC_D0/NF_WPN/GPIO98 AG2 EMMC_D0 [3]
(H) EMMC_D1/NF_DQS/GPIO108 AF3 EMMC_D1 [3]
(H) EMMC_D2/NF_DATA_6/GPIO109 AJ2 EMMC_D2 [3]
(H) EMMC_D3/NF_DATA_7/GPIO106 AK2 EMMC_D3 [3]
(H) EMMC_D4/NF_DATA_5/GPIO104 AG3 EMMC_D4 [3]
(H) EMMC_D5/NF_DATA_4/GPIO103 AF4 EMMC_D5 [3]
(H) EMMC_D6/NF_CLE/GPIO100 AF2 EMMC_D6 [3]
(H) EMMC_D7/NF_ALE/GPIO101 AK3 EMMC_D7 [3]
NAND (VIO_NAND)
NAND IO IS all WPU after reset
(H) SPI3_DO/NF_DATA_0/GPIO141 AE1 VDDQ_EN [3,8]
(H) SPI_TE/NF_DATA_1/GPIO76 AE5
(H) SPI3_CSN/NF_DATA_2/U6TXDG0/GPIO143 AE2 LCM_ID [11]
(H) SPI3_DI/NF_CEN0/GPIO140 AE4 OVP-DET [15]
(H) SPI3_CLK/NF_WEN/U6RXDG0/GPIO142 AD3
V5.5
NOTE: using alternate to change order by LP4x

V5.5 CHANGE

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EQA:
DATED:
COMPANY:
Spreadtrum communications, Inc.
APPROVED:
DATED:
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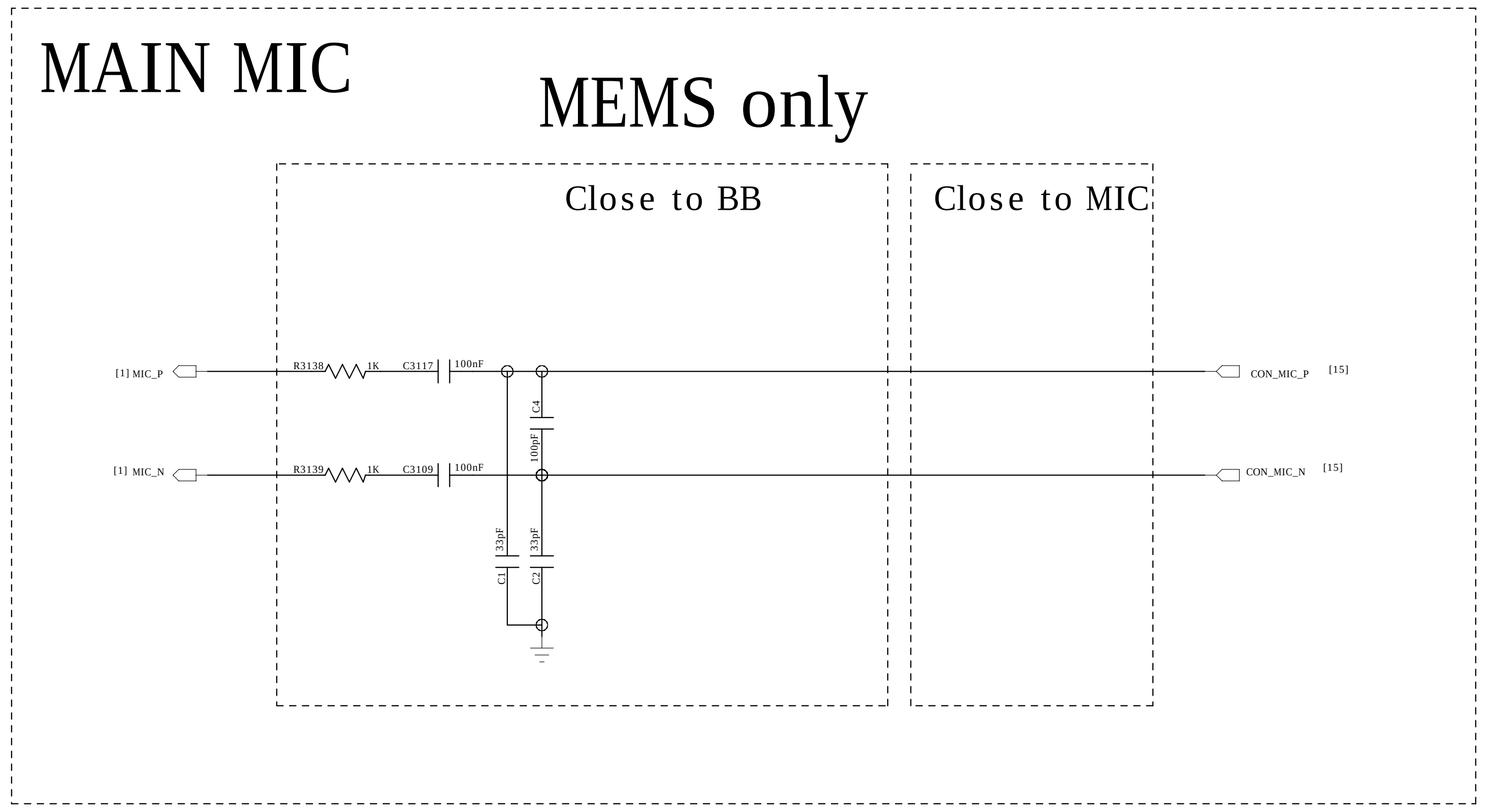

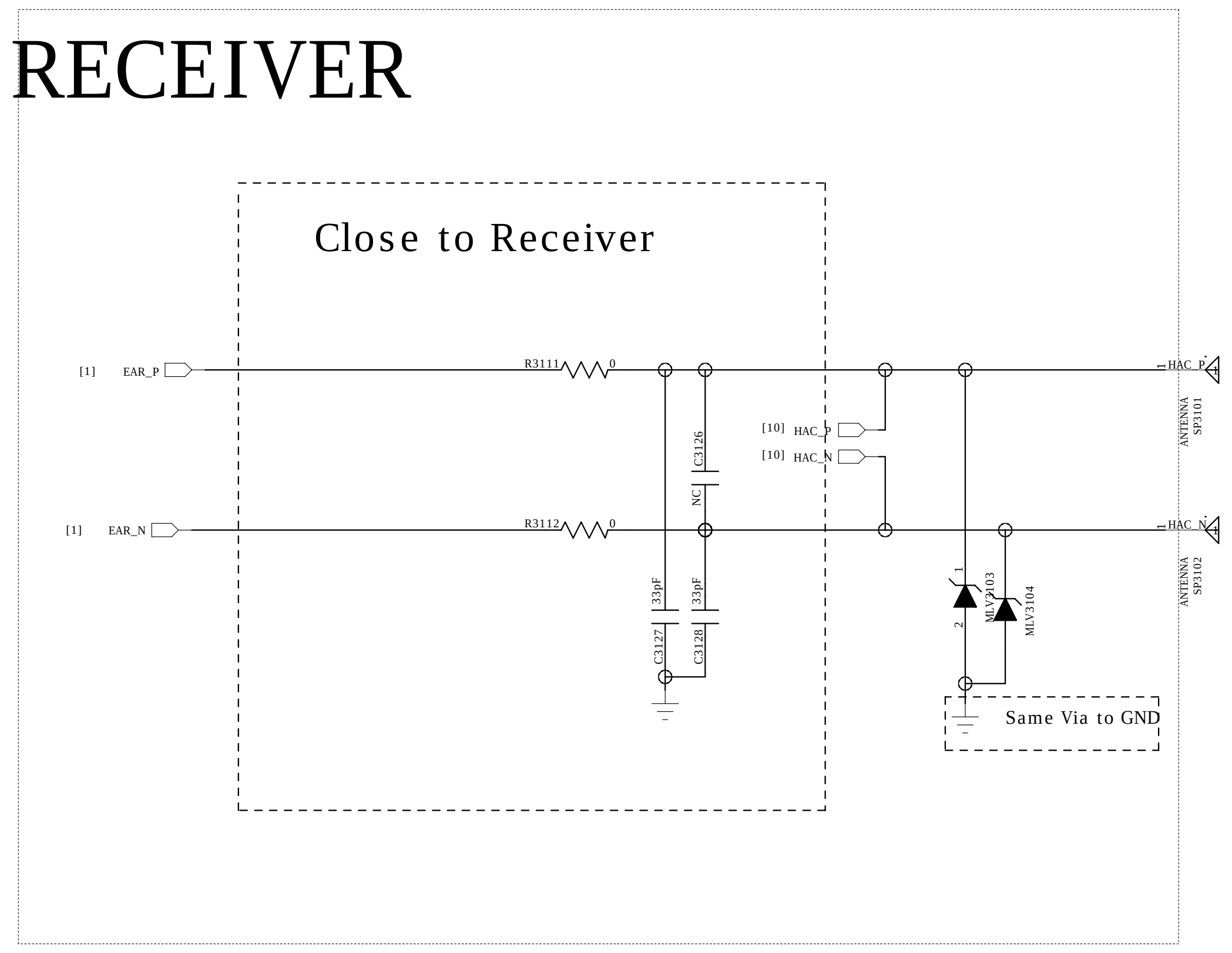

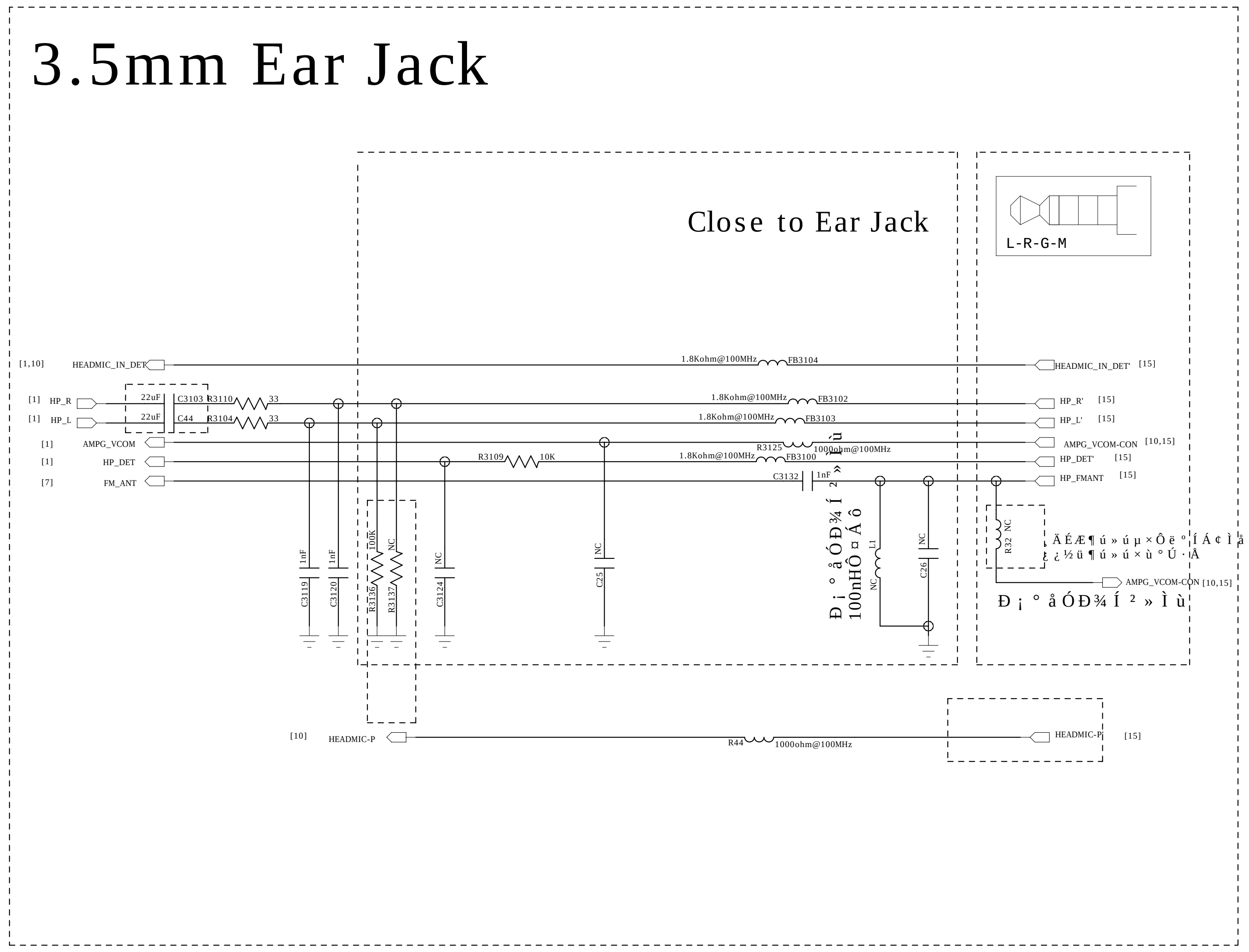

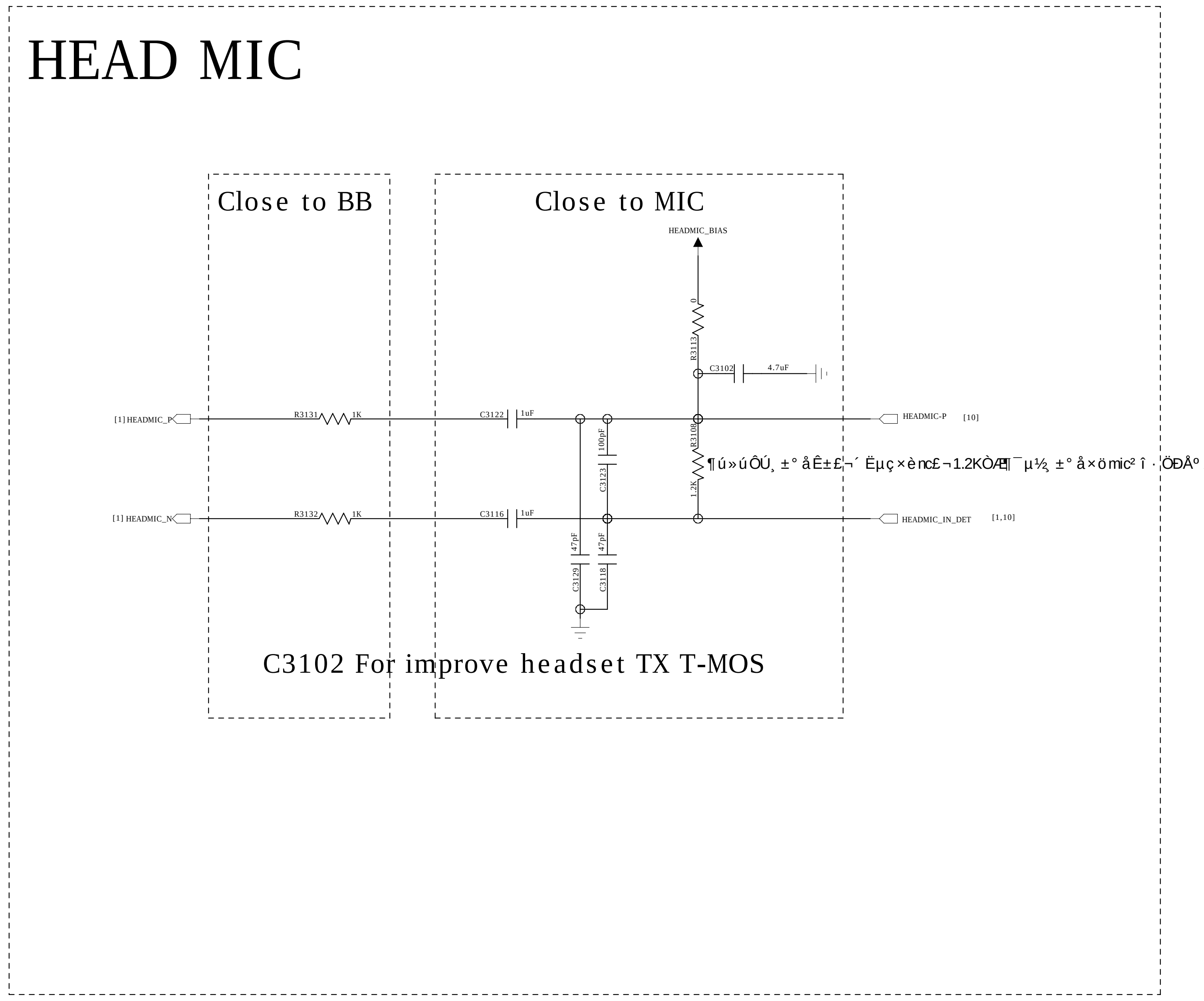

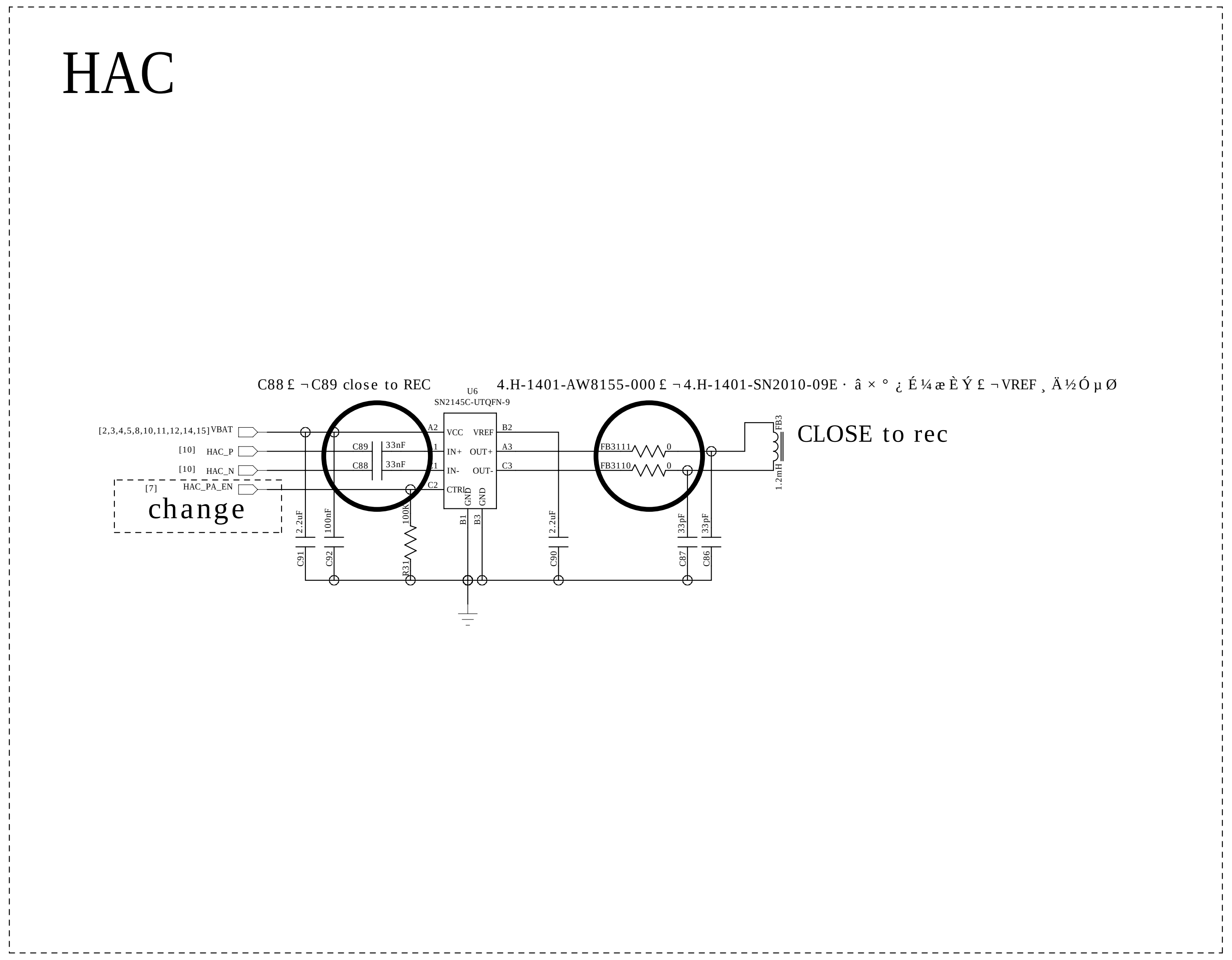

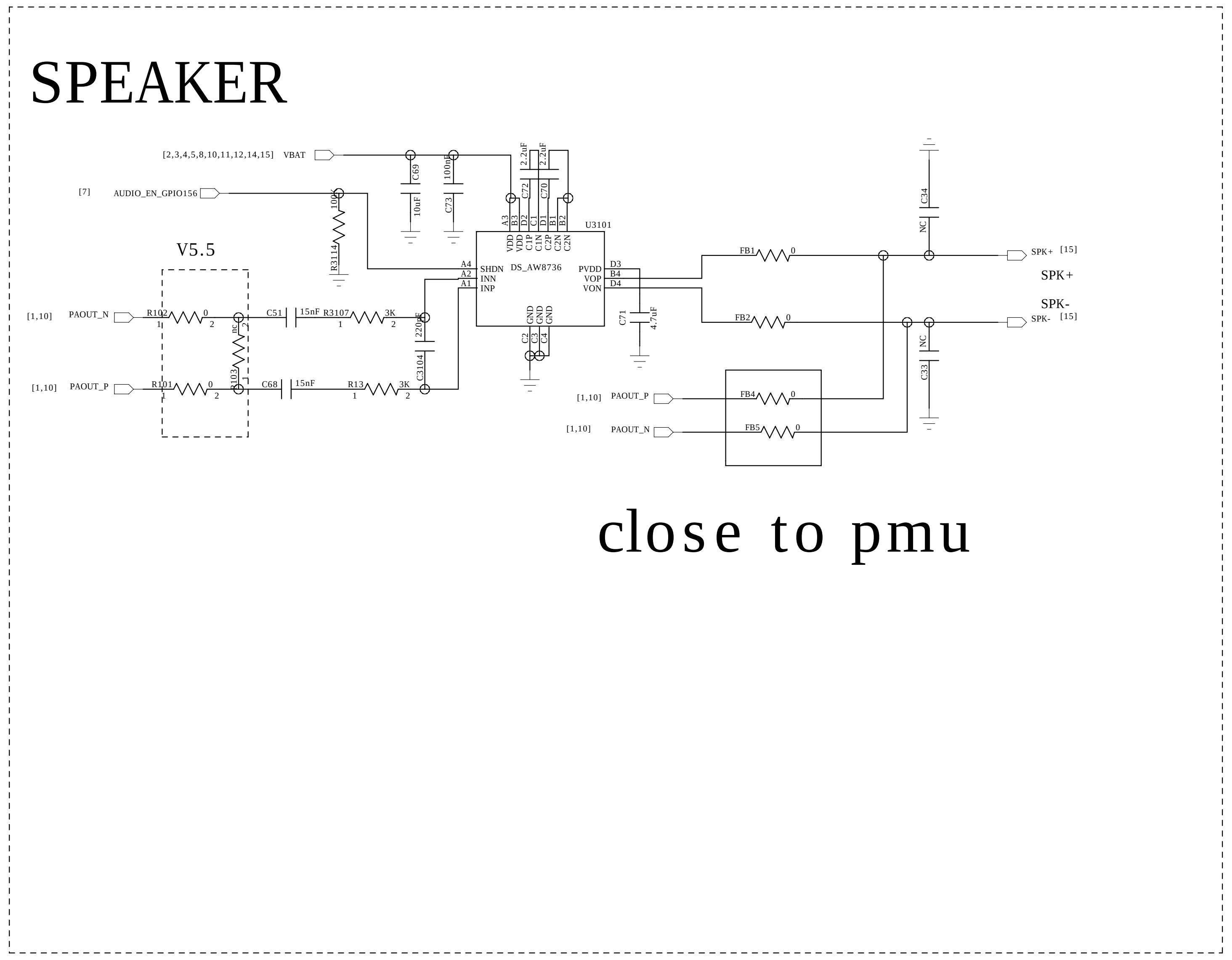

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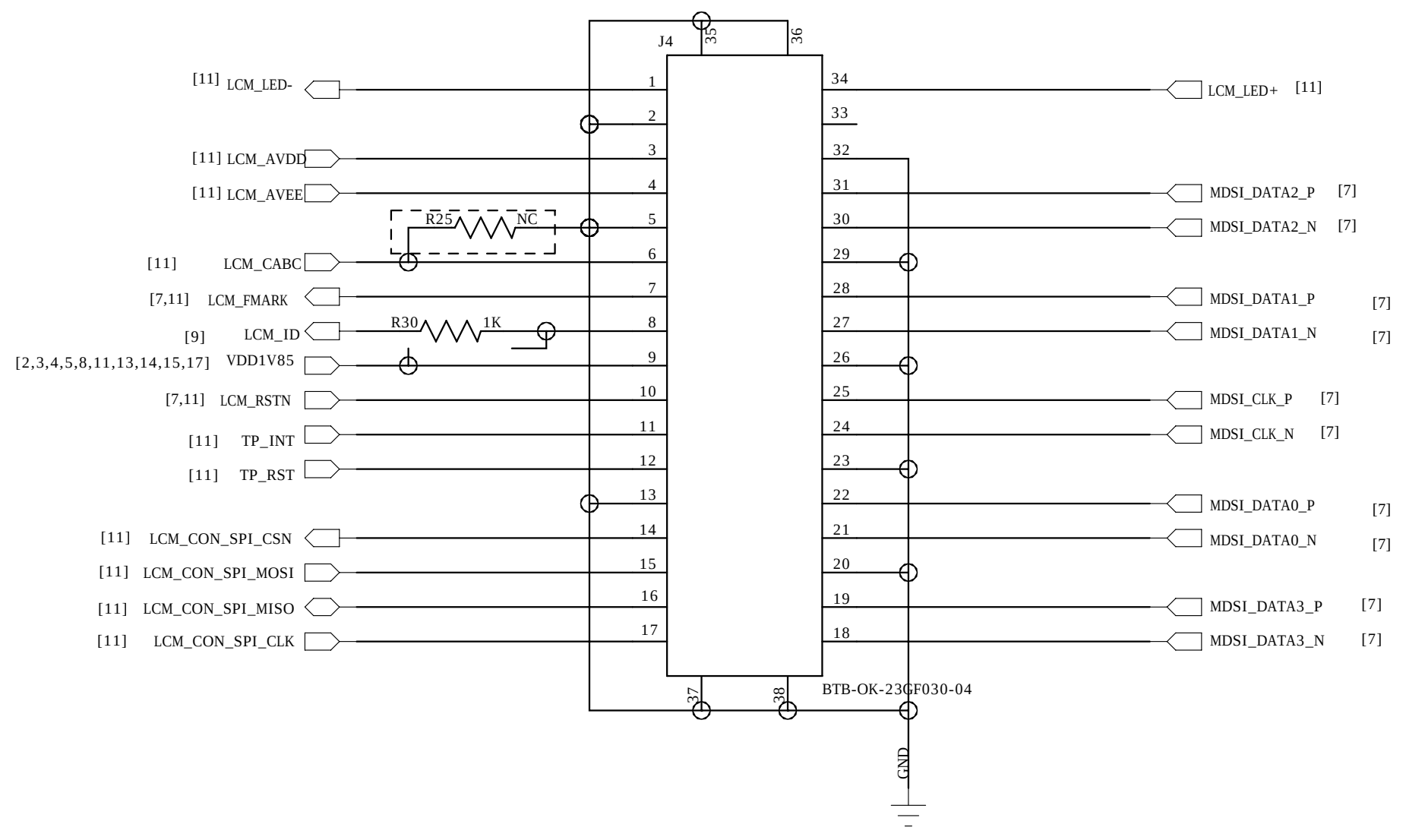
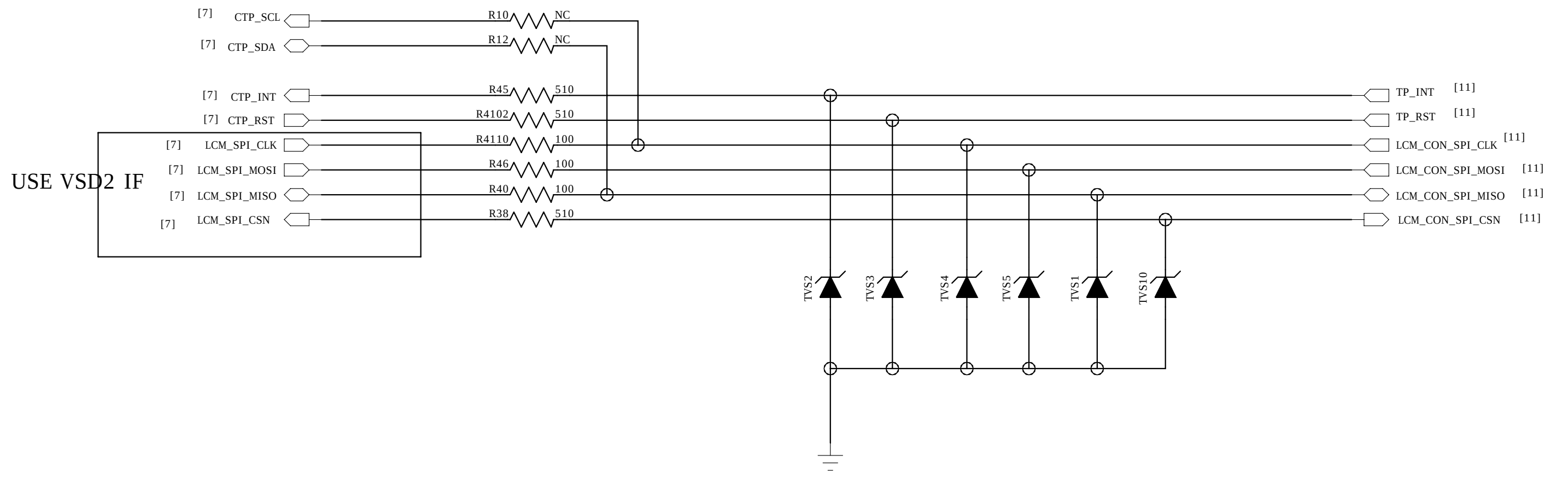
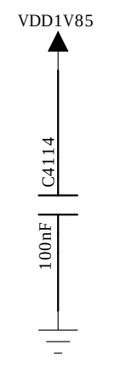
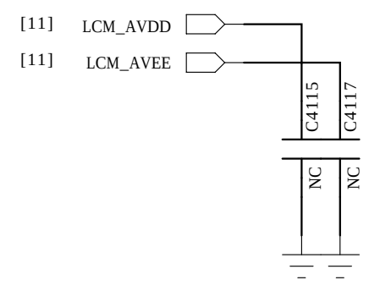
# 6.517" LCM(MIPI)

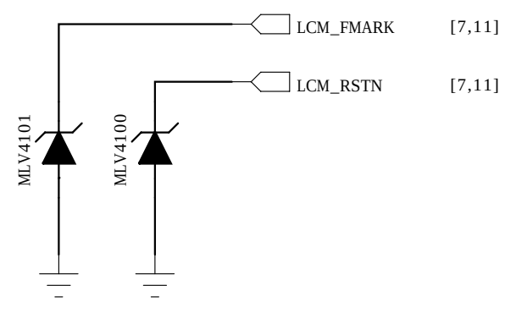


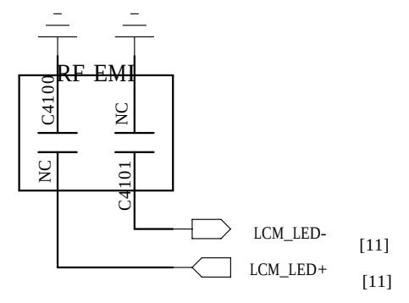
reserve for IIC CTP



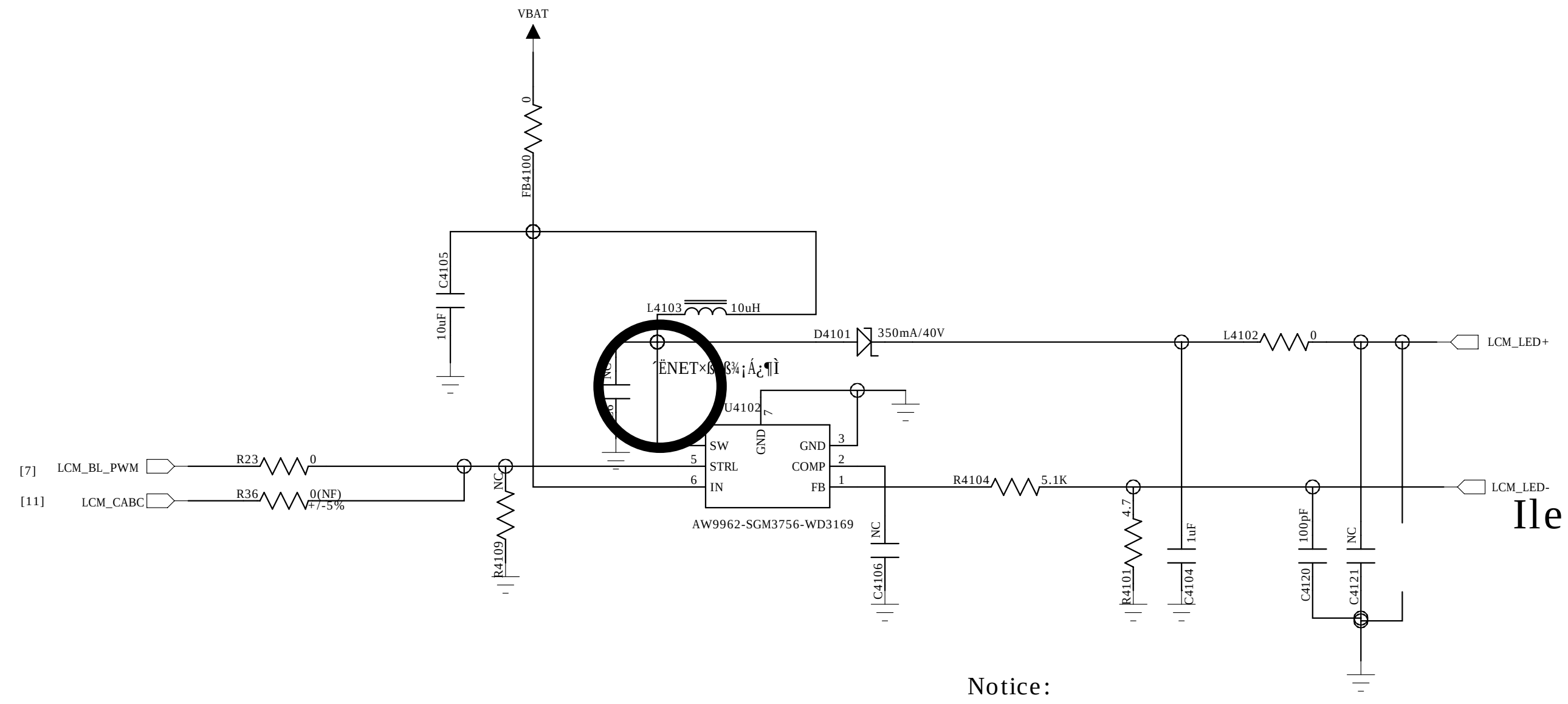








## Back Light Driver



Rated voltage >=50V
X5R or X7R

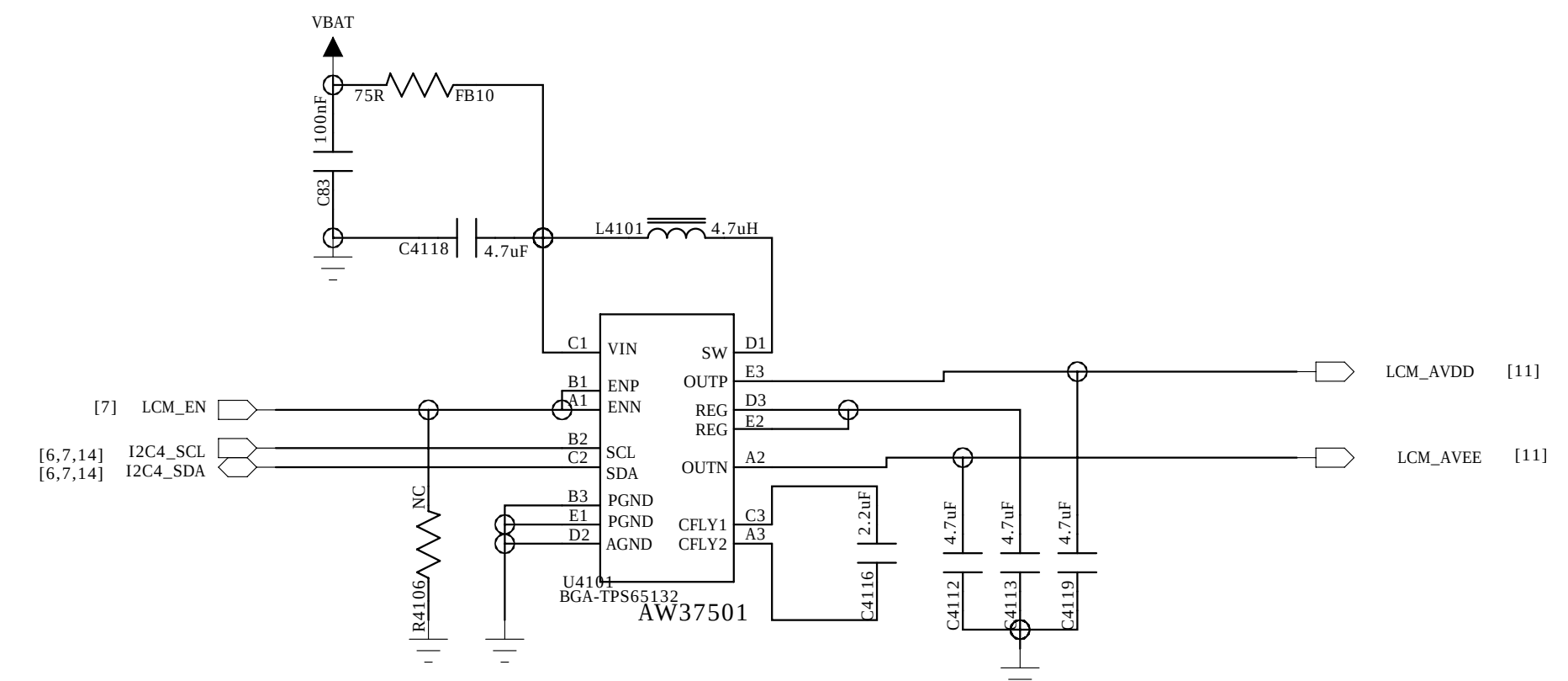
2x7LED

Iled=0.2V/4.7ohm=42mA

Notice:
3x6LED
SGM3732 :VFB=200mV
ALL:Iout=VFB/Rsense

## Source Driver

Notice:
VSP=+6V VSN=-6V



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Torch mode: Vfb=47mV,,,Itorch=47mV/0.36ohm=130mA

Flash mode: Vfb=1.26*10.2K/56k=0.2295V,,,Iflash=0.2295V/0.36ohm=637mA

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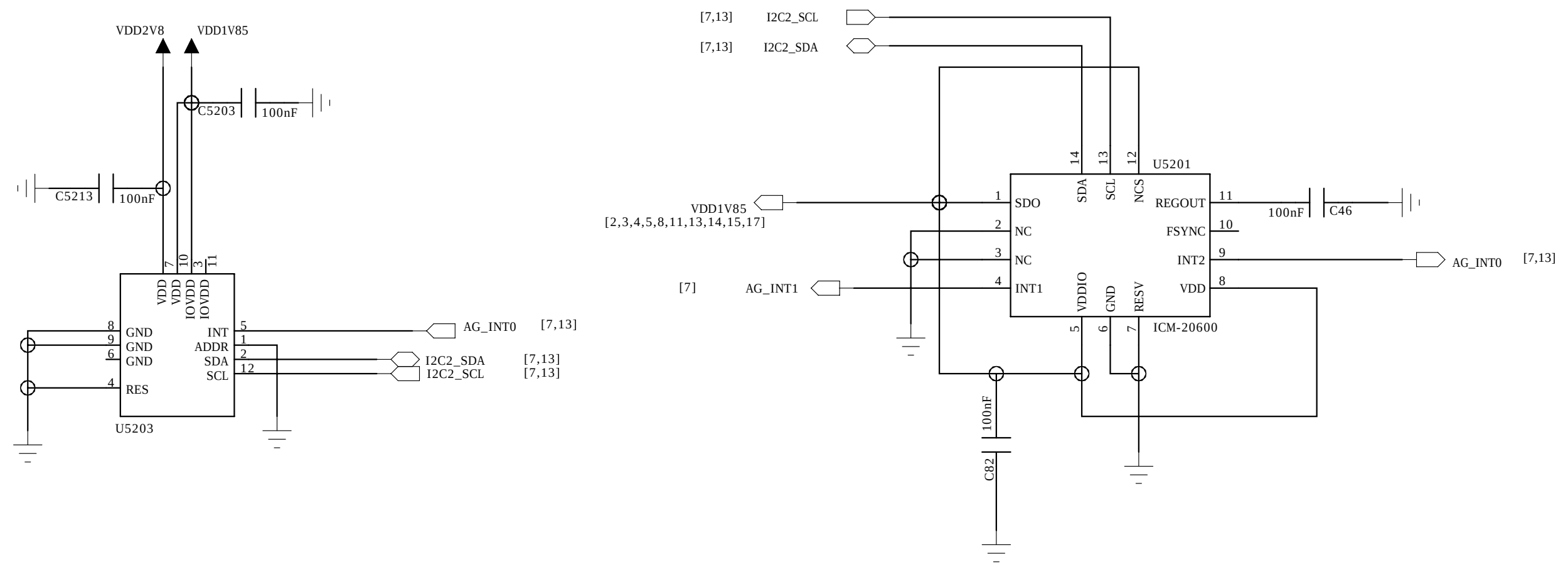
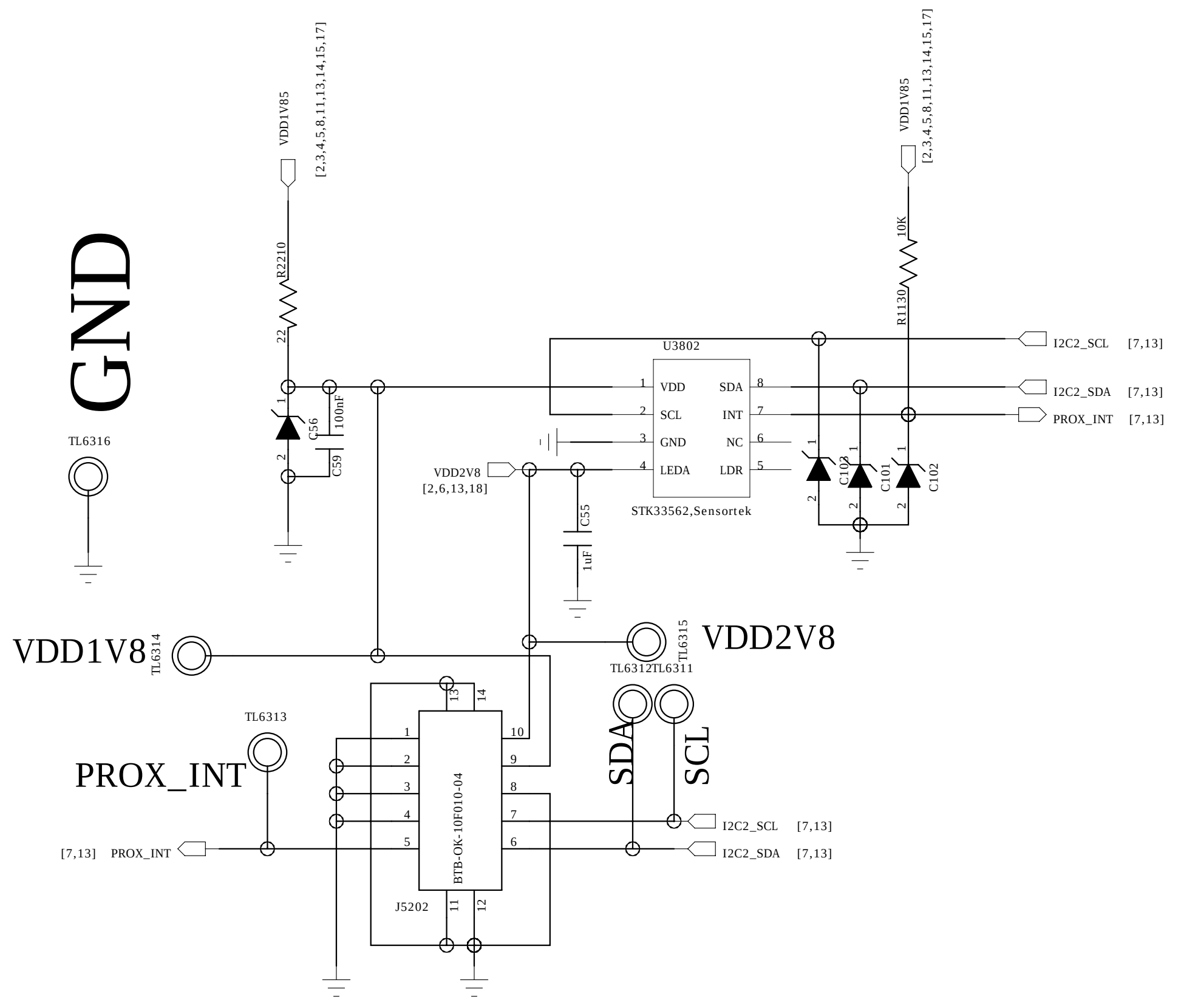
# Accelerometer
# I3C

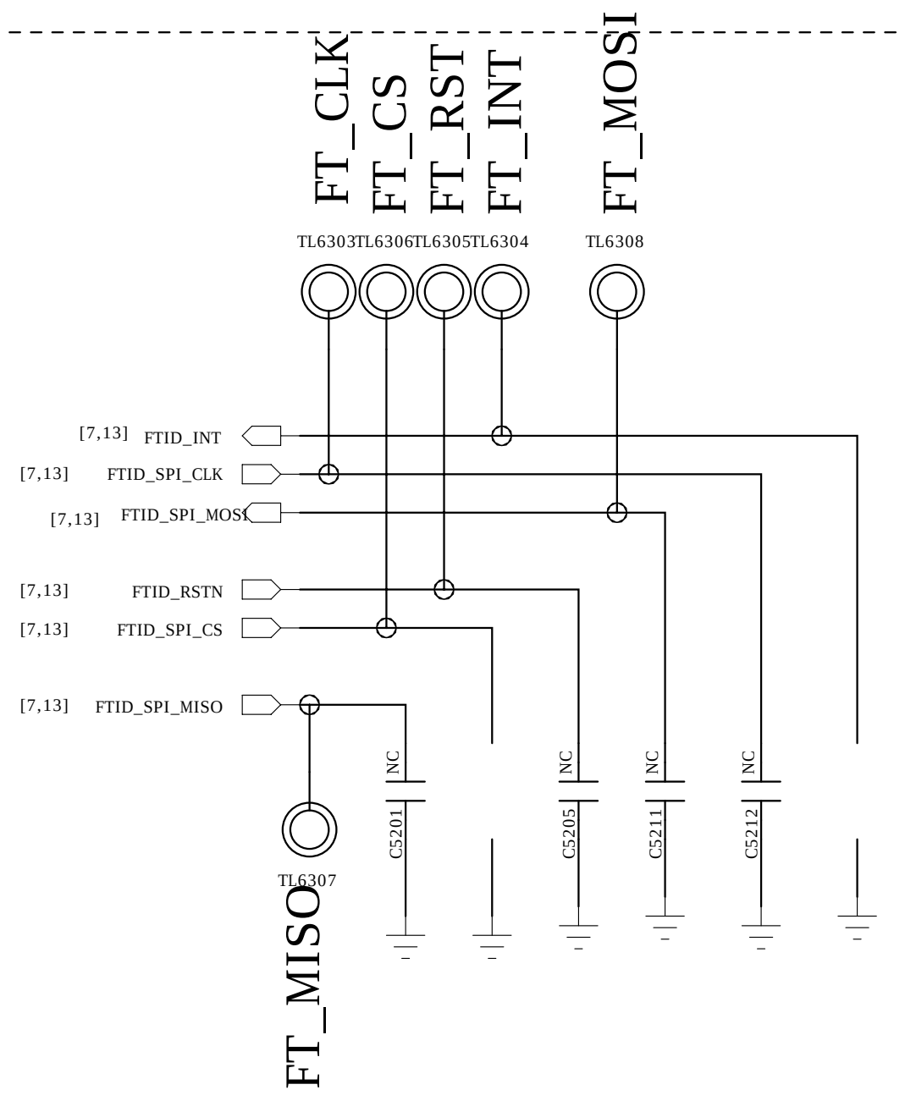


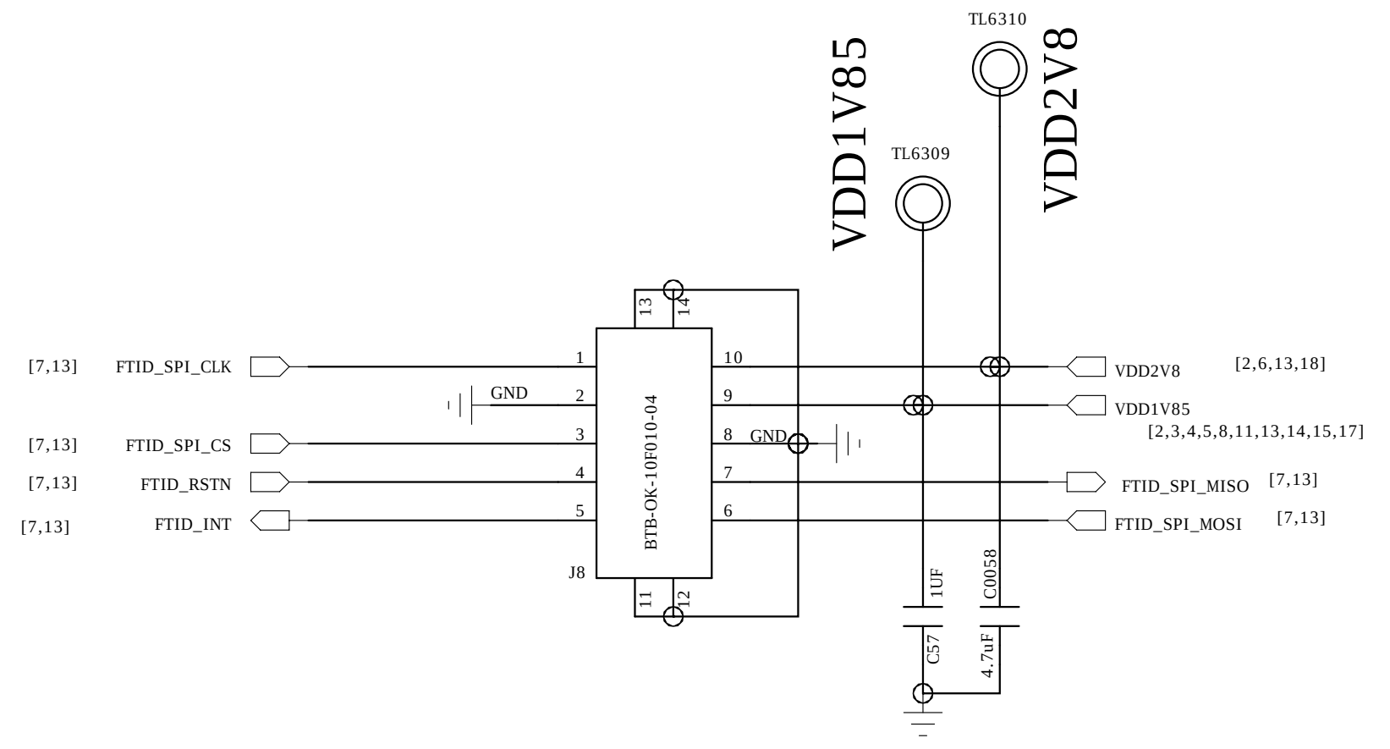
# ALS & PROX



# Magnetic Sensor

# FingerPrint ID





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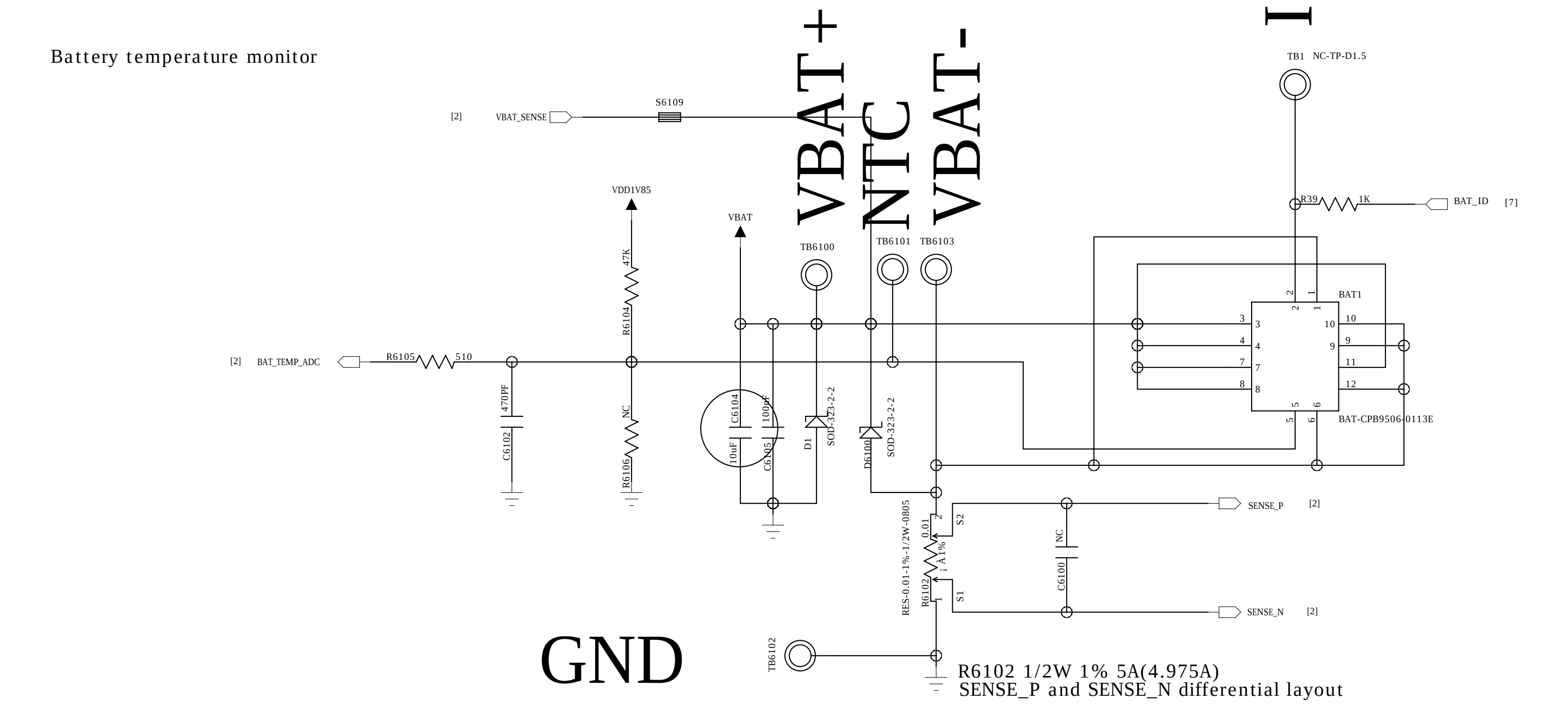
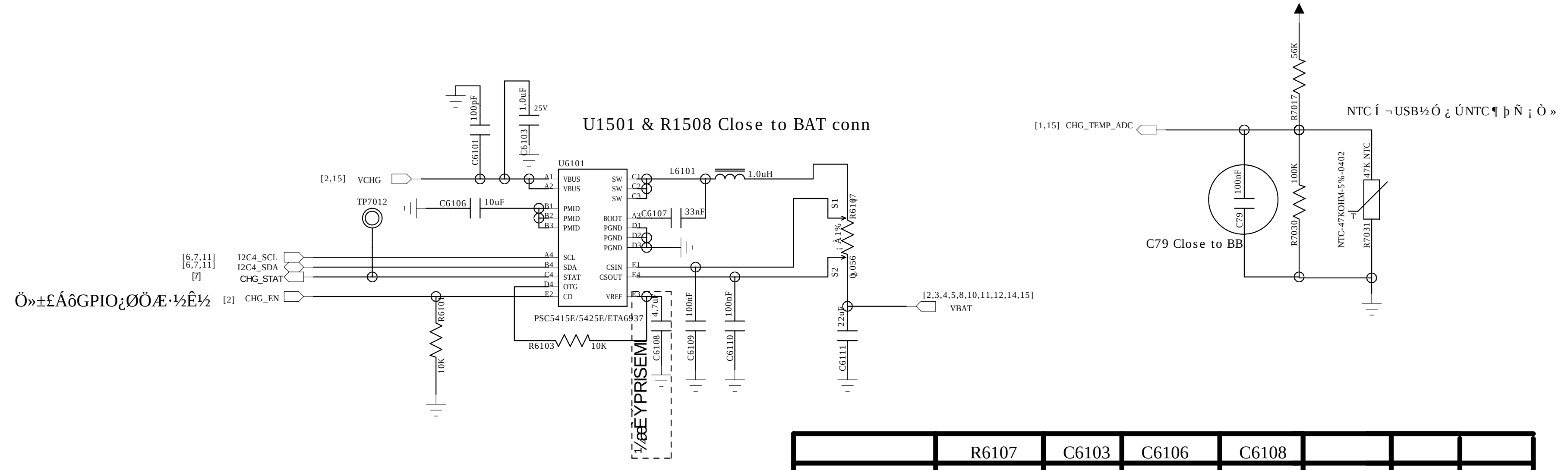
# BATTERY



R6102 1/2W 1% 5A(4.975A)
SENSE_P and SENSE_N differential layout

# CHARGE MAIN BUCK



| | | R6107 | C6103 | C6106 | C6108 | | | |
|---|---|---|---|---|---|---|---|---|
| | Max1.5A 5415E | 56 mohm | 1uf 25V | 22uf 6.3V | 2.2uf 6.3V | NF | 0 ohm | OVP |
| | Max2.25A 5425E | 47 mohm | 10uf 25V | 22uf 6.3V | 2.2uf 6.3V | NF | 0 ohm | OVP |
| default | 1A~2.5A ETA6937 | 0 ohm | 1uf 25V | 10uf 25 V | 1uf 6.3V | 0 ohm | NF | no OVP |

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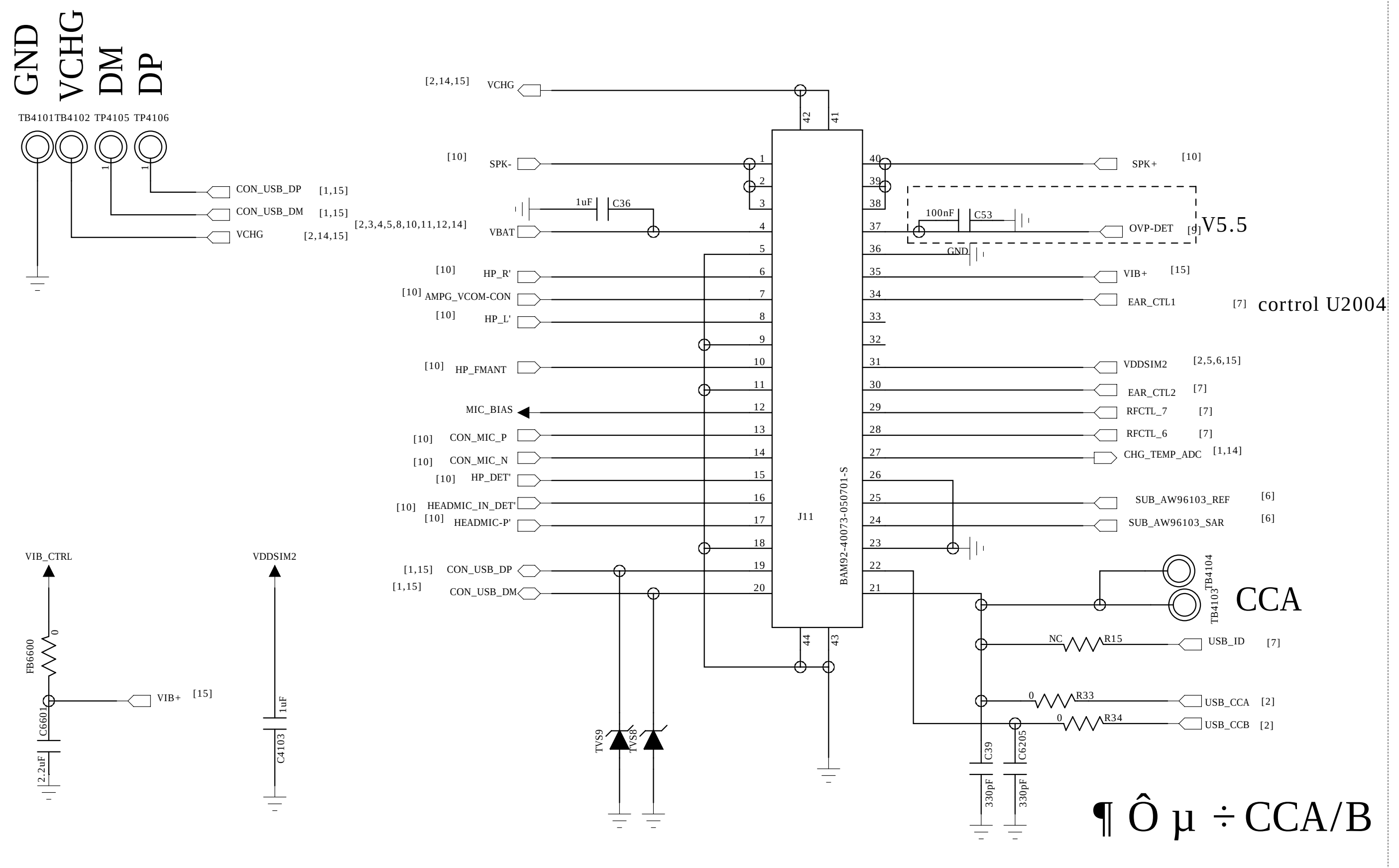
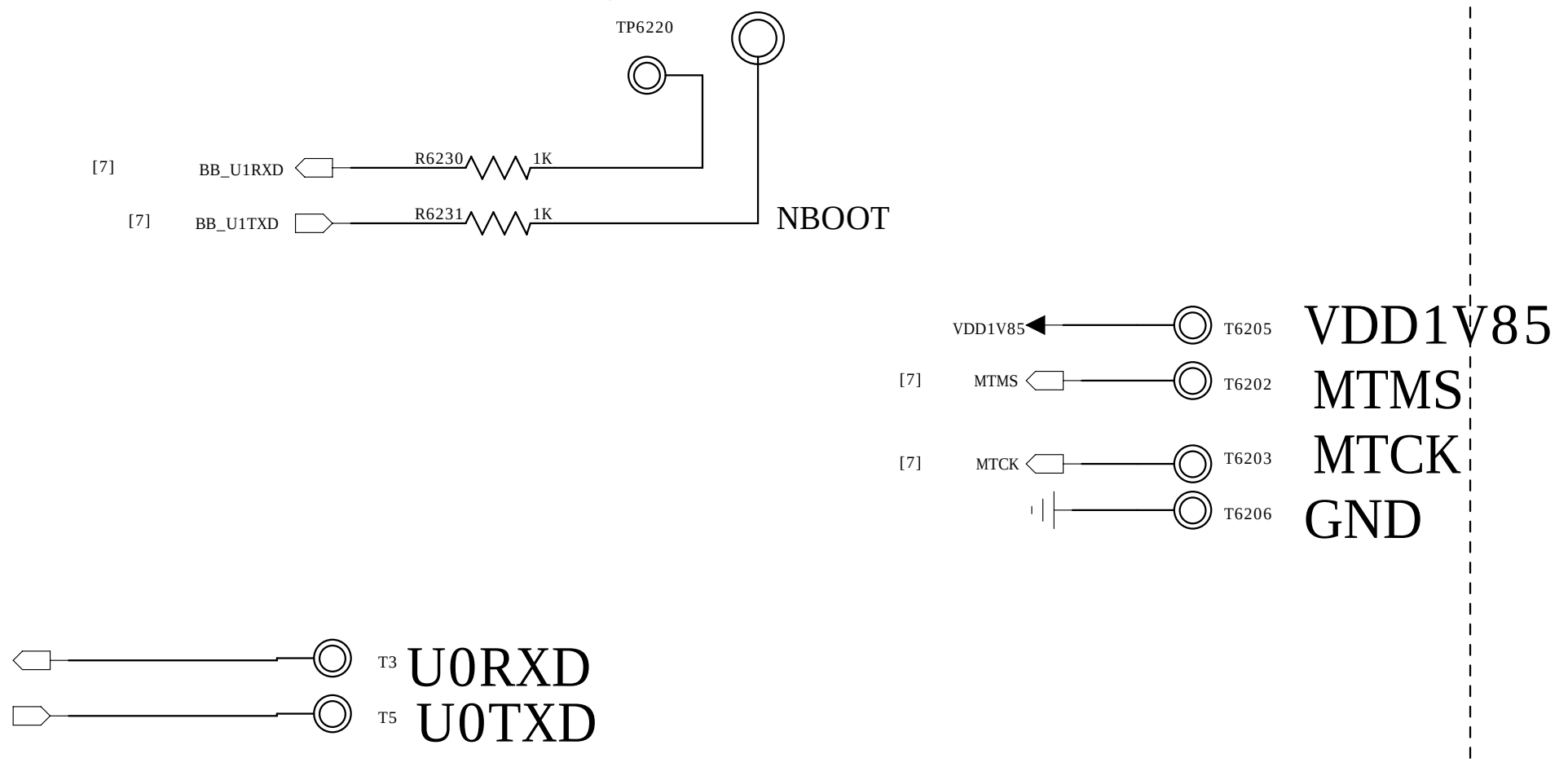
# KB Connector



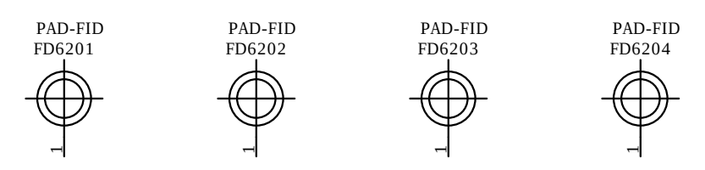
FPC É è ¼ Æ Ê ± Õ â Ð ©pin × ö Ö ± Á ¬ £ ¬ Ô ÚFPC ² » Ó ë gnd » ò Æ ä Ë ü Ð Å º Å Ï à Í ¨

# Strapping pin

# Test Points



# MARK POINT



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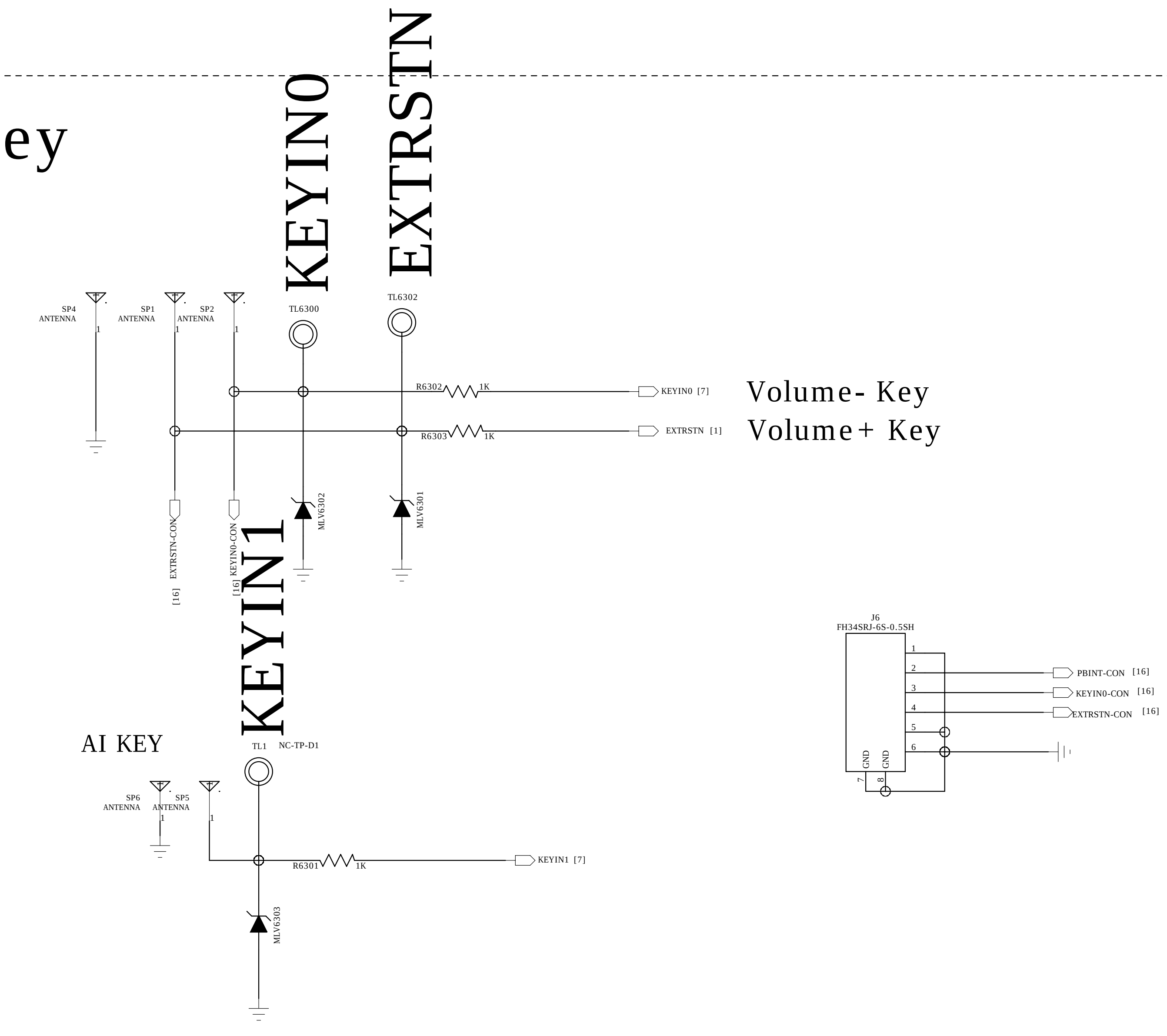
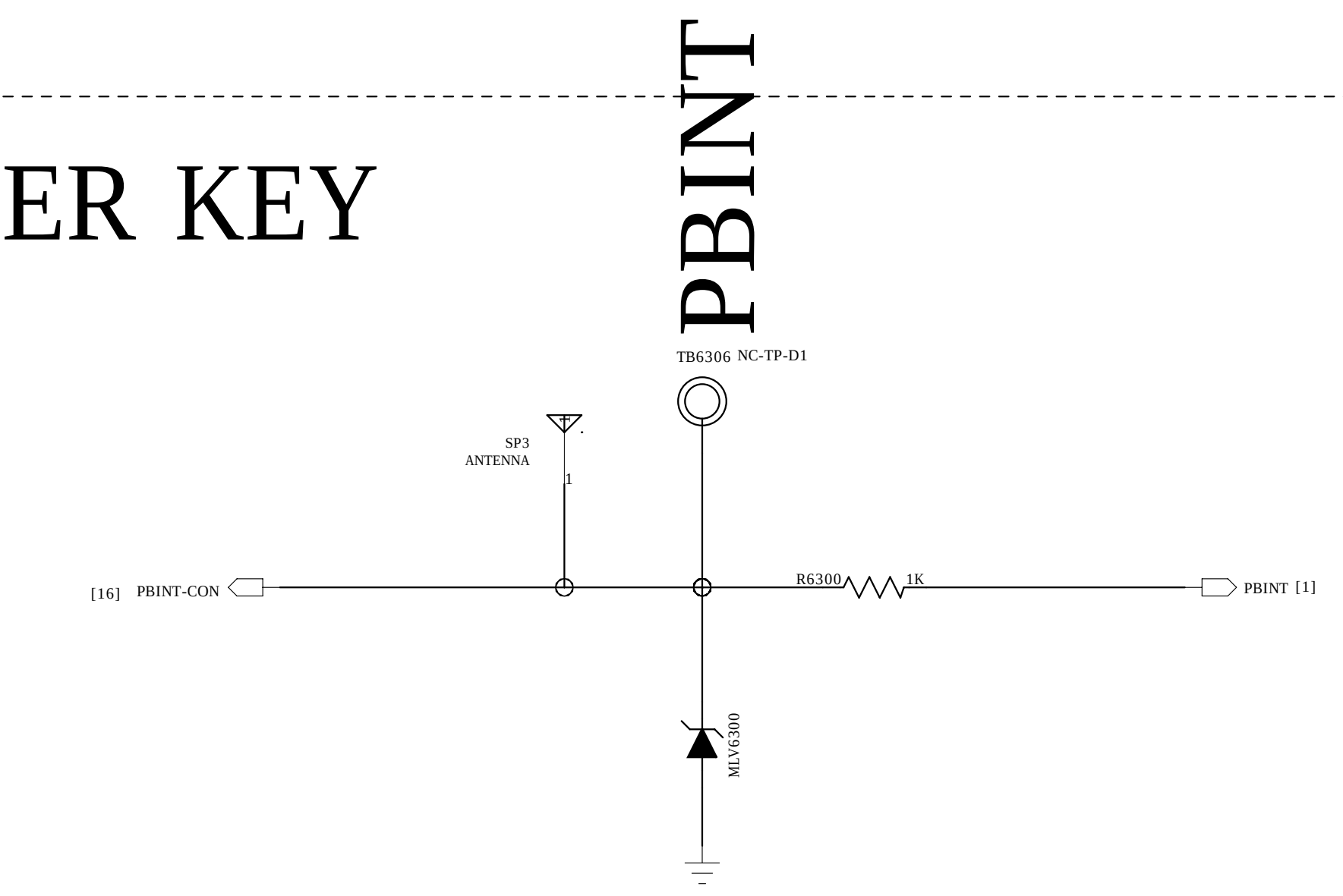
## Volume Key



spport two keys 7S reset ,also support single key 7S reset with UMP510G

Two keys :EXTRSTN+PBINT

## POWER KEY



## RGB

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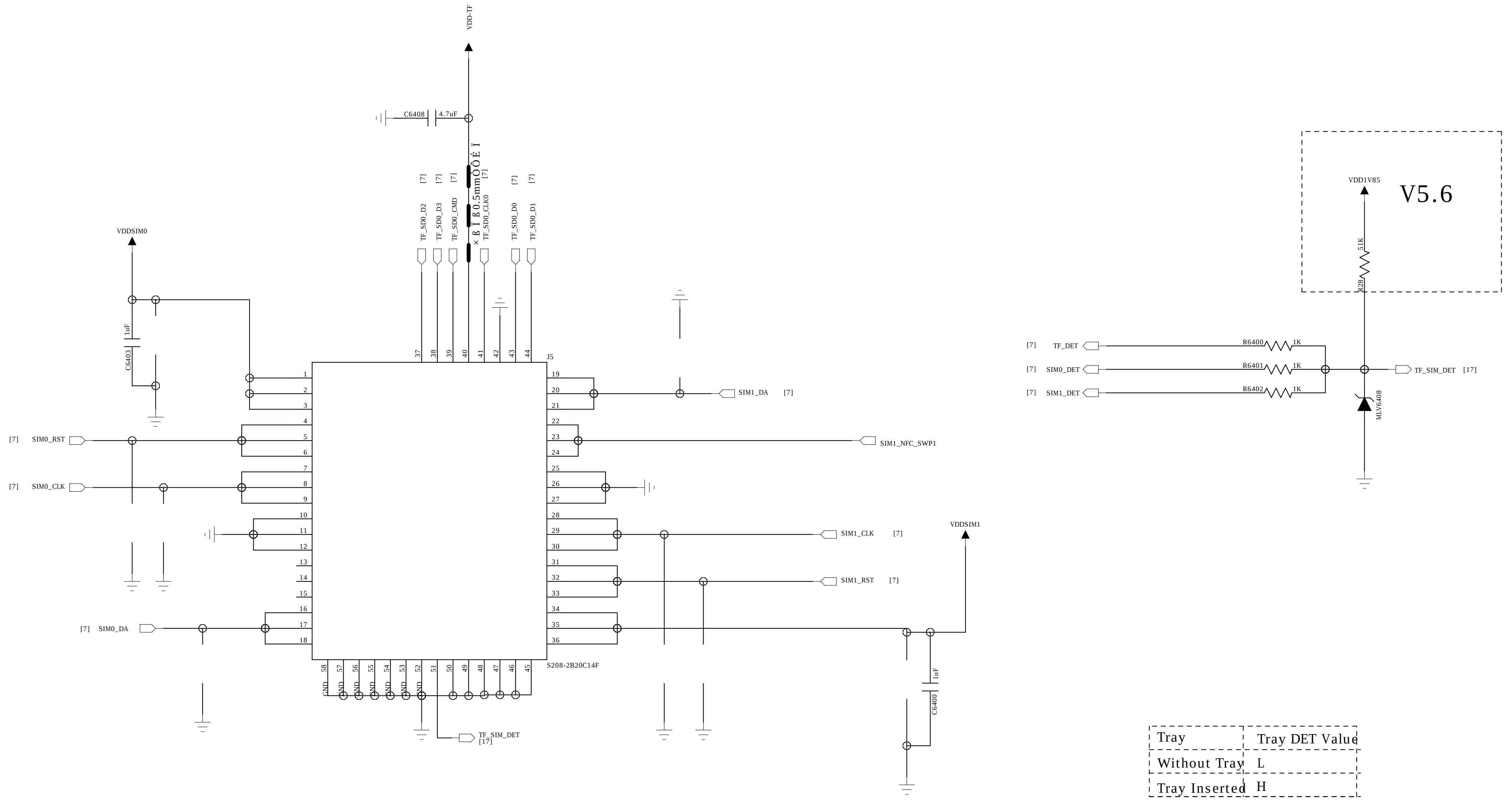
# SIM0 & SIM1 & T_Flash



| Tray | Tray DET Value |
|---|---|
| Without Tray | L |
| Tray Inserted | H |

# V5.5ADD

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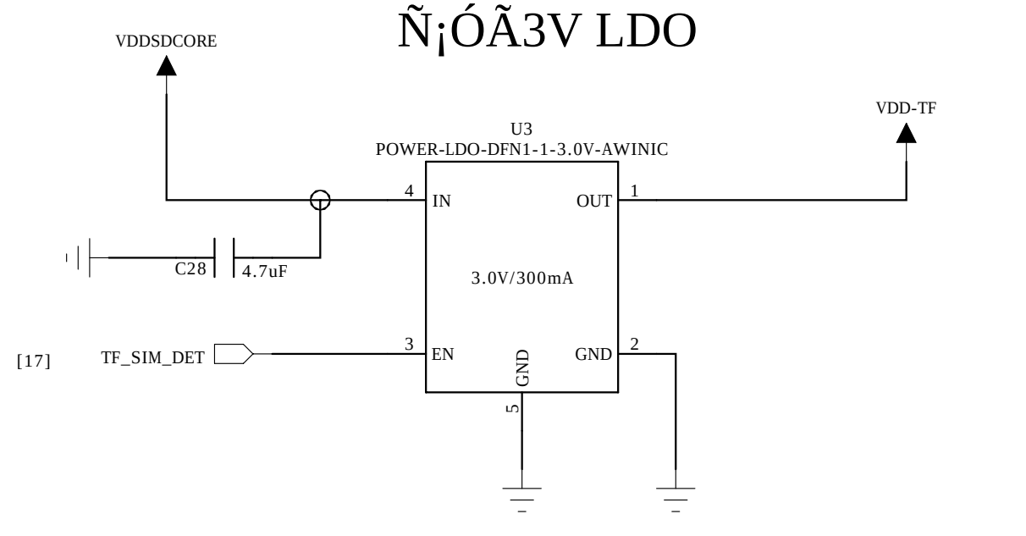
Ñ¡ÓÃ3V LDO



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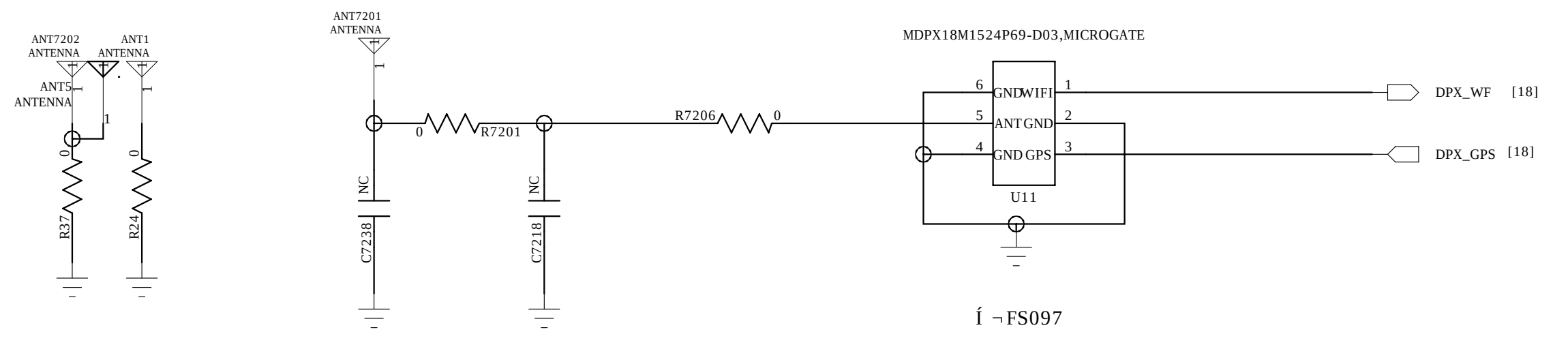
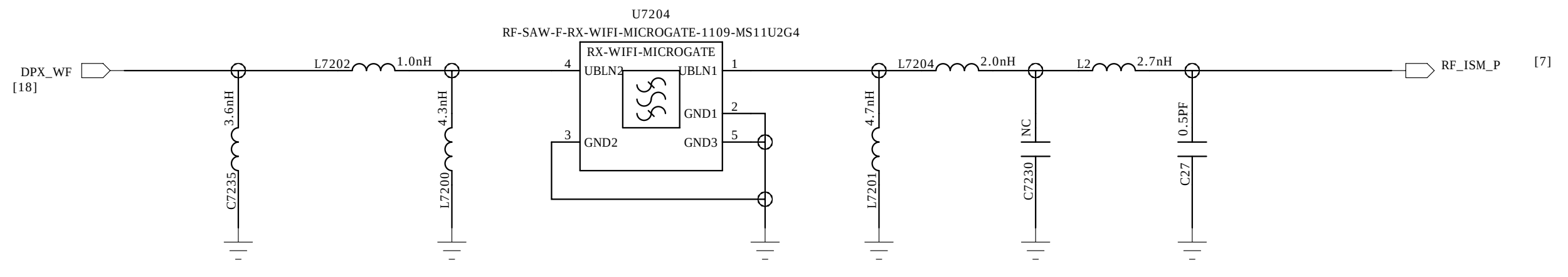
# WIFI&BT ANT

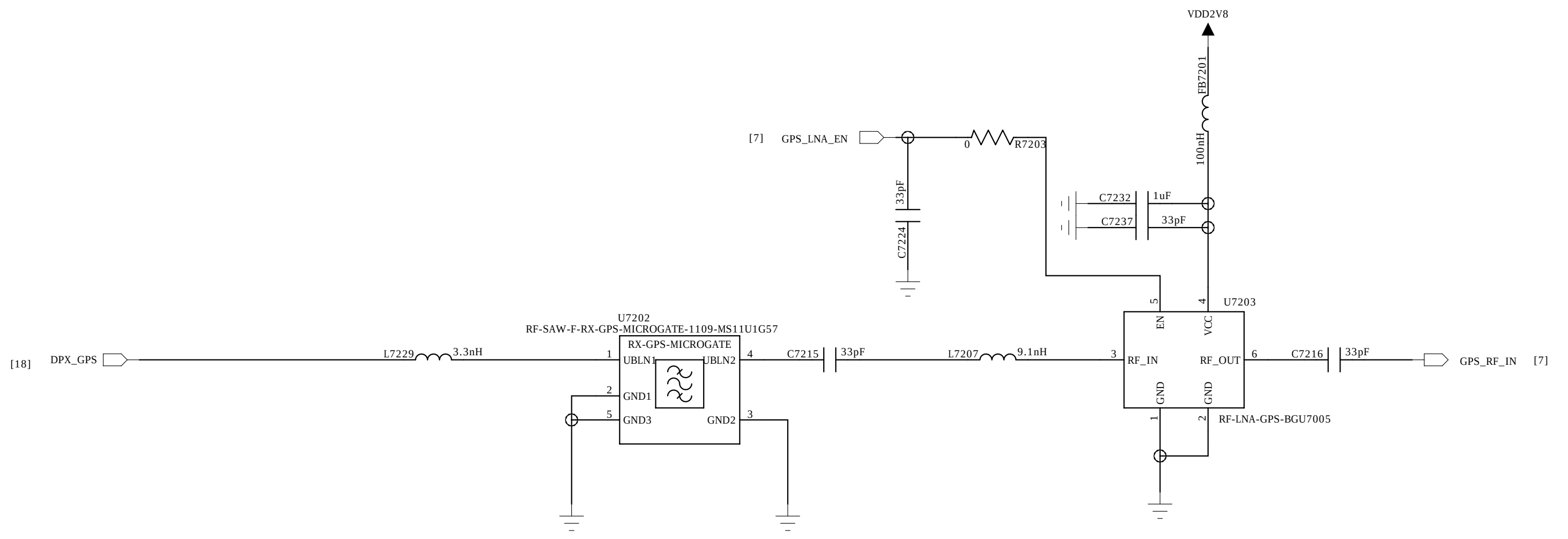


Í ¬FS097

# WIFI/BT SAW



# GNSS SAW LNA



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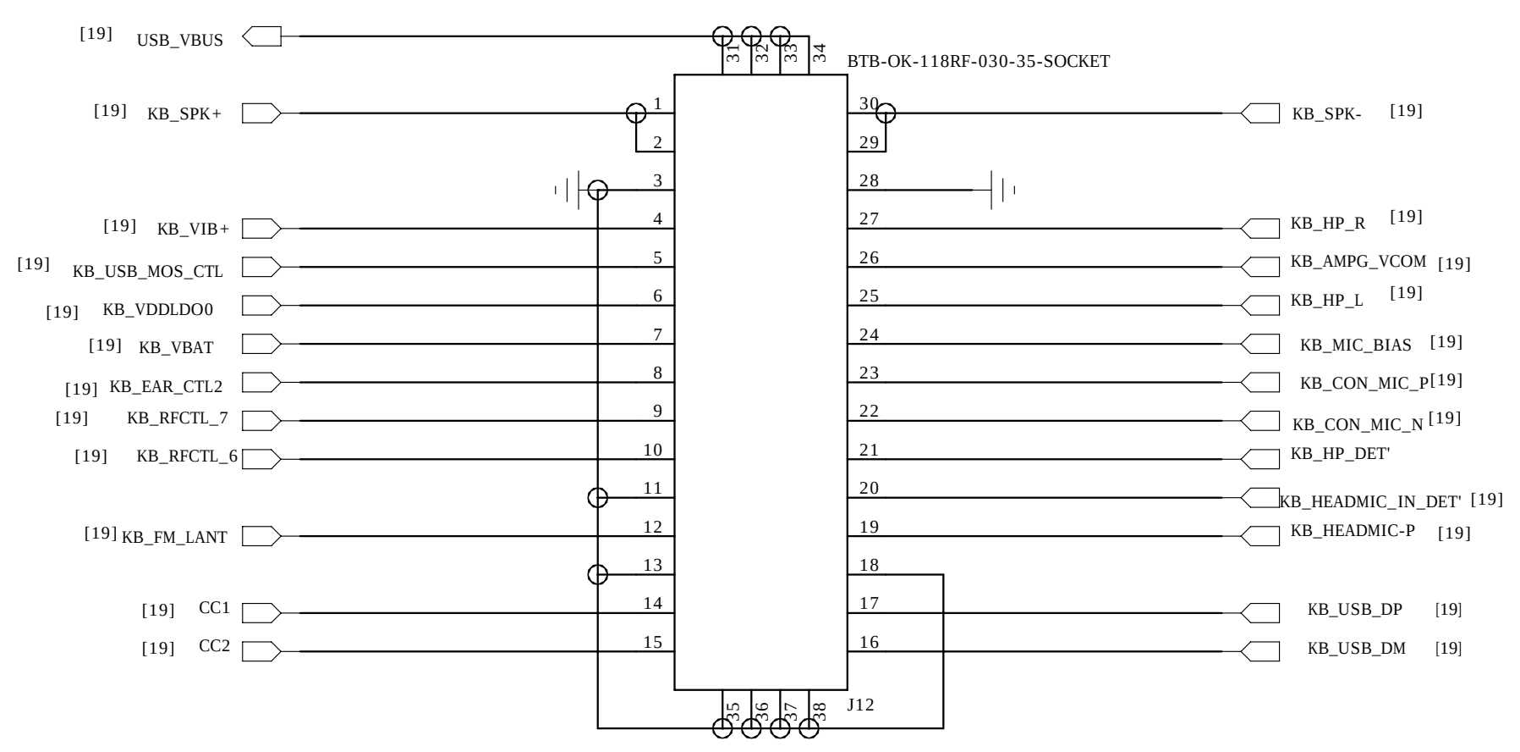
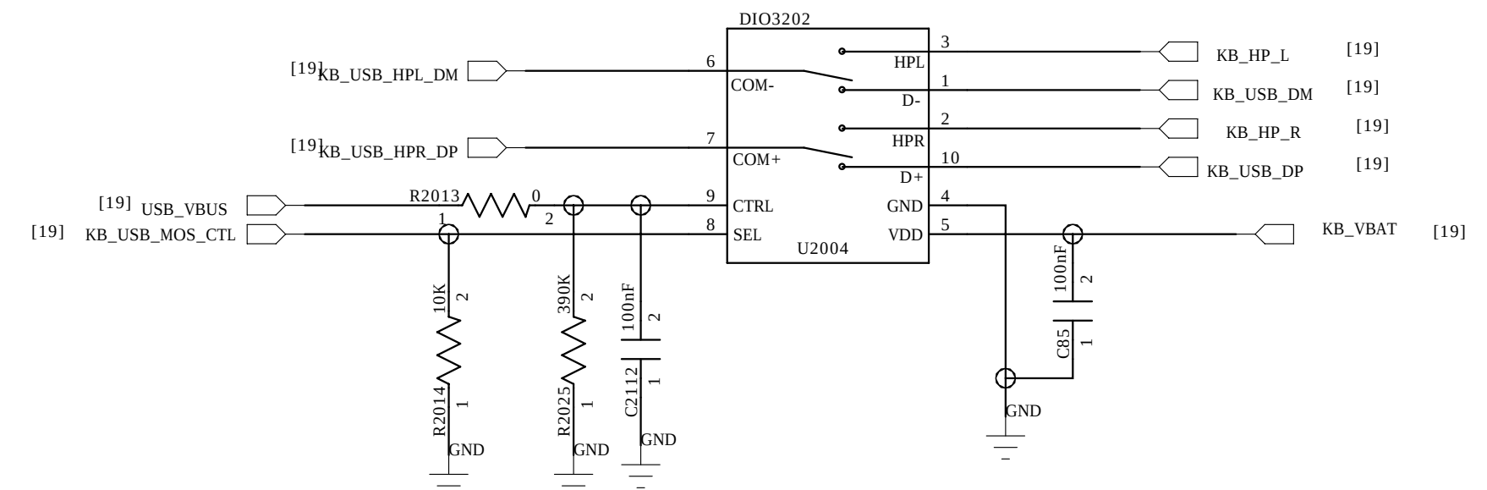
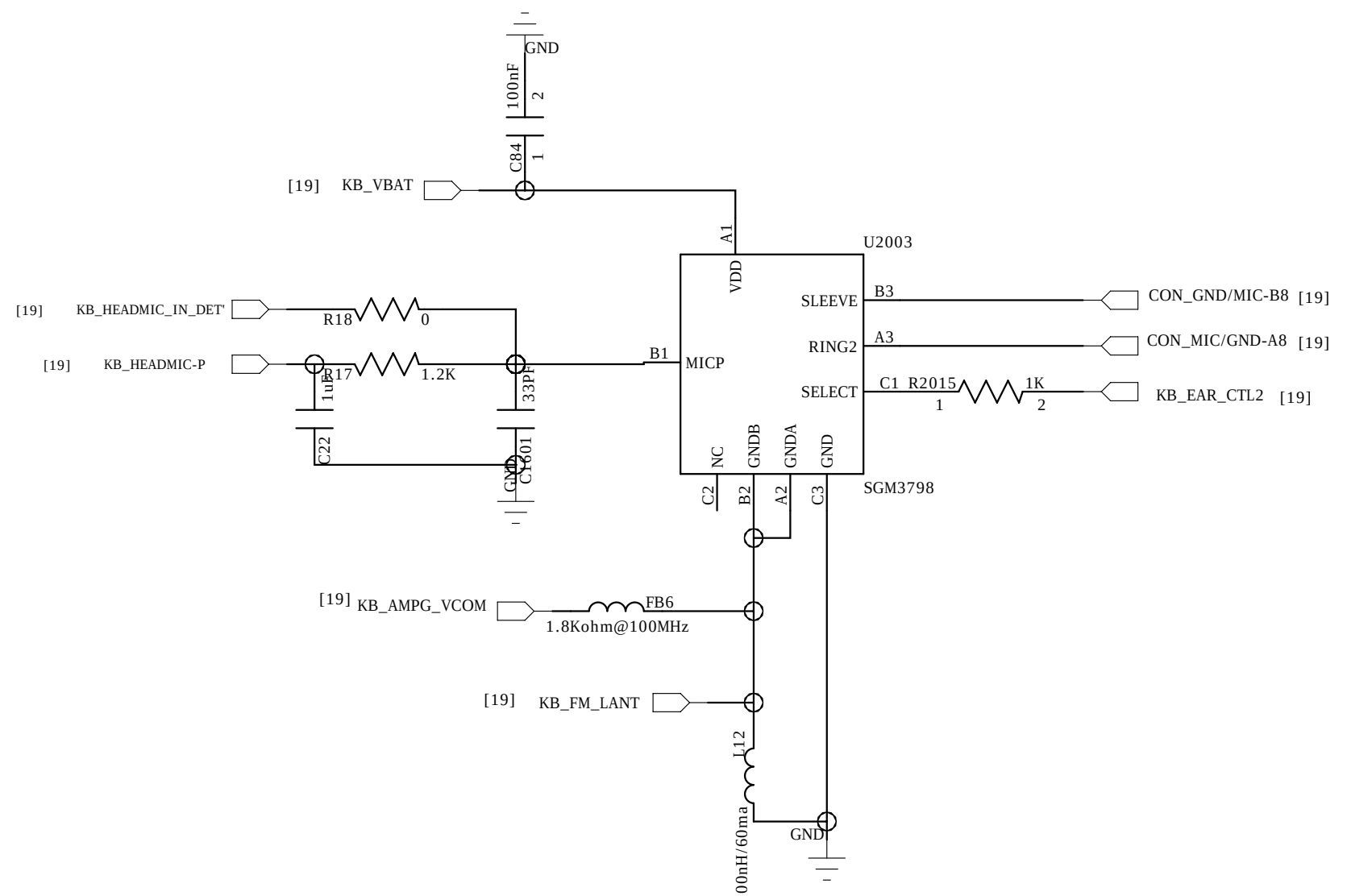
## MB Connector



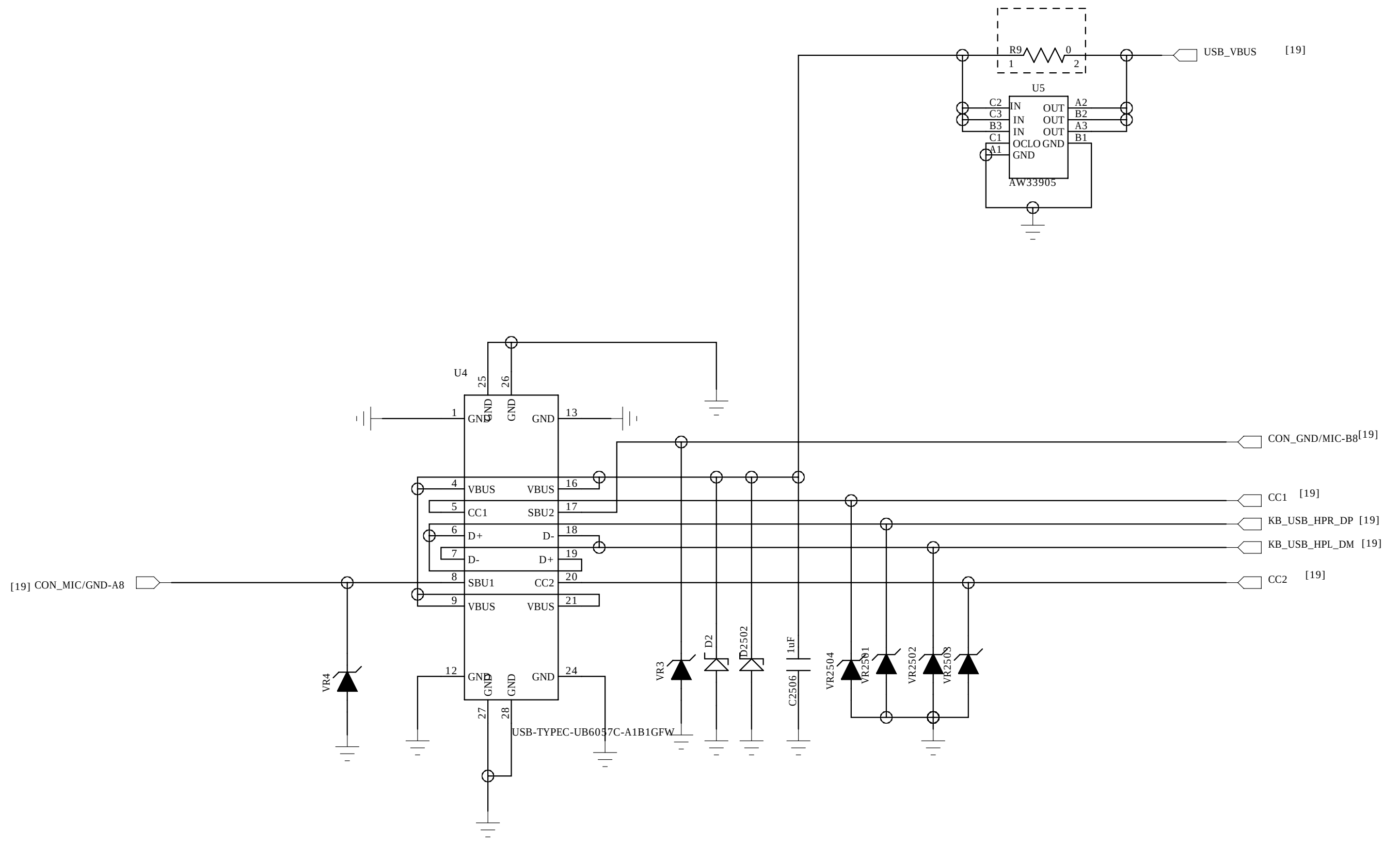
## Audio & USB Switch



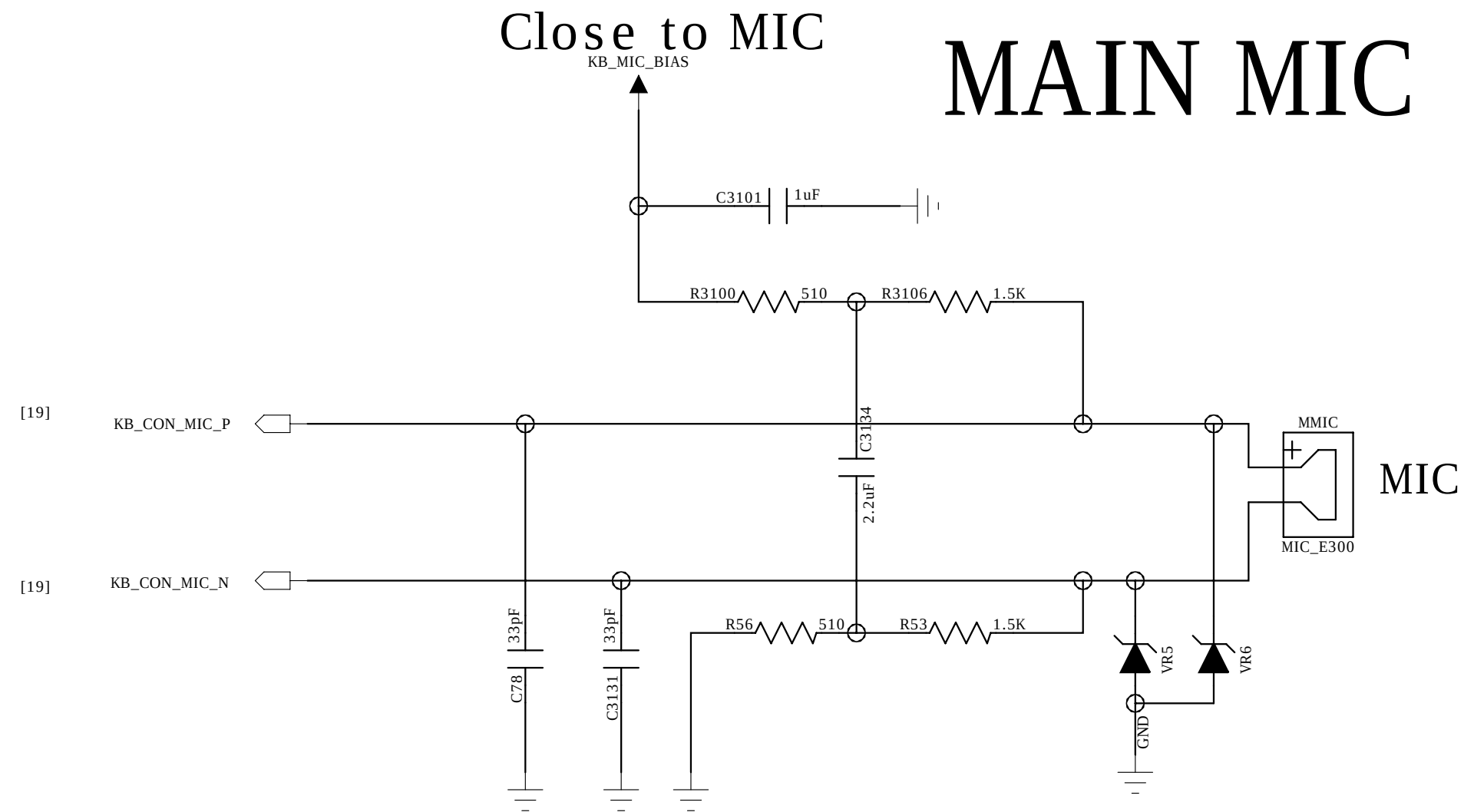
## MIC & GND Switch



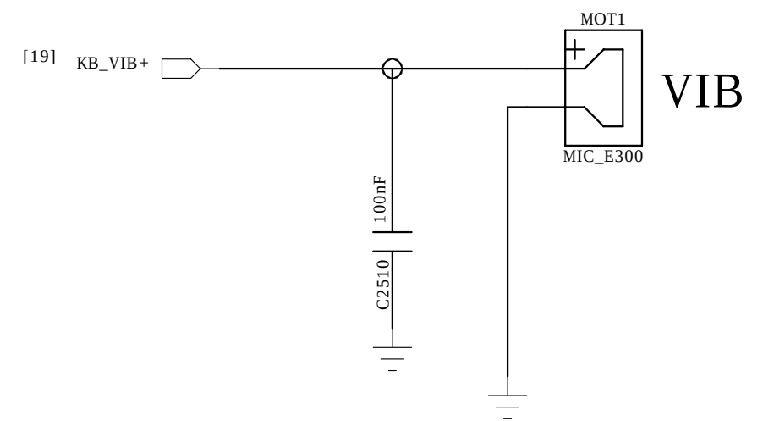
## TYPE_C_ Connector

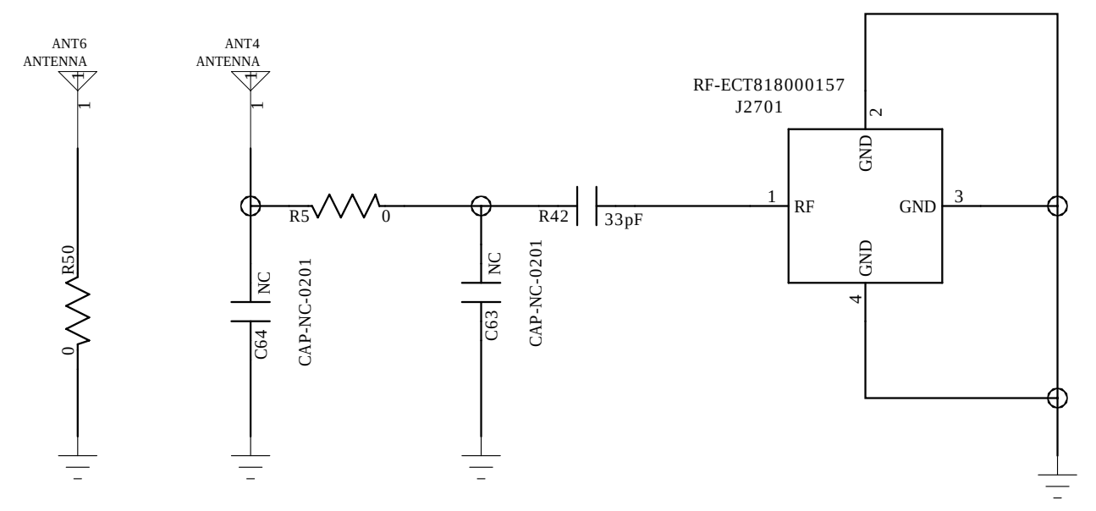


## MAIN MIC

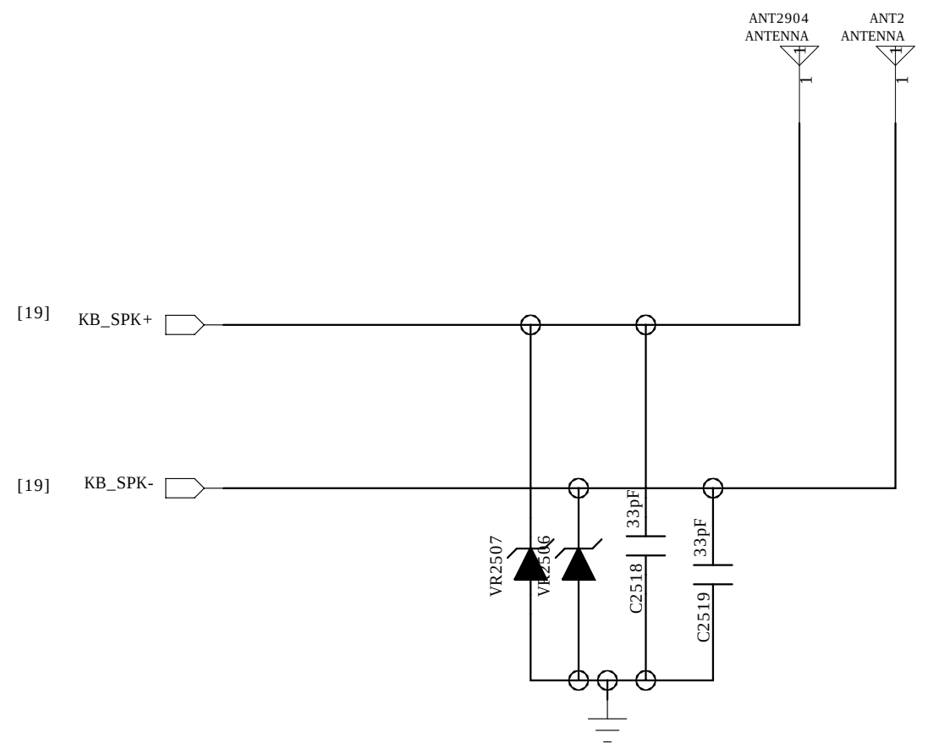


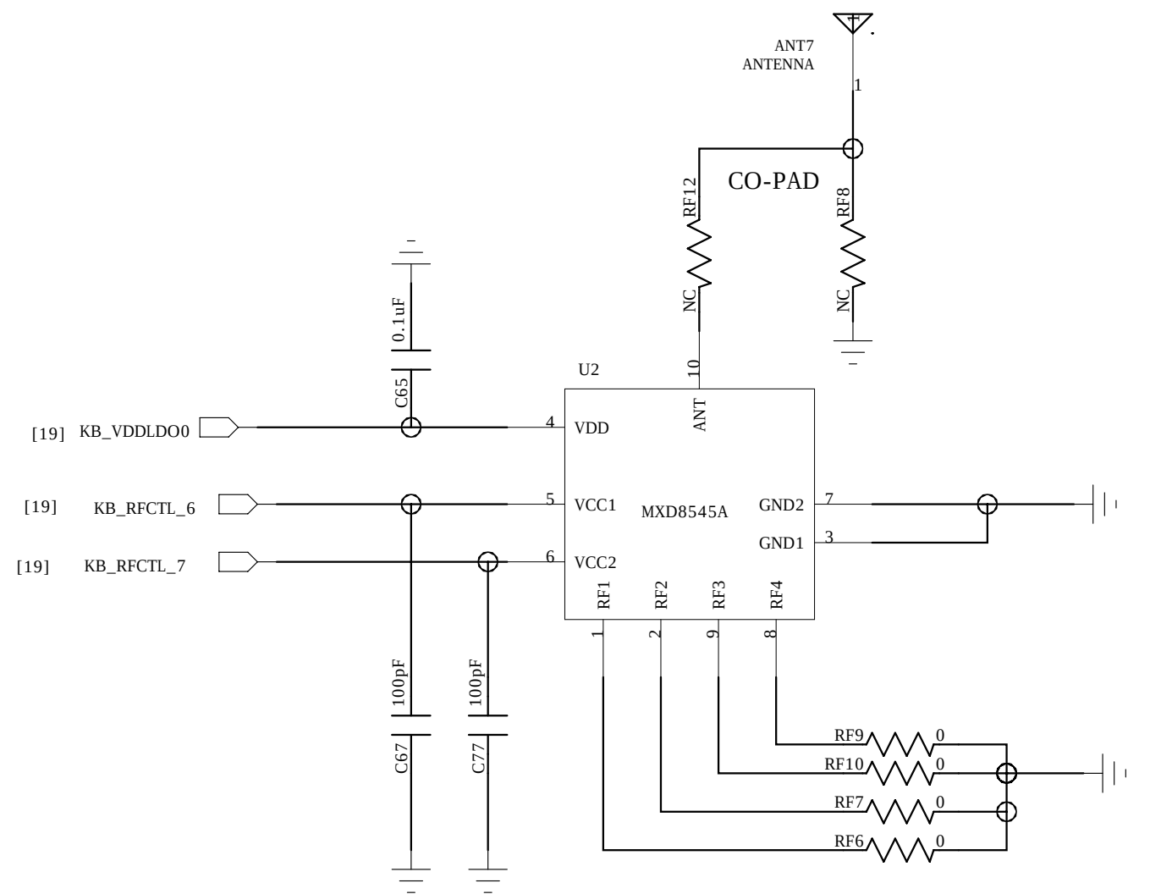
## VIB





## SPK





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| CHECKED: <Checked By> | DATED: <Checked Date> | | | | |
| QUALITY CONTROL: <QC By> | DATED: <QC Date> | | | | |
| RELEASED: <Released By> | DATED: <Release Date> | SCALE: <Scale> | | SHEET: 19 OF 19 | |