Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x04000000				**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
			Baud19200	0x004EA000																															
			Baud28800	0x0075C000																															
			Baud31250	0x00800000																															
			Baud38400	0x009D0000																															
			Baud56000	0x00E50000																															
			Baud57600	0x00EB0000																															
			Baud76800	0x013A9000																															
			Baud115200	0x01D60000																															
			Baud230400	0x03B00000																															
			Baud250000	0x04000000																															
			Baud460800	0x07400000																															
			Baud921600	0x0F000000																															
			Baud1M	0x10000000																															

6.19.9.44 RXD

RXD EasyDMA channel

6.19.9.44.1 RXD.PTR

Address offset: 0x534

Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	PTR																																	

Data pointer

See the memory chapter for details about which memories are available for EasyDMA.

6.19.9.44.2 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	MAXCNT		[1..0x1FFF]																															

Maximum number of bytes in receive buffer

6.19.9.44.3 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A A A A A A A A A A A A A A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	AMOUNT		[1..0x1FFF]	Number of bytes transferred in the last transaction

6.19.9.45 TXD

TXD EasyDMA channel

6.19.9.45.1 TXD.PTR

Address offset: 0x544

Data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PTR			Data pointer See the memory chapter for details about which memories are available for EasyDMA.

6.19.9.45.2 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A A A A A A A A A A A A A A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	MAXCNT		[1..0x1FFF]	Maximum number of bytes in transmit buffer

6.19.9.45.3 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A A A A A A A A A A A A A A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	AMOUNT		[1..0x1FFF]	Number of bytes transferred in the last transaction

6.19.9.46 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	C B B B
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
	RW	HWFC			Hardware flow control
			Disabled	0	Disabled
			Enabled	1	Enabled
B	RW	PARITY			Parity
			Excluded	0x0	Exclude parity bit
			Included	0x7	Include even parity bit
C	RW	STOP			Stop bits
			One	0	One stop bit
			Two	1	Two stop bits

6.19.10 Electrical specification

6.19.10.1 UARTE electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
f_{UARTE}	Baud rate for UARTE[22].			1000	kbps
$t_{UARTE,CTSH}$	CTS high time	1			µs
$t_{UARTE,START}$	Time from STARTRX/STARTTX task to transmission started		0.25		µs

6.20 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

```
timeout [s] = ( CRV + 1 ) / 32768
```

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter CLOCK — Clock control on page 70.

6.20.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

[22] High baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

6.20.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

6.20.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See Reset on page 56 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be reset from several reset sources, see Reset behavior on page 57.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.

6.20.4 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
WDT : S	0x50018000	US	NS	NA	No	Watchdog timer
WDT : NS	0x40018000					

Register overview

Register	Offset	TZ	Description
TASKS_START	0x000		Start the watchdog
SUBSCRIBE_START	0x080		Subscribe configuration for task START
EVENTS_TIMEOUT	0x100		Watchdog timeout
PUBLISH_TIMEOUT	0x180		Publish configuration for event TIMEOUT
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
RUNSTATUS	0x400		Run status
REQSTATUS	0x404		Request status
CRV	0x504		Counter reload value
RREN	0x508		Enable register for reload request registers
CONFIG	0x50C		Configuration register
RR[n]	0x600		Reload request n

6.20.4.1 TASKS_START

Address offset: 0x000

Start the watchdog

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_START			Start the watchdog
			Trigger	1	Trigger task

6.20.4.2 SUBSCRIBE_START

Address offset: 0x080

Subscribe configuration for task START

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task START will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

6.20.4.3 EVENTS_TIMEOUT

Address offset: 0x100

Watchdog timeout

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_TIMEOUT			Watchdog timeout
			NotGenerated	0	Event not generated
			Generated	1	Event generated

6.20.4.4 PUBLISH_TIMEOUT

Address offset: 0x180

Publish configuration for event TIMEOUT

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event TIMEOUT will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

6.20.4.5 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	TIMEOUT			Write '1' to enable interrupt for event TIMEOUT
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.20.4.6 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	TIMEOUT			Write '1' to disable interrupt for event TIMEOUT
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.20.4.7 RUNSTATUS

Address offset: 0x400

Run status

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
	R	RUNSTATUSWDT			Indicates whether or not the watchdog is running
			NotRunning	0	Watchdog not running
			Running	1	Watchdog is running

6.20.4.8 REQSTATUS

Address offset: 0x404

Request status

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				H G F E D C B A
Reset 0x00000001				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1**

ID	R/W	Field	Value ID	Value	Description
A-H	R	RR[i] (i=0..7)			Request status for RR[i] register
			DisabledOrRequested	0	RR[i] register is not enabled, or are already requesting reload
			EnabledAndUnrequested	1	RR[i] register is enabled, and are not yet requesting reload

6.20.4.9 CRV

Address offset: 0x504

Counter reload value

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	CRV		[0x0000000F..0xFFFFFFFF]																															
				Counter reload value in number of cycles of the 32.768 kHz clock																																

6.20.4.10 RREN

Address offset: 0x508

Enable register for reload request registers

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												H	G	F	E	D	C	B	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value																															
A-H	RW	RR[i] (i=0..7)																																	
				Enable or disable RR[i] register																																	
			Disabled	0																																	
				Disable RR[i] register																																	
			Enabled	1																																	
				Enable RR[i] register																																	

6.20.4.11 CONFIG

Address offset: 0x50C

Configuration register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																C			
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value																															
	RW	SLEEP																																	
				Configure the watchdog to either be paused, or kept running, while the CPU is sleeping																																	
			Pause	0																																	
				Pause watchdog while the CPU is sleeping																																	
			Run	1																																	
				Keep the watchdog running while the CPU is sleeping																																	
C	RW	HALT																																	
				Configure the watchdog to either be paused, or kept running, while the CPU is halted by the debugger																																	
			Pause	0																																	
				Pause watchdog while the CPU is halted by the debugger																																	
			Run	1																																	
				Keep the watchdog running while the CPU is halted by the debugger																																	

6.20.4.12 RR[n] (n=0..7)

Address offset: 0x600 + (n × 0x4)

Reload request n

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	RR																																	
				Reload request register																																	
			Reload	0x6E524635																																	
				Value to request a reload of the watchdog timer																																	

6.20.5 Electrical specification

6.20.5.1 Watchdog Timer Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
t_{WDT}	Time out interval	31 µs		36 h	

7 LTE modem

The nRF9161 SiP contains a Low-Power Wide-Area (LPWA) network processor with dedicated flash/RAM, which controls the radio and baseband hardware components. LTE capabilities are provided by installing Nordic Semiconductor firmware, which complies with 3GPP LTE release 14 Cat-M1 and Cat-NB1/NB2 standards.

The following is an overview of the LTE modem, with a figure showing key components:

- RF transceiver
- Modem baseband (BB)
- Embedded flash/RAM
- LPWA network processor and peripherals

They provide functions for the LTE L1, L2, and L3 (layers 1, 2, and 3 respectively) as well as IP communication layers. Peripherals provide hardware services for the LPWA network processor operating system and secure execution environment.

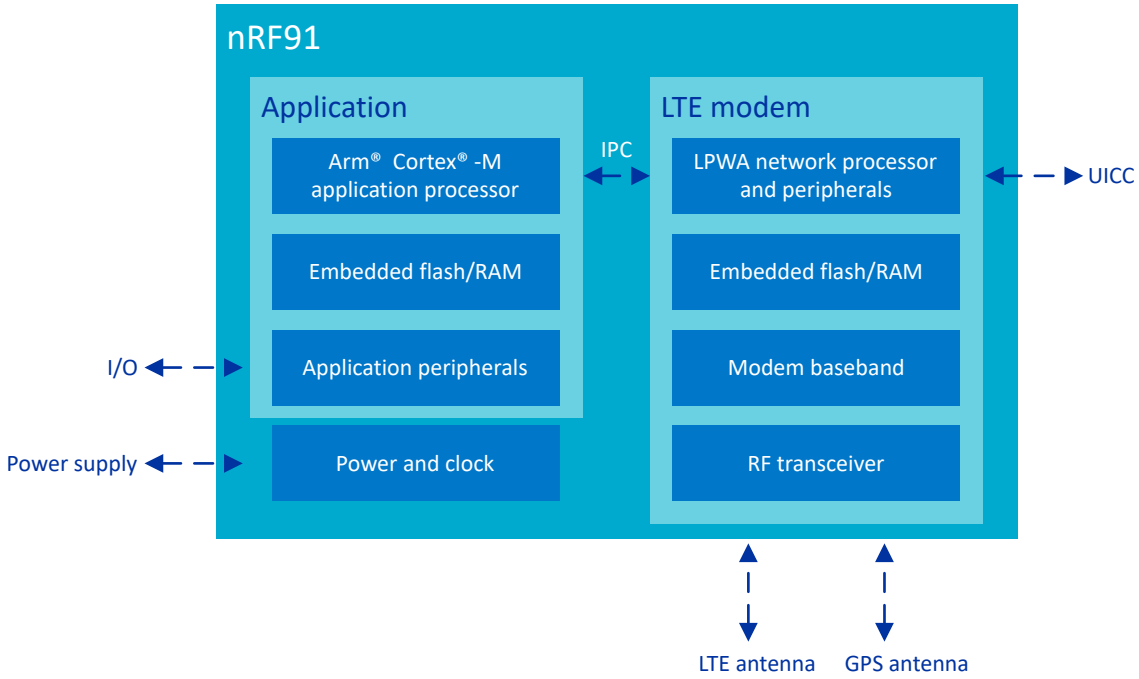


Figure 109: nRF9161 LTE modem functional overview

Application and LPWA network domains interact through the interprocessor communication (IPC) mechanism. The LTE modem is accessible to users through the modem API.

The application processor is the system master and is responsible for starting and stopping the LTE modem. The LPWA network processor enables the clocks and power required for its own operation. The platform handles shared resources, such as clocks, and does not need user participation. In cases where a hard fault is detected in the modem, the application domain will perform a hard reset of the modem.

The nRF9161 LTE modem feature set depends on the modem firmware version and the application firmware. For more information on the LTE modem API, see nRF Connect SDK API documentation and nRF91 AT Commands.

The key features of the LTE modem are:

- Complete modem with baseband and RF transceiver

- 3GPP release 14 compliant LTE categories:
  - Cat-M1 (eMTC - enhanced machine type communication)
  - Cat-NB1 (NB-IoT - narrowband Internet of things)
  - Cat-NB2 (NB-IoT)
- Power saving modes
- Supports LTE bands from 700 MHz to 2.2 GHz through a single 50 Ω antenna pin
  - ANT antenna pin is DC grounded
- RX sensitivity: -108 dBm for Cat-M1 and -114 dBm for Cat-NB1 and Cat-NB2
  - As defined in 3GPP conformance test specification TS 36.521-1
- 1.8 V MIPI RF Front-End (MIPI RFFE) digital control interface and MAGPIO control interface for external RF applications.
- LTE modem internal ADC that is also used for some AT command interface services, for example, for battery monitoring
- 1.8 V UICC (universal integrated circuit card) interface, based on ISO/IEC 7816-3 and compliant with:
  - UICC (ETSI TS 102 221)
  - eUICC (ETSI TS 103 383)

Note: The nRF9161 modem feature set depends on the modem firmware version and the application firmware.

7.1 SIM card interface

The LTE modem supports the universal integrated circuit card (UICC) interface.

Only UICCs with electrical interfaces specified in ISO/IEC 7816-3 are supported. UICCs with IC-USB, CLF or MMC interfaces are not supported.

The supported UICC/eUICC interface is compliant with:

- ETSI TS 102 221: Smart Cards; UICC-Terminal interface; Physical and logical characteristics
- ETSI TS 103 383: Smart Cards; Embedded UICC; Requirements Specification

The physical interface towards the eUICC is the same as that towards the removable UICC.

By default, only the class C (supply voltage 1.8 V nominal) operation is supported. Support for legacy class B (supply voltage 3.0 V nominal) operation must be built with external components, including an external power supply and the level shifters towards the LTE modem UICC interface.

The LTE modem supports powering down the UICC during PSM and eDRX idle mode if the UICC supports this feature as specified in 3GPP TS 24.301. To reach the lowest total power consumption of the complete cellular IoT product, only UICCs supporting power down mode during PSM and eDRX idle mode sleep intervals should be considered.

The LTE modem controls the physical interfaces towards the UICC and implements the transport protocol over the four-pin ISO/IEC 7816-3 interface:

- VCC (power supply) – LTE modem drives this
- CLK (clock signal) – LTE modem drives this
- RST (reset signal) – LTE modem drives this
- I/O (input/output serial data) – Bi-directional

The interface between the LTE modem, the UICC (SIM card) connector, and the ESD device is shown in the following figure.

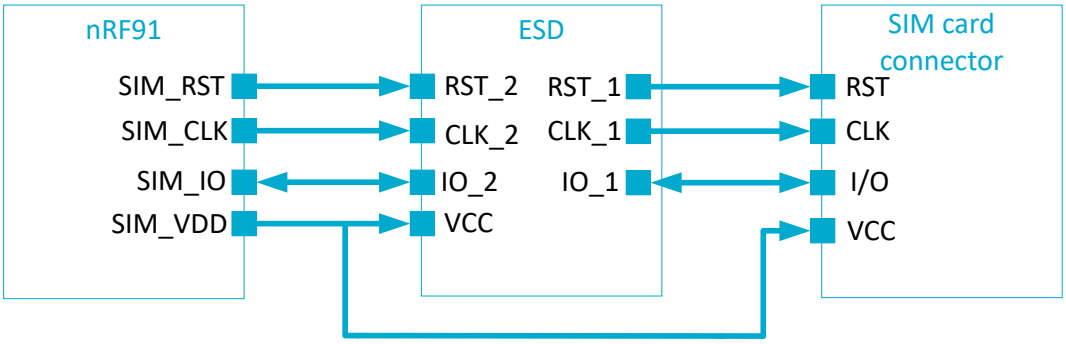


Figure 110: Connections between LTE modem, card connector, and the ESD device

Only standard transmission speeds are supported as specified in ETSI TS 102 221.

Note: Before removing the UICC, the LTE modem must be stopped through the modem API.

An electrostatic discharge (ESD) protection device compatible with UICC cards must be used between the removable card and the LTE modem, to protect LTE modem against harmful ESD from the card connector.

7.2 LTE coexistence interface

The LTE modem uses a dedicated three-pin interface for RF interference avoidance towards a companion radio device such as an external positioning device or *Bluetooth*® Low Energy device.

The interface has the following outputs:

- COEX0 – Output from the LTE modem to the external device. When internal GPS is used, COEX0 can be used as active high control for the external LNA component.
- COEX1 – Output from the LTE modem to the external device. When internal GPS is used, COEX1 delivers the GPS 1PPS (one pulse per second) time mark pulse. The 1PPS feature must not be used when LTE is enabled.
- COEX2 – Output from the LTE modem to the external device. When active high, this indicates that the LTE modem transceiver is turned on. COEX2 can also be treated as an active low grant from the LTE modem to the external device, indicating permission to transmit and receive.

Note: Using the COEX2 pin requires an external pull-down resistor in the 100 kΩ size range.

The COEX interface timing in relation to the LTE modem state is shown in the following figure.

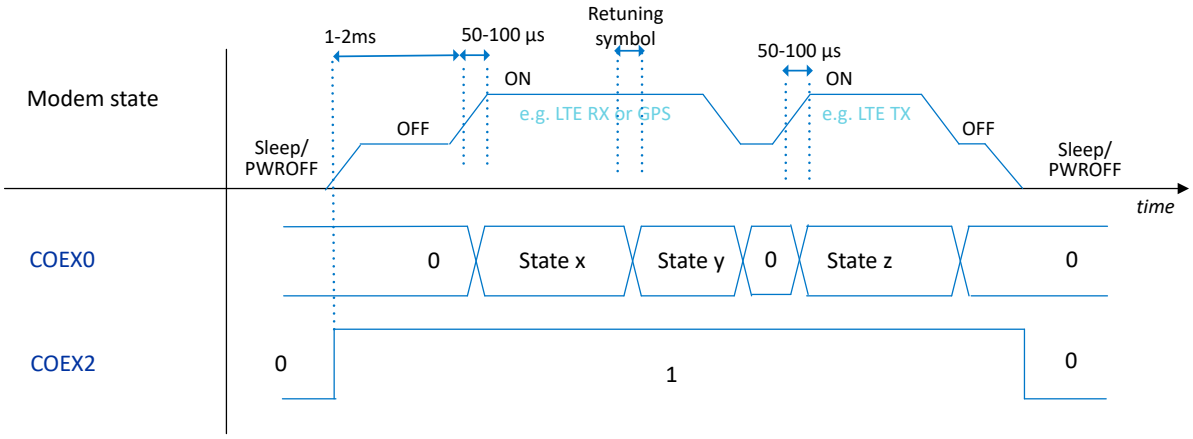


Figure 111: COEX interface timing

7.3 LTE RF control external interface

The LTE modem provides dedicated 1.8 V digital interfaces for controlling external RF applications, such as antenna tuner devices.

The LTE modem supports the following pins:

- MIPI RFFE interface pins – VIO, SCLK, SDATA
- MAGPIO interface pins – MAGPIO0, MAGPIO1, MAGPIO2

The LTE modem accurately drives the timing of these outputs according to the LTE protocol, to set the correct antenna tuner settings per used frequency, for example. The LTE modem API must be used to inform the LTE modem about the external RF application, so that LTE modem knows to drive it.

Note: For details regarding the modem API and supported RF external control features, see nRF91 AT Commands.

Note: The MIPI RFFE capacitive load at SCLK or SDATA pins must not exceed 15 pF.

The MIPI RFFE interface timing in relation to modem state is shown in the following figure.

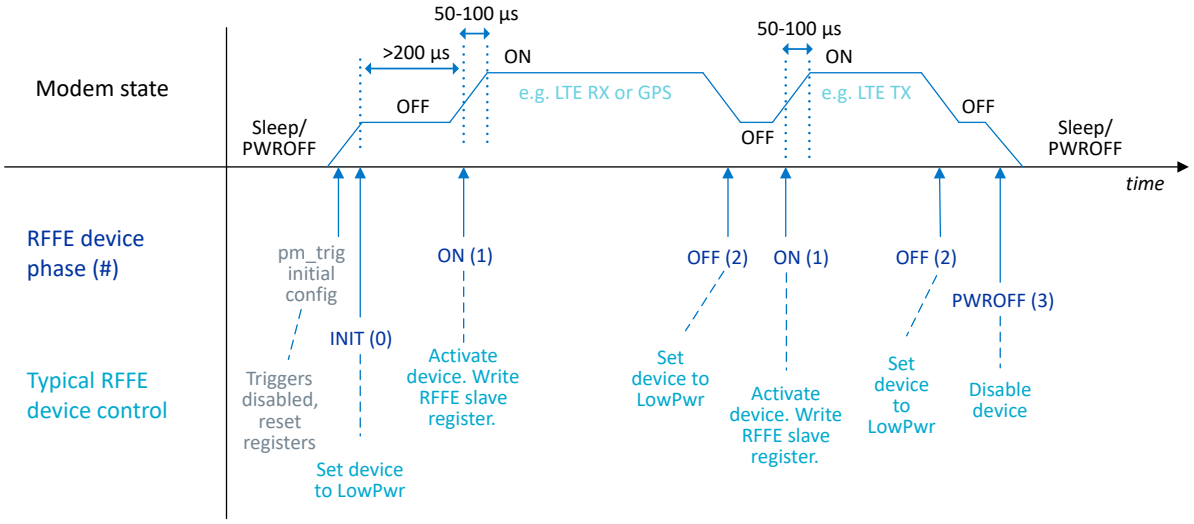


Figure 112: MIPI RFFE interface timing

The MAGPIO interface timing in relation to the LTE modem state is shown in the following figure.

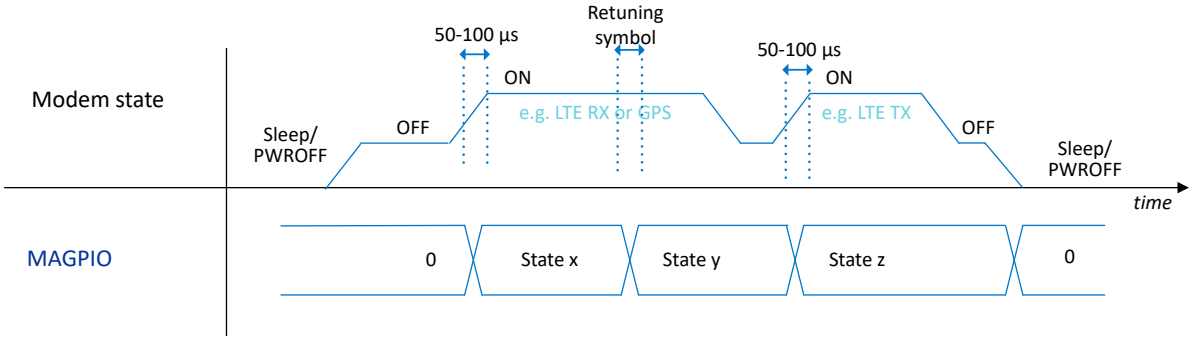


Figure 113: MAGPIO interface timing

7.4 RF front-end interface

The nRF9161 has a single-ended (SE) 50 Ω antenna interface to which an antenna is directly connected.

7.5 Registers

7.6 Electrical specification

7.6.1 Key RF parameters for Cat-M1

Note: For certification status, please refer to Regulatory information on page 461.

Symbol	Description	Min.	Typ.	Max.	Units
Supported LTE	Supported LTE standards		LTE Rel-14 Cat-M1 HD-FDD		
Bands supported	Bands supported		B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B28, B66, B85		
Transmission bandwidth	Maximum bandwidth		1.4		MHz

7.6.2 Key RF parameters for Cat-NB1 and Cat-NB2

Note: For certification status, please refer to Regulatory information on page 461.

Note: There is no foreseen NB-IoT network deployment for FCC bands closer than 200 kHz from band edge, hence our device will not transmit in FCC bands on channels that are closer than 200kHz to band edge.

Symbol	Description	Min.	Typ.	Max.	Units
Supported LTE	Supported LTE standards		LTE Rel-14 Cat-NB1 and Cat-NB2 HD-FDD		
Bands supported	Bands supported		B1, B2, B3, B4, B5, B8, B12, B13, B17, B19, B20, B25, B26, B28, B65, B66, B85		
Transmission bandwidth	Maximum bandwidth		200		kHz

7.6.3 Receiver parameters for Cat-M1

Symbol	Description	Min.	Typ.	Max.	Units
$Freq_{range\_ANT\_RX}$	RX operation frequency range at ANT pin	617		2200	MHz
Z_{in}	Input impedance, single-ended		50		Ω
Sensitivity, low band	LTE 1.4 MHz without coverage extension	-103	-108		dBm
Sensitivity, mid band	LTE 1.4 MHz without coverage extension	-103	-107		dBm

7.6.4 Receiver parameters for Cat-NB1 and Cat-NB2

Symbol	Description	Min.	Typ.	Max.	Units
$Freq_{range\_ANT\_RX}$	RX operation frequency range at ANT pin	617		2200	MHz
Z_{in}	Input impedance, single-ended		50		Ω
Sensitivity, low band	NB 200 kHz without coverage extension	-108	-114		dBm
Sensitivity, mid band	NB 200 kHz without coverage extension	-108	-113		dBm

7.6.5 Transmitter parameters for Cat-M1

Symbol	Description	Min.	Typ.	Max.	Units
$Freq_{range\_ANT\_TX}$	TX operation frequency range at ANT pin	663		1980	MHz
Z_{out}	Output impedance, single-ended		50		Ω
Maximum output power	Maximum output power		23		dBm
Minimum output power	Minimum output power		-40		dBm
Pout maximum accuracy	Pout maximum accuracy		±2		dB

7.6.6 Transmitter parameters for Cat-NB1 and Cat-NB2

Symbol	Description	Min.	Typ.	Max.	Units
$Freq_{range\_ANT\_TX}$	TX operation frequency range at ANT pin	663		2010	MHz
Z_{out}	Output impedance, single-ended		50		Ω
Maximum output power	Maximum output power		23		dBm
Minimum output power	Minimum output power		-40		dBm
Pout maximum accuracy	Pout maximum accuracy		±2		dB

8 DECT NR+

The nRF9161 SiP contains a Low-Power Wide-Area (LPWA) network processor with dedicated flash/RAM, which controls the radio and baseband hardware components. DECT NR+ (NR+) capabilities are provided by installing Nordic Semiconductor firmware, that implements the physical layer (PHY) level operation of the NR+ radio protocol stack according to ETSI specifications (TS 103 636-2 and TS 103 636-3).

NR+ is a non-cellular radio standard included as part of the 5G standards by the International Telecommunication Union (ITU). It is designed for massive Machine Type Communication (mMTC) and for Ultra-Reliable Low Latency Communication (URLLC).

NR+ operates on the global and license-exempt 1.9 GHz band, which significantly cuts deployment costs by eliminating the need for frequency planning or heavy certification. The NR+ device developer can design optimal radio behavior since there is no need for third-party cellular infrastructure. Additionally, the range and dense topology properties of NR+ make it highly scalable. A square kilometer can be covered by as little as 100 devices or scaled up to over 1 million devices while maintaining the same reliable, low-latency communication.

The physical radio layer in NR+ reuses known techniques from cellular radios, reaching the same level of reliability that is proven by billions of devices already in the field.

The following are key features of NR+:

- License-exempt global band
- Built-in coexistence of multiple networks in the same location
- Flexible, low-latency system and network architectures
- High reliability, using hybrid ARQ
- Possibility of hiding the network, using AES-128 encryption and integrity protection
- Data rate up to 3.4 Mbps, depending on modulation

See ETSI TS 103 636-1 for more information.

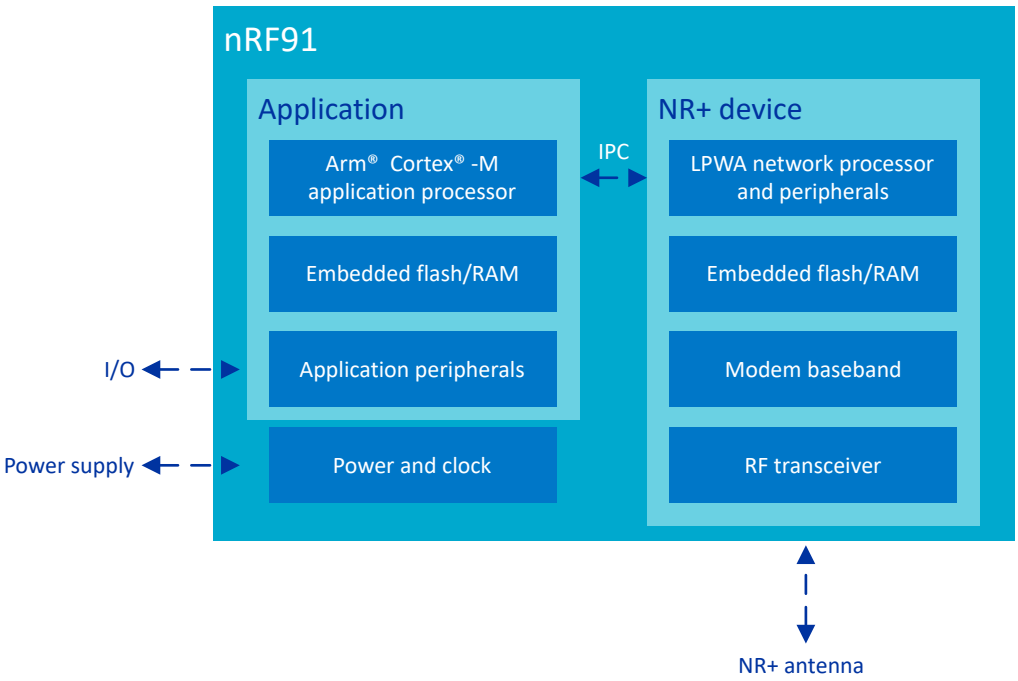


Figure 114: nRF9161 NR+ device functional overview

Application and LPWA network domains interact through the interprocessor communication (IPC) mechanism. The application processor is the system master and is responsible for starting and stopping the NR+ device. The LPWA network processor enables the clocks and power required for its own operation. The platform handles shared resources, such as clocks, and does not need user participation.

8.1 massive Machine Type Communication (mMTC)

mMTC is used for large networks with machine-type devices, connecting tens of billions of nodes that operate for many years using small batteries and transmit small amounts of data.

Typical use cases involve collecting measurements from many sensors, such as smart metering, which requires a low-maintenance and low-cost autonomous network structure.

A key feature of NR+ is its self-healing and self-organizing properties. Each node can function as a router to an access point with a connection to the internet. Nodes can change to a routing role based on the needs of the network. Multiple access points to the internet can be supported in a single network. These properties eliminates single points of failure and resolves high-traffic situations that can occur in dense IoT networks.

8.2 Ultra-Reliable Low-Latency Communication (URLLC)

URLLC enables mission-critical wireless use cases where failure is not an option.

Examples include management of self-driving factory vehicles, high-speed robots working alongside human operators in warehouses, and critical infrastructure in buildings, cities, and utilities.

NR+ is designed to reach one-millisecond latency between devices, opening the possibility for low-latency systems to consider wireless operation, even where ranges are over a kilometer. This makes NR+ an open, standardized alternative to existing proprietary technology.

8.3 DECT NR+ on the nRF9161

Nordic Semiconductor provides NR+ firmware that implements the physical layer (PHY) level operation of the NR+ radio protocol stack according to ETSI specifications (*TS 103 636-2 and TS 103 636-3*).

The NR+ standard and stack are still in development, contact the Nordic Semiconductor sales department for more information on the NR+ firmware.

The nRF9161 SiP supports NR+ bands 1, 2, and 9. The antenna interface and recommendations are the same as for the LTE modem. NR+ does not require a SIM or eSIM.

Note: While running DECT NR+ firmware, the nRF9161 SiP does not support LTE modem. See the LTE modem section for more information on alternative firmware.

8.4 Key RF Parameters

NR+ RF performance parameters are shown in the following table.

Description	Min	Typ	Max	Unit
Bands supported		1, 2, 9		
Transmission Bandwidth		1.728		MHz
Occupied Bandwidth		1.539		MHz
Antenna impedance, single-ended		50		Ω
RX: Sensitivity[23], modulation MCS1		-103		dBm
TX: Maximum output power		19		dBm
TX: Minimum output power		-40		dBm

Table 48: Common parameters

8.5 DECT NR+ coexistence interface

NR+ uses a dedicated two-pin coexistence interface to avoid RF interference to a companion radio device such as an external positioning device or a Bluetooth Low Energy device.

The user can configure COEX0 and COEX2 pin functions through the NR+ AT commands.

Note: Using the COEX2 pin requires an external pull-down resistor in the 100 kΩ range.

[23] The sensitivity level has not been measured using the same method as decribed in ETSI TS 103 636-2 chapter "7.2 Reference sensitivity". The reported sensitivity level is the signal level where 10% packet error rate (PER) occurs. This measurement method does not measure the throughput and does not include HARQ.

9 GPS receiver

The LPWA network processor supports GPS reception, if the onboard network protocol firmware supports it.

GPS receiver operation is time multiplexed with the LTE modem, and GPS and QZSS position can be received while the LTE modem is in RRC Idle mode, power saving mode (PSM), or completely deactivated.

The application processor is the system master and responsible for starting and stopping the GPS receiver. GPS can be run standalone or concurrently with QZSS. The GPS and QZSS reception can be configured through the GNSS interface API.

Note: For details regarding the GNSS API, refer to nRF Connect SDK API documentation.

Key features of the GPS receiver are as follows:

- GPS L1 C/A reception
- QZSS L1 C/A reception
- Optimized for low-power and low-cost IoT applications
- Modes of operation:
  - Single shot
  - Position fix per fixed interval, configurable to a value between 10 s to 65536 s
  - Continuous tracking
- Power saving mode:
  - Duty-cycled continuous tracking operation
- One pulse per second (1PPS) signal:
  - A pulse repeating once per second, accurately synchronized to coordinated universal time (UTC) full seconds
  - For more details on 1PPS programmability and power vs. accuracy trade-offs, see GNSS API documentation
  - Available on device COEX1 pin
    - For more details, see LTE modem on page 357, coexistence interface
- Antenna interface:
  - External low-noise amplifier (LNA) with SAW filter recommended on the GPS antenna input
  - Dedicated GPS antenna, or shared antenna with LTE
  - GPS antenna pin is DC grounded

Note: There must be minimum 27dB attenuation to out of band power to avoid blocking high power RF signals to GPS receiver input. This can be achieved by using a SAW filter, for example, at the external LNA output.

9.1 Electrical specification

The following is a summary of GPS receiver performance parameters.

Condition	Value
Environment	Open sky
Temperature	25°C
GPS sleep clock source	TCXO

Table 49: Common typical conditions

Note: Local and temporal conditions might lead to considerable variation in TTFF, positioning accuracy, 1PPS signal accuracy.

The figures in the following table assume the use of an external low-noise amplifier (LNA) with SAW filter.

Symbol	Description	Value	Unit
Sensitivity, cold	Acquisition sensitivity, cold start	-146.5	dBm
Sensitivity, hot	Acquisition sensitivity, hot start	-152.5	dBm
Sensitivity, tracking	Tracking sensitivity	-156.5	dBm
TTFF, cold	Time to first fix (TTFF), cold start	30.5	s
TTFF, hot	TTFF, hot start	1.3	s
TTFF, A-GPS	TTFF, A-GPS start	1.3	s
Accuracy, 2D, periodic	Positioning accuracy (CEP50), periodic tracking[24]	3.4	m
Accuracy, 2D, periodic, A-GPS	Positioning accuracy (CEP50), periodic tracking[24] with A-GPS[25]	3.1	m
Accuracy, 2D, continuous	Positioning accuracy (CEP50), continuous tracking	2.0	m
Accuracy, 2D, continuous, A-GPS	Positioning accuracy (CEP50), continuous tracking with A-GPS[25]	1.8	m
1PPS accuracy	1PPS signal accuracy, continuous tracking	±35	ns

Table 50: GPS electrical specification

[24] Fix interval 2 min.
[25] Including NeQuick ionospheric model parameters.

10 Debug and trace

The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

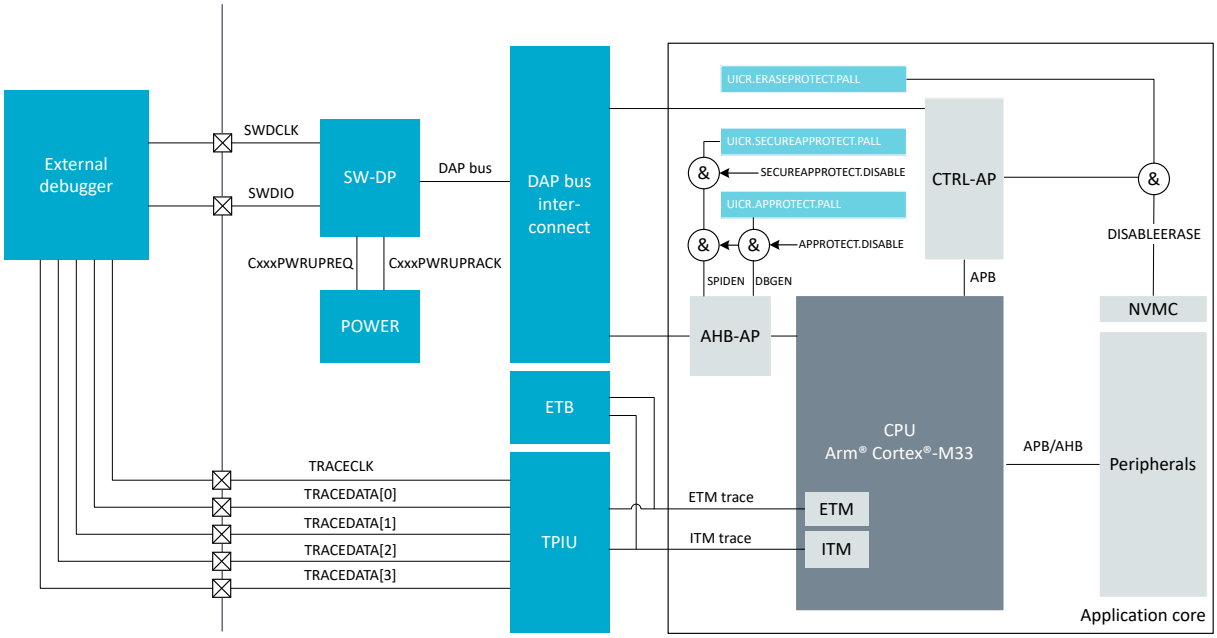


Figure 115: Debug and trace overview

The main features of the debug and trace system include:

- Two-pin serial wire debug (SWD) interface, protocol version 1
- Access port connection
  - Breakpoint unit (BPU) supports eight hardware breakpoint comparators
  - Data watchpoint and trace (DWT) unit supports four watchpoint comparators
  - Instrumentation trace macrocell (ITM)
  - Embedded trace macrocell (ETM)
  - Access protection through APPROTECT, ERASEPROTECT and SECUREAPPROTECT
- Embedded trace buffer (ETB)
- Trace port interface unit (TPIU)
  - 4-bit parallel trace of ITM and ETM trace data

Note: When a system contains multiple CPU domains, it is important to be aware that if one domain (subsystem A) has master rights on another domain (subsystem B), the master subsystem can access some data from the slave subsytem. In this example, even if subsystem B is locked by APPROTECT or ERASEPROTECT, subsystem A can access some data for subsystem B. Consequently, even if the security permissions are managed per subsystem, it is mandatory to have a global approach to the protection. Protecting a slave subsystem does not guarantee system security if the master subsystem is not protected.

10.1 DAP - Debug access port

An external debugger can access the device via the debug access port (DAP).

The DAP implements a standard Arm CoreSight serial wire debug port (SW-DP). The SW-DP implements the serial wire debug (SWD) protocol that is a two-pin serial interface, see SWDCLK and SWDIO illustrated in figure Debug and trace overview on page 368.

In addition to the default access port in the application CPU (AHB-AP), the DAP includes a custom control access port (CTRL-AP), described in more detail in CTRL-AP - Control access port on page 437.

Note:

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.

There are several access ports that connect to different parts of the system. An overview is given in the table below.

AP ID	Type	Description
0	AHB-AP	Application subsystem access port
3	APB-AP	CoreSight subsystem access port
4	CTRL-AP	Application subsystem control access port

Table 51: Access port overview

The standard Arm components are documented in *Arm CoreSight SoC-400 Technical Reference Manual, revision r3p2*. The control access port (CTRL-AP) is proprietary, and described in more detail in CTRL-AP - Control access port on page 437.

10.2 Access port protection

Access port protection blocks the debugger from read and write access to all CPU registers and memory-mapped addresses when enabled. If needed, a debugger can be restricted to debug non-secure code only and access non-secure memory regions and peripherals using register SECUREAPPROTECT on page 41. Register APPROTECT on page 40 blocks all debugger access.

The following table gives an overview of the access port protection methods.

Debugging capability	Description
Non-secure code	The application core AHB-AP DBGEN signal controls all non-secure access through the application core AHB-AP. This can be used to provide readback protection of the flash contents. See Debugger access control for non-secure debug access on page 370. For more information about the DBGEN signal, see the *Arm CoreSight SoC-400 Technical Reference Manual, Revision r3p2*.
Secure code	The application core AHB-AP SPIDEN signal controls all secure access through the application core AHB-AP. This means that only the non-secure code can be debugged and accessed when secure accesses are blocked. To enable access to the secure access port, non-secure code must be unprotected. See Debugger access control for secure debug access on page 370. For more information about the SPIDEN signal, see the *Arm CoreSight SoC-400 Technical Reference Manual, Revision r3p2*.

Table 52: Application core access port protection overview

If a RAM or flash region has its permission set to allow code execution, the content of this region is visible to the debugger even if the read permission is not set. This allows a debugger to display the content of the code being executed. For more information on configuring permissions, see SPU — System protection unit on page 257.

Access port protection controlled by hardware and software

By default, access port protection is enabled.

The following table describes how non-secure debugger access is controlled.

Debugging capability	UICR.APPROTECT.PALL	APPROTECT.DISABLE	APPROTECT.FORCEPROTECT	Secure debug access
Non-secure code	HwUnprotected	SwUnprotected	Reset value	-
No debugging possible	Protected	Reset value	Force	-

Table 53: Debugger access control for non-secure debug access

The following table describes how secure debugger access is controlled.

Debugging capability	UICR.SECUREAPPROTECT.PALL	SECUREAPPROTECT.DISABLE	SECUREAPPROTECT.FORCEPROTECT	Non-secure debug access
Secure code	HwUnprotected	SwUnprotected	Reset value	Permitted
No debugging possible	Protected	Reset value	Force	Permitted
No debugging possible	-	-	-	Not permitted

Table 54: Debugger access control for secure debug access

Access port protection is enabled when the hardware and software disabling conditions are not present. For additional security, it is recommended to write `Protected` to UICR.SECUREAPPROTECT and UICR.APPROTECT, and have firmware write `Force` to SECUREAPPROTECT.FORCEPROTECT and APPROTECT.FORCEPROTECT.

Note: Registers SECUREAPPROTECT.FORCEPROTECT and APPROTECT.FORCEPROTECT are reset in System ON IDLE or after any reset.

Access port protection is disabled by issuing an ERASEALL command through CTRL-AP. Read ERASEALLSTATUS until the ERASEALL sequence is ready. When ERASEALL is ready, trigger and then release soft reset from the RESET register. Read APPROTECT.STATUS to ensure that access port protection is disabled. If access port is not disabled, do a reset and repeat the ERASEALL command. This command erases the flash, UICR, and RAM, including UICR.SECUREAPPROTECT and UICR.APPROTECT. CTRL-AP is described in more detail in CTRL-AP - Control access port on page 437. Access port protection remains disabled until one of the following occurs:

- Pin reset
- Power or brownout reset

- Watchdog reset
- Wake from System OFF if not in Emulated System OFF

To keep access port protection disabled, the following actions must be performed:

- Program UICR.SECUREAPPROTECT and UICR.APPROTECT to `HwUnprotected`. This disables the hardware part of the access port protection scheme after the first reset of any type. The hardware part of the access port protection stays disabled as long as UICR.SECUREAPPROTECT and UICR.APPROTECT are not overwritten.
- Firmware must write SECUREAPPROTECT.DISABLE and APPROTECT.DISABLE to `SwUnprotected`. This disables the software part of the access port protection scheme.

Note: Register SECUREAPPROTECT.DISABLE and APPROTECT.DISABLE are reset in System ON IDLE or after pin reset, power or brownout reset, watchdog reset, or wake from System OFF as mentioned above.

The following figure shows how a device with access port protection enabled is erased, programmed, and configured to allow debugging. Operations sent from the debugger and registers written by firmware affects the access port state.

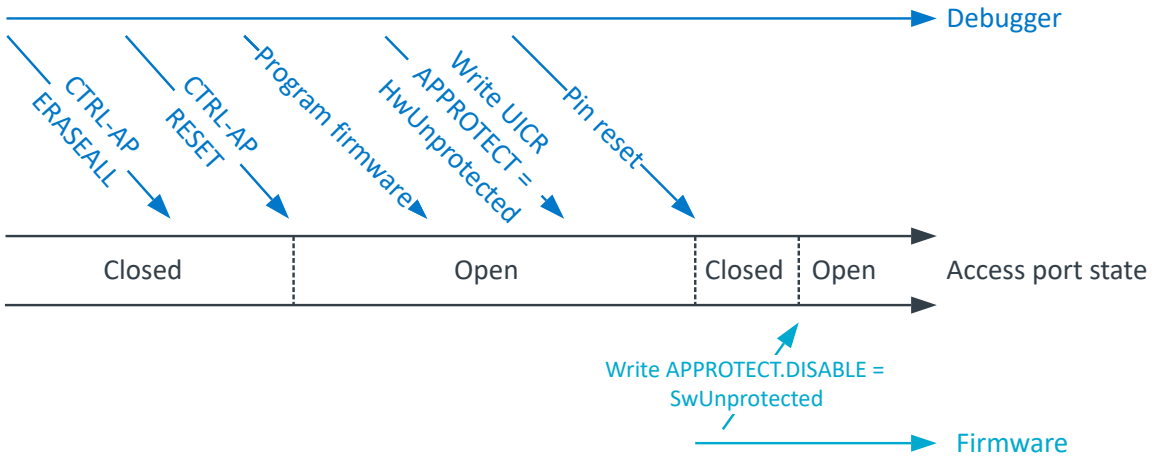


Figure 116: Access port unlocking

10.2.2 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
APPROTECT : S	0x50039000	HF	NS	NA	Yes	APPROTECT control
APPROTECT : NS	0x40039000					

Register overview

Register	Offset	TZ	Description
SECUREAPPROTECT.DISABLE	0xE00	S	Software disable SECUREAPPROTECT mechanism
SECUREAPPROTECT.FORCEPROTECT	0xE00	S	Software force SECUREAPPROTECT mechanism
APPROTECT.DISABLE	0xE10	NS	Software disable APPROTECT mechanism
APPROTECT.FORCEPROTECT	0xE10	NS	Software force APPROTECT mechanism

10.2.2.1 SECUREAPPROTECT.DISABLE

Address offset: 0xE00

Software disable SECUREAPPROTECT mechanism

Bit number							31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID							A A A A A A A A
Reset 0x00000001							**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1**
ID	R/W	TZ	Field	Value ID	Value	Description	
A	RW		DISABLE			Software disable SECUREAPPROTECT mechanism	
				SwUnprotected	0x5A	Software disable SECUREAPPROTECT mechanism	

10.2.2.2 SECUREAPPROTECT.FORCEPROTECT

Address offset: 0xE00

Software force SECUREAPPROTECT mechanism

Bit number							31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID							A
Reset 0x00000001							**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1**
ID	R/W	TZ	Field	Value ID	Value	Description	
A	RW W1S		FORCEPROTECT			Write 0x1 to force enable SECUREAPPROTECT mechanism	
				Force	0x1	Software force enable SECUREAPPROTECT mechanism	

10.2.2.3 APPROTECT.DISABLE

Address offset: 0xE10

Software disable APPROTECT mechanism

Bit number							31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID							A A A A A A A A
Reset 0x00000001							**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1**
ID	R/W	TZ	Field	Value ID	Value	Description	
A	RW		DISABLE			Software disable APPROTECT mechanism	
				SwUnprotected	0x5A	Software disable APPROTECT mechanism	

10.2.2.4 APPROTECT.FORCEPROTECT

Address offset: 0xE10

Software force APPROTECT mechanism

Bit number							31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID							A
Reset 0x00000001							**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1**
ID	R/W	TZ	Field	Value ID	Value	Description	
A	RW W1S		FORCEPROTECT			Write 0x1 to force enable APPROTECT mechanism	
				Force	0x1	Software force enable APPROTECT mechanism	

10.3 Debug interface mode

Before the external debugger can access the CPU's access port (AHB-AP) or the control access port (CTRL-AP), the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

As long as the debugger is requesting power via CxxxPWRUPREQ, the device will be in debug interface mode. Otherwise, the device is in normal mode. When a debug session is over, the external debugger must make sure to put the device back into normal mode and then a pin reset should be performed. The reason is that the overall power consumption is higher in debug interface mode compared to normal mode.

Some peripherals behave differently in debug interface mode compared to normal mode. The differences are described in more detail in the chapters of the affected peripherals.

For details on how to use the debug capabilities, please read the debug documentation of your IDE.

If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in RESETREAS on page 68 will be set.

10.4 Real-time debug

The device supports real-time debugging, which allows interrupts to execute to completion in real time when breakpoints are set in thread mode or lower priority interrupts.

Real-time debugging thus enables the developer to set a breakpoint and single-step through their code without a failure of the real-time event-driven threads running at higher priority. For example, this enables the device to continue to service the high-priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.

10.5 Registers

Register overview

Register	Offset	Description
TARGETID	0x042	The TARGETID register provides information about the target when the host is connected to a single device. The TARGETID register is accessed by a read of DP register 0x4 when the DPBANKSEL bit in the SELECT register is set to 0x2.

10.5.1 TARGETID

Address offset: 0x042

The TARGETID register provides information about the target when the host is connected to a single device.

The TARGETID register is accessed by a read of DP register 0x4 when the DPBANKSEL bit in the SELECT register is set to 0x2.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				D	D	D	D	C	C	C	C	C	C	C	C	C	C	C	C					B	B	B	B	B	B	B	B	B	B	B	A
Reset 0x10090289				**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	UNUSED																																	
				Reserved, read-as-one																																	
B	R	TDESIGNER																																	
				An 11-bit code: JEDEC JEP106 continuation code and identity code. The ID identifies the designer of the part.																																	
			NordicSemi	0x144																																	
				Nordic Semiconductor ASA																																	
C	R	TPARTNO																																	
				Part number																																	
D	R	TREVISION																																	
				Target revision																																	

10.6 Electrical specification

10.6.1 Trace port

Symbol	Description	Min.	Typ.	Max.	Units
T_{cyc}	Clock period, as defined by ARM (See ARM Infocenter, Embedded Trace Macrocell Architecture Specification, Trace Port Physical Interface, Timing specifications)	62.5			ns

10.7 Trace

The nRF9161 supports ETM and ITM trace.

Available trace sinks:

- 2 kB internal embedded trace buffer (ETB)
- External trace port interface through TPIU

Trace data from the ETM and the ITM can be sent to an internal embedded trace buffer (ETB) or an external debugger via a 4-bit wide parallel trace port (TPIU), see TRACEDATA[0] through TRACEDATA[3], and TRACECLK in Debug and trace overview on page 368.

The following diagram shows the trace components architecture of the device's embedded Arm CoreSight subsystem.

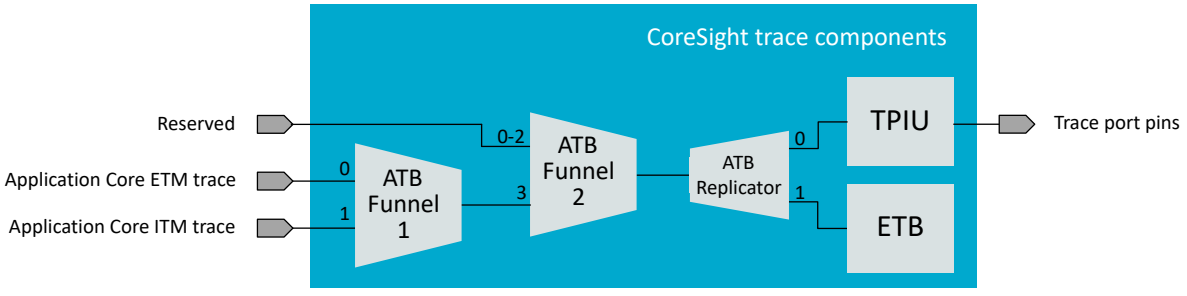


Figure 117: Trace components architecture

The standard Arm components are documented in *Arm CoreSight SoC-400 Technical Reference Manual, revision r3p2*. For details on how to use the trace capabilities, please read the debug documentation of your IDE.

TPIU's trace pins are multiplexed with GPIOs, see Pin assignments on page 450 for more information.

Note: To configure the trace data delivery to the device trace port, use the MDK system start-up file included as of MDK version 8.26.0.

Trace speed is configured in the TRACEPORTSPEED (Retained) on page 448 register. The speed of the trace pins depends on the DRIVE setting of the GPIOs that the trace pins are multiplexed with. See GPIO — General purpose input/output on page 97 for information about how to set drive settings. Only S0S1 and H0H1 drives are suitable for debugging. S0S1 is the default DRIVE at reset. If parallel or serial trace port signals are not fast enough in the debugging conditions, all GPIOs in use for tracing should be set to high drive (H0H1). The user shall make sure that DRIVE setting for these GPIOs is not overwritten by software during the debugging session.

10.7.1 ATB Funnel

The ARM® ATB Funnel funnels trace bus mesages from several sources into one output bus.

This document only provides a register-level description of this ARM component. See the ARM® CoreSight™ SoC-400 Technical Reference Manual for more details

10.7.1.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
ATBFUNNEL1	0xE005A000	HF	NS	NA	No	ATBFUNNEL unit 1
ATBFUNNEL2	0xE005B000	HF	NS	NA	No	ATBFUNNEL unit 2

Register overview

Register	Offset	TZ	Description
CTRLREG	0x000		The IDFILTER0 register enables the programming of ID filtering for master port 0.
PRIORITYCTRLREG	0x004		The Priority_Ctrl_Reg register defines the order in which inputs are selected. Each 3-bit field is a priority for each particular slave interface.
ITATBDATA0	0xEEC		The ITATBDATA0 register performs different functions depending on whether the access is a read or a write.
ITATBCTR2	0xEF0		The ITATBCTR2 register performs different functions depending on whether the access is a read or a write.
ITATBCTR1	0xEF4		The ITATBCTR1 register performs different functions depending on whether the access is a read or a write.
ITATBCTR0	0xEF8		The ITATBCTR0 register performs different functions depending on whether the access is a read or a write.
ITCTRL	0xF00		The ITCTRL register enables the component to switch from a functional mode, which is the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purposes of integration testing and topology detection.
CLAIMSET	0xFA0		Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMSET register sets bits in the claim tag, and determines the number of claim bits implemented.
CLAIMCLR	0xFA4		Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMCLR register sets the bits in the claim tag to 0 and determines the current value of the claim tag.
LAR	0xFB0		This is used to enable write access to device registers.

Register	Offset	TZ	Description
LSR	0xFB4		This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. Accesses to the extended stimulus port registers are not affected by the lock mechanism. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register.
AUTHSTATUS	0xFB8		Indicates the current level of tracing permitted by the system
DEVID	0xFC8		Indicates the capabilities of the component.
DEVTYPE	0xFCC		The DEVTYPE register provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.
PIDR4	0xFD0		Coresight peripheral identification registers.
PIDR[0]	0xFE0		Coresight peripheral identification registers.
PIDR[1]	0xFE4		Coresight peripheral identification registers.
PIDR[2]	0xFE8		Coresight peripheral identification registers.
PIDR[3]	0xFEC		Coresight peripheral identification registers.
CIDR[0]	0xFF0		Coresight component identification registers.
CIDR[1]	0xFF4		Coresight component identification registers.
CIDR[2]	0xFF8		Coresight component identification registers.
CIDR[3]	0xFFC		Coresight component identification registers.

10.7.1.1.1 CTRLREG

Address offset: 0x000

The IDFILTER0 register enables the programming of ID filtering for master port 0.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																								I	I	I	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID			Value																	Description											
A-H	RW	ENS[i] (i=0..7)																						Enable slave port i.											
				Disabled			0																	Slave port disabled. This excludes the port from the priority selection scheme.											
				Enabled			1																	Slave port enabled.											
I	RW	HT					[0:14]																	Hold Time. The formatting scheme can become inefficient when fast switching occurs, and you can use this setting to minimize switching. When a source has nothing to transmit, then another source is selected irrespective of the minimum number of transactions. The ATB funnel holds for the minimum hold time and one additional transaction. The actual hold time is the register value plus 1. The maximum value that can be entered is 0b1110 and this equates to 15 transactions. 0b1111 is reserved.											

10.7.1.1.2 PRIORITYCTRLREG

Address offset: 0x004

The Priority_Ctrl_Reg register defines the order in which inputs are selected. Each 3-bit field is a priority for each particular slave interface.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID												H	H	H	G	G	G	F	F	F	E	E	E	D	D	D	C	C	C	B	B	B	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID			Value																	Description											
A-H	RW	PRIPORT[i] (i=0..7)					[0:7]																	Priority value of port number i.											

10.7.1.1.3 ITATBDATA0

Address offset: 0xEEC

The ITATBDATA0 register performs different functions depending on whether the access is a read or a write.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																			Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID				Value																											
A-Q	RW	ATDATA[i] (i=0..16)																																	
				Low				0																											
				High				1																											

10.7.1.1.4 ITATBCTR2

Address offset: 0xEF0

The ITATBCTR2 register performs different functions depending on whether the access is a read or a write.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID				Value																											
A	RW	ATREADY																																	
				Low				0																											
				High				1																											
B	RW	AFVALID																																	
				Low				0																											
				High				1																											

10.7.1.1.5 ITATBCTR1

Address offset: 0xEF4

The ITATBCTR1 register performs different functions depending on whether the access is a read or a write.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID				Value																											
A	RW	ATVALIDM0																																	
				Low				0																											
				High				1																											

10.7.1.1.6 ITATBCTR0

Address offset: 0xEF8

The ITATBCTR0 register performs different functions depending on whether the access is a read or a write.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ATVALID			A read returns the value of the atvalids[n] signal, where the value of the CTRLREG at 0x000 defines n. A write outputs the value to atvalidm.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.
B	RW	AFREADY			A read returns the value of the afreadys[n] signal, where the value of the Ctrl_Reg at 0x000 defines n. A write outputs the value to afreadym.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.
C	RW	ATBYTES			A read returns the value of the atbytess[n] signal, where the value of the Ctrl_Reg at 0x000 defines n. A write outputs the value to atbytesm.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.

10.7.1.1.7 ITCTRL

Address offset: 0xF00

The ITCTRL register enables the component to switch from a functional mode, which is the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purposes of integration testing and topology detection.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	IME			Integration Mode Enable.
			Disabled	0	Integration mode disabled.
			Enabled	1	Integration mode enabled.

10.7.1.1.8 CLAIMSET

Address offset: 0xFA0

Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMSET register sets bits in the claim tag, and determines the number of claim bits implemented.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-D	RW	BIT[i] (i=0..3)			Set claim bit i and check if bit is implemented or not.
			NotImplemented	0	Claim bit i is not implemented.
			Implemented	1	Claim bit i is implemented.
			Set	1	Set claim bit i.

10.7.1.1.9 CLAIMCLR

Address offset: 0xFA4

Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMCLR register sets the bits in the claim tag to 0 and determines the current value of the claim tag.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-D	RW	BIT[i] (i=0..3)			Read or clear claim bit i.
			Cleared	0	Claim bit i is not set.
			Set	1	Claim bit i is set.
			Clear	1	Clear claim bit i.

10.7.1.1.10 LAR

Address offset: 0xFB0

This is used to enable write access to device registers.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ACCESS			A write of 0xC5ACCE55 enables further write access to this device. Any other write removes write access.
			UnLock	0xC5ACCE55	Unlock register interface.

10.7.1.1.11 LSR

Address offset: 0xFB4

This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. Accesses to the extended stimulus port registers are not affected by the lock mechanism. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	PRESENT			Indicates that a lock control mechanism exists for this device.
			NotImplemented	0	No lock control mechanism exists, writes to the Lock Access Register are ignored.
			Implemented	1	Lock control mechanism is present.
B	RW	LOCKED			Returns the current status of the Lock.
			UnLocked	0	Write access is allowed to this device.
			Locked	1	Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted.
C	RW	TYPE			Indicates if the Lock Access Register is implemented as 8-bit or 32-bit.
			Bits32	0	This component implements a 32-bit Lock Access Register.
			Bits8	1	This component implements an 8-bit Lock Access Register.

10.7.1.1.12 AUTHSTATUS

Address offset: 0xFB8

Indicates the current level of tracing permitted by the system

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												D	D	C	C	B	B	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	NSID																																	
			NotImplemented	0																															
			Implemented	1																															
B	RW	NSNID																																	
			NotImplemented	0																															
			Implemented	1																															
C	RW	SID																																	
			NotImplemented	0																															
			Implemented	1																															
D	RW	SNID																																	
			NotImplemented	0																															
			Implemented	1																															

10.7.1.1.13 DEVID

Address offset: 0xFC8

Indicates the capabilities of the component.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	PORTCOUNT		[2:8]																															
				Indicates the number of input ports connected. 0x0 and 0x1 are illegal values.																																

10.7.1.1.14 DEVTYPE

Address offset: 0xFCC

The DEVTYPE register provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												B	B	B	B	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	MAJOR																																	
			InputOutputDevice	2																															
B	R	SUB																																	
			Replicator	1																															

10.7.1.1.15 PIDR4

Address offset: 0xFD0

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.1.1.16 PIDR[0]

Address offset: 0xFE0

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.1.1.17 PIDR[1]

Address offset: 0xFE4

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.1.1.18 PIDR[2]

Address offset: 0xFE8

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.1.1.19 PIDR[3]

Address offset: 0xFEC

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.1.1.20 CIDR[0]

Address offset: 0xFF0

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.1.1.21 CIDR[1]

Address offset: 0xFF4

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.1.1.22 CIDR[2]

Address offset: 0xFF8

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.1.1.23 CIDR[3]

Address offset: 0xFFC

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.2 ATB Replicator

The ARM® ATB Replicator replicates incoming trace bus mesages across its outputs.

This document only provides a register-level description of this ARM component. See the ARM® CoreSight™ SoC-400 Technical Reference Manual for more details

10.7.2.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
ATBREPLICATOR	0xE0058000	HF	NS	NA	No	ATBREPLICATOR

Register overview

Register	Offset	TZ	Description
IDFILTER0	0x000		The IDFILTER0 register enables the programming of ID filtering for master port 0.
IDFILTER1	0x004		The IDFILTER1 register enables the programming of ID filtering for master port 1.
ITATBCTR1	0xEF8		The ITATBCTR1 register returns the value of the atreadym0, atreadym1, and atvalids inputs in integration mode.
ITATBCTR0	0xEFC		The ITATBCTR0 register controls the value of the atvalidm0, atvalidm1, and atreadys outputs in integration mode.
ITCTRL	0xF00		The ITCTRL register enables the component to switch from a functional mode, which is the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purposes of integration testing and topology detection.
CLAIMSET	0xFA0		Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMSET register sets bits in the claim tag, and determines the number of claim bits implemented.
CLAIMCLR	0xFA4		Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMCLR register sets the bits in the claim tag to 0 and determines the current value of the claim tag.
LAR	0xFB0		This is used to enable write access to device registers.
LSR	0xFB4		This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. Accesses to the extended stimulus port registers are not affected by the lock mechanism. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register.
AUTHSTATUS	0xFB8		Indicates the current level of tracing permitted by the system
DEVID	0xFC8		Indicates the capabilities of the component.
DEVTYPE	0xFCC		The DEVTYPE register provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.
PIDR4	0xFD0		Coresight peripheral identification registers.
PIDR[0]	0xFE0		Coresight peripheral identification registers.
PIDR[1]	0xFE4		Coresight peripheral identification registers.
PIDR[2]	0xFE8		Coresight peripheral identification registers.
PIDR[3]	0xFEC		Coresight peripheral identification registers.
CIDR[0]	0xFF0		Coresight component identification registers.
CIDR[1]	0xFF4		Coresight component identification registers.
CIDR[2]	0xFF8		Coresight component identification registers.
CIDR[3]	0xFFC		Coresight component identification registers.

10.7.2.1.1 IDFILTER0

Address offset: 0x000

The IDFILTER0 register enables the programming of ID filtering for master port 0.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																									H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-H	RW	ID0_[i]0_[i]F (i=0..7)			Enable or disable ID filtering for IDs 0xi0_0xiF.
			NotFiltered	0	Transactions with these IDs are passed on to ATB master port 0.
			Selected	1	Transactions with these IDs are discarded by the replicator.

10.7.2.1.2 IDFILTER1

Address offset: 0x004

The IDFILTER1 register enables the programming of ID filtering for master port 1.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-H	RW	ID1_[i]0_[i]F (i=0..7)																																	
			NotFiltered	0																															
			Selected	1																															

10.7.2.1.3 ITATBCTR1

Address offset: 0xEF8

The ITATBCTR1 register returns the value of the atreadym0, atreadym1, and atvalids inputs in integration mode.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																C		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	ATREADYM0																																	
			Low	0																															
			High	1																															
B	RW	ATREADYM1																																	
			Low	0																															
			High	1																															
C	RW	ATVALIDS																																	
			Low	0																															
			High	1																															

10.7.2.1.4 ITATBCTR0

Address offset: 0xEFC

The ITATBCTR0 register controls the value of the atvalidm0, atvalidm1, and atreadys outputs in integration mode.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																C	B		A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	ATVALIDM0																																	
			Low	0																															
			High	1																															
B	RW	ATVALIDM1																																	
			Low	0																															
			High	1																															
C	RW	ATREADYS																																	
			Low	0																															
			High	1																															

10.7.2.1.5 ITCTRL

Address offset: 0xF00

The ITCTRL register enables the component to switch from a functional mode, which is the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purposes of integration testing and topology detection.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	IME			Integration Mode Enable.
			Disabled	0	Integration mode disabled.
			Enabled	1	Integration mode enabled.

10.7.2.1.6 CLAIMSET

Address offset: 0xFA0

Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMSET register sets bits in the claim tag, and determines the number of claim bits implemented.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-D	RW	BIT[i] (i=0..3)			Set claim bit i and check if bit is implemented or not.
			NotImplemented	0	Claim bit i is not implemented.
			Implemented	1	Claim bit i is implemented.
			Set	1	Set claim bit i.

10.7.2.1.7 CLAIMCLR

Address offset: 0xFA4

Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMCLR register sets the bits in the claim tag to 0 and determines the current value of the claim tag.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-D	RW	BIT[i] (i=0..3)			Read or clear claim bit i.
			Cleared	0	Claim bit i is not set.
			Set	1	Claim bit i is set.
			Clear	1	Clear claim bit i.

10.7.2.1.8 LAR

Address offset: 0xFB0

This is used to enable write access to device registers.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ACCESS			A write of 0xC5ACCE55 enables further write access to this device. Any other write removes write access.
			UnLock	0xC5ACCE55	Unlock register interface.

10.7.2.1.9 LSR

Address offset: 0xFB4

This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. Accesses to the extended stimulus port registers are not affected by the lock mechanism. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	PRESENT			Indicates that a lock control mechanism exists for this device.
			NotImplemented	0	No lock control mechanism exists, writes to the Lock Access Register are ignored.
			Implemented	1	Lock control mechanism is present.
B	RW	LOCKED			Returns the current status of the Lock.
			UnLocked	0	Write access is allowed to this device.
			Locked	1	Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted.
C	RW	TYPE			Indicates if the Lock Access Register is implemented as 8-bit or 32-bit.
			Bits32	0	This component implements a 32-bit Lock Access Register.
			Bits8	1	This component implements an 8-bit Lock Access Register.

10.7.2.1.10 AUTHSTATUS

Address offset: 0xFB8

Indicates the current level of tracing permitted by the system

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D C C B B A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	NSID			Non-secure Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
B	RW	NSNID			Non-secure Non-Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
C	RW	SID			Secure Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
D	RW	SNID			Secure Non-Invasive Debug
			NotImplemented	0	The feature is not implemented.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D C C B B A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			Implemented	1	The feature is implemented.

10.7.2.1.11 DEVID

Address offset: 0xFC8

Indicates the capabilities of the component.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	PORTNUM		[0:15]	Indicates the number of master ports implemented.

10.7.2.1.12 DEVTYPE

Address offset: 0xFCC

The DEVTYPE register provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	MAJOR			The main type of the component
			InputOutputDevice	2	Indicates that this component has ATB inputs and outputs.
B	R	SUB			The sub-type of the component
			Replicator	2	Indicates that this component replicates trace from a single source to multiple targets.

10.7.2.1.13 PIDR4

Address offset: 0xFD0

Coresight peripheral identification registers.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description

10.7.2.1.14 PIDR[0]

Address offset: 0xFE0

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.2.1.15 PIDR[1]

Address offset: 0xFE4

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.2.1.16 PIDR[2]

Address offset: 0xFE8

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.2.1.17 PIDR[3]

Address offset: 0xFEC

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.2.1.18 CIDR[0]

Address offset: 0xFF0

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.2.1.19 CIDR[1]

Address offset: 0xFF4

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.2.1.20 CIDR[2]

Address offset: 0xFF8

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.2.1.21 CIDR[3]

Address offset: 0xFFC

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.3 ETB — Embedded trace buffer

The ARM embedded trace buffer captures trace and stores it in an on-chip RAM for later inspection.

This document only provides a register-level description of this ARM component. See the Arm® CoreSight SoC-400 Technical Reference Manual for more details.

10.7.3.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
ETB	0xE0051000	HF	NS	NA	No	ETB

Register overview

Register	Offset	TZ	Description
RDP	0x4		ETB RAM Depth Register
STS	0xC		ETB Status Register
RRD	0x10		ETB RAM Read Data Register
RRP	0x14		ETB RAM Read Pointer Register
RWP	0x18		ETB RAM Write Pointer Register
TRG	0x1C		ETB Trigger Counter Register
CTL	0x20		ETB Control Register
RWD	0x24		ETB RAM Write Data Register
FFSR	0x300		ETB Formatter and Flush Status Register

Register	Offset	TZ	Description
FFCR	0x304		ETB Formatter and Flush Control Register
ITMISCOP0	0xEE0		Integration Test Miscellaneous Output Register 0
ITTRFLINACK	0xEE4		Integration Test Trigger In and Flush In Acknowledge Register
ITTRFLIN	0xEE8		Integration Test Trigger In and Flush In Register
ITATBDATA0	0xEEC		Integration Test ATB Data Register 0
ITATBCTR2	0xEF0		Integration Test ATB Control Register 2
ITATBCTR1	0xEF4		Integration Test ATB Control Register 1
ITATBCTR0	0xEF8		Integration Test ATB Control Register 0
ITCTRL	0xF00		Integration Mode Control Register
CLAIMSET	0xFA0		Claim Tag Set Register
CLAIMCLR	0xFA4		Claim Tag Clear Register
LAR	0xFB0		Lock Access Register
LSR	0xFB4		Lock Status Register
AUTHSTATUS	0xFB8		Authentication Status Register
DEVID	0xFC8		Device Configuration Register
DEVTYPE	0xFCC		Device Type Identifier Register
PERIPHID4	0xFD0		Peripheral ID4 Register
PERIPHID0	0xFE0		Peripheral ID0 Register
PERIPHID1	0xFE4		Peripheral ID1 Register
PERIPHID2	0xFE8		Peripheral ID2 Register
PERIPHID3	0xFEC		Peripheral ID3 Register
COMPID0	0xFF0		Component ID0 Register
COMPID1	0xFF4		Component ID1 Register
COMPID2	0xFF8		Component ID2 Register
COMPID3	0xFFC		Component ID3 Register

10.7.3.1.1 RDP

Address offset: 0x4

ETB RAM Depth Register

Defines the depth, in words, of the trace RAM. This value is configurable in the RTL, but fixed at synthesis. Supported depth in powers of 2 only.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	ETB_RAM_DEPTH			Defines the depth, in words, of the trace RAM.

10.7.3.1.2 STS

Address offset: 0xC

ETB Status Register

This register indicates the status of the ETB.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000008				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	FULL			RAM Full. The flag indicates when the RAM write pointer has wrapped around.
B	R	TRIGGERED			The Triggered bit is set when a trigger has been observed. This does not indicate that a trigger has been embedded in the trace data by the formatter, but is determined by the programming of the Formatter and Flush Control Register.
C	R	ACQCOMP			The acquisition complete flag indicates that capture has been completed when the formatter stops because of any of the methods defined in the Formatter and Flush Control Register, or TraceCaptEn = 0. This also results in FtStopped in the Formatter and Flush Status Register going HIGH.
D	R	FTEMPTY			Formatter pipeline empty. All data stored to RAM.

10.7.3.1.3 RRD

Address offset: 0x10

ETB RAM Read Data Register

When trace capture is disabled, the contents of the ETB Trace RAM at the location addressed by the RAM Read Pointer Registers are placed in this register. Reading this register increments the RAM Read Pointer Register and triggers a RAM access cycle. If trace capture is enabled (FtStopped=0, TraceCaptEn=1), and ETB RAM reading is attempted, a read from this register outputs 0xFFFFFFFF and the RAM Read Pointer Register does not auto-increment. A constant stream of 1s being output corresponds to a synchronization output in the formatter protocol, which is not applicable to the ETB, and so can be used to signify a read error, when formatting is enabled.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	RAM_READ_DATA			Data read from the ETB Trace RAM.

10.7.3.1.4 RRP

Address offset: 0x14

ETB RAM Read Pointer Register

The RAM Read Pointer Register sets the read pointer used to read entries from the Trace RAM over the APB interface. When this register is written to, a RAM access is initiated. The RAM Read Data Register is then updated. The register can also be read to determine the current memory location being referenced. This register must not be written to when trace capture is enabled (FtStopped=0, TraceCaptEn=1). If access is attempted, the register is not updated.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	RAM_READ_POINTER			Sets the read pointer used to read entries from the Trace RAM over the APB interface.

10.7.3.1.5 RWP

Address offset: 0x18

ETB RAM Write Pointer Register

The RAM Write Pointer Register sets the write pointer used to write entries from the CoreSight bus into Trace RAM. During trace capture the pointer increments when the DataValid flag is asserted by the Formatter. When this register increments from its maximum value back to zero, the Full flag is set. This register can also be written to over APB to set the pointer for write accesses carried out through the APB interface. This register must not be written to when trace capture is enabled (FtStopped=0, TraceCaptEn=1). If access is attempted, the register is not updated. The register can also be read to determine the current memory location being referenced. It is recommended that addresses are 128-bit aligned when the formatter is used in normal or continuous modes.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	RAM_WRITE_POINTER			Sets the write pointer used to write entries from the CoreSight bus into the Trace RAM.

10.7.3.1.6 TRG

Address offset: 0x1C

ETB Trigger Counter Register

The Trigger Counter Register disables write access to the Trace RAM by stopping the Formatter after a defined number of words have been stored following the trigger event. The number of 32-bit words written into the Trace RAM following the trigger event is equal to the value stored in this register+1.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	TRIGGER_COUNTER			The counter is used as follows:Trace after - The counter is set to a large value, slightly less than the number of entries in the RAM. Trace before - The counter is set to a small value. Trace about - The counter is set to half the depth of the Trace RAM. This register must not be written to when trace capture is enabled (FtStopped=0, TraceCaptEn=1). If a write is attempted, the register is not updated. A read access is permitted with trace capture enabled.

10.7.3.1.7 CTL

Address offset: 0x20

ETB Control Register

This register controls trace capture by the ETB.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	TRACECAPTEN			ETB Trace Capture Enable. This is the master enable bit forcing FtStopped HIGH when TraceCaptEn is LOW. When capture is disabled, any remaining data in the ATB formatter is stored to RAM. When all data is stored the formatter outputs FtStopped. Capture is fully disabled, or complete, when FtStopped goes HIGH. See ETB Formatter and Flush Status Register, FFSR, 0x300.

10.7.3.1.8 RWD

Address offset: 0x24

ETB RAM Write Data Register

Data written to the ETB Trace RAM.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	RAM_WRITE_DATA			Data written to the ETB Trace RAM. When trace capture is disabled, the contents of this register are placed into the ETB Trace RAM when this register is written to. Writing to this register increments the RAM Write Pointer Register. If trace capture is enabled, and this register is accessed, then a read from this register outputs 0xFFFFFFFF. Reads of this register never increment the RAM Write Pointer Register. A constant stream of 1s being output corresponds to a synchronization output from the ETB. If a write access is attempted, the data is not written into Trace RAM.

10.7.3.1.9 FFSR

Address offset: 0x300

ETB Formatter and Flush Status Register

This register indicates the implemented Trigger Counter multipliers and other supported features of the trigger system.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000002				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0**
ID	R/W	Field	Value ID	Value	Description
A	R	FLINPROG			Flush In Progress. This is an indication of the current state of afvalids.
B	R	FTSTOPPED			Formatter stopped. The formatter has received a stop request signal and all trace data and post-amble has been output. Any more trace data on the ATB interface is ignored and atreadys goes HIGH.

10.7.3.1.10 FFCR

Address offset: 0x304

ETB Formatter and Flush Control Register

This register controls the generation of stop, trigger, and flush events. To disable formatting and put the formatter into bypass mode, bits 1 and 0 must be clear. If both bits are set, then the formatter inserts triggers into the formatted stream. All three flush generating conditions can be enabled together. However, if a second or third flush event is generated then the current flush completes before the next flush is serviced. Flush from flushin takes priority over flush from Trigger, which in turn completes before a manually activated flush. All Trigger indication conditions can be enabled simultaneously although this can cause the appearance of multiple triggers if flush using trigger is also enabled. Both 'Stop On' settings can be enabled, although if flush on trigger, FOnTrig, is set up then none of the flushed data is stored. When the system stops, it returns ATREADY and does not store the accepted data packets. This is to avoid stalling of any other connected devices using a Trace Replicator. If an event in the Formatter and Flush Control Register is required, it must be enabled before the originating event starts. Because requests from flushes and triggers can originate in an asynchronous clock domain, the exact time the component acts on the request cannot be determined with respect to configuring the control. Note - To perform a stop on flush completion through a manually-generated flush request, two write operations to the register are required: one to enable the stop event, if it is not already enabled; one to generate the manual flush.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																						J	I		H	G	F		E	D	C			B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	ENFTC																																	
				Do not embed Triggers into the formatted stream. Trace disable cycles and triggers are indicated by TRACECTL, where fitted. Can only be changed when FtStopped is HIGH. This bit is clear on reset.																																	
B	RW	ENFCONT																																	
				Continuous mode in the ETB corresponds to normal mode with the embedding of triggers. Can only be changed when FtStopped is HIGH. This bit is clear on reset.																																	
C	RW	FONFLIN																																	
				Set this bit to enable use of the flushin connection. This is clear on reset.																																	
D	RW	FONTRIG																																	
				Generate flush using Trigger event. Set this bit to cause a flush of data in the system when a Trigger Event occurs. This bit is clear on reset. A Trigger Event is defined as when the Trigger counter reaches zero (where fitted) or, in the case of the trigger counter being zero (or not fitted), when trigin is HIGH.																																	
E	RW	FONMAN																																	
				Setting this bit causes a flush to be generated. This is cleared when this flush has been serviced. This bit is clear on reset.																																	
F	RW	TRIGIN																																	
				Indicate a trigger on trigin being asserted.																																	
G	RW	TRIGEVT																																	
				Indicate a trigger on a Trigger Event.																																	
H	RW	TRIGFL																																	
				Indicates a trigger on Flush completion (afreadys being returned).																																	
I	RW	STOPFL																																	
				This forces the FIFO to drain off any part-completed packets. Setting this bit enables this function but this is clear on reset (disabled).																																	
J	RW	STOPTRIG																																	
				Stop the formatter after a Trigger Event is observed. Reset to disabled (zero).																																	

10.7.3.1.11 ITMISCOP0

Address offset: 0xEE0

Integration Test Miscellaneous Output Register 0

The Integration Test Miscellaneous Output Register 0 controls the values of some outputs from the ETB.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	ACQCOMP																																	
				Set the value of acqcomp.																																	
B	W	FULL																																	
				Set the value of full output port.																																	

10.7.3.1.12 ITTRFLINACK

Address offset: 0xEE4

Integration Test Trigger In and Flush In Acknowledge Register

The Integration Test Trigger In and Flush In Acknowledge Register enables control of the triginack and flushinack outputs from the ETB.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	TRIGINACK																																	
				Set the value of triginack.																																	
B	W	FLUSHINACK																																	
				Set the value of flushinack.																																	

10.7.3.1.13 ITTRFLIN

Address offset: 0xEE8

Integration Test Trigger In and Flush In Register

The Integration Test Trigger In and Flush In Register contains the values of the flushin and trigin inputs to the ETB.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	TRIGIN																																	
				Read the value of trigin.																																	
B	R	FLUSHIN																																	
				Read the value of flushin.																																	

10.7.3.1.14 ITATBDATA0

Address offset: 0xEEC

Integration Test ATB Data Register 0

The Integration Test ATB Data Register 0 contains the value of the atdatas inputs to the ETB. The values are only valid when atvalids is HIGH.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	ATDATA_0																																	

A	R	ATDATA_0			Read the value of atdatas[0].
B	R	ATDATA_7			Read the value of atdatas[7].
C	R	ATDATA_15			Read the value of atdatas[15].
D	R	ATDATA_23			Read the value of atdatas[23].
E	R	ATDATA_31			Read the value of atdatas[31].

10.7.3.1.15 ITATBCTR2

Address offset: 0xEF0

Integration Test ATB Control Register 2

The Integration Test ATB Control Register 2 enables control of the atreadys and afvalids outputs of the ETB.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	ATREADYS																																	
B	W	AFVALIDS																																	

A	W	ATREADYS			Set the value of atreadys.
B	W	AFVALIDS			Set the value of afvalids.

10.7.3.1.16 ITATBCTR1

Address offset: 0xEF4

Integration Test ATB Control Register 1

The Integration Test ATB Control Register 1 contains the value of the atids input to the ETB. This is only valid when atvalids is HIGH.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	ATID																																	

A	R	ATID			Read the value of atids.

10.7.3.1.17 ITATBCTR0

Address offset: 0xEF8

Integration Test ATB Control Register 0

The Integration Test ATB Control Register 0 captures the values of the atvalids, afreadys, and atbytess inputs to the ETB. To ensure the integration registers work correctly in a system, the value of atbytess is only valid when atvalids, bit [0], is HIGH.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	C C B A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	ATVALID			Read the value of atvalids.
B	R	AFREADY			Read the value of afreadys.
C	R	ATBYTES			Read the value of atbytess.

10.7.3.1.18 ITCTRL

Address offset: 0xF00

Integration Mode Control Register

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note: When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	INTEGRATION_MODE			Allows the component to switch from functional mode to integration mode or back.

10.7.3.1.19 CLAIMSET

Address offset: 0xFA0

Claim Tag Set Register

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A A A A
Reset 0x0000000F	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1**

ID	R/W	Field	Value ID	Value	Description
A	RW	CLAIMSET			This claim tag bit is implemented

10.7.3.1.20 CLAIMCLR

Address offset: 0xFA4

Claim Tag Clear Register

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CLAIMCLR			The value present reflects the current setting of the Claim Tag.

10.7.3.1.21 LAR

Address offset: 0xFB0

Lock Access Register

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	ACCESS_W			A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

10.7.3.1.22 LSR

Address offset: 0xFB4

Lock Status Register

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														C	B	A
Reset 0x00000003	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**

ID	R/W	Field	Value ID	Value	Description
A	R	LOCKEXIST			Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
B	R	LOCKGRANT			Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
C	R	LOCKTYPE			Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit

10.7.3.1.23 AUTHSTATUS

Address offset: 0xFB8

Authentication Status Register

Reports what functionality is currently permitted by the authentication interface.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D C C B B A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	NSID			Indicates the security level for non-secure invasive debug
B	R	NSNID			Indicates the security level for non-secure non-invasive debug
C	R	SID			Indicates the security level for secure invasive debug
D	R	SNID			Indicates the security level for secure non-invasive debug

10.7.3.1.24 DEVID

Address offset: 0xFC8

Device Configuration Register

This register indicates the capabilities of the ETB.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	EXTMUXNUM			When non-zero this value indicates the type/number of ATB multiplexing present on the input to the ATB.
B	R	RAMCLK			This bit returns 0 on reads indicating that the ETB RAM operates synchronously to atclk.

10.7.3.1.25 DEVTYPE

Address offset: 0xFCC

Device Type Identifier Register

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B A A A A
Reset 0x00000021				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1**
ID	R/W	Field	Value ID	Value	Description
A	R	MAJOR_TYPE			Major classification grouping for this debug/trace component
B	R	SUB_TYPE			Sub-classification within the major category

10.7.3.1.26 PERIPHID4

Address offset: 0xFD0

Peripheral ID4 Register

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B A A A A
Reset 0x00000004				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	DES_2			JEDEC continuation code indicating the designer of the component (along with the identity code)
B	R	SIZE			This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.

10.7.3.1.27 PERIPHID0

Address offset: 0xFE0

Peripheral ID0 Register

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x00000007				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	PART_0			Bits [7:0] of the component's part number. This is selected by the designer of the component.

10.7.3.1.28 PERIPHID1

Address offset: 0xFE4

Peripheral ID1 Register

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B A A A A
Reset 0x000000B9				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 0 0 1**
ID	R/W	Field	Value ID	Value	Description
A	R	PART_1			Bits [11:8] of the component's part number. This is selected by the designer of the component.
B	R	DES_0			Bits 3:0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

10.7.3.1.29 PERIPHID2

Address offset: 0xFE8

Peripheral ID2 Register

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C C C C B A A A
Reset 0x0000004B				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	DES_1			Bits 6:4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
B	R	JEDEC			Always set. Indicates that a JEDEC assigned value is used
C	R	REVISION			The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.

10.7.3.1.30 PERIPHID3

Address offset: 0xFEC

Peripheral ID3 Register

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	CMOD			Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.
B	R	REVAND			This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.

10.7.3.1.31 COMPID0

Address offset: 0xFF0

Component ID0 Register

A component identification register, that indicates that the identification registers are present.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x0000000D				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1**
ID	R/W	Field	Value ID	Value	Description
A	R	PRMBL_0			Contains bits [7:0] of the component identification

10.7.3.1.32 COMPID1

Address offset: 0xFF4

Component ID1 Register

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B A A A A
Reset 0x00000090				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	PRMBL_1			Contains bits [11:8] of the component identification
B	R	CLASS			Class of the component. E. g. ROM table, CoreSight component etc. Constitutes bits [15:12] of the component identification.

10.7.3.1.33 COMPID2

Address offset: 0xFF8

Component ID2 Register

A component identification register, that indicates that the identification registers are present.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x00000005				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1**
ID	R/W	Field	Value ID	Value	Description
A	R	PRMBL_2			Contains bits [23:16] of the component identification

10.7.3.1.34 COMPID3

Address offset: 0xFFC

Component ID3 Register

A component identification register, that indicates that the identification registers are present.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x000000B1				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 1**
ID	R/W	Field	Value ID	Value	Description
A	R	PRMBL_3			Contains bits [31:24] of the component identification

10.7.4 ETM — Embedded trace macrocell

The ARM embedded trace macorcell implements instruction, data and event tracing.

This document only provides a register-level description of this ARM component. See the Arm® Embedded Trace Macrocell Architecture Specification for more details

10.7.4.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
ETM	0xE0041000	HF	NS	NA	No	ETM

Register overview

Register	Offset	TZ	Description
TRCPRGCTLR	0x004		Enables the trace unit.

Register	Offset	TZ	Description
TRCPROCSELR	0x008		Controls which PE to trace. Might ignore writes when the trace unit is enabled or not idle. Before writing to this register, ensure that TRCSTATR.IDLE == 1 so that the trace unit can synchronize with the chosen PE. Implemented if TRCIDR3.NUMPROC is greater than zero.
TRCSTATR	0x00C		Idle status bit
TRCCONFIGR	0x010		Controls the tracing options This register must always be programmed as part of trace unit initialization. Might ignore writes when the trace unit is enabled or not idle.
TRCEVENTCTL0R	0x20		Controls the tracing of arbitrary events. If the selected event occurs a trace element is generated in the trace stream according to the settings in TRCEVENTCTL1R.DATAEN and TRCEVENTCTL1R.INSTEN.
TRCEVENTCTL1R	0x24		Controls the behavior of the events that TRCEVENTCTL0R selects. This register must always be programmed as part of trace unit initialization. Might ignore writes when the trace unit is enabled or not idle.
TRCSTALLCTLR	0x2C		Enables trace unit functionality that prevents trace unit buffer overflows. Might ignore writes when the trace unit is enabled or not idle. Must be programmed if TRCIDR3.STALLCTL == 1.
TRCTSCTLR	0x30		Controls the insertion of global timestamps in the trace streams. When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams. Might ignore writes when the trace unit is enabled or not idle. Must be programmed if TRCCONFIGR.TS == 1.
TRCSYNCPR	0x34		Controls how often trace synchronization requests occur. Might ignore writes when the trace unit is enabled or not idle. If writes are permitted then the register must be programmed.
TRCCCCTLR	0x38		Sets the threshold value for cycle counting. Might ignore writes when the trace unit is enabled or not idle. Must be programmed if TRCCONFIGR.CCI==1.
TRCBBCTLR	0x3C		Controls which regions in the memory map are enabled to use branch broadcasting. Might ignore writes when the trace unit is enabled or not idle. Must be programmed if TRCCONFIGR.BB == 1.
TRCTRACEIDR	0x40		Sets the trace ID for instruction trace. If data trace is enabled then it also sets the trace ID for data trace, to (trace ID for instruction trace) + 1. This register must always be programmed as part of trace unit initialization. Might ignore writes when the trace unit is enabled or not idle.
TRCQCTLR	0x44		Controls when Q elements are enabled. Might ignore writes when the trace unit is enabled or not idle. This register must be programmed if it is implemented and TRCCONFIGR.QE is set to any value other than 0b00.
TRCVICTLR	0x080		Controls instruction trace filtering. Might ignore writes when the trace unit is enabled or not idle. Only returns stable data when TRCSTATR.PMSTABLE == 1. Must be programmed, particularly to set the value of the SSSTATUS bit, which sets the state of the start/stop logic.

Register	Offset	TZ	Description
TRCVIIECTLR	0x084		ViewInst exclude control. Might ignore writes when the trace unit is enabled or not idle. This register must be programmed when one or more address comparators are implemented.
TRCVISSCTLR	0x088		Use this to set, or read, the single address comparators that control the ViewInst start/stop logic. The start/stop logic is active for an instruction which causes a start and remains active up to and including an instruction which causes a stop, and then the start/stop logic becomes inactive. Might ignore writes when the trace unit is enabled or not idle. If implemented then this register must be programmed.
TRCVIPCSSCTLR	0x08C		Use this to set, or read, which PE comparator inputs can control the ViewInst start/stop logic. Might ignore writes when the trace unit is enabled or not idle. If implemented then this register must be programmed.
TRCVDCTLR	0x0A0		Controls data trace filtering. Might ignore writes when the trace unit is enabled or not idle. This register must be programmed when data tracing is enabled, that is, when either TRCCONFIGR.DA == 1 or TRCCONFIGR.DV == 1.
TRCVDSACCTLR	0x0A4		ViewData include / exclude control. Might ignore writes when the trace unit is enabled or not idle. This register must be programmed when one or more address comparators are implemented.
TRCVDARCCTLR	0x0A8		ViewData include / exclude control. Might ignore writes when the trace unit is enabled or not idle. This register must be programmed when one or more address comparators are implemented.
TRCSEQEVR[n]	0x100		Moves the sequencer state according to programmed events. Might ignore writes when the trace unit is enabled or not idle. When the sequencer is used, all sequencer state transitions must be programmed with a valid event.
TRCSEQRSTEVR	0x118		Moves the sequencer to state 0 when a programmed event occurs. Might ignore writes when the trace unit is enabled or not idle. When the sequencer is used, all sequencer state transitions must be programmed with a valid event.
TRCSEQSTR	0x11C		Use this to set, or read, the sequencer state. Might ignore writes when the trace unit is enabled or not idle. Only returns stable data when TRCSTATR.PMSTABLE == 1. When the sequencer is used, all sequencer state transitions must be programmed with a valid event.
TRCEXTINSELR	0x120		Use this to set, or read, which external inputs are resources to the trace unit. Might ignore writes when the trace unit is enabled or not idle. Only returns stable data when TRCSTATR.PMSTABLE == 1. When the sequencer is used, all sequencer state transitions must be programmed with a valid event.
TRCCNTRLDVR[n]	0x140		This sets or returns the reload count value for counter n. Might ignore writes when the trace unit is enabled or not idle.
TRCCNTCTLR[n]	0x150		Controls the operation of counter n. Might ignore writes when the trace unit is enabled or not idle.

Register	Offset	TZ	Description
TRCCNTVR[n]	0x160		This sets or returns the value of counter n. The count value is only stable when TRCSTATR.PMSTABLE == 1. If software uses counter n then it must write to this register to set the initial counter value. Might ignore writes when the trace unit is enabled or not idle.
TRCRSCTLR[n]	0x200		Controls the selection of the resources in the trace unit. Might ignore writes when the trace unit is enabled or not idle. If software selects a non-implemented resource then CONSTRAINED UNPREDICTABLE behavior of the resource selector occurs, so the resource selector might fire unexpectedly or might not fire. Reads of the TRCRSCTLRn might return UNKNOWN.
TRCSSCCR0	0x280		Controls the single-shot comparator.
TRCSSCSR0	0x2A0		Indicates the status of the single-shot comparators. TRCSSCSR0 is sensitive toinstruction addresses.
TRCSSPCICR0	0x2C0		Selects the processor comparator inputs for Single-shot control.
TRCPDCR	0x310		Controls the single-shot comparator.
TRCPDSR	0x314		Indicates the power down status of the ETM.
TRCITATBIDR	0xEE4		Sets the state of output pins.
TRCITIATBINR	0xEF4		Reads the state of the input pins.
TRCITIATBOUTR	0xEFC		Sets the state of the output pins.
TRCITCTRL	0xF00		Enables topology detection or integration testing, by putting ETM-M33 into integration mode.
TRCCLAIMSET	0xFA0		Sets bits in the claim tag and determines the number of claim tag bits implemented.
TRCCLAIMCLR	0xFA4		Clears bits in the claim tag and determines the current value of the claim tag.
TRCAUTHSTATUS	0xFB8		Indicates the current level of tracing permitted by the system
TRCDEVARCH	0xFBC		The TRCDEVARCH identifies ETM-M33 as an ETMv4.2 component
TRCDEVTYPE	0xFCC		Controls the single-shot comparator.
TRCPIDR[n]	0xFD0		Coresight peripheral identification registers.
TRCCIDR[n]	0xFF0		Coresight component identification registers.

10.7.4.1.1 TRCPRGCTLR

Address offset: 0x004

Enables the trace unit.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EN			Trace unit enable bit
			Disabled	0	The trace unit is disabled. All trace resources are inactive and no trace is generated.
			Enabled	1	The trace unit is enabled.

10.7.4.1.2 TRCPROCSELR

Address offset: 0x008

Controls which PE to trace.

Might ignore writes when the trace unit is enabled or not idle.

Before writing to this register, ensure that TRCSTATR.IDLE == 1 so that the trace unit can synchronize with the chosen PE.

Implemented if TRCIDR3.NUMPROC is greater than zero.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	PROCSEL			PE select bits that select the PE to trace.

10.7.4.1.3 TRCSTATR

Address offset: 0x00C

Idle status bit

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	IDLE			Trace unit enable bit
			NotIdle	0	The trace unit is not idle.
			Idle	1	The trace unit is idle.
B	RW	PMSTABLE			Programmers' model stable bit
			NotStable	0	The programmers' model is not stable.
			Stable	1	The programmers' model is stable.

10.7.4.1.4 TRCCONFIGR

Address offset: 0x010

Controls the tracing options

This register must always be programmed as part of trace unit initialization.

Might ignore writes when the trace unit is enabled or not idle.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				M L K J J I H G G G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	LOADASP0INST			Instruction P0 load field. This field controls whether load instructions are traced as P0 instructions.
			No	0	Do not trace load instructions as P0 instructions.
			Yes	1	Trace load instructions as P0 instructions.
B	RW	STOREASP0INST			Instruction P0 field. This field controls whether store instructions are traced as P0 instructions.
			No	0	Do not trace store instructions as P0 instructions.
			Yes	1	Trace store instructions as P0 instructions.
C	RW	BB			Branch broadcast mode bit.
			Disabled	0	Branch broadcast mode is disabled.
			Enabled	1	Branch broadcast mode is enabled.
D	RW	CCI			Cycle counting instruction trace bit.
			Disabled	0	Cycle counting in the instruction trace is disabled.
			Enabled	1	Cycle counting in the instruction trace is enabled.
E	RW	CID			Context ID tracing bit.
			Disabled	0	Context ID tracing is disabled.
			Enabled	1	Context ID tracing is enabled.
F	RW	VMID			Virtual context identifier tracing bit.
			Disabled	0	Virtual context identifier tracing is disabled.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				M L K J J I H G G G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			Enabled	1	Virtual context identifier tracing is enabled.
G	RW	COND			Conditional instruction tracing bit.
			Disabled	0	Conditional instruction tracing is disabled.
			LoadOnly	1	Conditional load instructions are traced.
			StoreOnly	2	Conditional store instructions are traced.
			LoadAndStore	3	Conditional load and store instructions are traced.
			All	7	All conditional instructions are traced.
H	RW	TS			Global timestamp tracing bit.
			Disabled	0	Global timestamp tracing is disabled.
			Enabled	1	Global timestamp tracing is enabled.
I	RW	RS			Return stack enable bit.
			Disabled	0	Return stack is disabled.
			Enabled	1	Return stack is enabled.
J	RW	QE			Q element enable field.
			Disabled	0	Q elements are disabled.
			OnlyWithoutInstCou	1	Q elements with instruction counts are enabled. Q elements without instruction counts are disabled.
			Enabled	3	Q elements with and without instruction counts are enabled.
K	RW	VMIDOPT			Control bit to select the Virtual context identifier value used by the trace unit, both for trace generation and in the Virtual context identifier comparators.
			VTTBR_EL2	0	VTTBR_EL2.VMID is used. If the trace unit supports a Virtual context identifier larger than the VTTBR_EL2.VMID, the upper unused bits are always zero. If the trace unit supports a Virtual context identifier larger than 8 bits and if the VTCR_EL2.VS bit forces use of an 8-bit Virtual context identifier, bits [15:8] of the trace unit Virtual context identifier are always zero.
			CONTEXTIDR_EL2	1	CONTEXTIDR_EL2 is used.
L	RW	DA			Data address tracing bit.
			Disabled	0	Data address tracing is disabled.
			Enabled	1	Data address tracing is enabled.
M	RW	DV			Data value tracing bit.
			Disabled	0	Data value tracing is disabled.
			Enabled	1	Data value tracing is enabled.

10.7.4.1.5 TRCEVENTCTL0R

Address offset: 0x20

Controls the tracing of arbitrary events.

If the selected event occurs a trace element is generated in the trace stream according to the settings in TRCEVENTCTL1R.DATAEN and TRCEVENTCTL1R.INSTEN.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENT		[0:255]	Select which event should generate trace elements.

10.7.4.1.6 TRCEVENTCTL1R

Address offset: 0x24

Controls the behavior of the events that TRCEVENTCTL0R selects.

This register must always be programmed as part of trace unit initialization.

Might ignore writes when the trace unit is enabled or not idle.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																							G	F								E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-D	RW	INSTEN[i] (i=0..3)																																	
			Disabled	0																															
			Enabled	1																															
E	RW	DATAEN																																	
			Disabled	0																															
			Enabled	1																															
F	RW	ATB																																	
			Disabled	0																															
			Enabled	1																															
G	RW	LPOVERRIDE																																	
			Disabled	0																															
			Enabled	1																															

10.7.4.1.7 TRCSTALLCTLR

Address offset: 0x2C

Enables trace unit functionality that prevents trace unit buffer overflows.

Might ignore writes when the trace unit is enabled or not idle.

Must be programmed if TRCIDR3.STALLCTL == 1.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																							G	F	E	D	C	B				A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	LEVEL		[15:0]																															
				If LEVEL is nonzero then a trace unit might suppress the generation of: Global timestamps in the instruction trace stream and the data trace stream. Cycle counting in the instruction trace stream, although the cumulative cycle count remains correct.																																		
			Min	0																															
			Max	15																															

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				G F E D C B A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
B	RW	ISTALL			Instruction stall bit. Controls if a trace unit can stall the PE when the instruction trace buffer space is less than LEVEL.
			Disabled	0	The trace unit must not stall the PE.
			Enabled	1	The trace unit can stall the PE.
C	RW	DSTALL			Data stall bit. Controls if a trace unit can stall the PE when the data trace buffer space is less than LEVEL.
			Disabled	0	The trace unit must not stall the PE.
			Enabled	1	The trace unit can stall the PE.
D	RW	INSTPRIORITY			Prioritize instruction trace bit. Controls if a trace unit can prioritize instruction trace when the instruction trace buffer space is less than LEVEL.
			Disabled	0	The trace unit must not prioritize instruction trace.
			Enabled	1	The trace unit can prioritize instruction trace. A trace unit might prioritize instruction trace by preventing output of data trace, or other means which ensure that the instruction trace has a higher priority than the data trace.
E	RW	DATADISCARDLOAD			Data discard field. Controls if a trace unit can discard data trace elements on a load when the data trace buffer space is less than LEVEL.
			Disabled	0	The trace unit must not discard any data trace elements.
			Enabled	1	The trace unit can discard P1 and P2 elements associated with data loads.
F	RW	DATADISCARDSTORE			Data discard field. Controls if a trace unit can discard data trace elements on a store when the data trace buffer space is less than LEVEL.
			Disabled	0	The trace unit must not discard any data trace elements.
			Enabled	1	The trace unit can discard P1 and P2 elements associated with data stores.
G	RW	NOOVERFLOW			Trace overflow prevention bit.
			Disabled	0	Trace overflow prevention is disabled.
			Enabled	1	Trace overflow prevention is enabled. This might cause a significant performance impact.

10.7.4.1.8 TRCTSCTLR

Address offset: 0x30

Controls the insertion of global timestamps in the trace streams.

When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams.

Might ignore writes when the trace unit is enabled or not idle.

Must be programmed if TRCCONFIGR.TS == 1.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENT		[0:255]	Select which event should generate time stamps.

10.7.4.1.9 TRCSYNCPR

Address offset: 0x34

Controls how often trace synchronization requests occur.

Might ignore writes when the trace unit is enabled or not idle.

If writes are permitted then the register must be programmed.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	PERIOD		[31:0]	Controls how many bytes of trace, the sum of instruction and data, that a trace unit can generate before a trace synchronization request occurs. The number of bytes is always a power of two, calculated by 2^PERIOD
			Disabled	0	Trace synchronization requests are disabled. This setting does not disable other types of trace synchronization request.

10.7.4.1.10 TRCCCCTLR

Address offset: 0x38

Sets the threshold value for cycle counting.

Might ignore writes when the trace unit is enabled or not idle.

Must be programmed if TRCCONFIGR.CCI==1.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	THRESHOLD		[2047:0]	Sets the threshold value for instruction trace cycle counting.

10.7.4.1.11 TRCBBCTLR

Address offset: 0x3C

Controls which regions in the memory map are enabled to use branch broadcasting.

Might ignore writes when the trace unit is enabled or not idle.

Must be programmed if TRCCONFIGR.BB == 1.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	RANGE[i] (i=0..7)			Address range field. Selects which address range comparator pairs are in use with branch broadcasting. Each field represents an address range comparator pair, so field[i] controls the selection of address range comparator pair i.
			Disabled	0	The address range that address range comparator pair i defines, is not selected.
			Enabled	1	The address range that address range comparator pair n defines, is selected.

10.7.4.1.12 TRCTRACEIDR

Address offset: 0x40

Sets the trace ID for instruction trace. If data trace is enabled then it also sets the trace ID for data trace, to (trace ID for instruction trace) + 1.

This register must always be programmed as part of trace unit initialization.

Might ignore writes when the trace unit is enabled or not idle.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	TRACEID			Trace ID field. Sets the trace ID value for instruction trace. Bit[0] must be zero if data trace is enabled. If data trace is enabled then a trace unit sets the trace ID for data trace, to TRACEID+1.

10.7.4.1.13 TRCQCTLR

Address offset: 0x44

Controls when Q elements are enabled.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed if it is implemented and TRCCONFIGR.QE is set to any value other than 0b00.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	RANGE[i] (i=0..7)			Specifies the address range comparators to be used for controlling Q elements.
			Disabled	0	Address range comparator i is disabled.
			Enabled	1	Address range comparator i is selected for use.
I	RW	MODE			Selects whether the address range comparators selected by the RANGE field indicate address ranges where the trace unit is permitted to generate Q elements or address ranges where the trace unit is not permitted to generate Q elements:
			Exclude	0	Exclude mode. The address range comparators selected by the RANGE field indicate address ranges where the trace unit cannot generate Q elements. If no ranges are selected, Q elements are permitted across the entire memory map.
			Include	1	Include mode. The address range comparators selected by the RANGE field indicate address ranges where the trace unit can generate Q elements. If all the implemented bits in RANGE are set to 0 then Q elements are disabled.

10.7.4.1.14 TRCVICTLR

Address offset: 0x080

Controls instruction trace filtering.

Might ignore writes when the trace unit is enabled or not idle.

Only returns stable data when TRCSTATR.PMSTABLE == 1.

Must be programmed, particularly to set the value of the SSSTATUS bit, which sets the state of the start/stop logic.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				L K J I H G F E D C B A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENT_SEL			Select which resource number should be filtered.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				L K J I H G F E D C B A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			Disabled	0	This event is not filtered.
			Enabled	1	This event is filtered.
B	RW	SSSTATUS			When TRCIDR4.NUMACPAIRS > 0 or TRCIDR4.NUMPC > 0, this bit returns the status of the start/stop logic.
			Stopped	0	The start/stop logic is in the stopped state.
			Started	1	The start/stop logic is in the started state.
C	RW	TRCRESET			Controls whether a trace unit must trace a Reset exception.
			Disabled	0	The trace unit does not trace a Reset exception unless it traces the exception or instruction immediately prior to the Reset exception.
			Enabled	1	The trace unit always traces a Reset exception.
D	RW	TRCERR			When TRCIDR3.TRCERR==1, this bit controls whether a trace unit must trace a System error exception.
			Disabled	0	The trace unit does not trace a System error exception unless it traces the exception or instruction immediately prior to the System error exception.
			Enabled	1	The trace unit always traces a System error exception, regardless of the value of ViewInst.
E-H	RW	EXLEVEL[i]_S (i=0..3)			In Secure state, each bit controls whether instruction tracing is enabled for the corresponding Exception level i.
			Disabled	1	The trace unit does not generate instruction trace, in Secure state, for Exception level i.
			Enabled	0	The trace unit generates instruction trace, in Secure state, for Exception level i.
I-L	RW	EXLEVEL[i]_NS (i=0..3)			In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding Exception level i.
			Disabled	1	The trace unit does not generate instruction trace, in Non-secure state, for Exception level i.
			Enabled	0	The trace unit generates instruction trace, in Non-secure state, for Exception level i.

10.7.4.1.15 TRCVIIECTLR

Address offset: 0x084

ViewInst exclude control.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed when one or more address comparators are implemented.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	INCLUDE[i] (i=0..7)			Include range field. Selects which address range comparator pairs are in use with ViewInst include control.
			Disabled	0	The address range that address range comparator pair i defines, is not selected for ViewInst include control.
			Enabled	1	The address range that address range comparator pair i defines, is selected for ViewInst include control.
I-P	RW	EXCLUDE[i] (i=0..7)			Exclude range field. Selects which address range comparator pairs are in use with ViewInst exclude control.
			Disabled	0	The address range that address range comparator pair i defines, is not selected for ViewInst exclude control.
			Enabled	1	The address range that address range comparator pair i defines, is selected for ViewInst exclude control.

10.7.4.1.16 TRCVISSCTLR

Address offset: 0x088

Use this to set, or read, the single address comparators that control the ViewInst start/stop logic. The start/stop logic is active for an instruction which causes a start and remains active up to and including an instruction which causes a stop, and then the start/stop logic becomes inactive.

Might ignore writes when the trace unit is enabled or not idle.

If implemented then this register must be programmed.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	START[i] (i=0..7)			Selects which single address comparators are in use with ViewInst start/stop control, for the purpose of starting trace.
			Disabled	0	The single address comparator i, is not selected as a start resource.
			Enabled	1	The single address comparator i, is selected as a start resource.
I-P	RW	STOP[i] (i=0..7)			Selects which single address comparators are in use with ViewInst start/stop control, for the purpose of stopping trace
			Disabled	0	The single address comparator i, is not selected as a stop resource.
			Enabled	1	The single address comparator i, is selected as a stop resource.

10.7.4.1.17 TRCVIPCSSCTLR

Address offset: 0x08C

Use this to set, or read, which PE comparator inputs can control the ViewInst start/stop logic.

Might ignore writes when the trace unit is enabled or not idle.

If implemented then this register must be programmed.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	START[i] (i=0..7)			Selects which PE comparator inputs are in use with ViewInst start/stop control, for the purpose of starting trace
			Disabled	0	The single PE comparator input i, is not selected as a start resource.
			Enabled	1	The single PE comparator input i, is selected as a start resource.
I-P	RW	STOP[i] (i=0..7)			Selects which PE comparator inputs are in use with ViewInst start/stop control, for the purpose of stopping trace.
			Disabled	0	The single PE comparator input i, is not selected as a stop resource.
			Enabled	1	The single PE comparator input i, is selected as a stop resource.

10.7.4.1.18 TRCVDCTLR

Address offset: 0x0A0

Controls data trace filtering.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed when data tracing is enabled, that is, when either TRCCONFIGR.DA == 1 or TRCCONFIGR.DV == 1.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				L K J I I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	EVENT[i] (i=0..7)			Event unit enable bit.
			Disabled	0	The trace event is not selected for trace filtering.
			Enabled	1	The trace event is selected for trace filtering.
I	RW	SPREL			Controls whether a trace unit traces data for transfers that are relative to the Stack Pointer (SP).
			Enabled	0	The trace unit does not affect the tracing of SP-relative transfers.
			DataOnly	2	The trace unit does not trace the address portion of SP-relative transfers. If data value tracing is enabled then the trace unit generates a P1 data address element.
			Disabled	3	The trace unit does not trace the address or value portions of SP-relative transfers.
J	RW	PCREL			Controls whether a trace unit traces data for transfers that are relative to the Program Counter (PC).
			Enabled	0	The trace unit does not affect the tracing of PC-relative transfers.
			Disabled	1	The trace unit does not trace the address or value portions of PC-relative transfers.
K	RW	TBI			Controls which information a trace unit populates in bits[63:56] of the data address.
			SignExtend	0	The trace unit assigns bits[63:56] to have the same value as bit[55] of the data address, that is, it sign-extends the value.
			Copy	1	The trace unit assigns bits[63:56] to have the same value as bits[63:56] of the data address.
L	RW	TRCEXDATA			Controls the tracing of data transfers for exceptions and exception returns on Armv6-M, Armv7-M, and Armv8-M PEs.
			Disabled	0	Exception and exception return data transfers are not traced.
			Enabled	1	Exception and exception return data transfers are traced if the other aspects of ViewData indicate that the data transfers must be traced.

10.7.4.1.19 TRCVDSACCTLR

Address offset: 0x0A4

ViewData include / exclude control.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed when one or more address comparators are implemented.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A-H	RW	INCLUDE[i] (i=0..7)			Selects which single address comparators are in use with ViewData include control.
			Disabled	0	The single address comparator i, is not selected for ViewData include control.
			Enabled	1	The single address comparator i, is selected for ViewData include control.
I-P	RW	EXCLUDE[i] (i=0..7)			Selects which single address comparators are in use with ViewData exclude control.
			Disabled	0	The single address comparator i, is not selected for ViewData exclude control.
			Enabled	1	The single address comparator i, s selected for ViewData exclude control.

10.7.4.1.20 TRCVDARCCTLR

Address offset: 0x0A8

ViewData include / exclude control.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed when one or more address comparators are implemented.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A-H	RW	INCLUDE[i] (i=0..7)			Include range field. Selects which address range comparator pairs are in use with ViewData include control.
			Disabled	0	The address range that address range comparator i defines, is not selected for ViewData include control.
			Enabled	1	The address range that address range comparator i defines, is selected for ViewData include control.
I-P	RW	EXCLUDE[i] (i=0..7)			Exclude range field. Selects which address range comparator pairs are in use with ViewData exclude control.
			Disabled	0	The address range that address range comparator i defines, is not selected for ViewData exclude control.
			Enabled	1	The address range that address range comparator i defines, s selected for ViewData exclude control.

10.7.4.1.21 TRCSEQEVR[n] (n=0..2)

Address offset: 0x100 + (n × 0x4)

Moves the sequencer state according to programmed events.

Might ignore writes when the trace unit is enabled or not idle.

When the sequencer is used, all sequencer state transitions must be programmed with a valid event.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	F[i] (i=0..7)			Forward field.
			Disabled	0	The trace event does not affect the sequencer.
			Enabled	1	When the event occurs then the sequencer state moves from state n to state n+1.
I-P	RW	B[i] (i=0..7)			Backward field.
			Disabled	0	The trace event does not affect the sequencer.
			Enabled	1	When the event occurs then the sequencer state moves from state n+1 to state n.

10.7.4.1.22 TRCSEQRSTEVR

Address offset: 0x118

Moves the sequencer to state 0 when a programmed event occurs.

Might ignore writes when the trace unit is enabled or not idle.

When the sequencer is used, all sequencer state transitions must be programmed with a valid event.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENT		[0:255]	Select which event should reset the sequencer.

10.7.4.1.23 TRCSEQSTR

Address offset: 0x11C

Use this to set, or read, the sequencer state.

Might ignore writes when the trace unit is enabled or not idle.

Only returns stable data when TRCSTATR.PMSTABLE == 1.

When the sequencer is used, all sequencer state transitions must be programmed with a valid event.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	STATE			Sets or returns the state of the sequencer.
			State0	0	The sequencer is in state 0.
			State1	1	The sequencer is in state 1.
			State2	2	The sequencer is in state 2.
			State3	3	The sequencer is in state 3.

10.7.4.1.24 TRCEXTINSELR

Address offset: 0x120

Use this to set, or read, which external inputs are resources to the trace unit.

Might ignore writes when the trace unit is enabled or not idle.

Only returns stable data when TRCSTATR.PMSTABLE == 1.

When the sequencer is used, all sequencer state transitions must be programmed with a valid event.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				D	D	D	D	D	D	D	D	C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-D	RW	SEL[i] (i=0..3)		[0:255]																															
				Each field in this collection selects an external input as a resource for the trace unit.																																

10.7.4.1.25 TRCCNTRLDVR[n] (n=0..3)

Address offset: 0x140 + (n × 0x4)

This sets or returns the reload count value for counter n.

Might ignore writes when the trace unit is enabled or not idle.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	VALUE		[0:65535]																															
				Contains the reload value for counter n. When a reload event occurs for counter n then the trace unit copies the VALUEn field into counter n.																																

10.7.4.1.26 TRCCNTCTLR[n] (n=0..3)

Address offset: 0x150 + (n × 0x4)

Controls the operation of counter n.

Might ignore writes when the trace unit is enabled or not idle.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																				D	C	B	B	B	B	B	B	B	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CNTEVENT		[0:255]																															
				Selects an event, that when it occurs causes counter n to decrement.																																
B	RW	RLDEVENT		[0:255]																															
				Selects an event, that when it occurs causes a reload event for counter n.																																
C	RW	RLDSELF																																	
				Controls whether a reload event occurs for counter n, when counter n reaches zero.																																
			Disabled	0																															
				The counter is in Normal mode.																																
			Enabled	1																															
				The counter is in Self-reload mode.																																
D	RW	CNTCHAIN																																	
				For TRCCNTCTLR3 and TRCCNTCTLR1, this bit controls whether counter n decrements when a reload event occurs for counter n-1.																																
			Disabled	0																															
				Counter n does not decrement when a reload event for counter n-1 occurs.																																
			Enabled	1																															
				Counter n decrements when a reload event for counter n-1 occurs. This concatenates counter n and counter n-1, to provide a larger count value.																																

10.7.4.1.27 TRCCNTVR[n] (n=0..3)

Address offset: 0x160 + (n × 0x4)

This sets or returns the value of counter n.

The count value is only stable when TRCSTATR.PMSTABLE == 1.

If software uses counter n then it must write to this register to set the initial counter value.

Might ignore writes when the trace unit is enabled or not idle.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	VALUE		[0:65535]	Contains the count value of counter n.

10.7.4.1.28 TRCRSCTLR[n] (n=2..31)

Address offset: 0x200 + (n × 0x4)

Controls the selection of the resources in the trace unit.

Might ignore writes when the trace unit is enabled or not idle.

If software selects a non-implemented resource then CONSTRAINED UNPREDICTABLE behavior of the resource selector occurs, so the resource selector might fire unexpectedly or might not fire. Reads of the TRCRSCTLRn might return UNKNOWN.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EN			Trace unit enable bit
			Disabled	0	The trace unit is disabled. All trace resources are inactive and no trace is generated.
			Enabled	1	The trace unit is enabled.

10.7.4.1.29 TRCSSCCR0

Address offset: 0x280

Controls the single-shot comparator.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	RST			Enables the single-shot comparator resource to be reset when it occurs, to enable another comparator match to be detected
			Disabled	0	Multiple matches can not be detected.
			Enabled	1	Multiple matches can occur.

10.7.4.1.30 TRCSSCSR0

Address offset: 0x2A0

Indicates the status of the single-shot comparators. TRCSSCSR0 is sensitive toinstruction addresses.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	INST			Instruction address comparator support
			False	0	Single-shot instruction address comparisons not supported.
			True	1	Single-shot instruction address comparisons supported.
B	RW	DA			Data address comparator support
			False	0	Data address comparisons not supported.
			True	1	Data address comparisons supported.
C	RW	DV			Data value comparator support
			False	0	Data value comparisons not supported.
			True	1	Data value comparisons supported.
D	RW	PC			Process counter value comparator support
			False	0	Process counter value comparisons not supported.
			True	1	Process counter value comparisons supported.
E	RW	STATUS			Single-shot status. This indicates whether any of the selected comparators have matched.
			NoMatch	0	Match has not occurred.
			Match	1	Match has occurred at least once.

10.7.4.1.31 TRCSSPCICR0

Address offset: 0x2C0

Selects the processor comparator inputs for Single-shot control.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A-D	RW	PC[i] (i=0..3)			Selects processor comparator i inputs for Single-shot control
			Disabled	0	Processor comparator i is not selected for Single-shot control.
			Enabled	1	Processor comparator i is selected for Single-shot control.

10.7.4.1.32 TRCPDCR

Address offset: 0x310

Controls the single-shot comparator.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PU			Power up request, to request that power to ETM and access to the trace registers is maintained.
			Disabled	0	Power not requested.
			Enabled	1	Power requested.

10.7.4.1.33 TRCPDSR

Address offset: 0x314

Indicates the power down status of the ETM.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	POWER			Indicates ETM is powered up
			NotPoweredUp	0	ETM is not powered up. All registers are not accessible.
			PoweredUp	1	ETM is powered up. All registers are accessible.
B	RW	STICKYPD			Sticky power down state. This bit is set to 1 when power to the ETM registers is removed, to indicate that programming state has been lost. It is cleared after a read of the TRCPDSR
			NotPoweredDown	0	Trace register power has not been removed since the TRCPDSR was last read.
			PoweredDown	1	Trace register power has been removed since the TRCPDSR was last read.

10.7.4.1.34 TRCITATBIDR

Address offset: 0xEE4

Sets the state of output pins.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-G	RW	ID[i] (i=0..6)			Drives the ATIDMI[i] output pin.

10.7.4.1.35 TRCITIATBINR

Address offset: 0xEF4

Reads the state of the input pins.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ATVALID			Returns the value of the ATVALIDMI input pin.
B	RW	AFREADY			Returns the value of the AFREADYMI input pin.

10.7.4.1.36 TRCITIATBOUTR

Address offset: 0xEFC

Sets the state of the output pins.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ATVALID			Drives the ATVALIDMI output pin.
B	RW	AFREADY			Drives the AFREADYMI output pin.

10.7.4.1.37 TRCITCTRL

Address offset: 0xF00

Enables topology detection or integration testing, by putting ETM-M33 into integration mode.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	IME			Integration mode enable
			Disabled	0	ETM is not in integration mode.
			Enabled	1	ETM is in integration mode.

10.7.4.1.38 TRCCLAIMSET

Address offset: 0xFA0

Sets bits in the claim tag and determines the number of claim tag bits implemented.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-D	RW	SET[i] (i=0..3)			Claim tag set register
			NotSet	0	Claim tag i is not set.
			Set	1	Claim tag i is set.
			Claim	1	Set claim tag i.

10.7.4.1.39 TRCCLAIMCLR

Address offset: 0xFA4

Clears bits in the claim tag and determines the current value of the claim tag.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-D	RW	CLR[i] (i=0..3)			Claim tag clear register
			NotSet	0	Claim tag i is not set.
			Set	1	Claim tag i is set.
			Clear	1	Clear claim tag i.

10.7.4.1.40 TRCAUTHSTATUS

Address offset: 0xFB8

Indicates the current level of tracing permitted by the system

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D C C B B A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	NSID			Non-secure Invasive Debug

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D C C B B A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
B	RW	NSNID			Non-secure Non-Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
C	RW	SID			Secure Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
D	RW	SNID			Secure Non-Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.

10.7.4.1.41 TRCDEVARCH

Address offset: 0xFBC

The TRCDEVARCH identifies ETM-M33 as an ETMv4.2 component

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D D D D D D D D D D C B B B B A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	ARCHID			Architecture ID
			ETMv42	0x4A13	Component is an ETMv4 component
B	R	REVISION			Architecture revision
			v2	2	Component is part of architecture 4.2
C	R	PRESENT			This register is implemented
			Absent	0	The register is not implemented.
			Present	1	The register is implemented.
D	R	ARCHITECT			Defines the architect of the component
			Arm	0x23B	This peripheral was architected by Arm.

10.7.4.1.42 TRCDEVTYPE

Address offset: 0xFCC

Controls the single-shot comparator.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	MAJOR			The main type of the component
			TraceSource	3	Peripheral is a trace source.
B	R	SUB			The sub-type of the component
			ProcessorTrace	1	Peripheral is a processor trace source.

10.7.4.1.43 TRCPIDR[n] (n=0..7)

Address offset: 0xFD0 + (n × 0x4)

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.4.1.44 TRCCIDR[n] (n=0..3)

Address offset: 0xFF0 + (n × 0x4)

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.5 TPIU — Trace port interface unit

The ARM® CoreSight™ TPIU connects an ATB to an external trace port.

This document only provides a register-level description of this ARM component. See the ARM® CoreSight™ SoC-400 Technical Reference Manual for more details

10.7.5.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
TPIU	0xE0054000	HF	NS	NA	No	TPIU

Register overview

Register	Offset	TZ	Description
SUPPORTEDPORTSIZES	0x000		Each bit location is a single port size that is supported on the device.
CURRENTPORTSIZE	0x004		Each bit location is a single port size. One bit can be set, and indicates the current port size.
SUPPORTEDTRIGGERMODES	0x100		The Supported_trigger_modes register indicates the implemented trigger counter multipliers and other supported features of the trigger system.
TRIGGERCOUNTERVALUE	0x104		The Trigger_counter_value register enables delaying the indication of triggers to any external connected trace capture or storage devices.
TRIGGERMULTIPLIER	0x108		The Trigger_multiplier register contains the selectors for the trigger counter multiplier.
SUPPPORTEDTESTPATTERNMODES	0x200		The Supported_test_pattern_modes register provides a set of known bit sequences or patterns that can be output over the trace port and can be detected by the TPA or other associated trace capture device.
CURRENTTESTPATTERNMODES	0x204		Current_test_pattern_mode indicates the current test pattern or mode selected.
TPRCR	0x208		The TPRCR register is an 8-bit counter start value that is decremented. A write sets the initial counter value and a read returns the programmed value.
FFSR	0x300		The FFSR register indicates the current status of the formatter and flush features available in the TPIU.
FFCR	0x304		The FFCR register controls the generation of stop, trigger, and flush events.
FSCR	0x308		The FSCR register enables the frequency of synchronization information to be optimized to suit the Trace Port Analyzer (TPA) capture buffer size.

Register	Offset	TZ	Description
EXTCTLINPORT	0x400		Two ports can be used as a control and feedback mechanism for any serializers, pin sharing multiplexers, or other solutions that might be added to the trace output pins either for pin control or a high-speed trace port solution.
EXTCTLOUTPORT	0x404		Two ports can be used as a control and feedback mechanism for any serializers, pin sharing multiplexers, or other solutions that might be added to the trace output pins either for pin control or a high speed trace port solution. These ports are raw register banks that sample or export the corresponding external pins.
ITTRFLINACK	0xEE4		The ITTRFLINACK register enables control of the triginack and flushinack outputs from the TPIU.
ITTRFLIN	0xEE8		The ITTRFLIN register contains the values of the flushin and trigin inputs to the TPIU.
ITATBDATA0	0xEEC		The ITATBDATA0 register contains the value of the atdatas inputs to the TPIU. The values are valid only when atvalids is HIGH.
ITATBCTR2	0xEF0		Enables control of the atreadys and afvalids outputs of the TPIU.
ITATBCTR1	0xEF4		The ITATBCTR1 register contains the value of the atids input to the TPIU. This is only valid when atvalids is HIGH.
ITATBCTR0	0xEF8		The ITATBCTR0 register captures the values of the atvalids, afreadys, and atbytess inputs to the TPIU. To ensure the integration registers work correctly in a system, the value of atbytess is only valid when atvalids, bit[0], is HIGH.
ITCTRL	0xF00		Used to enable topology detection. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for integration testing and topology solving.
CLAIMSET	0xFA0		Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMSET register sets bits in the claim tag, and determines the number of claim bits implemented.
CLAIMCLR	0xFA4		Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMCLR register sets the bits in the claim tag to 0 and determines the current value of the claim tag.
LAR	0xFB0		This is used to enable write access to device registers.
LSR	0xFB4		This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. Accesses to the extended stimulus port registers are not affected by the lock mechanism. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register.
AUTHSTATUS	0xFB8		Indicates the current level of tracing permitted by the system
DEVID	0xFC8		Indicates the capabilities of the component.
DEVTYPE	0xFCC		The DEVTYPE register provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.
PIDR4	0xFD0		Coresight peripheral identification registers.
PIDR[0]	0xFE0		Coresight peripheral identification registers.
PIDR[1]	0xFE4		Coresight peripheral identification registers.
PIDR[2]	0xFE8		Coresight peripheral identification registers.
PIDR[3]	0xFEC		Coresight peripheral identification registers.
CIDR[0]	0xFF0		Coresight component identification registers.
CIDR[1]	0xFF4		Coresight component identification registers.
CIDR[2]	0xFF8		Coresight component identification registers.
CIDR[3]	0xFFC		Coresight component identification registers.

10.7.5.1.1 SUPPORTEDPORTSIZES

Address offset: 0x000

Each bit location is a single port size that is supported on the device.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-f	RW	PORT_SIZE_[i+1] (i=0..31)																																	
			NotSupported	0																															
			Supported	1																															

			Indicates whether the TPIU supports port size of i+1-bit.
			Port size i+1 is not supported.
			Port size i+1 is supported.

10.7.5.1.2 CURRENTPORTSIZE

Address offset: 0x004

Each bit location is a single port size. One bit can be set, and indicates the current port size.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-f	RW	PORT_SIZE_[i+1] (i=0..31)																																	
			NotSelected	0																															
			Selected	1																															

			Indicates which port size is currently selected.
			Port size i+1 is not selected.
			Port size i+1 is selected.

10.7.5.1.3 SUPPORTEDTRIGGERMODES

Address offset: 0x100

The Supported_trigger_modes register indicates the implemented trigger counter multipliers and other supported features of the trigger system.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																		H	G								F				E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-E	RW	MULT[i] (i=0..4)																																	
			NotSelected	0																															
			Selected	1																															
F	RW	TCOUNT8																																	
			NotImplemented	0																															
			Implemented	1																															
G	RW	TRIGGERED																																	
			NotOccured	0																															
			Occured	1																															
H	RW	TRGRUN																																	
			NotOccured	0																															
			Occured	1																															

			Indicates whether multiplying the trigger counter by 2^(i+1) is supported.
			Multiplying the trigger counter by 2^(i+1) is supported.
			Multiplying the trigger counter by 2^(i+1) is supported.
			Indicates whether an 8-bit wide counter register is implemented.
			An 8-bit wide counter register is implemented.
			An 8-bit wide counter register is implemented.
			A trigger has occurred and the counter has reached 0.
			Trigger has not occurred.
			Trigger has occurred.
			A trigger has occurred but the counter is not at 0.
			Either a trigger has not occurred or the counter is at 0.
			A trigger has occurred but the counter is not at 0.

10.7.5.1.4 TRIGGERCOUNTERVALUE

Address offset: 0x104

The Trigger_counter_value register enables delaying the indication of triggers to any external connected trace capture or storage devices.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	TrigCount		[0:255]	8-bit counter value for the number of words to be output from the formatter before a trigger is inserted.

10.7.5.1.5 TRIGGERMULTIPLIER

Address offset: 0x108

The Trigger_multiplier register contains the selectors for the trigger counter multiplier.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-E	RW	MULT[i] (i=0..4)			Multiply the Trigger Counter by 2^n.
			Disabled	0	Multiplier disabled.
			Enabled	1	Multiplier enabled.

10.7.5.1.6 SUPPPORTEDTESTPATTERNMODES

Address offset: 0x200

The Supported_test_pattern_modes register provides a set of known bit sequences or patterns that can be output over the trace port and can be detected by the TPA or other associated trace capture device.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	PATW1			Indicates whether the walking 1s pattern is supported as output over the trace port.
			NotSupported	0	Test pattern is not supported.
			Supported	1	Test pattern is supported.
B	RW	PATW0			Indicates whether the walking 0s pattern is supported as output over the trace port.
			NotSupported	0	Test pattern is not supported.
			Supported	1	Test pattern is supported.
C	RW	PATA5			Indicates whether the AA/55 pattern is supported as output over the trace port.
			NotSupported	0	Test pattern is not supported.
			Supported	1	Test pattern is supported.
D	RW	PATF0			Indicates whether the FF/00 pattern is supported as output over the trace port.
			NotSupported	0	Test pattern is not supported.
			Supported	1	Test pattern is supported.
E	RW	PTIMEEN			Indicates whether timed mode is supported.
			NotSupported	0	Mode is not supported.
			Supported	1	Mode is supported.
F	RW	PCONTEN			Indicates whether continuous mode is supported.
			NotSupported	0	Mode is not supported.
			Supported	1	Mode is supported.

10.7.5.1.7 CURRENTTESTPATTERNMODES

Address offset: 0x204

Current_test_pattern_mode indicates the current test pattern or mode selected.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PATW1			Indicates whether the walking 1s pattern is supported as output over the trace port.
			Disabled	0	Test pattern is disabled.
			Enabled	1	Test pattern is enabled.
B	RW	PATW0			Indicates whether the walking 0s pattern is supported as output over the trace port.
			Disabled	0	Test pattern is disabled.
			Enabled	1	Test pattern is enabled.
C	RW	PATA5			Indicates whether the AA/55 pattern is supported as output over the trace port.
			Disabled	0	Test pattern is disabled.
			Enabled	1	Test pattern is enabled.
D	RW	PATF0			Indicates whether the FF/00 pattern is supported as output over the trace port.
			Disabled	0	Test pattern is disabled.
			Enabled	1	Test pattern is enabled.
E	RW	PTIMEEN			Indicates whether timed mode is supported.
			Disabled	0	Mode is disabled.
			Enabled	1	Mode is enabled.
F	RW	PCONTEN			Indicates whether continuous mode is supported.
			Disabled	0	Mode is disabled.
			Enabled	1	Mode is enabled.

10.7.5.1.8 TPRCR

Address offset: 0x208

The TPRCR register is an 8-bit counter start value that is decremented. A write sets the initial counter value and a read returns the programmed value.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PATTCOUNT		[0:255]	8-bit counter value to indicate the number of traceclkin cycles for which a pattern runs before it switches to the next pattern.

10.7.5.1.9 FFSR

Address offset: 0x300

The FFSR register indicates the current status of the formatter and flush features available in the TPIU.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	FLINPROG			Flush in progress.
			NotInProgress	0	A flush is not in progress.
			InProgress	1	A flush is in progress.
B	RW	FTSTOPPED			The formatter has received a stop request signal and all trace data and post-amble is sent. Any additional trace data on the ATB interface is ignored and atreadys goes HIGH.
			Running	0	Formatter has not stopped.
			Stopped	1	Formatter has stopped.
C	RW	TCPRESENT			Indicates whether the TRACECTL pin is available for use.
			NotPresent	0	TRACECTL pin is not present.
			Present	1	TRACECTL pin is present.

10.7.5.1.10 FFCR

Address offset: 0x304

The FFCR register controls the generation of stop, trigger, and flush events.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	ENFTC			Do not embed triggers into the formatted stream. Trace disable cycles and triggers are indicated by tracectl, where present.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
B	RW	ENFCONT			Is embedded in trigger packets and indicates that no cycle is using sync packets.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
C	RW	FONFLIN			Enables the use of the flushin connection.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
D	RW	FONTRIG			Initiates a manual flush of data in the system when a trigger event occurs.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
E	RW	FONMANR			Generates a flush. This bit is set to 0 when this flush is serviced.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
F	RW	FONMANW			Generates a flush. This bit is set to 1 when this flush is serviced.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
G	RW	TRIGIN			Indicates a trigger when trigin is asserted.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
H	RW	TRIGEVT			Indicates a trigger on a trigger event.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
I	RW	TRIGFL			Indicates a trigger when flush completion on afreadys is returned.
			Disabled	0	The formatting feature is disabled.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			Enabled	1	The formatting feature is enabled.
J	RW	STOPFL			Forces the FIFO to drain off any part-completed packets.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.
K	RW	STOPTRIG			Stops the formatter after a trigger event is observed. Reset to disabled or 0.
			Disabled	0	The formatting feature is disabled.
			Enabled	1	The formatting feature is enabled.

10.7.5.1.11 FSCR

Address offset: 0x308

The FSCR register enables the frequency of synchronization information to be optimized to suit the Trace Port Analyzer (TPA) capture buffer size.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CYCCOUNT		[0:1024]	12-bit counter reload value. Indicates the number of complete frames between full synchronization packets.

10.7.5.1.12 EXTCTLINPORT

Address offset: 0x400

Two ports can be used as a control and feedback mechanism for any serializers, pin sharing multiplexers, or other solutions that might be added to the trace output pins either for pin control or a high-speed trace port solution.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	EXTCTLIN[i] (i=0..7)			EXTCTL inputs.
			Low	0	Input EXTCTLi is low.
			High	1	Input EXTCTLi is high.

10.7.5.1.13 EXTCTLOUTPORT

Address offset: 0x404

Two ports can be used as a control and feedback mechanism for any serializers, pin sharing multiplexers, or other solutions that might be added to the trace output pins either for pin control or a high speed trace port solution. These ports are raw register banks that sample or export the corresponding external pins.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	EXTCTLOUT[i] (i=0..7)			EXTCTL outputs.
			Low	0	Output EXTCTLi is low.
			High	1	Output EXTCTLi is high.

10.7.5.1.14 ITTRFLINACK

Address offset: 0xEE4

The ITTRFLINACK register enables control of the triginack and flushinack outputs from the TPIU.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	TRIGINACK			Sets the value of triginack.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.
B	RW	FLUSHINACK			Sets the value of flushinack.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.

10.7.5.1.15 ITTRFLIN

Address offset: 0xEE8

The ITTRFLIN register contains the values of the flushin and trigin inputs to the TPIU.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	TRIGIN			Reads the value of trigin.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.
B	RW	FLUSHIN			Reads the value of flushin.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.

10.7.5.1.16 ITATBDATA0

Address offset: 0xEEC

The ITATBDATA0 register contains the value of the atdatas inputs to the TPIU. The values are valid only when atvalids is HIGH.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A-E	RW	ATDATA[i] (i=0..4)			A read access returns the value of a pin on atdatas_x of the enabled port. A write access writes to the corresponding atdatam pin of the enabled port.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.

10.7.5.1.17 ITATBCTR2

Address offset: 0xEF0

Enables control of the atreadys and afvalids outputs of the TPIU.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	ATREADY			Sets the value of afvalid.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.
B	RW	AFVALID			Sets the value of atready.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.

10.7.5.1.18 ITATBCTR1

Address offset: 0xEF4

The ITATBCTR1 register contains the value of the atids input to the TPIU. This is only valid when atvalids is HIGH.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	ATID			Reads the value of atids.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.

10.7.5.1.19 ITATBCTR0

Address offset: 0xEF8

The ITATBCTR0 register captures the values of the atvalids, afreadys, and atbytess inputs to the TPIU. To ensure the integration registers work correctly in a system, the value of atbytess is only valid when atvalids, bit[0], is HIGH.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ATVALID			Reads the value of atvalids.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.
B	RW	AFREADY			Reads the value of afreadys.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.
C	RW	ATBYTES			Reads the value of atbytess.
			Low	0	Pin is logic 0.
			High	1	Pin is logic 1.

10.7.5.1.20 ITCTRL

Address offset: 0xF00

Used to enable topology detection. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for integration testing and topology solving.

Note: When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	INTEGRATIONMODE			Enables the component to switch from functional mode to integration mode and back. If no integration functionality is implemented, this register must read as zero.
			Disabled	0	Integration mode is disabled.
			Enabled	1	Integration mode is Enabled.

10.7.5.1.21 CLAIMSET

Address offset: 0xFA0

Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMSET register sets bits in the claim tag, and determines the number of claim bits implemented.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-D	RW	BIT[i] (i=0..3)			Set claim bit i and check if bit is implemented or not.
			NotImplemented	0	Claim bit i is not implemented.
			Implemented	1	Claim bit i is implemented.
			Set	1	Set claim bit i.

10.7.5.1.22 CLAIMCLR

Address offset: 0xFA4

Software can use the claim tag to coordinate application and debugger access to trace unit functionality. The claim tags have no effect on the operation of the component. The CLAIMCLR register sets the bits in the claim tag to 0 and determines the current value of the claim tag.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-D	RW	BIT[i] (i=0..3)																																	
			Cleared	0																															
			Set	1																															
			Clear	1																															

10.7.5.1.23 LAR

Address offset: 0xFB0

This is used to enable write access to device registers.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	ACCESS																																	
			UnLock	0xC5ACCE55																															

10.7.5.1.24 LSR

Address offset: 0xFB4

This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. Accesses to the extended stimulus port registers are not affected by the lock mechanism. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PRESENT			Indicates that a lock control mechanism exists for this device.
			NotImplemented	0	No lock control mechanism exists, writes to the Lock Access Register are ignored.
			Implemented	1	Lock control mechanism is present.
B	RW	LOCKED			Returns the current status of the Lock.
			UnLocked	0	Write access is allowed to this device.
			Locked	1	Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted.
C	RW	TYPE			Indicates if the Lock Access Register is implemented as 8-bit or 32-bit.
			Bits32	0	This component implements a 32-bit Lock Access Register.
			Bits8	1	This component implements an 8-bit Lock Access Register.

10.7.5.1.25 AUTHSTATUS

Address offset: 0xFB8

Indicates the current level of tracing permitted by the system

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D C C B B A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	NSID			Non-secure Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
B	RW	NSNID			Non-secure Non-Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
C	RW	SID			Secure Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.
D	RW	SNID			Secure Non-Invasive Debug
			NotImplemented	0	The feature is not implemented.
			Implemented	1	The feature is implemented.

10.7.5.1.26 DEVID

Address offset: 0xFC8

Indicates the capabilities of the component.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F E D C C C B A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	MUXNUM			Indicates the hidden level of input multiplexing. When non-zero, this value indicates the type of multiplexing on the input to the ATB. Currently only 0x00 is supported, that is, no multiplexing is present. This value helps detect the ATB structure.
B	R	CLKRELAT			Indicates the relationship between atclk and traceclkin.
			Synchronous	0	atclk and traceclkin are synchronous.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F E D C C C B A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			ASynchronous	1	atclk and traceclkin are asynchronous.
C	R	FIFOSIZE			FIFO size in powers of 2.
			Entries4	2	FIFO size of 4 entries, that is, 16 bytes.
D	R	TCLKDATA			Indicates whether trace clock plus data is supported.
			Supported	0	Trace clock and data is supported.
			NotSupported	1	Trace clock and data is not supported.
E	R	SWOMAN			Indicates whether Serial Wire Output, Manchester encoded format, is supported.
			NotSupported	0	Serial Wire Output, Manchester encoded format, is not supported.
			Supported	1	Serial Wire Output, Manchester encoded format, is supported.
F	R	SWOUARTNRZ			Indicates whether Serial Wire Output, UART or NRZ, is supported.
			NotSupported	0	Serial Wire Output, UART or NRZ, is not supported.
			Supported	1	Serial Wire Output, UART or NRZ, is supported.

10.7.5.1.27 DEVTYPE

Address offset: 0xFCC

The DEVTYPE register provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	MAJOR			The main type of the component
			TraceSource	1	Peripheral is a trace sink.
B	R	SUB			The sub-type of the component
			TracePort	1	Indicates that this component is a trace port component.

10.7.5.1.28 PIDR4

Address offset: 0xFD0

Coresight peripheral identification registers.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description

10.7.5.1.29 PIDR[0]

Address offset: 0xFE0

Coresight peripheral identification registers.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description

10.7.5.1.30 PIDR[1]

Address offset: 0xFE4

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.5.1.31 PIDR[2]

Address offset: 0xFE8

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.5.1.32 PIDR[3]

Address offset: 0xFEC

Coresight peripheral identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.5.1.33 CIDR[0]

Address offset: 0xFF0

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.5.1.34 CIDR[1]

Address offset: 0xFF4

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.5.1.35 CIDR[2]

Address offset: 0xFF8

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.7.5.1.36 CIDR[3]

Address offset: 0xFFC

Coresight component identification registers.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description

10.8 CTRL-AP - Control access port

The control access port (CTRL-AP) is a custom access port that enables control of the device when other debug access ports (DAP) have been disabled by the access port protection.

For an overview of the other debug access ports, see DAP - Debug access port on page 368.

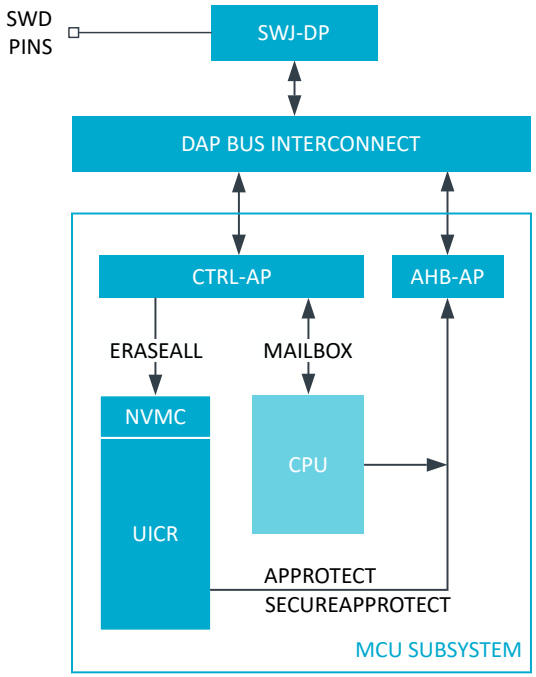


Figure 118: Control access port details

Access port protection (APPROTECT) blocks the debugger access to the AHB-AP, and prevents read and write access to all CPU registers and memory-mapped addresses. To enable port protection access for both secure and non-secure modes, use the registers SECUREAPPROTECT on page 41 and APPROTECT on

page 40 respectively. The debugger can use the register APPROTECT.STATUS on page 441 to read the status of secure and non-secure access port protection.

CTRL-AP has the following features:

- Soft reset
- Erase all
- Mailbox interface
- Debug of protected devices

10.8.1 Reset request

The debugger can request the device to perform a soft reset.

Use the register RESET on page 440 to request a soft reset. Once the soft reset is performed, the reset reason is accessible on the on-chip firmware through the RESETREAS register. For more information about the soft reset, see Reset on page 56.

10.8.2 Erase all

The erase all function lets the debugger trigger an erase of flash, user information configuration registers (UICR), RAM, all peripheral settings, and also removes the access port protection.

To trigger an erase all function, the debugger writes to the register ERASEALL on page 440. The register ERASEALLSTATUS on page 440 will read as busy for the duration of the operation. After the next reset, the access port protection is removed.

If the debugger performs an erase all function on a slave MCU, the erase sequence will always erase the application MCU first, independently of how the application is protected, before erasing the slave MCU.

Erase all protection

It is possible to prevent the debugger from performing an erase all operation by writing to the UICR.ERASEPROTECT register. Once the register is configured and the device is reset, the CTRL-AP ERASEALL operation is disabled, and all flash write and erase operations are restricted to the firmware. In addition, it is still possible to write/erase from the debugger as long as the UICR.APPROTECT register is not set.

Note: Setting the UICR.ERASEPROTECT register only affects the erase all operation and not the debugger access.

The register ERASEPROTECT.STATUS on page 441 holds the status for erase protection.

10.8.3 Mailbox interface

CTRL-AP implements a mailbox interface which enables the CPU to communicate with a debugger over the SWD interface.

The mailbox interface consists of a transmit register MAILBOX.TXDATA on page 442 with its corresponding status register MAILBOX.TXSTATUS on page 442, and a receive register MAILBOX.RXDATA on page 442 with its corresponding status register MAILBOX.RXSTATUS on page 442. Status bits in the TXSTATUS/RXSTATUS registers are set and cleared automatically when the TXDATA/RXDATA registers are written to and read from, independently of the direction.

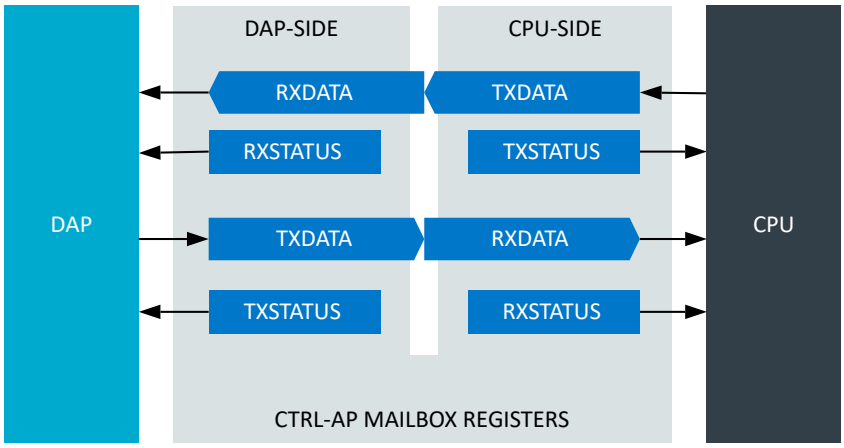


Figure 119: Mailbox register interface

Mailbox transfer sequence

1. Sender writes TXDATA.
2. Hardware sets sender's TXSTATUS to DataPending.
3. Hardware sets receiver's RXSTATUS to DataPending.
4. Receiver reads RXDATA.
5. Hardware sets receiver's RXSTATUS to NoDataPending.
6. Hardware sets sender's TXSTATUS to NoDataPending.

10.8.4 Disabling erase protection

The erase protection mechanism can be disabled to return a device to factory default settings on next reset.

The debugger can read the erase protection status in the register ERASEPROTECT.STATUS on page 441.

If ERASEPROTECT has been enabled, both the debugger and on-chip firmware must write the same non-zero 32-bit KEY value into their respective ERASEPROTECT.DISABLE registers to disable the erase protection. When both registers have been written with the same non-zero 32-bit KEY value, the device is automatically erased as described in Erase all on page 438. The access ports will be re-enabled on the next reset once the secure erase sequence has completed.

The write-once register ERASEPROTECT.LOCK on page 444 should be set to *Locked* as early as possible in the start-up sequence, preferably as soon as the on-chip firmware has determined it does not need to communicate with a debugger over the CTRL-AP mailbox interface. Once written, it will not be possible to remove the erase protection until the next reset.

10.8.5 Debugger registers

CTRL-AP has a set of registers that can only be accessed from the debugger over the SWD interface. These are not accessible from the CPU.

10.8.5.1 Debugger registers

Register overview

Register	Offset	Description
RESET	0x000	System reset request
ERASEALL	0x004	Perform a secure erase of the device, where flash, SRAM and UICR will be erased in sequence. The device will be returned to factory default settings upon next reset.

Register	Offset	Description
ERASEALLSTATUS	0x008	This is the status register for the ERASEALL operation.
APPROTECT.STATUS	0x00C	This is the status register for the UICR access port protection.
ERASEPROTECT.STATUS	0x018	This is the status register for the UICR ERASEPROTECT configuration.
ERASEPROTECT.DISABLE	0x01C	This register disables ERASEPROTECT and performs ERASEALL.
MAILBOX.TXDATA	0x020	Data sent from the debugger to the CPU.
MAILBOX.TXSTATUS	0x024	This register shows a status that indicates if data sent from the debugger to the CPU has been read.
MAILBOX.RXDATA	0x028	Data sent from the CPU to the debugger.
MAILBOX.RXSTATUS	0x02C	This register shows a status that indicates if data sent from the CPU to the debugger has been read.
IDR	0x0FC	CTRL-AP Identification Register, IDR

10.8.5.1.1 RESET

Address offset: 0x000

System reset request

This register is automatically deactivated during an ERASEALL operation.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID				Value																		Description									
A	RW	RESET																								System reset request and status									
				NoReset				0																		Write to release reset Reading '0' means reset is not active									
				Reset				1																		Write to hold reset Reading '1' means reset is active									

10.8.5.1.2 ERASEALL

Address offset: 0x004

Perform a secure erase of the device, where flash, SRAM and UICR will be erased in sequence. The device will be returned to factory default settings upon next reset.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID				Value																		Description									
A	W	ERASEALL																								Return device to factory default settings									
				NoOperation				0																		No operation									
				Erase				1																		Erase flash, SRAM, and UICR in sequence									

10.8.5.1.3 ERASEALLSTATUS

Address offset: 0x008

This is the status register for the ERASEALL operation.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	ERASEALLSTATUS			Status bit for the ERASEALL operation
			Ready	0	ERASEALL is ready
			Busy	1	ERASEALL is busy (on-going)

10.8.5.1.4 APPROTECT.STATUS

Address offset: 0x00C

This is the status register for the UICR access port protection.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	APPROTECT			Status bit for access port protection
					Note: The reset value is auto read from the APPROTECT register in UICR.
			Enabled	0	APPROTECT is enabled
			Disabled	1	APPROTECT is disabled
B	R	SECUREAPPROTECT			Status bit for secure access port protection
					Note: The reset value is auto read from the SECUREAPPROTECT register in UICR.
			Enabled	0	SECUREAPPROTECT is enabled
			Disabled	1	SECUREAPPROTECT is disabled

10.8.5.1.5 ERASEPROTECT.STATUS

Address offset: 0x018

This is the status register for the UICR ERASEPROTECT configuration.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	PALL			Status bit for erase protection
					Note: The reset value is auto read from the ERASEPROTECT register in UICR.
			Enabled	0	ERASEPROTECT is enabled
			Disabled	1	ERASEPROTECT is not enabled and ERASEALL can be performed

10.8.5.1.6 ERASEPROTECT.DISABLE

Address offset: 0x01C

This register disables ERASEPROTECT and performs ERASEALL.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW1	KEY			The ERASEALL sequence will be initiated if value of the KEY fields are non-zero and the KEY fields match on both the CPU and debugger sides.

10.8.5.1.7 MAILBOX.TXDATA

Address offset: 0x020

Data sent from the debugger to the CPU.

Writing to this register will automatically set a DataPending value in the TXSTATUS register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	Data			Data sent from debugger

10.8.5.1.8 MAILBOX.TXSTATUS

Address offset: 0x024

This register shows a status that indicates if data sent from the debugger to the CPU has been read.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	Status			Status of register DATA
			NoDataPending	0	No data pending in register TXDATA
			DataPending	1	Data pending in register TXDATA

10.8.5.1.9 MAILBOX.RXDATA

Address offset: 0x028

Data sent from the CPU to the debugger.

Reading from this register will automatically set a NoDataPending value in the RXSTATUS register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	Data			Data sent from CPU

10.8.5.1.10 MAILBOX.RXSTATUS

Address offset: 0x02C

This register shows a status that indicates if data sent from the CPU to the debugger has been read.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	Status			Status of register DATA
			NoDataPending	0	No data pending in register RXDATA
			DataPending	1	Data pending in register RXDATA

10.8.5.1.11 IDR

Address offset: 0x0FC

CTRL-AP Identification Register, IDR

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				E E E E D D D D C C C C C C C B B B B B A A A A A A A A
Reset 0x12880000				**0 0 0 1 0 0 1 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	APID			AP Identification
B	R	CLASS			Access Port (AP) class
			NotDefined	0x0	No defined class
			MEMAP	0x8	Memory Access Port
C	R	JEP106ID			JEDEC JEP106 identity code
D	R	JEP106CONT			JEDEC JEP106 continuation code
E	R	REVISION			Revision

10.8.6 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
CTRL_AP_PERI	0x50006000	HF	S	NA	No	CTRL-AP-PERI

Register overview

Register	Offset	TZ	Description
MAILBOX.RXDATA	0x400		Data sent from the debugger to the CPU.
MAILBOX.RXSTATUS	0x404		This register shows a status that indicates if data sent from the debugger to the CPU has been read.
MAILBOX.TXDATA	0x480		Data sent from the CPU to the debugger.
MAILBOX.TXSTATUS	0x484		This register shows a status that indicates if the data sent from the CPU to the debugger has been read.
ERASEPROTECT.LOCK	0x500		This register locks the ERASEPROTECT.DISABLE register from being written until next reset.
ERASEPROTECT.DISABLE	0x504		This register disables the ERASEPROTECT register and performs an ERASEALL operation.

10.8.6.1 MAILBOX.RXDATA

Address offset: 0x400

Data sent from the debugger to the CPU.

Reading from this register will automatically set a NoDataPending value in the RXSTATUS register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	RXDATA																																	
				Data received from debugger																															

10.8.6.2 MAILBOX.RXSTATUS

Address offset: 0x404

This register shows a status that indicates if data sent from the debugger to the CPU has been read.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	RXSTATUS																																	
			NoDataPending	0																															
			DataPending	1																															

10.8.6.3 MAILBOX.TXDATA

Address offset: 0x480

Data sent from the CPU to the debugger.

Writing to this register will automatically set a DataPending value in the TXSTATUS register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	TXDATA																																	
				Data sent to debugger																															

10.8.6.4 MAILBOX.TXSTATUS

Address offset: 0x484

This register shows a status that indicates if the data sent from the CPU to the debugger has been read.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	TXSTATUS																																	
			NoDataPending	0																															
			DataPending	1																															

10.8.6.5 ERASEPROTECT.LOCK

Address offset: 0x500

This register locks the ERASEPROTECT.DISABLE register from being written until next reset.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW1	LOCK																																	
			Unlocked	0																															
			Locked	1																															

			Lock ERASEPROTECT.DISABLE register from being written until next reset
	Unlocked	0	Register ERASEPROTECT.DISABLE is writeable
	Locked	1	Register ERASEPROTECT.DISABLE is read-only

10.8.6.6 ERASEPROTECT.DISABLE

Address offset: 0x504

This register disables the ERASEPROTECT register and performs an ERASEALL operation.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW1	KEY																																	

			The ERASEALL sequence is initiated if the value of the KEY fields are non-zero and the KEY fields match on both the CPU and debugger sides.

10.9 TAD - Trace and debug control

Configuration interface for trace and debug

Please refer to the Trace section for more information about how to configure the trace and debug interface.

Note: Although there are PSEL registers for the trace port, each function can only be mapped to a single pin due to pin speed requirements. Setting the PIN field to anything else will not have any effect. See Pin assignment chapter for more information

10.9.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
TAD	0xE0080000	HF	S	NA	No	Trace and debug control

Register overview

Register	Offset	TZ	Description
TASKS_CLOCKSTART	0x000		Start all trace and debug clocks.
TASKS_CLOCKSTOP	0x004		Stop all trace and debug clocks.
ENABLE	0x500		Enable debug domain and aquire selected GPIOs
PSEL.TRACECLK	0x504		Pin configuration for TRACECLK
PSEL.TRACEDATA0	0x508		Pin configuration for TRACEDATA[0]
PSEL.TRACEDATA1	0x50C		Pin configuration for TRACEDATA[1]
PSEL.TRACEDATA2	0x510		Pin configuration for TRACEDATA[2]
PSEL.TRACEDATA3	0x514		Pin configuration for TRACEDATA[3]
TRACEPORTSPEED	0x518		Clocking options for the Trace Port debug interface Reset behavior is the same as debug components This register is retained.

10.9.1.1 TASKS_CLOCKSTART

Address offset: 0x000

Start all trace and debug clocks.

Note: The TASKS_CLOCKSTART task asserts the CTRL/STAT.CSYSPWRUPACK and CTRL/STAT.CDBGPWRUPACK registers high (see *Arm CoreSight SoC-400 Technical Reference Manual, revision r3p2*).

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID				Value																		Description									
A	W	TASKS_CLOCKSTART																								Start all trace and debug clocks.									
																										Note: The TASKS_CLOCKSTART task asserts the CTRL/STAT.CSYSPWRUPACK and CTRL/STAT.CDBGPWRUPACK registers high (see *Arm CoreSight SoC-400 Technical Reference Manual, revision r3p2*).									
				Trigger				1																		Trigger task									

10.9.1.2 TASKS_CLOCKSTOP

Address offset: 0x004

Stop all trace and debug clocks.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID				Value																		Description									
A	W	TASKS_CLOCKSTOP																								Stop all trace and debug clocks.									
				Trigger				1																		Trigger task									

10.9.1.3 ENABLE

Address offset: 0x500

Enable debug domain and aquire selected GPIOs

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ENABLE			
			DISABLED	0	Disable debug domain and release selected GPIOs
			ENABLED	1	Enable debug domain and aquire selected GPIOs

10.9.1.4 PSEL.TRACECLK

Address offset: 0x504

Pin configuration for TRACECLK

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	PIN			Pin number
			Traceclk	21	TRACECLK pin
					Note: Only this pin is valid
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

10.9.1.5 PSEL.TRACEDATA0

Address offset: 0x508

Pin configuration for TRACEDATA[0]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	PIN			Pin number
			Tracedata0	22	TRACEDATA0 pin
					Note: Only this pin is valid
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

10.9.1.6 PSEL.TRACEDATA1

Address offset: 0x50C

Pin configuration for TRACEDATA[1]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	PIN			Pin number
			Tracedata1	23	TRACEDATA1 pin
					Note: Only this pin is valid
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

10.9.1.7 PSEL.TRACEDATA2

Address offset: 0x510

Pin configuration for TRACEDATA[2]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	PIN			Pin number
			Tracedata2	24	TRACEDATA2 pin
					Note: Only this pin is valid
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

10.9.1.8 PSEL.TRACEDATA3

Address offset: 0x514

Pin configuration for TRACEDATA[3]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	PIN			Pin number
			Tracedata3	25	TRACEDATA3 pin
					Note: Only this pin is valid
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

10.9.1.9 TRACEPORTSPEED (Retained)

Address offset: 0x518

Clocking options for the Trace Port debug interface

Reset behavior is the same as debug components

This register is retained.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	TRACEPORTSPEED																																	
			32MHz	0																															
			16MHz	1																															
			8MHz	2																															
			4MHz	3																															

Description
Speed of Trace Port clock. Note that the TRACECLK pin output will be divided again by two from the Trace Port clock.
Trace Port clock is: 32MHz
Trace Port clock is: 16MHz
Trace Port clock is: 8MHz
Trace Port clock is: 4MHz

11 Hardware and layout

The following sections describe nRF9161 hardware and layout specifications.

11.1 Pin assignments

This section describes the pin assignment and the pin functions of the nRF9161.

The device provides flexibility when it comes to routing and configuration of the GPIO pins. However, for some pins there are recommendations on pin usage and configuration. See following table for more information about this.

11.1.1 LGA pin assignments

The pin assignment table and figure describe the assignments.

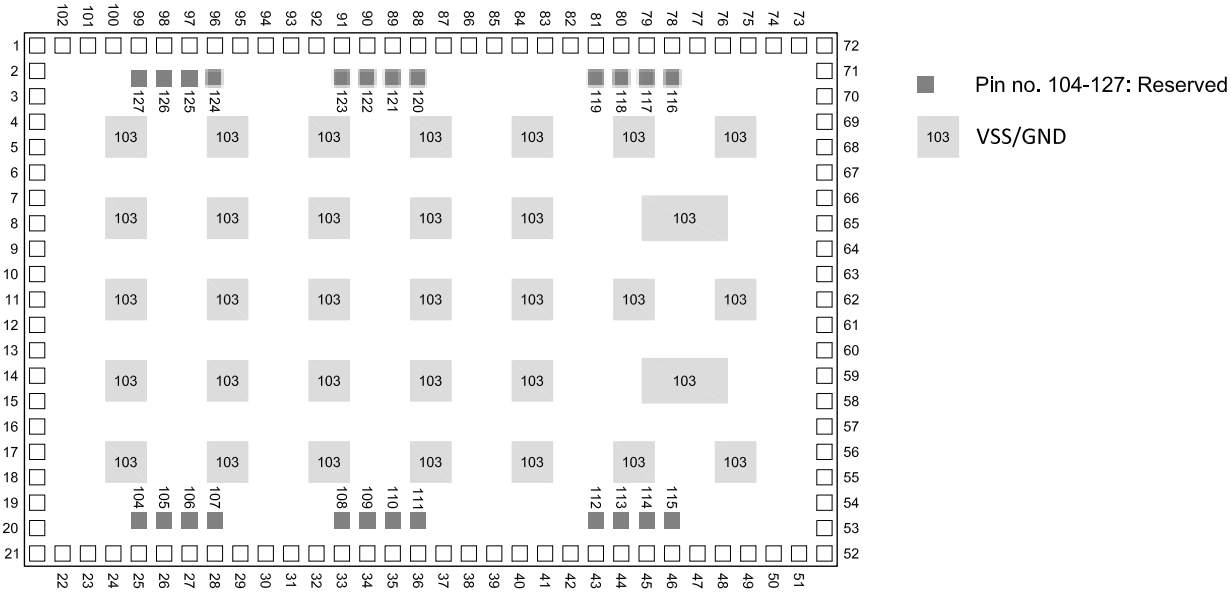


Figure 120: LGA pin assignments, top view

Pin no	Pin name	Function	Description
1	GND	Power	Ground
2	P0.05	Digital I/O (SoC)	General purpose I/O
3	P0.06	Digital I/O (SoC)	General purpose I/O
4	P0.07	Digital I/O (SoC)	General purpose I/O
5	GND	Power	Ground
6	GND	Power	Ground
7	GND	Power	Ground
8	GND	Power	Ground
9	GND	Power	Ground
10	RES		Do not connect/reserved for future use
11	GND	Power	Ground
12	VDD_GPIO	Power	GPIO power supply input and logic level
13	DEC0	Power	Power supply decoupling. Reserved for Nordic use.
14	GND	Power	Ground

Pin no	Pin name	Function	Description
15	P0.08	Digital I/O (SoC)	General purpose I/O
16	P0.09	Digital I/O (SoC)	General purpose I/O
17	GND	Power	Ground
18	P0.10	Digital I/O (SoC)	General purpose I/O
19	P0.11	Digital I/O (SoC)	General purpose I/O
20	P0.12	Digital I/O (SoC)	General purpose I/O
21	GND	Power	Ground
22	VDD2	Power	Supply voltage input
23	P0.13	Digital I/O (SoC)	General purpose I/O.
	AIN0	Analog input	Analog input.
24	P0.14	Digital I/O (SoC)	General purpose I/O.
	AIN1	Analog input	Analog input.
25	P0.15	Digital I/O (SoC)	General purpose I/O.
	AIN2	Analog input	Analog input.
26	P0.16	Digital I/O (SoC)	General purpose I/O.
	AIN3	Analog input	Analog input.
27	GND	Power	Ground
28	P0.17	Digital I/O (SoC)	General purpose I/O.
	AIN4	Analog input	Analog input.
29	P0.18	Digital I/O (SoC)	General purpose I/O.
	AIN5	Analog input	Analog input.
30	P0.19	Digital I/O (SoC)	General purpose I/O.
	AIN6	Analog input	Analog input.
31	GND	Power	Ground
32	nRESET	Digital I/O (SoC)	SoC reset pin [26,27]
33	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
34	SWDIO	Digital I/O	Serial wire debug I/O for debug and programming
35	P0.20	Digital I/O (SoC)	General purpose I/O.
	AIN7	Analog input	Analog input.
36	GND	Power	Ground
37	P0.21	Digital I/O (SoC)	General purpose I/O.
	TRACECLK	Trace clock	Trace buffer clock (optional).
38	P0.22	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA[0]	Trace data	Trace buffer TRACEDATA[0] (optional).
39	P0.23	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA[1]	Trace data	Trace buffer TRACEDATA[1] (optional).
40	P0.24	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA[2]	Trace data	Trace buffer TRACEDATA[2] (optional).
41	GND	Power	Ground
42	P0.25	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA[3]	Trace data	Trace buffer TRACEDATA[3] (optional).
43	SIM_RST	Digital I/O (SoC)	SIM reset
44	GND	Power	Ground
45	SIM_DET	Digital I/O (SoC)	SIM detect
			Not used. Must be left floating.

[26] External pull-up not allowed.

[27] For implementations that require the ERASEALL functionality, enable access to the nRESET pin. See Erase all on page 438 for more information.

Pin no	Pin name	Function	Description
46	SIM_CLK	Digital I/O (SoC)	SIM clock
47	GND	Power	Ground
48	SIM_IO	Digital I/O (SoC)	SIM data
49	SIM_1V8	Power	SIM 1.8 V power supply output
50	GND	Power	Ground
51	RES		Do not connect/reserved for future use
52	GND	Power	Ground
53	MAGPIO2	Digital I/O (SoC)	1.8 V general purpose I/O
54	MAGPIO1	Digital I/O (SoC)	1.8 V general purpose I/O
55	MAGPIO0	Digital I/O (SoC)	1.8 V general purpose I/O
56	GND	Power	Ground
57	VIO	Power	MIPI RFFE control interface
58	SCLK	Digital I/O (SoC)	MIPI RFFE control interface
59	SDATA	Digital I/O (SoC)	MIPI RFFE control interface
60	GND	Power	Ground
61	ANT	RF	Single-ended 50 Ω LTE antenna pin
62	GND	Power	Ground
63	GND	Power	Ground
64	AUX	RF	Single-ended 50 Ω ANT loop-back pin
65	GND	Power	Ground
66	GND	Power	Ground
67	GPS	RF	Single-ended 50 Ω GPS input pin
68	GND	Power	Ground
69	GND	Power	Ground
70	RES		Do not connect/reserved for future use
71	RES		Do not connect/reserved for future use
72	GND	Power	Ground
73	RES		Do not connect/reserved for future use
74	GND	Power	Ground
75	GND	Power	Ground
76	GND	Power	Ground
77	GND	Power	Ground
78	GND	Power	Ground
79	GND	Power	Ground
80	GND	Power	Ground
81	GND	Power	Ground
82	GND	Power	Ground
83	P0.26	Digital I/O (SoC)	General purpose I/O
84	P0.27	Digital I/O (SoC)	General purpose I/O
85	GND	Power	Ground
86	P0.28	Digital I/O (SoC)	General purpose I/O
87	P0.29	Digital I/O (SoC)	General purpose I/O
88	P0.30	Digital I/O (SoC)	General purpose I/O
89	P0.31	Digital I/O (SoC)	General purpose I/O
90	GND	Power	Ground
91	COEX2	Digital I/O (SoC)	Coexistence interface
92	COEX1	Digital I/O (SoC)	Coexistence interface
93	COEX0	Digital I/O (SoC)	Coexistence interface
94	GND	Power	Ground
95	P0.00	Digital I/O (SoC)	General purpose I/O
96	P0.01	Digital I/O (SoC)	General purpose I/O
97	P0.02	Digital I/O (SoC)	General purpose I/O
98	GND	Power	Ground

Pin no	Pin name	Function	Description
99	P0.03	Digital I/O (SoC)	General purpose I/O
100	P0.04	Digital I/O (SoC)	General purpose I/O
101	ENABLE		Enable for the SiP internal regulator for the nRF91 SoC. **Note:** The nRF91 will not start until this pin is enabled.
102	VDD1	Power	Supply voltage
103	GND	Power	Ground
104-127	RES		Do not connect/reserved for future use

Table 55: LGA pin assignments

11.2 Mechanical specifications

The mechanical specifications show the package dimensions in millimeters.

11.2.1 16.0 x 10.5 mm package

Dimensions in millimeters for the nRF9161 LGA 16.0 x 10.5 x 1.04 mm package.

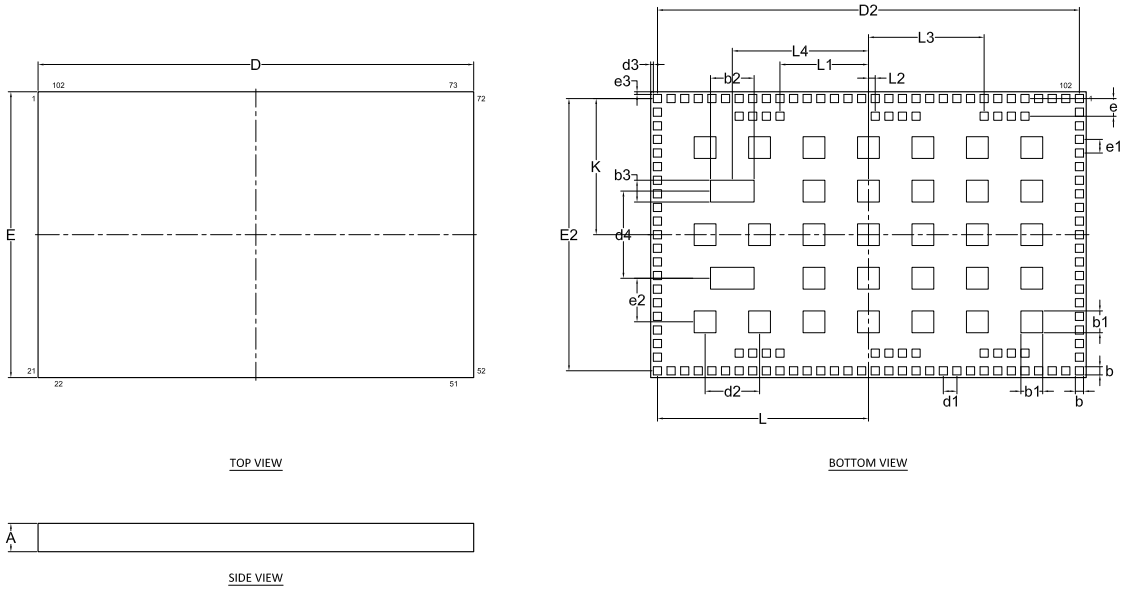


Figure 121: LGA 16.0 x 10.5 mm package

	A	b	b1	D	E	e	d1	e1	D2	E2	b2	d2	e2	b3	d3	e3	d4	K	L	L1	L2	L3	L4
Min.	0.98			15.90	10.40																		
Nom.	1.04	0.30	0.80	16.00	10.50	0.65	0.50	0.50	15.50	10.00	1.60	2.00	1.60	0.80	0.10	0.10	3.20	5.00	7.75	3.25	0.25	4.25	5.00
Max.	1.10			16.10	10.60																		

Table 56: LGA dimensions in millimeters

11.3 Reference circuitry

To ensure good RF performance when designing PCBs, using the PCB layouts and component values provided by Nordic Semiconductor is highly recommended .

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from the product page at www.nordicsemi.com.

This section contains reference circuitry showing the components to support the design of on-chip features.

Note: This is not a complete list of configurations, but all required circuitry is shown for further configurations.

11.3.1 nRF9161 reference design

Circuit configuration schematic for the nRF9161 SiP.

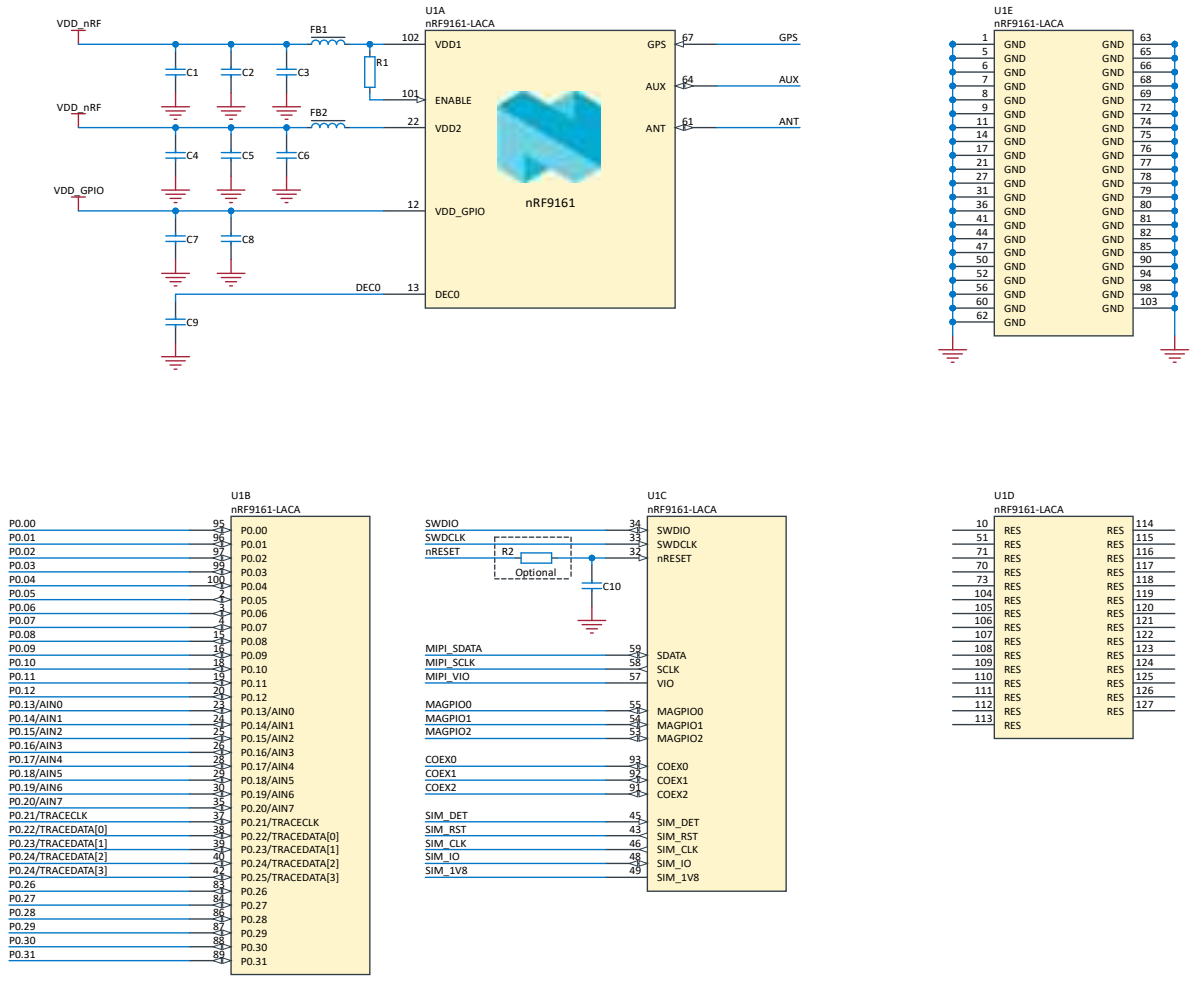


Figure 122: nRF9161 reference design

For Bill of Materials (BOM), PCB layout and thermal design, see the *nRF9161 Hardware Design Guidelines*.

11.4 Reflow conditions

The recommended reflow profile is JEDEC J-STD-020D. The maximum amount of reflows is three.

11.5 Shelf and floor life

If floor life is exceeded, see Shelf Life of Dry Packed Integrated Circuits for shelf and floor life and recommended baking (drying of parts) requirements.

12 Operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Battery input voltage	Including voltage drop, ripple and spikes.	3.0	3.7	5.5	V
VDD_GPIO	GPIO input voltage		1.7		3.6	V
$GPIO_H$	GPIO high level voltage				VDD_GPIO	V
$MAGPIO_H$	MAGPIO high level voltage	Supply from internal LDO	1.7	1.8	1.9	V
VIO	VIO high level voltage	Supply from internal LDO	1.7	1.8	1.9	V
TA	Operating temperature		-40	25	85	°C
COEX	COEX high level voltage				VDD_GPIO	V
SIMIF	SIMIF output high level voltage	Supply from internal LDO	1.7	1.8	1.9	V

Table 57: Operating conditions

Note: There can be excessive leakage at VDD and/or VDD_GPIO if any of these supply voltages is outside its range given in the table above.

Note: It is not recommended to use high voltage, high drive GPIO outputs ($V_{OH,HDH}$ and $V_{OH,HDL}$) with high frequency, high capacitance loads unless needed, as this may increase noise level and affect radio receiver performance. High drive/high load should especially be avoided on GPIO pins close to the radio front end.

12.1 VDD_GPIO considerations

VDD_GPIO is the supply to the general purpose I/O.

The following restrictions should be taken into considerations:

- VDD_GPIO should be applied after VDD has been supplied
- VDD_GPIO should be removed before removing VDD
- If VDD is supplied and VDD_GPIO is grounded, an extra current consumption can be generated on VDD
- If ENABLE is low, VDD_GPIO should also be low

13 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

	Note	Min.	Max.	Unit
Supply voltages				
VDD		-0.3	5.5[28]	V
VDD_GPIO		-0.3	3.9	V
SIM_1V8		1.65	1.95	V
VSS			0	V
I/O pin voltage				
$V_{I/O}$, VDD_GPIO ≤ 3.6 V		-0.3	VDD_GPIO + 0.3	V
$V_{I/O}$, VDD_GPIO > 3.6 V		-0.3	3.9	V
Radio				
ANT antenna input level			10	dBm
GPS antenna input level	LNA turned on, max gain		-15	dBm
RF port ruggedness	Maximum deviation from 50 Ω without damaging the module		10:1	VSWR
Environmental (LGA package)				
Storage temperature		-40	95	°C
MSL	Moisture Sensitivity Level		3	
ESD HBM	Human Body Model		1.5	kV
ESD HBM Class	Human Body Model Class		1C	
ESD CDM	Charged Device Model		250	V
Flash memory				
Endurance		10 000		Write/erase cycles
Retention		10 years at 85°C		
ATEX compliance				
Ci			83	µF
Li			9.0	µH
Ui			5.0	V
Ii			600	mA

No internal voltage boost converters

Table 58: Absolute maximum ratings

[28] ATEX compliance requires a maximum of 5.0 V.

14 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

14.1 SiP marking

The nRF9161 package is marked as shown in the following figure.

n	R	F	9	1	6	1		<L	A>	<C	A>		<H>	<P>
								<Y	Y>	<W	W>	<L	L>	

Figure 123: SiP package marking

14.2 Box labels

The following figures show the box labels used for the nRF9161.

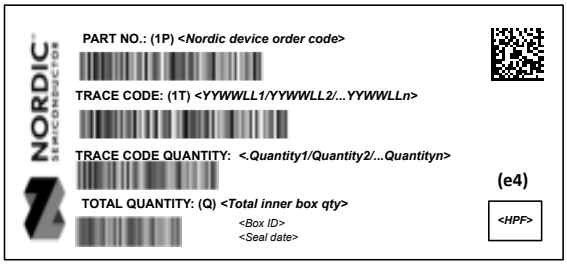


Figure 124: Inner box label

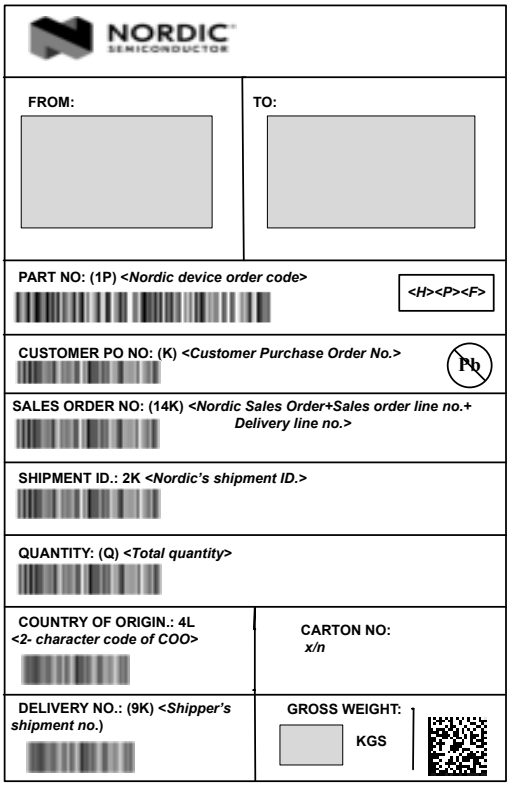


Figure 125: Outer box label

14.3 Order code

The following are the order codes and definitions for the nRF9161.

n	R	F	9	1	6	1	-	<L	A>	<C	A>	-	<H>	<P>	<F>	-	<C	C>

Figure 126: Order code

Abbreviation	Definition and implemented codes
N91/nRF91	nRF91 Series product
61	Part code
<LA>	Package variant code
<CA>	Function variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 59: Abbreviations

14.4 Code ranges and values

The nRF9161 code ranges and values are defined here.

<PP>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
LA	LGA	16.00 x 10.50	127	0.50

Table 60: Package variant codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 61: Hardware version codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 62: Production configuration codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 63: Production version codes

<YY>	Description
[23 . . 99]	Production year: 2023 to 2099

Table 64: Year codes

<WW>	Description
[01 . . 52]	Week of production

Table 65: Week codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 66: Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel

Table 67: Container codes

14.5 Ordering options

The nRF9161 SiP ordering codes and minimum ordering quantity are described in the following table.

Order code	Minimum ordering quantity (MOQ)	Comment
nRF9161-LACA-R	2500	
nRF9161-LACA-R7	100	

Table 68: nRF9161 order codes

15 Regulatory information

The nRF9161 undergoes regulatory certifications, ensuring both regional compliances and compatibility with the LTE 3GPP specification.

15.1 Certified bands

The following table shows the FCC and ISED certified Cat-M1 bands for nRF9161.

Band	FCC certification	ISED certification
Band 2	Yes	Yes
Band 4	Yes	Yes
Band 5	Yes	Yes
Band 8	Yes	Yes
Band 12	Yes	Yes
Band 13	Yes	Yes
Band 25	Yes	Yes
Band 26	Yes	No
Band 66	Yes	Yes
Band 85	Yes	Yes

Table 69: FCC and ISED certified bands

The following table shows the FCC and ISED certified Cat-NB1 and Cat-NB1 bands for nRF9161.

Band	FCC certification	ISED certification
Band 2	Yes	Yes
Band 4	Yes	Yes
Band 5	Yes	Yes
Band 8	Yes	Yes
Band 12	Yes	Yes
Band 13	Yes	Yes
Band 17	Yes	Yes
Band 25	Yes	Yes
Band 26	Yes	No
Band 66	Yes	Yes
Band 85	Yes	Yes

Table 70: FCC and ISED certified CAT-NB1/NB2 bands

15.2 Supported FCC/ISED rules

The nRF9161 module has been certified to comply with FCC and ISED rules.

The nRF9161 SiP has been certified to comply with the following FCC rules.

- 47 CFR Part 22
- 47 CFR Part 24
- 47 CFR Part 27
- 47 CFR Part 90
- 47 CFR Part 2.1091

The nRF9161 SiP has been certified to comply with the following ISED rules.

- RSS-132 Issue 4
- RSS-130 Issue 2
- RSS-139 Issue 4
- RSS-133 Issue 6

A host manufacturer who integrates the nRF9161 SiP to a host device, can apply the certifications to the host device, except for FCC Part 15 Subpart B which must be retested.

The host manufacturer can use nRF9161's FCC ID if the device meets the conditions of the FCC certificate. Normally, the conditions are the following:

- A minimum of 20 cm distance from the human body.
- No colocation with other transmitters. Typically, this condition needs to be reviewed by the FCC lab.
- Antenna gain below the requirements.

15.3 FCC/ISED regulatory notices

FCC/ISED regulatory notices cover modification and interference statements, wireless and FCC Class B digital device notices, permitted antennas and labeling requirements.

Modification statement

Nordic Semiconductor has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Nordic Semiconductor n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference statement

This device complies with Part 15 of the FCC Rules and Industry Canada's licence-exempt RSS standards. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Wireless notice

This equipment complies with FCC and ISED radiation exposure limits set forth for an uncontrolled environment. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Cet appareil est conforme aux limites d'exposition aux rayonnements de l'ISDE pour un environnement non contrôlé. L'antenne doit être installée de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

Permitted antenna

This radio transmitter has been approved by FCC and ISED to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Band	Max gain for SMD antenna type
Band 2	9.0 dBi
Band 4	6.0 dBi
Band 5	7.1 dBi
Band 8	7.32 dBi
Band 12	6.6 dBi
Band 13	6.9 dBi
Band 17 (Cat-NB1/NB2)	6.6 dBi
Band 25	9.0 dBi
Band 26	7.0 dBi
Band 66	6.0 dBi
Band 85	6.6 dBi

Le présent émetteur radio a été approuvé par ISDE pour fonctionner avec les types d'antenne énumérés ci dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Bande	Gain maximal pour CMS antenne
Bande 2	9.0 dBi
Bande 4	6.0 dBi
Bande 5	7.1 dBi
Band 8	7.32 dBi
Bande 12	6.6 dBi
Bande 13	6.9 dBi
Bande 17 (Cat-NB1/NB2)	6.6 dBi
Bande 25	9.0 dBi
Bande 26	7.0 dBi
Bande 66	6.0 dBi
Bande 85	6.6 dBi

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna

- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

CAN ICES-3 (B)/NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

Labeling requirements for the host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as shown in the following examples:

Contains FCC ID: 2ANPO00NRF9161
Contains IC: 24529-NRF9161

L'équipement hôte doit être correctement étiqueté pour identifier les modules dans l'équipement. L'étiquette de certification du module doit être clairement visible en tout temps lorsqu'il est installé dans l'hôte, l'équipement hôte doit être étiqueté pour afficher le FCC ID et IC du module, précédé des mots "Contient le module émetteur", ou le mot "Contient", ou un libellé similaire exprimant la même signification, comme suit:

Contient FCC ID: 2ANPO00NRF9161
Contient IC: 24529-NRF9161

15.4 RF exposure considerations

The nRF9161 has been tested and certified as a mobile device for use of a minimum of 20 cm distance from the human body with no colocation with other transmitters. If the device is to be used closer than 20 cm from the human body and/or with other transmiters simultaneously, the host product manufacturer is required to perform additional evaluation, testing, or testing and Class 2 permissive change. It is required to take responsibility of the module through a change in the FCC ID (new application). The host product manufacturer must also inform the end user about RF Exposure conditions.

15.5 Host device manufacturer responsibility

The nRF9161 device is only authorized for the rules listed in Supported FCC/ISED rules on page 462.
The host device manufacturer is responsible for compliance to any other FCC rules that apply to the host device not covered by the nRF9161 grant of certification. It is mandatory for the host device manufacturer to assure the final device’s compliance with FCC Part 15 Subpart B even if certification has been granted to nRF9161.

15.6 Antenna interface

The nRF9161 module has a single-ended 50 Ω antenna port where the antenna solution shall be connected. nRF9161 is evaluated with a 50 Ω antenna load. To ensure good overall RF performance,

antenna impedance and the characteristic impedance of the transmission line (i.e. cable) connecting the antenna and antenna port must be 50 Ω. Impedance mismatch may lead to performance degradation. Maximum antenna VSWR 2:1 is recommended but VSWR 3:1 can still be accepted in the final device. Respective minimum return loss values are 9.5 dB and 6.0 dB.

The length of the transmission line from the antenna to the nRF9161 antenna port should be kept as short as possible to minimize losses, as this loss is directly deteriorating the module's transmitted and received power. Additionally, low-loss matching circuit between the antenna and the nRF9161 antenna port is recommended to minimize loss caused by antenna and PCB routing mismatch. Reserving space from device manufacturer's application board for matching components (e.g. π-circuit) is recommended. This is because, for example, catalog antennas are typically tuned on reference board and differences to device mechanics may impact antenna impedance. It is also possible that device mechanics change during the development phase of the final device, and these modifications may impact antenna performance. Matching components can be used to compensate the impact of mechanics change to antenna impedance, and thus it may not be mandatory to modify the antenna itself.

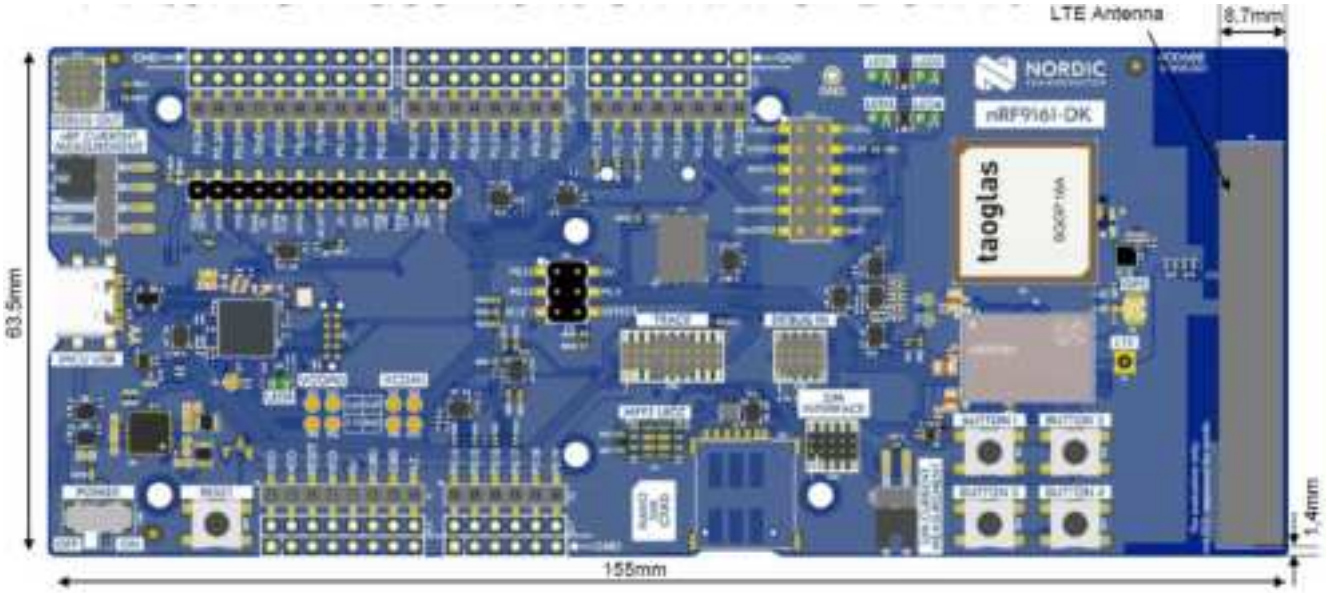
The nRF9161 module has an internal ESD circuit in the antenna port, but additional ESD components at device manufacturer's application board may be used. The design of the ESD circuit shall be such that the impact on RF frequencies is negligible

Note: ESD filtering may be necessary for some active components that can be used at antenna path. Such components can be, for example, RF switches and antenna tuners. For further ESD requirements, see the RF switch and antenna tuner datasheets.

15.7 Antenna port test connector

To run conductive RF tests, a test connector nearby the nRF9161 antenna port in the RF transmission line is needed. The 50 Ω impedance requirement applies also to the test connector, and VSWR and insertion loss should be minimal. Regardless of whether the nRF9161 antenna port is connected to an actual antenna or test equipment, the load at the nRF9161 antenna should remain as close to 50 Ω as possible.

For a test connector, microwave coaxial switch connectors (for example, Murata MM8130-2600) are a good choice for this purpose. For conductive tests, a test cable is plugged in which connects the nRF9161 antenna port to the test equipment instead of the antenna. When the test cable is plugged off, the nRF9161 antenna port is connected to the antenna for real use case or radiated testing. The layout for the connector must be carefully designed to fulfil the 50 Ω requirement. For detailed guidance on this, see the coaxial switch connectors datasheets.



15.8 Reference Circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

The information on layout of trace design is confidential; host manufacturer shall need to contact module's grantee to obtain this information.

This module can only be used when installed in a host device that follows the required instructions for use of the layout of trace design. Any deviation(s) from the defined parameters of the layout of trace design, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the layout of trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.
Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

16 Legal notices

By using this documentation you agree to our terms and conditions of use. Nordic Semiconductor may change these terms and conditions at any time without notice.

Liability disclaimer

Nordic Semiconductor ASA reserves the right to make changes without further notice to the product to improve reliability, function, or design. Nordic Semiconductor ASA does not assume any liability arising out of the application or use of any product or circuits described herein.

Nordic Semiconductor ASA does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. If there are any discrepancies, ambiguities or conflicts in Nordic Semiconductor's documentation, the Product Specification prevails.

Nordic Semiconductor ASA reserves the right to make corrections, enhancements, and other changes to this document without notice.

Customer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that anticipate dangerous consequences of failures, monitor failures and their consequences, and lessen the likelihood of failures that might cause harm, and to take appropriate remedial actions.

Nordic Semiconductor ASA assumes no liability for applications assistance or the design of customers' products. Customers are solely responsible for the design, validation, and testing of its applications as well as for compliance with all legal, regulatory, and safety-related requirements concerning its applications.

Nordic Semiconductor ASA's products are not designed for use in life-critical medical equipment, support appliances, devices, or systems where malfunction of Nordic Semiconductor ASA's products can reasonably be expected to result in personal injury. Customer may not use any Nordic Semiconductor ASA's products in life-critical medical equipment unless adequate design and operating safeguards by customer's authorized officers have been made. Customer agrees that prior to using or distributing any life-critical medical equipment that include Nordic Semiconductor ASA's products, customer will thoroughly test such systems and the functionality of such products as used in such systems.

Customer will fully indemnify Nordic Semiconductor ASA and its representatives against any damages, costs, losses, and/or liabilities arising out of customer's non-compliance with this section.

RoHS and REACH statement

Refer to www.nordicsemi.com for complete hazardous substance reports, material composition reports, and latest version of Nordic's RoHS and REACH statements.

Trademarks

All trademarks, service marks, trade names, product names, and logos appearing in this documentation are the property of their respective owners.

Copyright notice


QUALITY SYSTEM CERTIFICATION
DNV
ISO 9001