

AME-4221SR (HU)

schematic modify history

DATE	Version	Change List	PCBA version	PCB version
2021/09/23	A00	First Draft	970DQB0AD00N128 A	490DQB00 A

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970DQB0AD00N128

01 History

Rev
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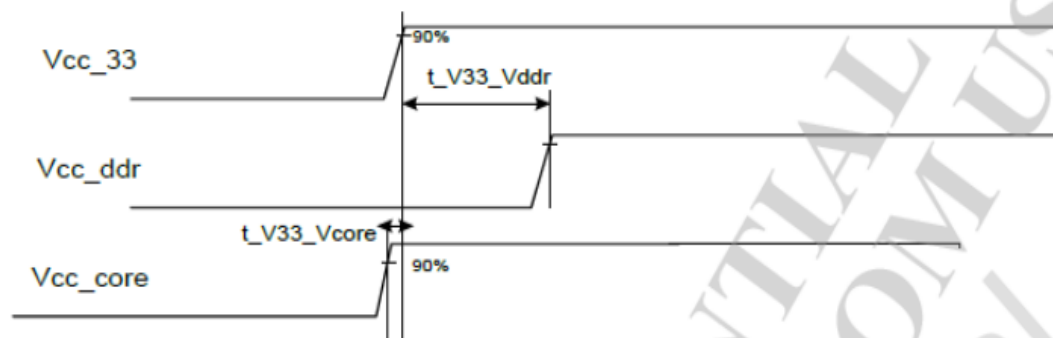
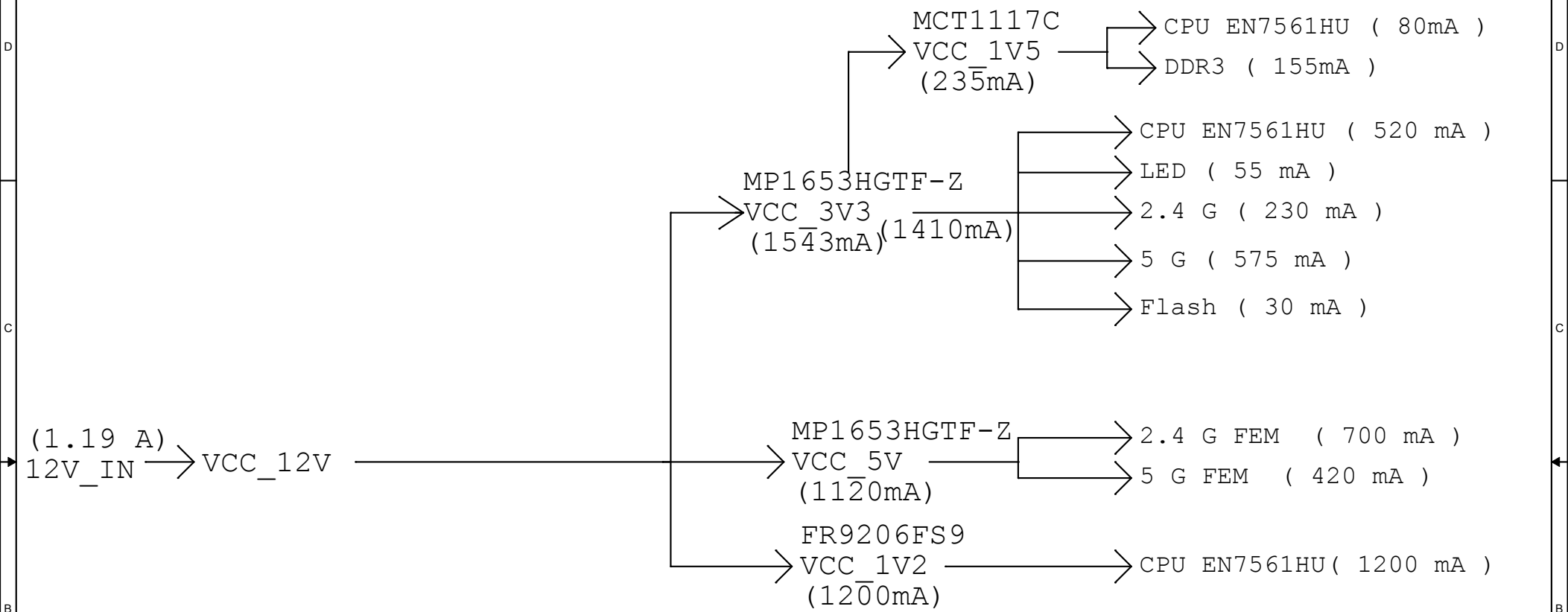


Figure 5-4 Power-on Sequence

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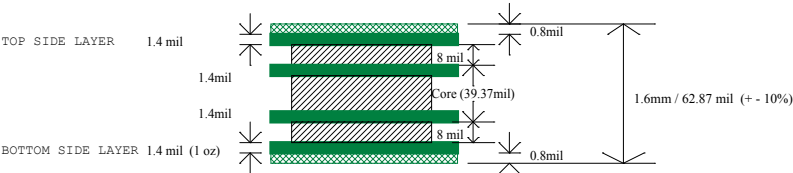
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03 Power Tree

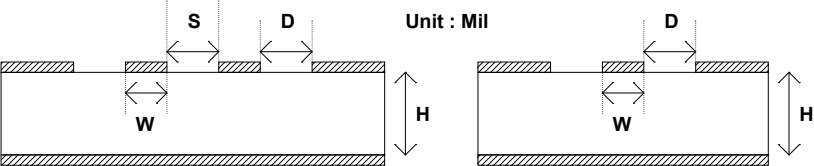
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PCB Structure for 4 layers FR4 PCB



Layout trace guide



Differential Pair

Impedance	W	S	D	H	Line Mark
100 Ohm GPHY/PCIE	6mil	5.5mil	9.25mil		

Single End

50 Ohm RF	12mil		9mil		

GPHY - Layout Guidelines & Notes

- Trace impedance: 100 Ohm differential impedance.
- Match trace length of differential pairs, 20 mils max within a pair, and 500 mils max between pairs. Do NOT try to match trace lengths by adding extra length or serpentes. It is more important to maintain a pair as differential traces.
- Max distance from SoC to Magnetics = 4.0 inches

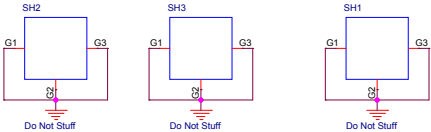
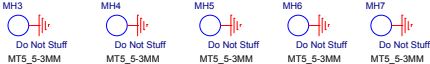
PCle - Layout Guidelines & Notes

- Trace impedance: 100 Ohm differential impedance.
- No matching needed pair-to-pair.
- Match trace length of differential pairs, 5 mils max within a pair. Symmetric routing for each pair (within a pair)
- At least 2X pair to pair spacing than intra-pair spacing.

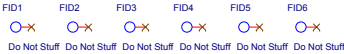
USB2.0 - Layout Guidelines & Notes

- Route DM/DP pair with 90 ohms differential impedance.
- The P and N traces are length matched, with max differential skew, within 20mils
- Differential trace length must be less than 5 inches
- No more than 2 vias per trace, prefer zero.

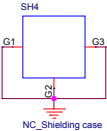
Heatsink hole



FID



2021/09/22: Add SH4 for CPU4DDR bot reserved



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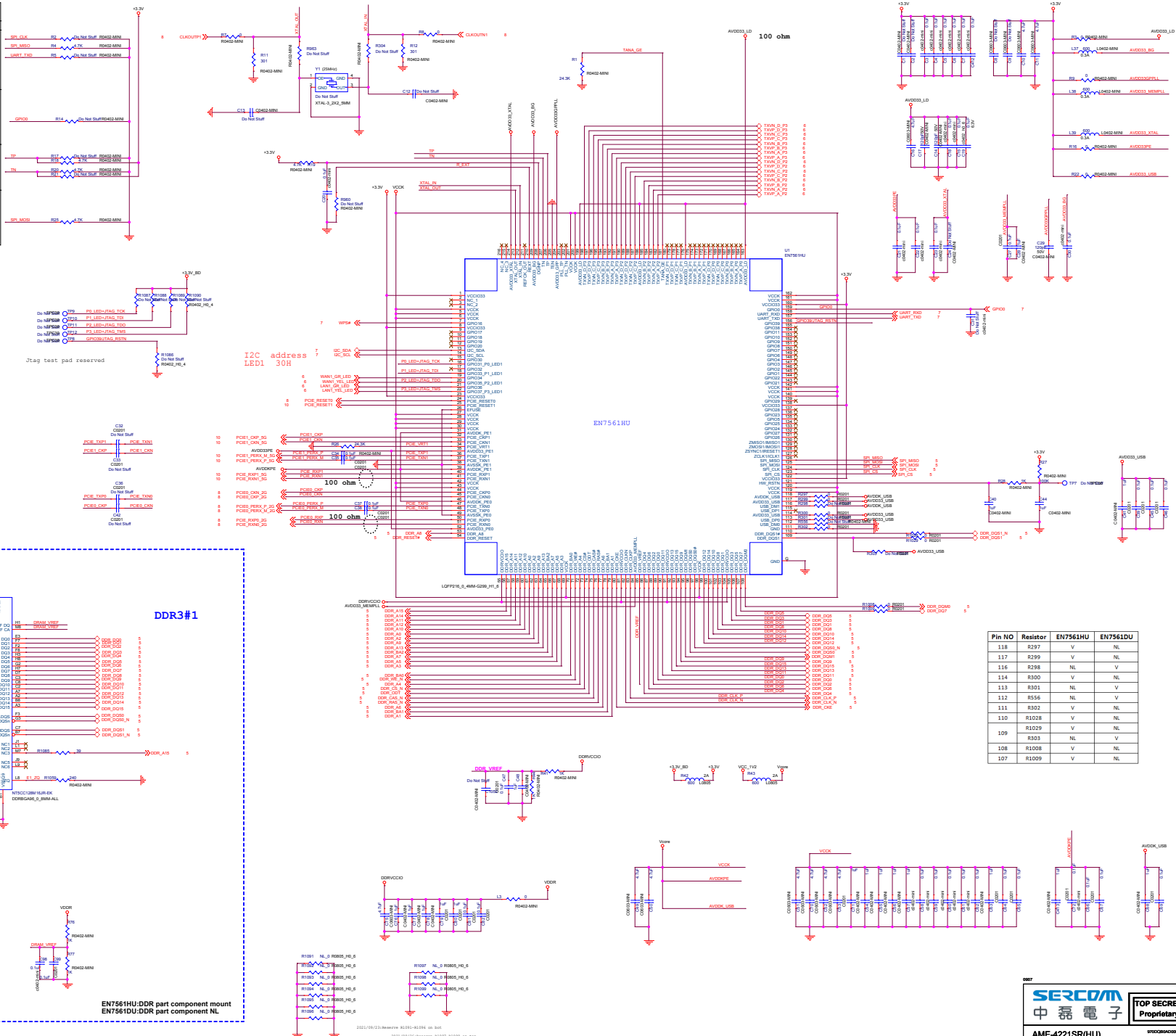
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04 Appendix

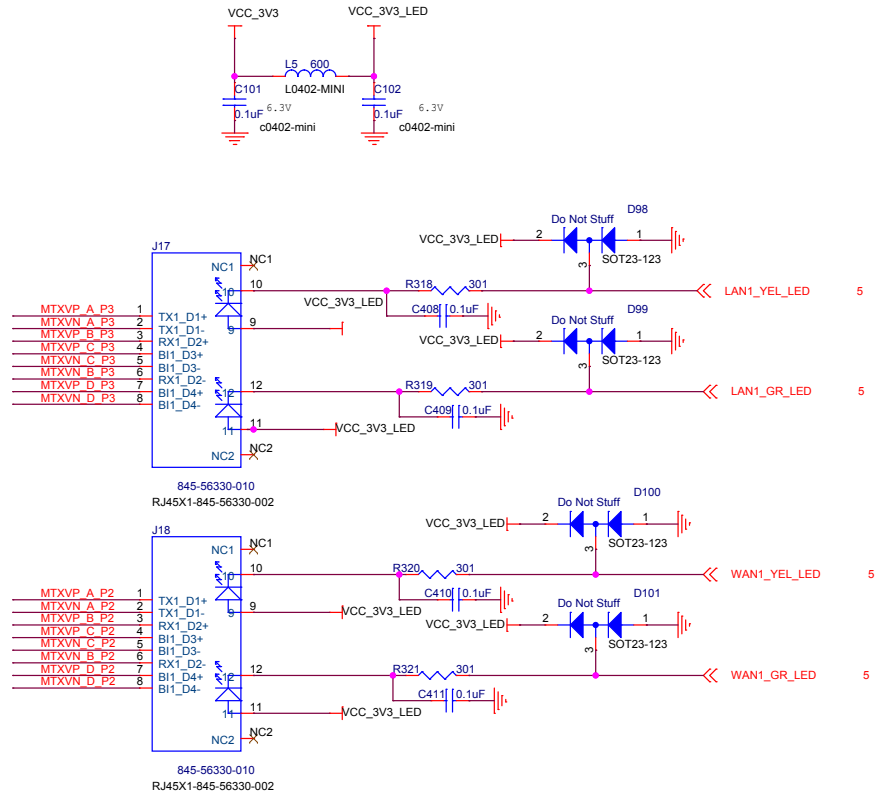
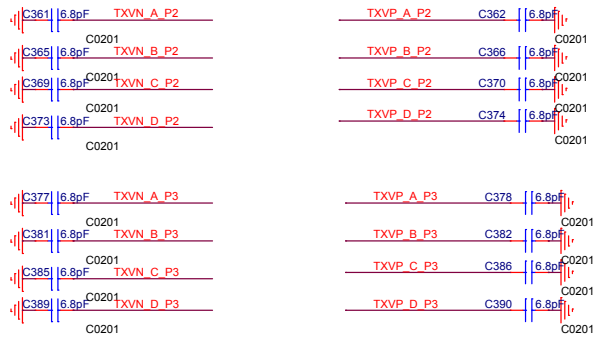
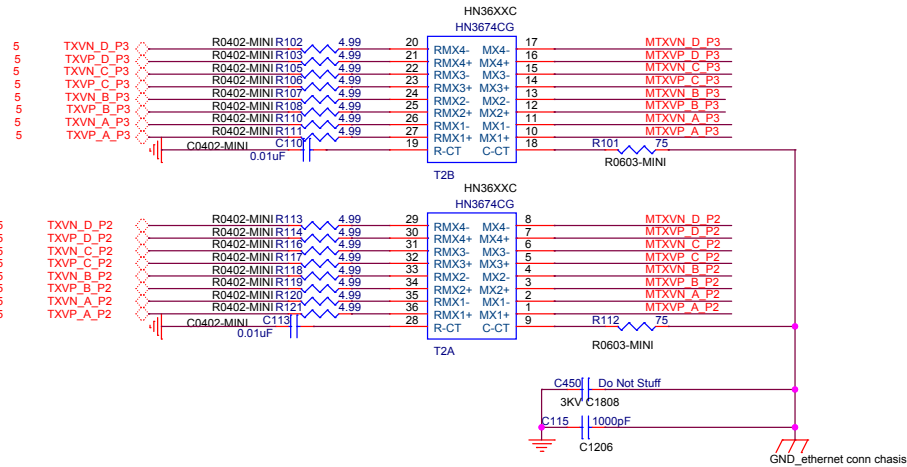
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Pin Name	Description	Default
SPIN_CLK, SPI_MISO, UART_TXD	SPIN[®]C mode selection: *0000: SPI NAND dummy preprogram controller ECC(SPI0(Boot from internal rom)) *0001: SPI NAND dummy preprogram controller ECC(SPI0(Boot from internal rom)) *0010: SPI NAND dummy preprogram Flash ECC(SPI0(Boot from internal rom)) *0100: SPI NAND dummy preprogram Flash ECC(SPI0(Boot from Flash)) *0101: SPI NOR 48 mode(SPI0(Boot from Flash)) *0110: SPI NOR 38 mode(SPI0(Boot from Flash)) *1010: NFD mode (boot from internal rom). FW definition trap bit 0 *1011: NFD mode (boot from internal rom). FW definition trap bit 1	*Tb11
GPIO0	boot from flash : *boot from flash *Tb1: disable (boot from internal ROM) *Tb1: enable (boot from SPI(NAND flash))	*Tb1
TP_TN	Input clock mode selection: *000: 25MHz XTAL mode *001: 25MHz single clock input mode(from XO) *010: 25MHz Differential clock input mode *011: 40MHz Differential clock input mode	
SPI_MOSI	CPU endian format *Tb1: little-endian *Tb1: big-endian	*Tb1



Pin NO	Resistor	EN7561HU	EN7561DU
118	R297	V	NL
117	R299	V	NL
116	R298	NL	V
114	R300	V	NL
113	R301	NL	V
112	R556	NL	V
111	R302	V	NL
110	R1028	V	NL
109	R1029	V	NL
	R303	NL	V
108	R1008	V	NL
107	R1009	V	NL



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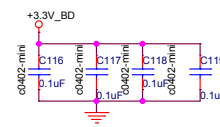
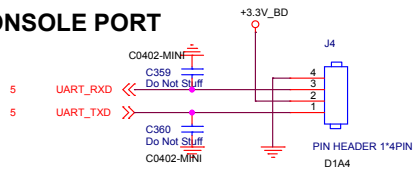
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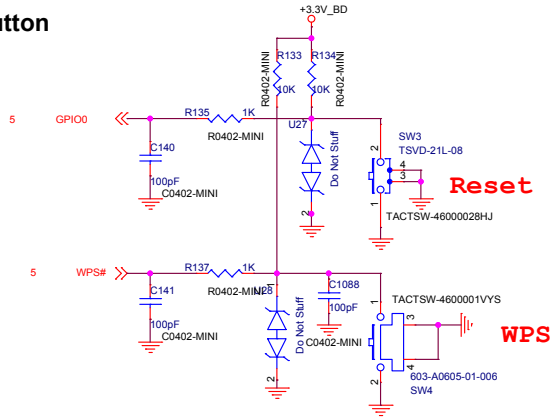
06 GE Port

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CONSOLE PORT



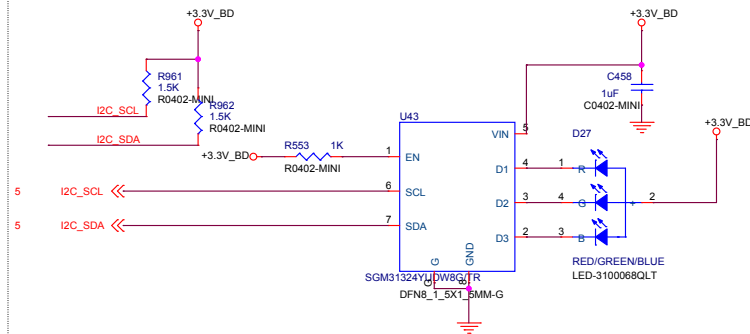
Button



2021/09/06:Change WPS button to 4600001VYS 3.3mm for layout
2021/09/15:Swap WPS pin1/2 for layout
2021/09/17:Add C1088 close SW4

LED1

ADDRESS 30H



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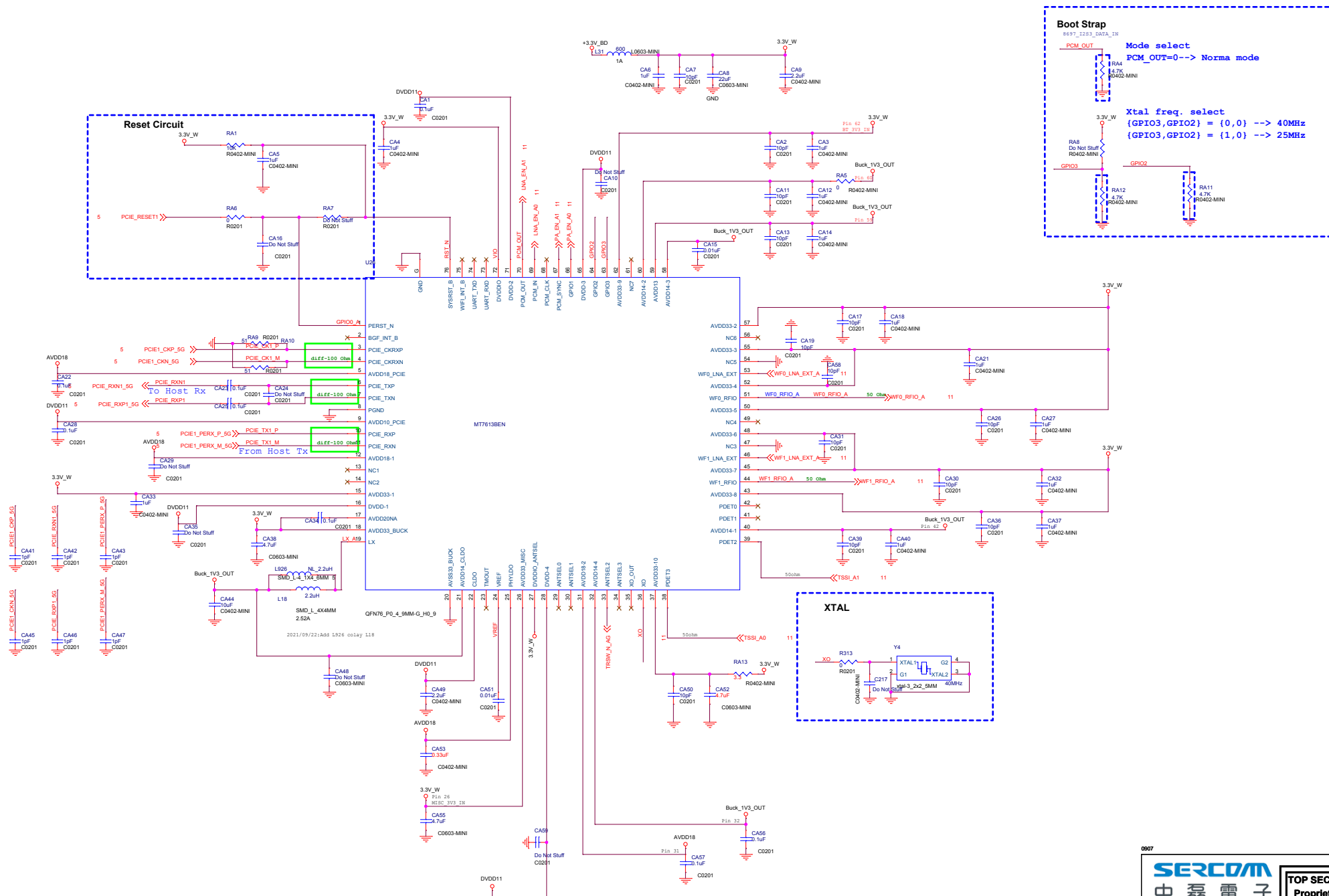
07 LED, Console, USB, Button

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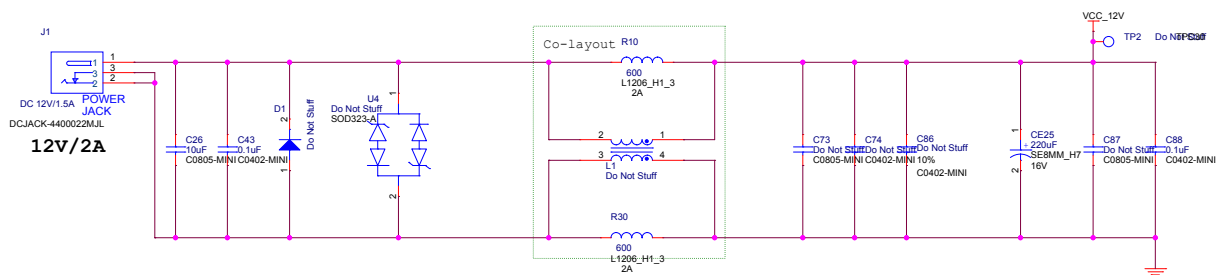
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WFO



System DC Power

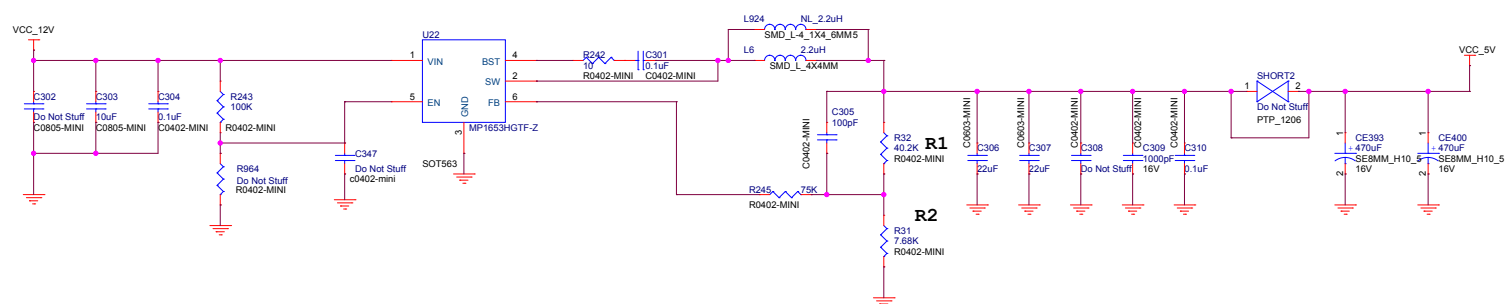


5V/3A FEM

$$V_{out} = 0.805 * (1 + R_1/R_2) = 0.805 * (1 + 40.2/7.68) = 5.02$$

$$L = 2.2 \mu H$$

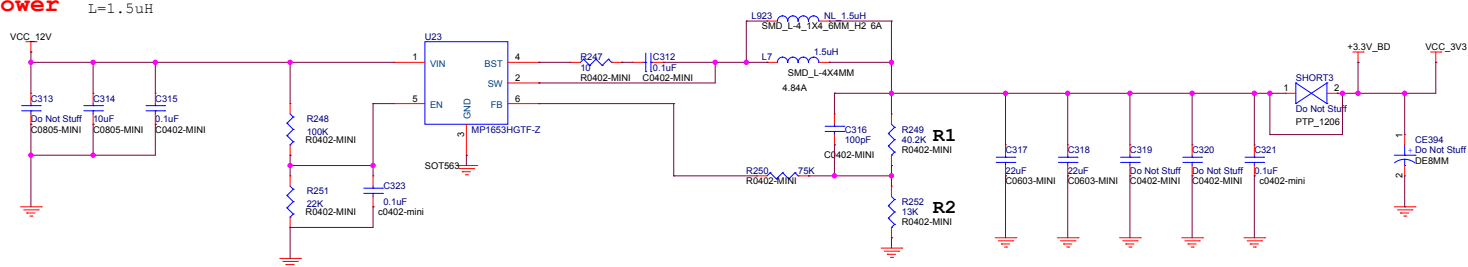
2021/09/18:Add L924 colav L6



3V3/3A Power

$$V_{out} = 0.805 * (1 + R_1/R_2) = 0.805 * (1 + 40.2/13) = 3.294$$
$$L = 1.5\mu H$$

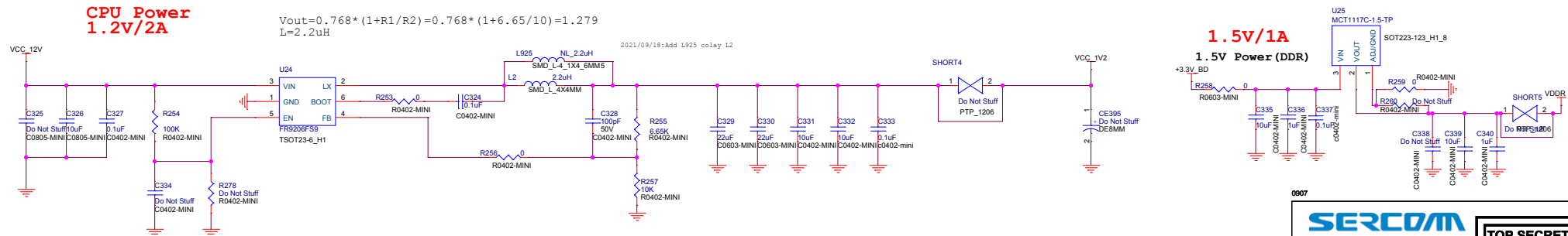
2021/09/18: Add L923 colav L7



CPU Power
1.2V/2A

$$V_{out} = 0.768 * (1 + R_1/R_2) = 0.768 * (1 + 6.65/10) = 1.279$$
$$L = 2.2 \mu H$$

2021/09/18:Add L925 colav L2



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12 Power Circuit

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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