HCM511S Hardware Design

Short-Range Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-12-26	Luke FU/Vic CHENG	Creation of the document
1.0.0	2023-12-26	Luke FU/Vic CHENG	Preliminary

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines HCM511S in QuecOpen® solution and describes its hardware interfaces and air interfaces, which are connected with your applications. The document provides a quick insight into interface specifications, RF performance, electrical and mechanical specifications, as well as other related information of the module.

Hereby, Quectel Wireless Solutions Co., Ltd. declares that the radio equipment type HCM511S is in compliance with Directive 2014/53/EU.
The full text of the EU declaration of conformity is available at the following internet address: http://www.quectel.com/support/technical.htm

The device could be used with a separation distance of 20cm to the human body.

Disposal of old electrical appliances

The European directive 2012/19/EU on Waste Electrical and Electronic Equipment (WEEE), requires that old household electrical appliances must not be disposed of in the normal unsorted municipal waste stream. Old appliances must be collected separately in order to optimize the recovery and recycling of the materials they contain, and reduce the impact on human health and the environment.
The crossed out "wheeled bin" symbol on the product reminds you of your obligation, that when you dispose of the appliance, it must be separately collected.
Consumers should contact their local authority or retailer for information concerning the correct disposal of their old appliance.

2 Product Overview

HCM511S is a low-power and high performance MCU Bluetooth module supporting BLE 5.4 protocol. The module, integrating a highly configurable radio transceiver, supports multiple interfaces such as USART, EUART, SWD, JTAG, I2C, IADC and PDM for various applications.

It is an SMD module with compact packaging. The general features of the module are as follows:

- Embedded 32-bit ARM Cortex-M33 processor with a frequency of up to 76.8 MHz
- 32 KB RAM memory and 352 KB/ 512 KB Flash
- Flexible and efficient power management
- Support for Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- Support for OTA (Over-The-Air Upgrade)
- Support for secondary development

Table 1: Basic Information

HCM511S	
Packaging type	LCC
Pin counts	24
Dimensions	(16.6 +0.3/-0.15) mm × (11.2 +0.3/-0.15) mm × (2.1 ±0.2) mm
Weight	Approx. 0.57g

2.1. Key Features

Table 2: Key Features

Basic Information	
Protocol and Standard	• Bluetooth protocol: BLE 5.4 • All hardware components are fully compliant with EU RoHS directive
Power Supply	**VBAT Power Supply:** • 1.71–3.8 V • Typ.: 3.3 V
Temperature Ranges	• Normal operating temperature [1]: -40 to +85 °C • Storage temperature: -45 to +95 °C
TE-B Kit	HCM511S-TE-B [2]
Antenna	
Antenna	• PCB antenna • 50 Ω characteristic impedance
Application Interface [3]	
Application Interfaces	USART, EUART, SWD, JTAG, I2C, IADC, PDM, GPIO

[1] Within the operating temperature range, the module's related performance meets Bluetooth specifications.
[2] Quectel supplies an evaluation board (HCM511S-TE-B) with accessories to develop and test the module. For more details, see ***document [1]***.
[3] For more details about the interfaces, see ***Chapter 3.3*** and ***Chapter 3.4***.

3 Application Interfaces

3.1. Pin Assignment

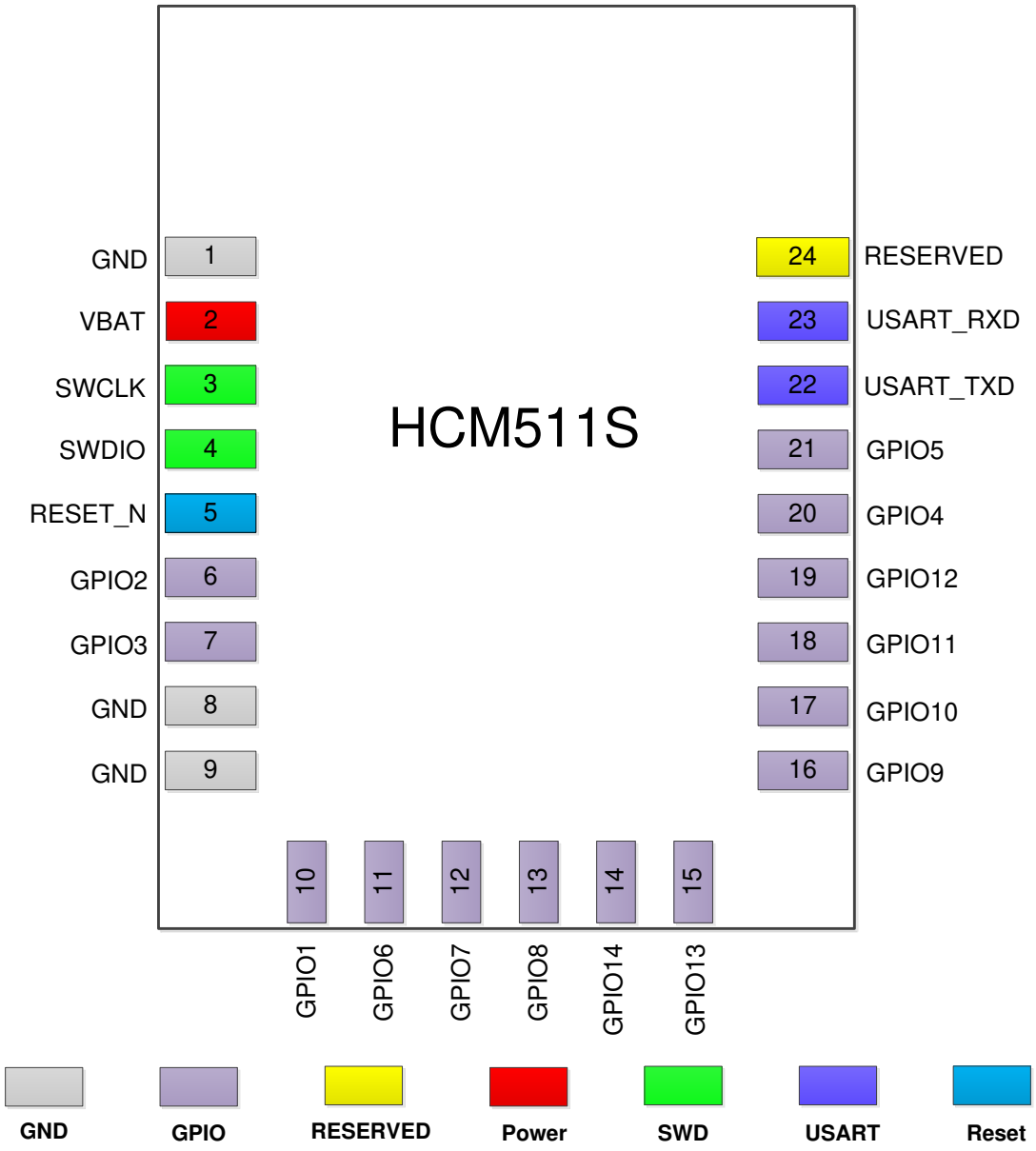


Figure 1: Pin Assignment (Top View)

NOTE

1. Keep the RESERVED and all unused pins unconnected.
2. All GND pins should be connected to ground.
3. The module supports 1 USART, 1 SWD and 14 GPIO interfaces by default. In the case of multiplexing, it supports interfaces including EUART, SWD, JTAG, I2C, IADC and PDM. For more details, see ***Chapter 3.3*** and ***Chapter 3.4***.

3.2. Pin Description

Table 3: Parameter Description

Parameter	Description
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input

DC characteristics include power domain and rated current.

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
VBAT	2	PI	Power supply for the module	Vmax = 3.8 V Vmin = 1.71 V Vnom = 3.3 V	It must be provided with sufficient current more than 0.3 A.
GND	1, 8, 9				
Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
RESET_N	5	DI	Reset the module	VBAT	Hardware reset. Internally pulled up to VBAT. Active low.

USART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
USART_TXD	22	DO	USART transmit	VBAT	Used for debugging.
USART_RXD	23	DI	USART receive		
SWD Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
SWDIO	4	DIO	Serial wire debugging input/output	VBAT	Used for program downloading. Enabled after power-up. With a built-in pull-up.
SWCLK	3	DI	Serial wire debugging clock		Used for program downloading. Enabled after power-up. With a built-in pull-down.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
GPIO1	10	DIO	General-purpose input/output	VBAT	Support asynchronous external pin interrupting.
GPIO2	6	DIO	General-purpose input/output		
GPIO3	7	DIO	General-purpose input/output		
GPIO4	20	DIO	General-purpose input/output		
GPIO5	21	DIO	General-purpose input/output		
GPIO6	11	DIO	General-purpose input/output		
GPIO7	12	DIO	General-purpose input/output		
GPIO8	13	DIO	General-purpose input/output		
GPIO9	16	DIO	General-purpose input/output		
GPIO10	17	DIO	General-purpose input/output		

GPIO11	18	DIO	General-purpose input/output
GPIO12	19	DIO	General-purpose input/output
GPIO13	15	DIO	General-purpose input/output
GPIO14	14	DIO	General-purpose input/output
Reserved Pin			
Pin Name	**Pin No.**		**Comment**
RESERVED	24		Keep it unconnected

3.3. GPIO Multiplexing

The module provides 14 GPIO interfaces by default, and can support up to 18 GPIO interfaces in the case of multiplexing. Pins are defined as follows:

Table 5: GPIO Multiplexing (Digital Pins)

Multiplexing Function	GPIO Interface			
	SWCLK, SWDIO, GPIO1–5	GPIO6–8	USART_TXD, USART_RXD, GPIO9–12	GPIO13, GPIO14
CMU_CLKIN0	-	-	√	√
CMU_CLKOUT0	-	-	√	√
CMU_CLKOUT1	-	-	√	√
CMU_CLKOUT2	√	√	-	-
EUART0_CTS	√	√	√	√
EUART0_RTS	√	√	√	√
EUART0_RXD	√	√	√	√
EUART0_TXD	√	√	√	√
FRC_DCLK	-	-	√	√

FRC_DFRAME	-	-	√	√
FRC_DOUT	-	-	√	√
I2C0_SCL	√	√	√	√
I2C0_SDA	√	√	√	√
I2C1_SCL	-	-	√	√
I2C1_SDA	-	-	√	√
LETIMER0_OUT0	√	√	-	-
LETIMER0_OUT1	√	√	-	-
MODEM_ANT0	√	√	√	√
MODEM_ANT1	√	√	√	√
MODEM_ANT_ROLL_OVER	-	-	√	√
MODEM_ANT_RR0	-	-	√	√
MODEM_ANT_RR1	-	-	√	√
MODEM_ANT_RR2	-	-	√	√
MODEM_ANT_RR3	-	-	√	√
MODEM_ANT_RR4	-	-	√	√
MODEM_ANT_RR5	-	-	√	√
MODEM_ANT_SW_EN	-	-	√	√
MODEM_ANT_SW_US	-	-	√	√
MODEM_ANT_TRIG	-	-	√	√
MODEM_ANT_TRIG_STOP	-	-	√	√
MODEM_DCLK	√	√	-	-
MODEM_DIN	√	√	-	-
MODEM_DOUT	√	√	-	-
PDM_CLK	√	√	√	√
PDM_DATA0	√	√	√	√

PDM_DATA1	√	√	√	√
PRS_ASYNCH0	√	√	-	-
PRS_ASYNCH1	√	√	-	-
PRS_ASYNCH10	-	-	√	√
PRS_ASYNCH11	-	-	√	√
PRS_ASYNCH2	√	√	-	-
PRS_ASYNCH3	√	√	-	-
PRS_ASYNCH4	√	√	-	-
PRS_ASYNCH5	√	√	-	-
PRS_ASYNCH6	-	-	√	√
PRS_ASYNCH7	-	-	√	√
PRS_ASYNCH8	-	-	√	√
PRS_ASYNCH9	-	-	√	√
PRS_SYNCH0	√	√	√	√
PRS_SYNCH1	√	√	√	√
PRS_SYNCH2	√	√	√	√
PRS_SYNCH3	√	√	√	√
TIMER0_CC0	√	√	√	√
TIMER0_CC1	√	√	√	√
TIMER0_CC2	√	√	√	√
TIMER0_CDTI0	√	√	√	√
TIMER0_CDTI1	√	√	√	√
TIMER0_CDTI2	√	√	√	√
TIMER1_CC0	√	√	√	√
TIMER1_CC1	√	√	√	√
TIMER1_CC2	√	√	√	√

TIMER1_CDTI0	√	√	√	√
TIMER1_CDTI1	√	√	√	√
TIMER1_CDTI2	√	√	√	√
TIMER2_CC0	√	√	-	-
TIMER2_CC1	√	√	-	-
TIMER2_CC2	√	√	-	-
TIMER2_CDTI0	√	√	-	-
TIMER2_CDTI1	√	√	-	-
TIMER2_CDTI2	√	√	-	-
TIMER3_CC0	-	-	√	√
TIMER3_CC1	-	-	√	√
TIMER3_CC2	-	-	√	√
TIMER3_CDTI0	-	-	√	√
TIMER3_CDTI1	-	-	√	√
TIMER3_CDTI2	-	-	√	√
TIMER4_CC0	√	√	-	-
TIMER4_CC1	√	√	-	-
TIMER4_CC2	√	√	-	-
TIMER4_CDTI0	√	√	-	-
TIMER4_CDTI1	√	√	-	-
TIMER4_CDTI2	√	√	-	-
USART0_CLK	√	√	√	√
USART0_CS	√	√	√	√
USART0_CTS	√	√	√	√
USART0_RTS	√	√	√	√
USART0_RXD	√	√	√	√

USART0_TXD	√	√	√	√
USART1_CLK	√	√	-	-
USART1_CS	√	√	-	-
USART1_CTS	√	√	-	-
USART1_RTS	√	√	-	-
USART1_RXD	√	√	-	-
USART1_TXD	√	√	-	-

Table 6: GPIO Multiplexing (Analog Pins)

Multiplexing Function	Signal	SWCLK, SWDIO, GPIO1–5		GPIO6–8		USART_TXD, USART_RXD, GPIO9–12		GPIO13, GPIO14	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
IADC0	ana_neg	√	√	√	√	√	√	√	√
	ana_pos	√	√	√	√	√	√	√	√

NOTE

1. All GPIO pins are selectable as interrupts in EM0 and EM1 modes.
2. SWCLK, SWDIO, GPIO1–5, GPIO6–8 pins are selectable as interrupts down to EM2 and EM3 modes.
3. GPIO7, GPIO12, GPIO4, USART_TXD are available for wake-up function in EM4 mode.

3.4. Application Interfaces

3.4.1. USARTs

The module supports 1 UASRT by default. In the case of multiplexing, it provides up to 3 USARTs. See

Table 5 for more details. The USART supports communications with interfaces as below:

- UART (supporting full-duplex communication and hardware flow control)
- RS-485
- SPI
- MicroWire
- 3-wire
- ISO7816 Smart-Cards
- IrDA
- I2S

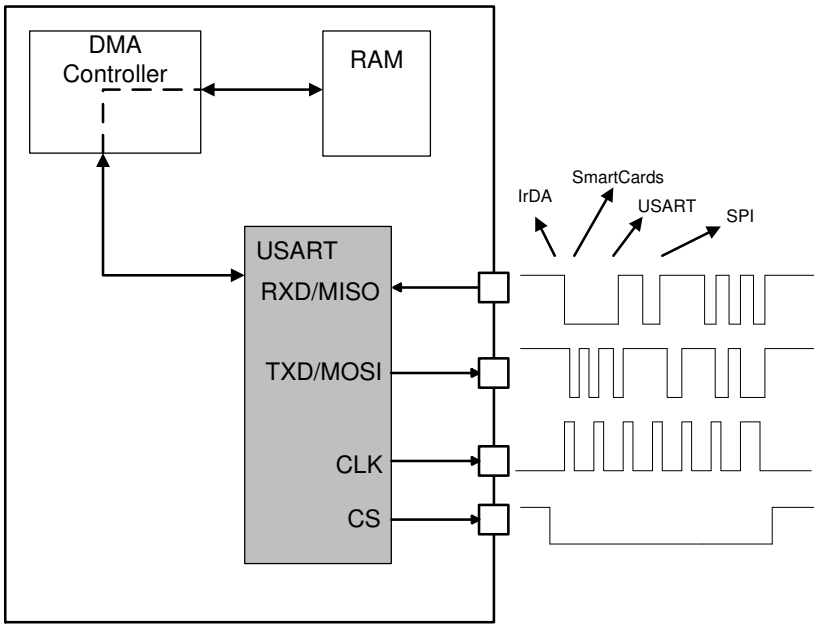


Figure 2: USART Functional Diagram

The USART operates in either asynchronous or synchronous mode:

- In synchronous mode, a separate clock signal generated by the bus master is transmitted with the data. Both the master and slave transmit data according to this clock. The synchronous communication mode is compatible with the SPI Bus standard.
- In asynchronous mode, no separate clock signal is transmitted with the data on the bus. The USART receiver thus has to determine where to sample the data on the bus from the actual data. To make it possible, additional synchronization bits are added to the data when operating in asynchronous mode.

Asynchronous or synchronous mode can be selected by configuring SYNC in register (USARTn_CTRL). The mode options with supported protocols are listed below:

Table 7: USART Synchronous/Asynchronous Mode

SYNC	Communication Mode	Protocol
0	Asynchronous	RS-232, RS-485 (with external driver), IrDA, ISO 7816
1	Synchronous	SPI, MicroWire, 3-wire

USART can be used as UART for AT command communication and data transmission. In such case, it supports self-configurable baud rate with default baud rate of 115200 bps. The USART connection between the module and MCU is illustrated below. (The dotted lines are optional as required.)

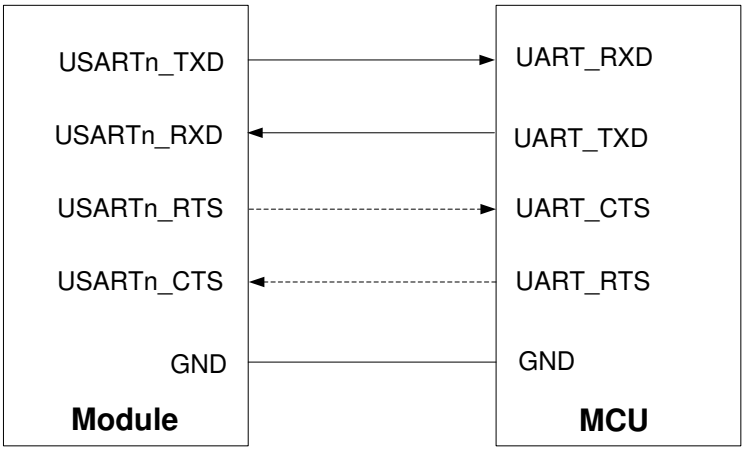


Figure 3: UART Connection

The following figure shows the USART connection between the module and the host when used as SPI.

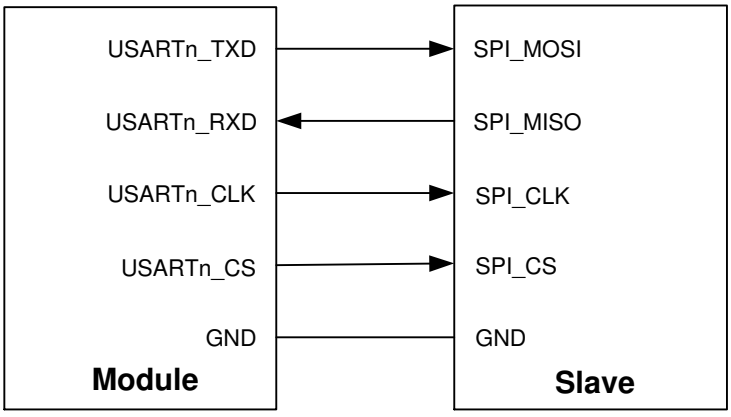


Figure 4: SPI Connection (Master Mode)

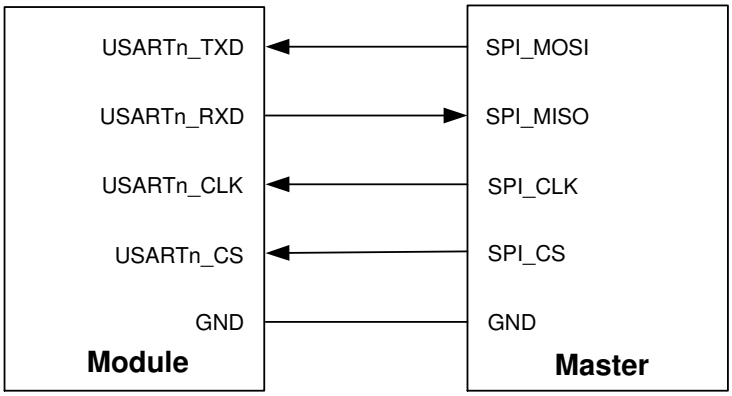


Figure 5: SPI Connection (Slave Mode)

NOTE

The output and input to the USART used as SPI are swapped when in slave mode, making the receiver take its input from USARTn_TXD (SPI_MOSI) and the transmitter drive USARTn_RXD (SPI_MISO).

The following figure shows the USART connection between the module and the host when used as I2S.

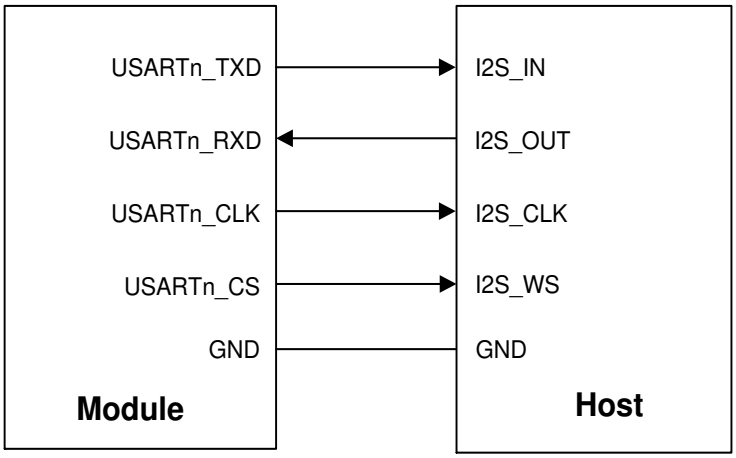


Figure 6: I2S Connection

The following figure shows the USART connection between the module and the host when used as RS-485.

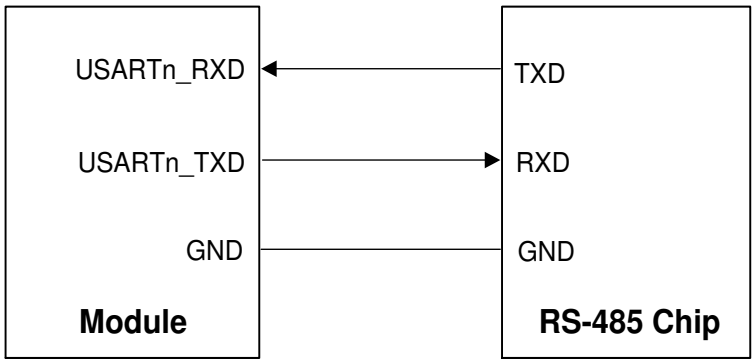


Figure 7: RS-485 Connection

3.4.2. EUART

In the case of multiplexing, the module supports 1 EUART for handling high-speed UART and IrDA communication, and see ***Table 6*** for more details. The EUART has a wide selection of operating modes, frame formats and baud rates. The multiprocessor mode allows the EUART to remain idle when not addressed. Triple buffering and DMA support makes high data-rate transmission possible with minimal CPU intervention. And it is possible to transmit and receive large frames while the MCU remains in EM1 sleep mode, which is supported by select I/O pins in lower-frequency operation under EM2 mode.

3.4.3. Debug Interface

The module supports a 2-pin SWD interface which can be multiplexed as a 4-pin JTAG interface. It also supports ETM for data/instruction tracing, and a Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages. The pin definitions of SWD interface are shown in the table below.

Table 8: Pin Definition of SWD Interface

Pin Name	Pin No.	I/O	Description	Comment
SWDIO	4	DIO	Serial wire debugging input/output	Used for program downloading. Enabled after power-up. With a built-in pull-up.
SWCLK	3	DI	Serial wire debugging clock	Used for program downloading. Enabled after power-up. With a built-in pull-down.

The SWD interface supports online program downloading and the common connection of SWD interface is shown below.

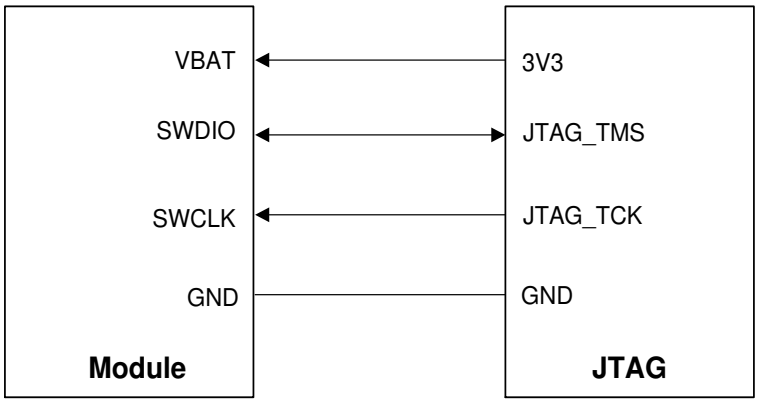


Figure 8: SWD Interface Connection

In the case of multiplexing, the module supports JTAG interface. The pin definitions of JTAG interface are shown in the table below.

Table 9: Pin Definition of JTAG Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
SWDIO	4	JTAG_TMS	DIO	JTAG test mode select	Enabled after power-up. With a built-in pull-up.
SWCLK	3	JTAG_TCK	DI	JTAG test clock	Enabled after power-up. With a built-in pull-down
GPIO2	6	JTAG_TDO	DO	JTAG test data output	Enabled after power-up. Remain in high-Z state until the first valid JTAG command is received.
GPIO3	7	JTAG_TDI	DI	JTAG test data input	Enabled after power-up. Remain in high-Z state until the first valid JTAG command is received. Once enabled, the pin has a built-in pull-up.

The JTAG interface supports debugging and program downloading and the common connection of JTAG interface is shown below.

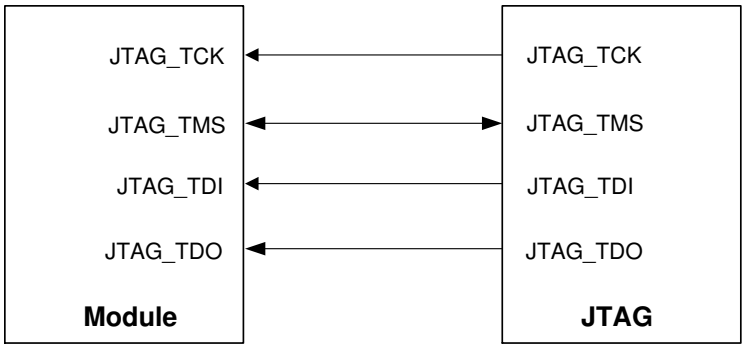


Figure 9: JTAG Interface Connection

3.4.4. I2C Interfaces

In the case of multiplexing, the module supports up to 2 I2C interfaces capable of acting as both a master and a slave and supporting multi-master buses. See ***Table 5*** for more details of the multiplexing functions. The interface supports standard-mode (100 kbps), fast-mode (400 kbps) and fast-mode plus (1 Mbps) speeds. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. Automatic recognition of slave addresses is provided in all energy modes (EM0–EM3) except EM4.

Both the I2C interfaces are open-drain. The maximum value of the pull-up resistor (Rp) can be calculated by the maximal rise-time (Tr) for the given bus speed and the estimated bus capacitance (Cb) as shown below:

Rp = Tr / (0.8473 × Cb)

The maximal rise times for 100 kHz, 400 kHz and 1 MHz I2C are 1 µs, 300 ns and 120 ns respectively.

3.4.5. IADC Interface

The module supports IADC interface multiplexed with GPIOs, and see ***Table 6*** for more details. The interfaces support a resolution of up to 12 bits when operating at one million samples per second (1 Msps). The flexible incremental architecture uses oversampling to allow applications to trade speed for higher resolution.

The key features of IADC interface are as below:

- Flexible oversampled architecture allows for tradeoffs between speed and resolution:
  - 1 Msps with oversampling ratio = 2
  - 555 ksps with oversampling ratio = 4
  - 76.9 ksps with oversampling ratio = 32
- Internal and external conversion trigger sources

- Immediate (software triggered)
- Local IADC timer
- External TIMER module (synchronous with output/PWM generation)
- General PRS hardware signal

- Selectable reference sources
  - 1.21 V internal reference
  - External precision reference
  - Analog supply

3.4.6. PDM Interface

The module supports a PDM interface multiplexed with GPIOs, and see ***Table 5*** for more details. The PDM interface provides a decimation filter for Pulse Density Modulation (PDM) microphones, isolated Sigma-Delta ADCs, digital sensors and other PDM or Sigma-Delta bit stream peripherals. A programmable Cascaded Integrator Comb (CIC) filter is used to decimate the incoming bit streams. PDM supports stereo or mono input data and DMA transfer.

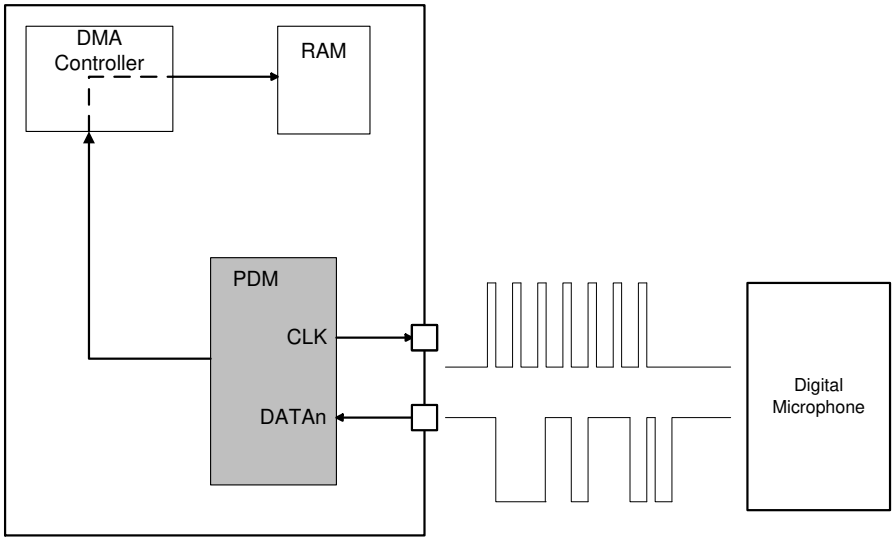


Figure10：PDM Interface Functional Diagram

3.4.7. GPIO Interfaces

In the case of multiplexing, the module supports up to 18 GPIO interfaces, and see ***Table 5*** for more details of the multiplexing functions. All the interfaces can be individually configured as either an output or input. More advanced configurations like open-drain, open-source, and glitch filtering can be configured for each individual GPIO pin. After a reset, both input and output are disabled for all pins on the device, except for the SWD pins (SWDIO and SWCLK). Peripheral resources, like Timer, PWM outputs or USART_RXD/_TXD can be routed to the GPIO pins as desired. The input value of a pin can be routed through the Peripheral Reflex System to other peripherals or used to trigger an external interrupt.

4 Operating Characteristics

4.1. Power Supply

Power supply pin and ground pins of the module are defined in the following table.

Table 10: Pin Definition of Power Supply and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	2	PI	Power supply for the module	1.71	3.3	3.8	V
GND	1, 8, 9						

4.1.1. Reference Design for Power Supply

The module is powered by VBAT, and it is recommended to use a power supply chip that can provide sufficient current more than 0.3 A. For better power supply performance, it is recommended to parallel a 22 µF decoupling capacitor, and two filter capacitors (1 µF and 100 nF) near the module's VBAT pin. C4 is reserved for debugging and not mounted by default. In addition, it is recommended to add a TVS near the VBAT to improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT trace is, the wider it should be.

VBAT reference circuit is shown below:

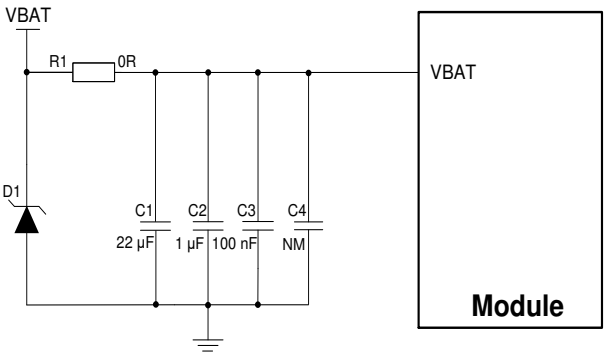


Figure 11: VBAT Reference Circuit

4.2. Turn On

The module can automatically start up after the VBAT is powered on.

The turn-on timing is shown below:

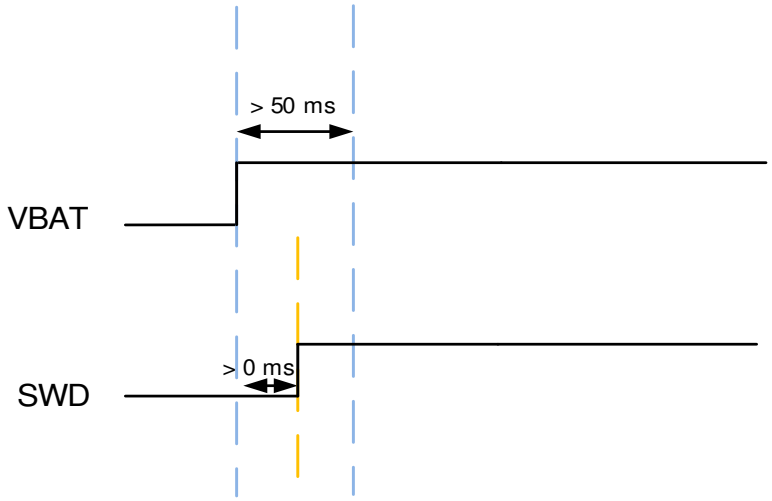


Figure 12: Turn-on Timing

4.3. Reset

Pull the RESET_N low for at least 50 ms and then release it to reset the module.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	5	DI	Reset the module	Hardware reset. Internally pulled up to VBAT. Active low.

The reference design for resetting the module is shown below. Press the button directly to realize the resetting of the module. At the same time, it is recommended to place a TVS near the button for ESD protection.

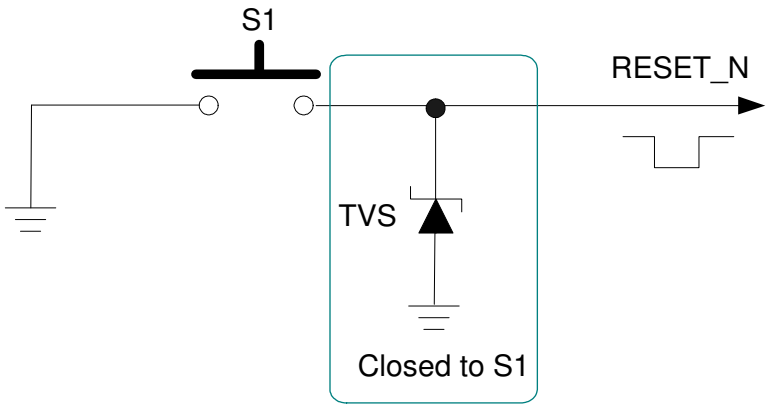


Figure 13: Reference Circuit for RESET_N with a Button

The module reset timing is illustrated in the following figure.

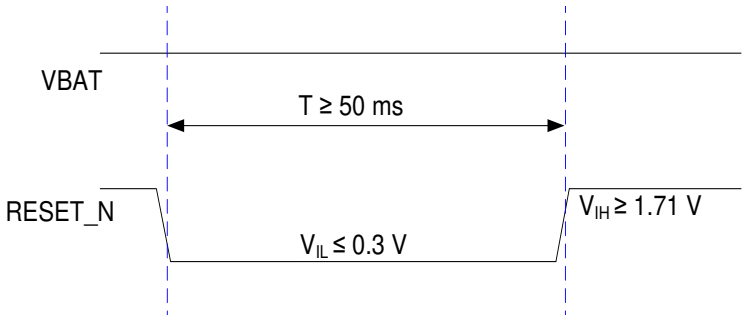


Figure 14: Reset Timing

5 RF Performances

5.1. Bluetooth Performances

Table 12: Bluetooth Performances

Operating Frequency		
2.400–2.4835 GHz		
Modulation		
GFSK		
Operating Mode		
BLE		
Condition (VBAT = 3.3 V; Temp. 25°C)	**Transmitting Power**	**Receiver Sensitivity**
BLE (1 Mbps)	≤ 6 dBm	-99.5 dBm ±2 dB
BLE (2 Mbps)	≤ 6 dBm	-95.5 dBm ±2 dB

5.2. PCB Antenna

The module supports PCB antenna and the antenna specifications are shown below:

Table 13: PCB Antenna Specifications

Parameter	Specification
Frequency Range (GHz)	2.400–2.500
Input Impedance (Ω)	50 (Typ.)
VSWR	≤ 2
Gain (dBi)	-0.5 (Max.)
Efficiency	30 % (Avg.)

During PCB on-board design, pay attention to the layout of PCB antenna on the motherboard to reduce its impact on the performance of the PCB antenna. The module should be placed at the edge of the motherboard with the PCB antenna area extending outside and the antenna feed points closest to the edge. It is recommended to place the module at area 1 and 5 as showing in the figure bellow.

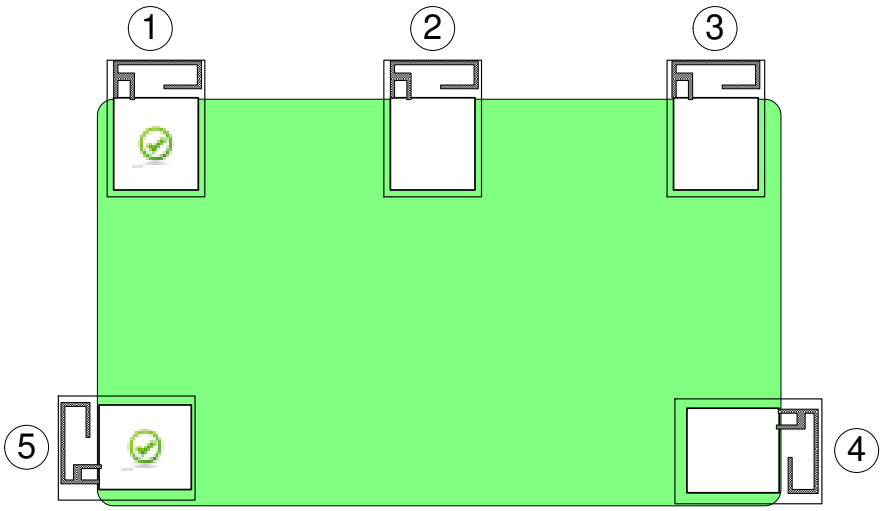


Figure 15: Module Placement

If the above placement positions are limited and cannot be implemented, the PCB antenna should be at least 16 mm away from the metal components, connectors, vias, traces, and copper pour area on the motherboard. On the motherboard, all PCB layers under the PCB antenna should be designed as the keepout area.

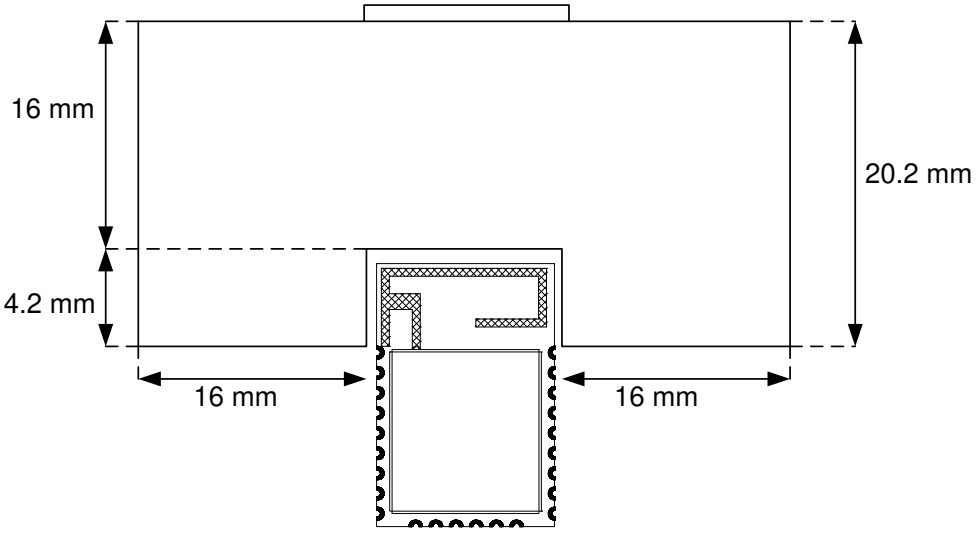


Figure 16: Keepout Area on Motherboard

To ensure module performance, do not route at the RF test point at the bottom of the module during PCB design. The prohibited area during routing is shown in the red box below:

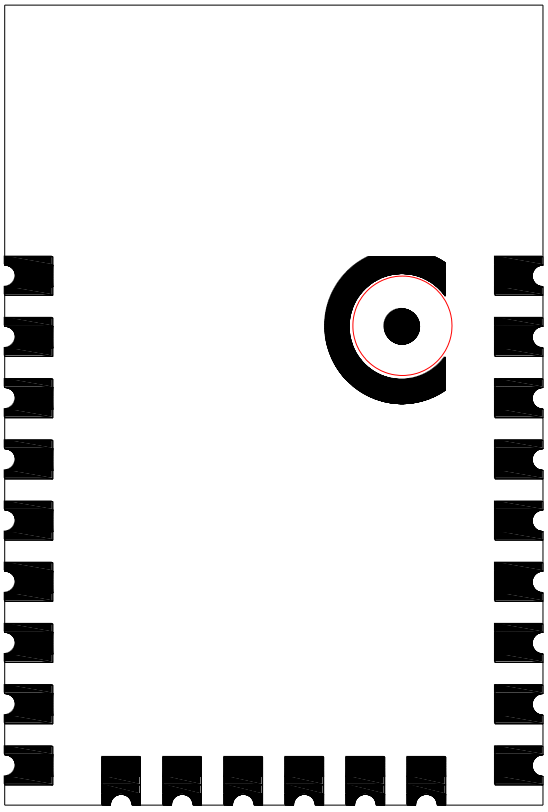


Figure 17: Prohibited Area During Routing (Bottom View)

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 14: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VBAT	-0.3	3.8
Voltage at Digital Pins	-0.3	4.1
Voltage at IADC	0	3.8

6.2. Power Supply Ratings

Table 15: Module Power Supply Ratings (Unit: V)

Parameter	Description	Condition	Min.	Typ.	Max.
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	1.71	3.3	3.8

6.3. Bluetooth Power Consumption

Table 16: Bluetooth Consumption (Unit: mA)

Condition (VBAT = 3.3 V; Tx 6 dBm)	Max.
BLE (1 Mbps)	6.18
BLE (2 Mbps)	4.03

6.4. Digital I/O Characteristics

Table 17: VBAT I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VBAT	VBAT
V_{IL}	Low-level input voltage	-0.3	0.3 × VBAT
V_{OH}	High-level output voltage	0.9 × VBAT	VBAT
V_{OL}	Low-level output voltage	0	0.1 × VBAT

6.5. ESD Protection

Static electricity occurs naturally and may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 18: ESD Characteristics (Unit: kV)

Model	Test Result	Standard
Human Body Model (HBM)	±4	*ANSI/ESDA/JEDEC JS-001-2017*
Charged Device Model (CDM)	±1	*ANSI/ESDA/JEDEC JS-002-2018*

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

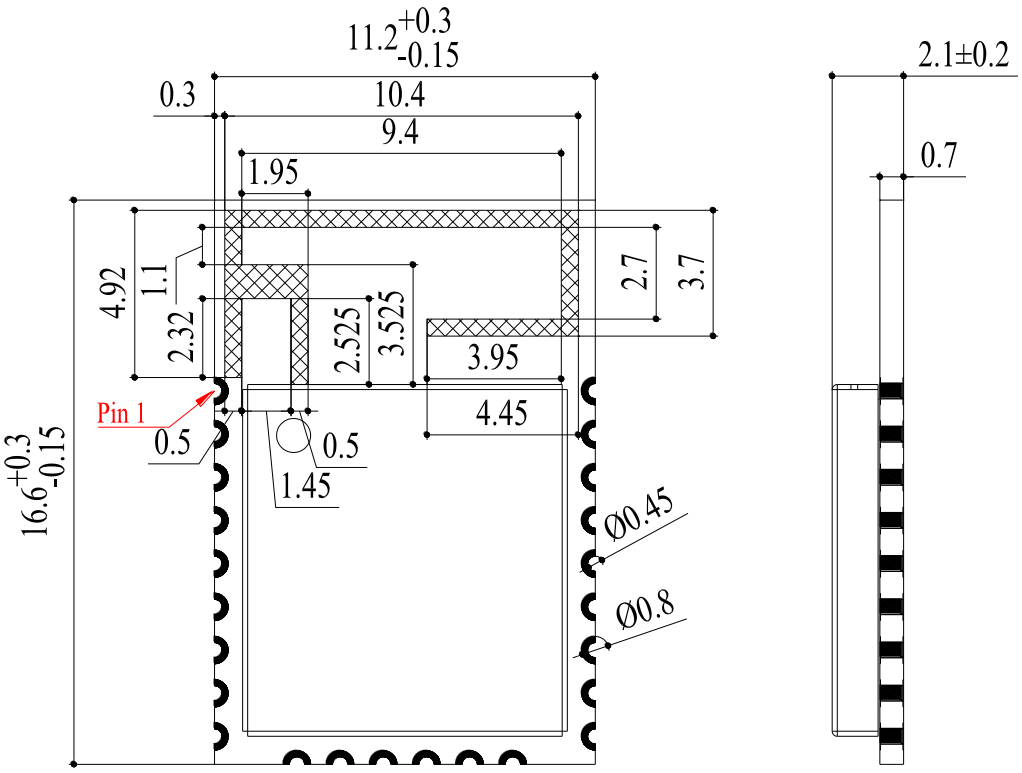


Figure 18: Top and Side Dimensions

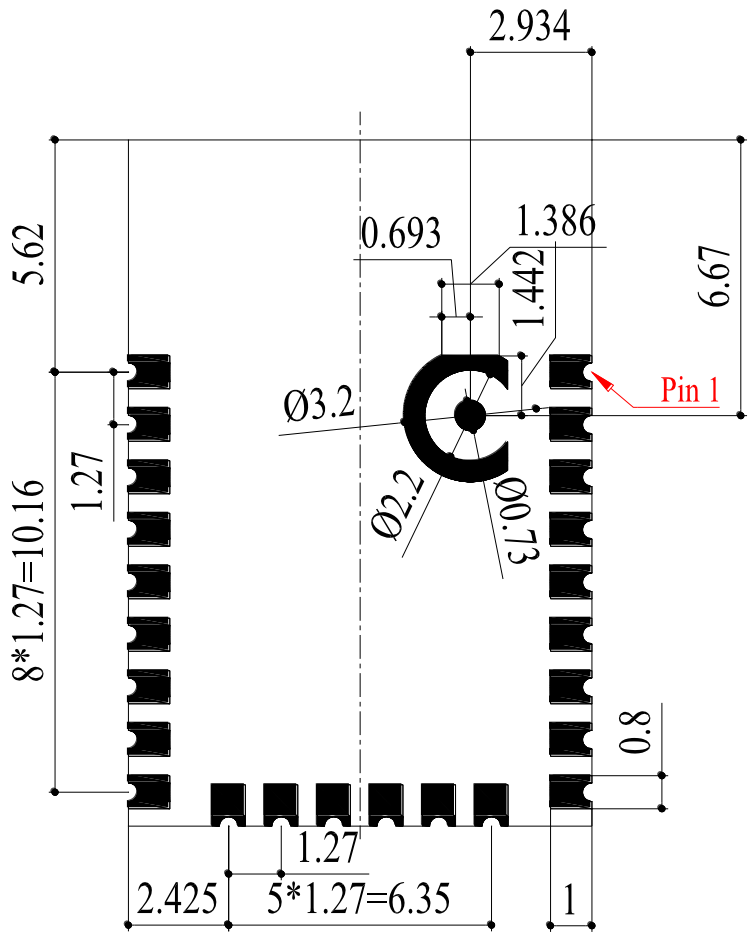


Figure 19: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

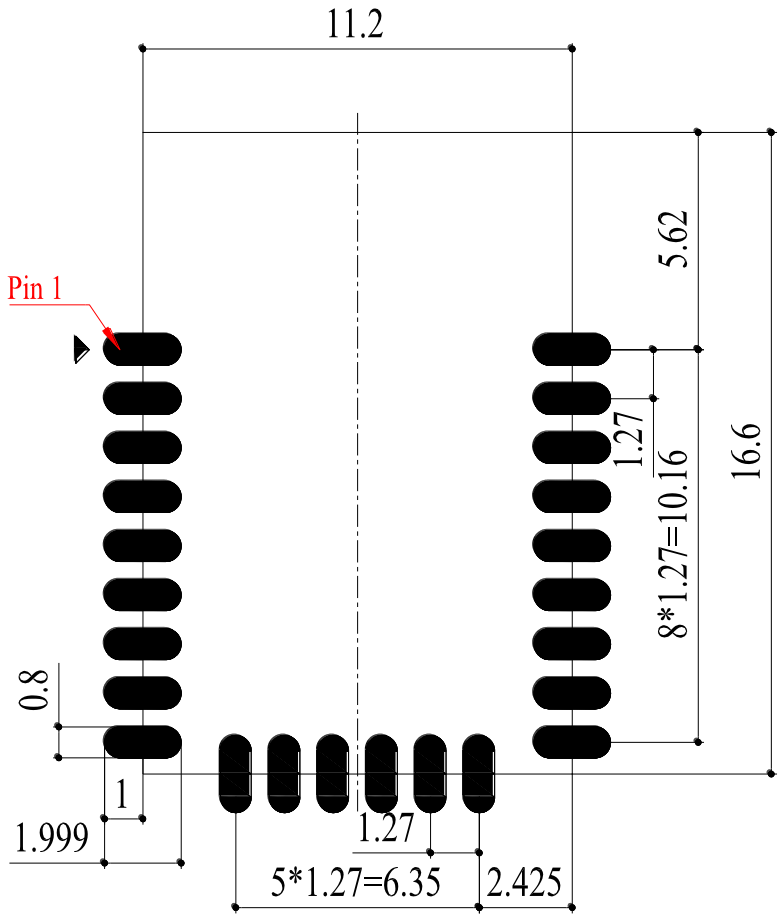


Figure 20: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 21: Top and Bottom Views

NOTE

Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [4] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[4] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

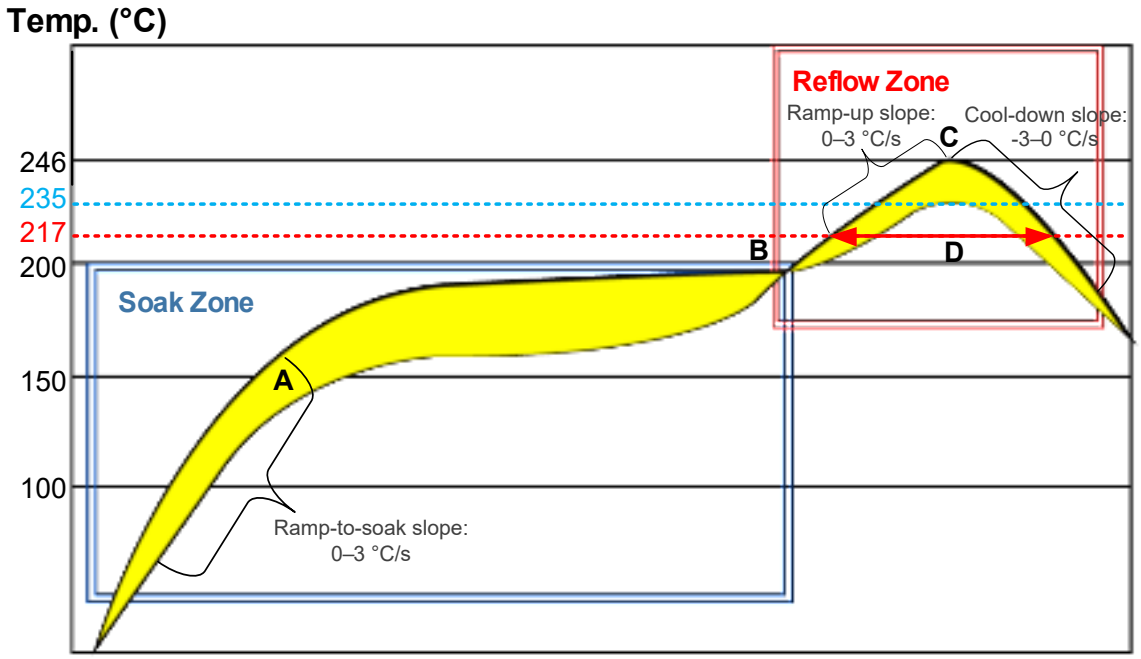


Figure 22: Recommended Reflow Soldering Thermal Profile

Table 19: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [3]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

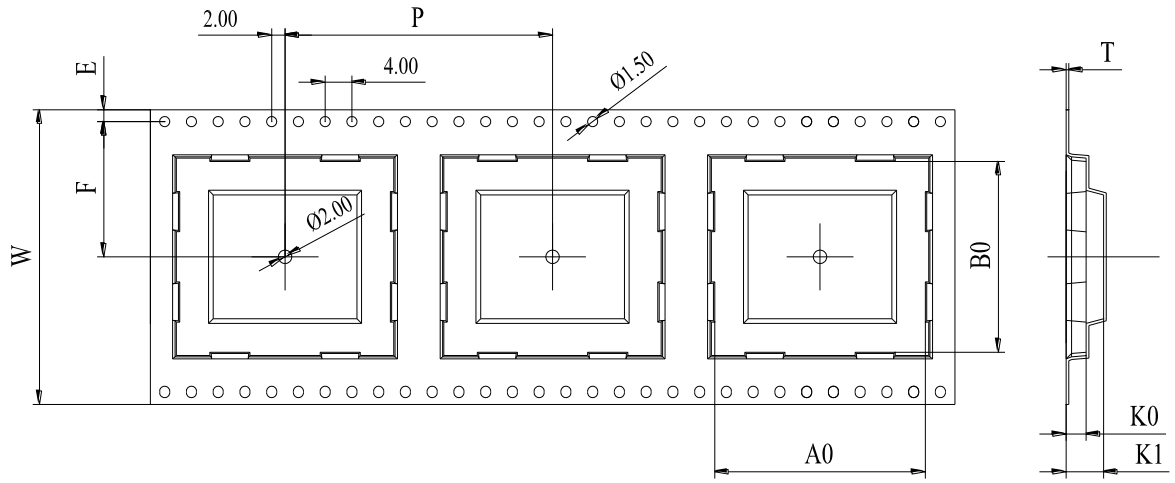


Figure 23: Carrier Tape Dimension Drawing (Unit: mm)

Table 20: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	11.6	17	2.6	4.6	14.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

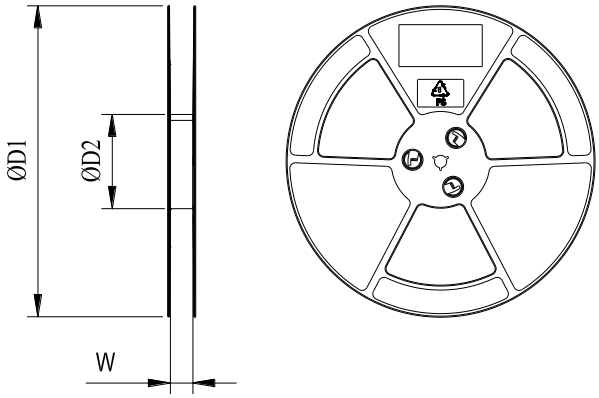


Figure 24: Plastic Reel Dimension Drawing

Table 21: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

8.3.3. Mounting Direction

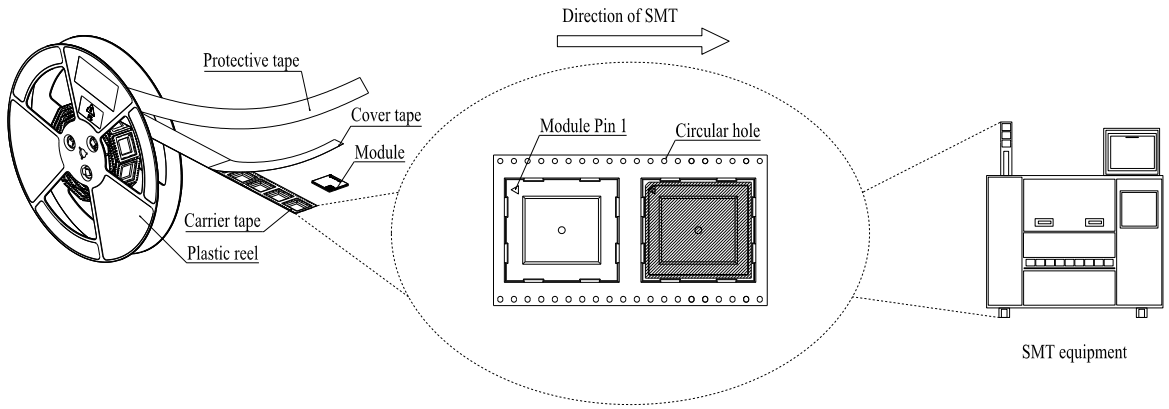
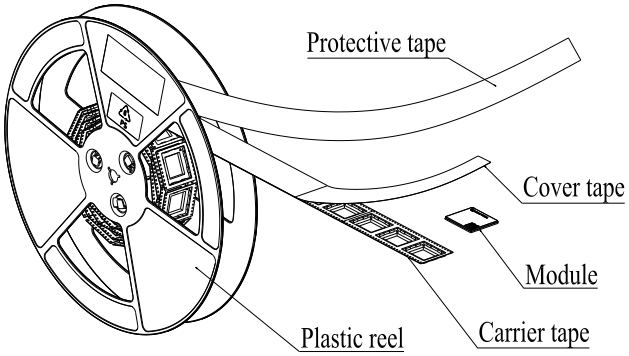


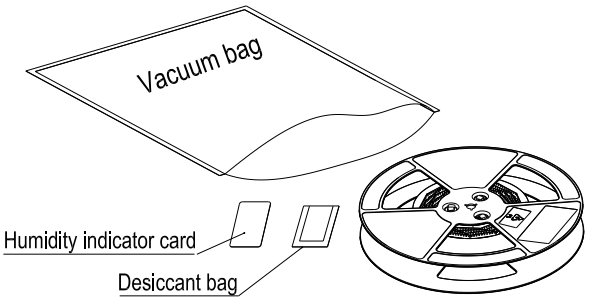
Figure 25: Mounting Direction

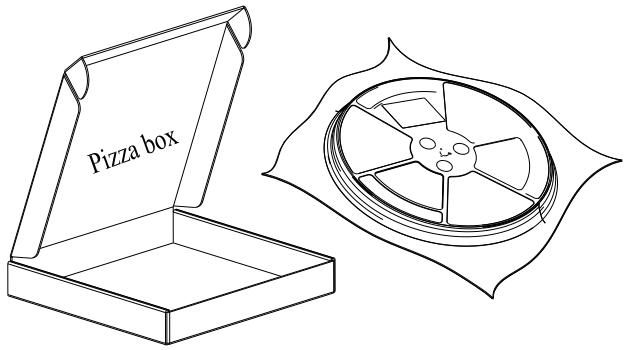
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

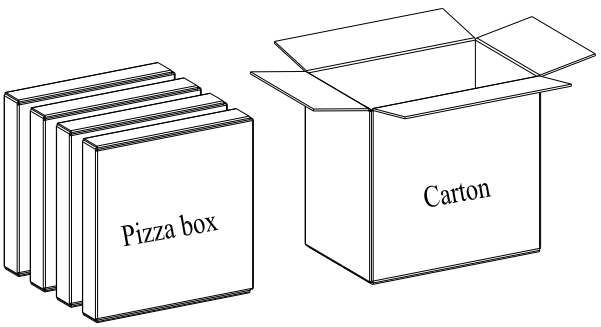


Figure 26: Packaging Process

9 Appendix References

Table 22: Reference Documents

Document Name
[1] Quectel_HCM511S_TE-B_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_SMT_Application_Note

Table 23: Terms and Abbreviations

Abbreviation	Description
ARM	Advanced RISC Machine
BLE	Bluetooth Low Energy
CDM	Charged Device Model
CMU	Clock Management Unit
CPU	Central Processing Unit
DC	Direct Current
DMA	Direct Memory Access
EM	Energy Mode
ESD	Electrostatic Discharge
ETM	Embedded Trace Macrocell
EUART	Enhanced Universal Asynchronous Receiver/Transmitter
FRC	Frame Controller

GFSK	Gauss frequency Shift Keying
GND	Ground
GPIO	General-Purpose Input/Output
HBM	Human Body Mode
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IADC	Incremental Analog to Digital Converter
I/O	Input/Output
IrDA	Infra-red Data Association
JTAG	Joint Test Action Group
LCC	Leadless Chip Carrier (package)
Mbps	Million Bits Per Second
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTA	Over-The-Air
PCB	Printed Circuit Board
PDM	Pulse Density Modulation
PRS	Peripheral Reflex System
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug

TVS	Transient Voltage Suppressor
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/ Transmitter
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time- averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2023HCM511S.
4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:
❒ Bluetooth LE:≤-0.5 dBi

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products. A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and
OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR2023HCM511S." or "Contains FCC ID: XMR2023HCM511S." must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user

that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user’s authority to operate the equipment.

IC Certification Requirements.

This device contains licence-exempt transmitteris)/receivers) that comply with Innovation, Science and EconomicDevelopment Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:
1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.

To comply with IC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:
❒ Bluetooth LE:≤-0.5 dBi

The host product shall be properly labelled to identify the modules within the host product.
The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows: “Contains IC: 10224A-2023HCM511S” or “where: 10224A-2023HCM511S is the module’s certification number”.

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. To comply with RSS-102 RF Exposure compliance requirements, this grant is applicable to only Mobile Configurations. The antennas used for the transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

L'appareil contient un émetteur / récepteur exempté de licence conforme au CNR exempté de licence d'innovation, sciences et développement économique Canada. Les opérations sont soumises aux deux conditions suivantes:

1. Cet appareil peut ne pas causer d'interférence.

L'appareil doit accepter toute interférence, y compris celles qui peuvent entraîner un fonctionnement ind ésirable de l'appareil.