BRIEF CIRCUIT DESCRIPTION

INTRODUCTION

The VHF and UHF radios comprise of two PCBs (RF and digital PCB). These boards are connected by an 18 pin female and male connector. The digital board which controls the radio and data receiving and sending is interfaced with external data equipment through the 15 pin d-sub female (DB-15) connector.

DIGITAL CIRCUITS

The Digital circuit contains the CPU, the channel select switch, and associated digital circuits.

TX-SIGNAL CIRCUIT

There are two signal paths in the Tx-signal circuit. One is FSK data signal path and the other is the audio signal path. The FSK data signal from Pin 1 of DB-15 connector (CON401) goes through IC406-C. The signal is amplified by IC404-C and then its amplitude is limited by IC404-D. After that, this signal is filtered by an 8'th order low pass filter (IC405) in order to reduce the required transmission bandwidth. The first two stages of the 8'th order LPF consist of a Gaussian filter for the improvement of ramp function response and the last two stages use a Butterworth filter for attenuation. The output of the LPF is then fed to the RF board for TX modulation.

Audio signal, from Pin 7 of DB-15 connector is fed into the 300Hz High pass filter(IC408) through the IC406-B and IC409. The HPF removes sub-audible voice products for application of Sub-audio(Tone) squelch system (CTCSS, DCS) and then the output from IC408 is fed into IC404-A&B with associated parts to form a mic amplifier and pre-emphasis circuit. After that, the pre-emphasized Tx-audio signal is inputted to the RF board for Tx modulation through the FSK data signal path.

RX-SIGNAL CIRCUIT

The Rx-signal circuit also has two signal paths. One is the data signal path and the other is the audio signal path. The Rx signal comes from the RF board, which is connected with pin 10 of CON405. Data signals are switched in IC406-D by a Busy signal which is activated when the radio receives a valid RF signal, and is filtered by IC416-A and then its amplitude level is adjusted (amplified) by IC416-B. The amplitude-adjusted signal goes to pin 2 of the DB-15 connector (CON401).

Audio signals are inputted to the 300Hz High pass filter (IC408) to eliminate sub-audible voice products through IC409. The output of the HPF is switched by IC406-A and de-emphasized by resister R471 and C452. After that, its level is adjusted by RV401 and then that is amplified by IC412 (LM386 : Audio

amplifier). The amplified signal goes to pin 9 of CON401 (DB-15).

ANALOG SWITCH

IC409 (MC14053B) is a digitally controlled analog switch which internally consists of three single pole, double throw switches. By placing a high (5V) or low (0V) on the control lines which consists of A, B and C. A controls the X ports, B controls the Y ports and C controls the Z ports. Example: A high on control A would connect X to X1. A low on control A would connect X to X0.

HIGH PASS FILTER

The 300Hz high pass filter is an 8-pole 1dB Chebeyshev active filter that comprises of IC410 and associated components. Received audio is passed to IC408 from Pin 4 of IC409 where sub-audible tones below 300Hz are removed. Tx (Mic) audio is also fed into IC408 via IC 409 (Pin 4) where sub-audible voice products below 300Hz are also removed.

CTCSS/DCS DECODE CIRCUITS

Discriminated audio from Pin 9 of IC6 is fed into IC411-B and associated parts which are the first 2 poles are part of a 6th order 250 Hz Chebeyshev low pass filter. The output from pin 1 (IC411-B) is fed into IC409 (Pin 2) and outputs to pin 15 (IC409). The signal is then fed to Pin 8 (IC410) which is a 6th order low pass Butterworth switched capacitor filter. The output from the Butterworth filter (Pin 3 of IC410) is then fed to the remaining second 4 poles part of the 6th order Chebeyshev filter, which consist of IC411-D and one of the two internal operational amplifiers of IC410 (MSNBLPS) along with associated components. Both the Chebeyshev and the Butterworth combines for a 4dB ripple low pass filter when programmed for 250 Hz. The output of IC411-D (Pin 14) is fed into the remaining internal operational amplifier of IC410 (MSNBLPS) which forms the squaring circuit for the signal decode. The signal is out from Pin 2 of IC411 (MSNBLPS) and fed into IC401 (MCU) where it is compared whether that is matched with preprogrammed data or not. If matched, valid data is decoded, shown by a green L.E.D. on the top panel of the radio, and audio is released through pin 9 of DB-15 Connector. If unmatched, the busy L.E.D. (Yellow) would be shown.

CTCSS/DCS ENCODE CIRCUITS

During TX encode, the tone squelch digital signal is produced as a 3-bit parallel word at Pins 33, 34, and 35 of the micro controller (IC401). The 3-bit digital signal is converted to an analog signal by resistors

R481, 482 and 483. The analog signal is fed into Pin 1of IC409 and out on Pin 15 (IC409) and then fed into Pin 8 of IC410 (6th order Butterworth clock tuned low pass filter). The filtered encode output from Pin 3 (IC410) is fed to IC411-A and RV402 (sub-audible gain control), the output of IC411-A is then fed to the audio mixer circuit of the RF board.

TWO TONE DECODE CIRCUITS

Two tone uses frequency with audio. Discriminated audio from the RF board is inputted to the comparator (two tone decoder : IC403-B) which forms the squaring circuit for the decode signal. The signal is output from Pin 7 of IC403-B and fed into IC401 (MCU) where it is compared whether it is matched with preprogrammed data or not. If matched valid data is decoded, which is shown by a green L.E.D. on the top panel of the radio and audio is released through pin 9 of the DB-15 Connector. If unmatched, the busy L.E.D. (Yellow) is shown.

RSSI DETECTOR

From the RF board, the RSSI (Received Signal Strength Indicator) signal flows to Pin 31 of IC401(MCU) through R513. Micro controller unit (IC401) detects received signal level using the inner 8-bit ADC(Analog to Digital Converter). The output of ADC is compared with the programmed RSSI level. If the MCU detects existence of a received signal through these comparison a yellow L.E.D. is shown on the top panel of the radio.

EEPROM

RX / TX channel and RSSI detection level as well as other data from the programmer are stored in the EEPROM. The stored data is retained without power supply. This is a non-volatile memory and re-programmable. IC402 is an EEPROM with 4096 (8 x 512) capacity and data is written and read serially.

CHANNEL SELECTOR

One of 16 channels may be selected using the Dip Switch (SW401) and serial commands. The hardware selector, SW401 encodes the channel number, selected into 4-bit binary code. The binary code plus one equals the channel number. The binary code is decoded by the CPU, which enables the appropriate RX or TX frequency and associated data to be selected from the EEPROM. External serial commands which come from Pin 8 of the DB-15 Connector (CON401) are fed into Pin 41 of IC401 (MCU). The micro controller uses UART (Universal asynchronous receiver transceiver) for serial communication and

decodes serial commands in order to control the radio.

DC TO DC CONVERTER

The main DC power is supplied to the switched mode DC to DC converter . The DC to DC converter regulates the various input power supply voltage and outputs a constant voltage of 6.5 Volts (SD-161, SD-164) or 7.5 Volts (SD-171, SD-174). It is a source for all of the RF and digital circuits. The DC to DC converter is formed by IC801, Q801, Q802, L801, R804 and voltage divider(R805, R806, R802). IC801 is a PWM controller that controls pulse width of the switching pulse output. Various input voltage appears as various output voltage of voltage divider. IC801 detects the voltage difference between inner reference voltage and the voltage divider output controls the switching pulse width in proportion to its difference. Wanted output voltage is decided by product of input voltage and duty ratio of switching pulse. As the switching pulses, Q801and Q802 switch the input DC of various supply voltages and generate the constant DC of supply voltage. IC801 controls maximum current of DC to DC converter by current detection through voltage drop of R804.

RF CIRCUITS

PLL SYNTHESIZER

12.8 MHz TCXO

The TCXO contains the 3-stage thermistor network compensation and crystal oscillator and modulation ports. Its compensation is ±5 PPM or less from -30c to +60c.

PLL IC DUAL MODULE PRESCALER

Input frequency of 12.8 MHz to pin 1 of IC2 MB15A02 (or MB15E03SL) is divided into 6.25 kHz or 5 kHz by the reference counter and then supplied to the comparator. RF signal input from the VCO is divided to 1/64 at the 64/65 modulus prescaler in IC2, divided by A and N counter in IC2 to determine frequency steps, and then supplied to the comparator. PLL comparison frequency is 6.25/5 kHz, so its minimum programmable frequency step is 6.25/5 kHz. The A and N counter is programmed to obtain the desired frequency by serial data in the CPU. In the comparator, the phase difference between reference and VCO signal is compared. When the phase of the reference frequency is leading, ΦP is the output, but

when the VCO frequency is leading, ΦR is the output. When ΦP= ΦR, phase detector out is a very small pulse.

EXTERNAL CHARGE PUMP

This is used to increase dynamic range of VCO. Voltage range is decided by the supply voltage of the charge pump and the DC to DC converter which supplies that voltage. 0-12v is necessary for controlling the VCO. In addition the radio adopts a current mode charge pump to take direct control of such parameters as charge pump voltage swing, current magnitude, TRI-STATE leakage, and temperature compensation. ΦP, ΦR logic signals are converted into current pulses to enable either charging or discharging of the loop filter components to control the output frequency of the PLL.

REFERENCE FREQUENCY LPF

The Loop Filter contains R9, C1 and C2. LPF settling time is 12mS with 1 kHz frequency. This also reduces the residual side-band noise for the best signal-to-noise ratio.

DC TO DC CONVERTER

The DC to DC converter converts 5v to 14-16v to supply the necessary voltage for wide range frequency in the VCO.

VCO

The radio adopts a two VCO system for RX and TX in order to maximize each performance. The TX and RX VCO generates RF carrier and local frequency and each VCO is switched by a TX/RX power source. It is configured as a Colpitts oscillator and connected to the buffer as a cascade, the bias circuit is a cascade configuration to save power. The varicap diode D201/D301are low-resistance elements and have different capacitance for reverse bias voltage. Using the change of reverse bias voltage (2 ~ 11V), the wanted frequency for each channel can be obtained. L203/L303 are resonant coils and C208/C308 are used to change the control voltage by the tuning core. D202 modulation diode modulates the audio signal. C204 compensates the non-linearity of the VCO due to the modulation diode and maintains a constant modulation regardless of frequency.

TRANSMITTER

The transmitter consists of:

1. Buffer
2. P.A. Module
3. Low Pass Filter
4. Antenna Switch
5. A.C.C. Circuits

BUFFER

VCO output level is -4dBm and amplified to +10dBm. The buffer consists of Q9 and Q10 for reverse isolation and gain.

P.A. BLOCK

The P.A. Block uses a three stage amplifier and contains Q501, Q502, and Q503. The SD-171, SD-174 have different amplifiers applied compared to the SD-161, SD-164 because different of a output power specification. Q501 amplifies the TX signal from +10 dBm to 100mW and Q502 amplifies to 0.5W and Q503 amplifies to 3W(SD-161, SD-164) or 6W(SD-171, SD-174) and then matched to 50 Ohms using the L.C. network or strip line, thereby reducing the harmonics by -30 dB.

LOW PASS FILTER

L7, L8, L9, C36, C37, C38 and C39 are the 7th order Chebyshev low pass filter. Unwanted harmonics are reduced by -70 dBc.

ANTENNA SWITCH

When transmitting, the diodes D3 and D5 are forward biased to enable to make an RF path to the antenna. D5 is shorted to ground to block the RF signal to the front-end. In receive, the diodes, D3 and D5, are reverse biased to pass the signal from the antenna through L10 and C61 to the front-end without signal loss.

AUTOMATIC CURRENT CONTROL (ACC) CIRCUITS

The ACC circuit consists of R63, variable resistor RV4, IC5(B) and transistors Q11 and Q12. The supplied current to the P.A. block is monitored by the voltage difference on R63 (0.1 Ohm). If the current

varies by RF power output or other reasons, it produces a voltage difference on R63 and then IC5A outputs a bias voltage to Q19 in proportion to that difference. The adjusted value of Q15 output by RV4 is compared with the reference voltage in IC5B and then a differential voltage at the output of IC5B is passed to Q12 and Q11 which controls the bias voltage of the P.A. module to maintain a constant power output to the antenna. RV4 is used to adjust the RF power level.

RECEIVER

FRONT-END

The front-end block consist of two band pass filters and a low noise amplifier (LNA). The Band pass filter is used for elimination of image frequency and impedance matching and the LNA is used to amplify weak RF signals without any increase of noise. The received signal comes from the antenna, then is input into a band pass filter of the front-end block with C601through C610, L601 through L604 at UHF and C622 through C608, L607 through L604 at VHF, and is coupled to the base of Q601 serving as an RF amplifier. Diode D601 serves as protection from static RF overload from nearby transmitters. The output of Q601 is then coupled to a second band pass filter consisting of C611 through C623 and L606 through L609 at UHF and C607 through C601, L603 through L601 at VHF. The output of the front-end block is then coupled to the double balanced diode mixer D6. The Front-end block is pre-tuned at factory and no more adjustment is required

FIRST MIXER

The Double balanced diode mixer consists of D9, T1 and T2 and generates the 45.1 MHz intermediate frequency output from RF and local frequency. The filtered frequency from the front-end module is coupled to T1and the local frequency from RX VCO is coupled to T2. The 45.1 MHz IF output is matched with the input of the 2-pole monolithic filter by L12, L13, C65 and C66. The crystal filter provides a bandwidth of ±7.5 kHz at the operating frequency for a high degree of spurious and inter-modulation protection. The IF filter provides additional attenuation for the image frequency of the second mixer. The output impedance of the filter is matched with the base of the post amplifier Q16 by C67 and C70.

SECOND OSCILLATOR MIXER LIMITER AND FM DETECTOR

The output of the post amplifier, Q16, is coupled via C71 to the input of IC6 (TA31136FN). IC6 is a monolithic single conversion FM transceiver, containing a mixer, the second local oscillator, limiter and

quadrature detector. Crystal X1, 44.645 MHz, is used to provide resultant 455kHz signal from the output of the second mixer. The mixer output is then routed to CF1 (455F) or CF2(455HT). These ceramic filters provide the adjacent channel selectivity of 25 kHz or 12.5 kHz bandwidth. After that, filtered signal is fed to the limiter and then audio is derived from the limited signal at the quadrature detector.

RSSI (RECEIVER SIGNAL STRENGTH INDICATOR)

The RSSI signal is output from IC6 on pin 12. The output is an analog DC voltage and varied as much as the received signal strength. The signal which is filtered unwanted noise by the low pass filter (IC4-B) in the RSSI signal is used for squelch system. Also, this signal is compensated with a thermistor (TH3) at temperature.