7. SECURITY

The Network Interface supports the IEEE compatible WEP64 and 128RC4 algorit
security in all data rate modes.

8. COMPATIBILITY

The Network Interface Card shall comply with the Mini PCI Specification, October 1999 [Ref. 16].

The Network Interface shall comply with the IEEE802.11 standardized Wireless Medium Access Control (WMAC) and the IEEE802.11 Physical Layer (PHY) standard for Direct-Sequence Spread Spectrum (DSSS).

The PHY standard covers 1Mbit/s Differential Binary Phase-Shift Keying (DBPSK), 2Mbit/s Differential Quadrature Phase-Shift Keying (DQPSK) and 5.5Mb/s and 11Mb/s Complementary Code Keying (CCK). The network interface card will conform to the specification adopted by the IEEE 802.11b for the 5.5 and 11Mbps data rates in addition to the existing standard for 1 and 2Mbps.

9. LEGAL, REGULATORY AND OTHER TECHNICAL CONSTRAINTS

For all regulatory information, refer to Ref. 15.

10. PERFORMANCE REQUIREMENTS

10.1. General

Receiver input levels and transmitter output levels are specified at the antenna connector.

10.1.1. Antenna port impedance

The nominal antenna port impedance is 50Ω.

The Network Interface Card shall not be damaged for any Voltage Standing Wave Ratio (VSWR) 1≤VSWR≤ ∞.

10.1.2. Power-on start-up time

The Network Interface Card shall be operational within 600ms after switching the power supply on. This includes a delay of max 500 ms for the Flash ROM power up sequence.

10.1.3. Doze to receive mode start-up time

The Network Interface Card shall be operational within 0.75ms after switching from Doze mode to Receive mode. This includes lock-in and stabilization of the synthesizers (see *10.1.6. RF center frequency*). Transmissions are not allowed during this period.

10.1.4. Receive to transmit turnaround time

The time from transition of the TXE control line (transmit enable control line from WMAC to DSP) from inactive state to active state until the RF section is in transmit mode shall be not more than 5µs. The NIC is said to be in transmit mode at the moment the RF output power level is within 90% of its final value.

10.1.5. Transmit to receive turnaround time

The time from transition of the TXE control line (transmit enable control line from WMAC to DSP) from active state to inactive state until the NIC is in receive mode shall be not more than 10µs.

10.1.6. RF center frequency

The RF function provides programming of the RF center frequency from 2400MHz to 2500MHz in steps of 1MHz. This covers all IEEE802.11 RF channel frequencies listed in *chapter 12.7. RF channel frequencies*.

The RF center frequency for transmission and reception shall be stable within 25kHz of its final value, 0.75ms after reprogramming or switching from doze mode to receive mode.

10.1.7. RF center frequency and clock accuracy

The master clock frequency and the RF center frequency shall be within +/–25ppm of the nominal value.

The carrier jitter is within 25kHz of its final value 40µs after switching between RX and TX mode.

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10.2. Transmitter

10.2.1. Transmit power-on and power-down ramp

The transmit power-on ramp from 10% to 90% of the maximum power shall not take longer than 2µs.

The transmit power-down ramp from 90% to 10% of the maximum power shall not take longer than 2µs.

The transmit power ramp shall be constructed such that the emissions comply with the radi regulations mentioned in *chapter 9. LEGAL, REGULATORY AND OTHER TECHNICAL CONSTRAINTS*.

10.2.2. Transmitted power level

The nominal transmitted power shall be 15 dBm +/- 2dB at full operational temperature range. This range complies with the IEEE802.11 PHY standard and the radio regulations a per Ref. 15.

The power density shall not exceed 10dBm/MHz EIRP.

10.2.3. Transmitted output spectrum

The transmitted spectral products shall be less than –30dBr (dB relative to the sin(x)/x peal for frequencies between 11MHz and 22MHz from the center frequency and –50dBr for frequencies more than 22MHz from the center frequency as illustrated in Figure 3. The measurement shall be made at the antenna port using 100kHz resolution bandwidth.

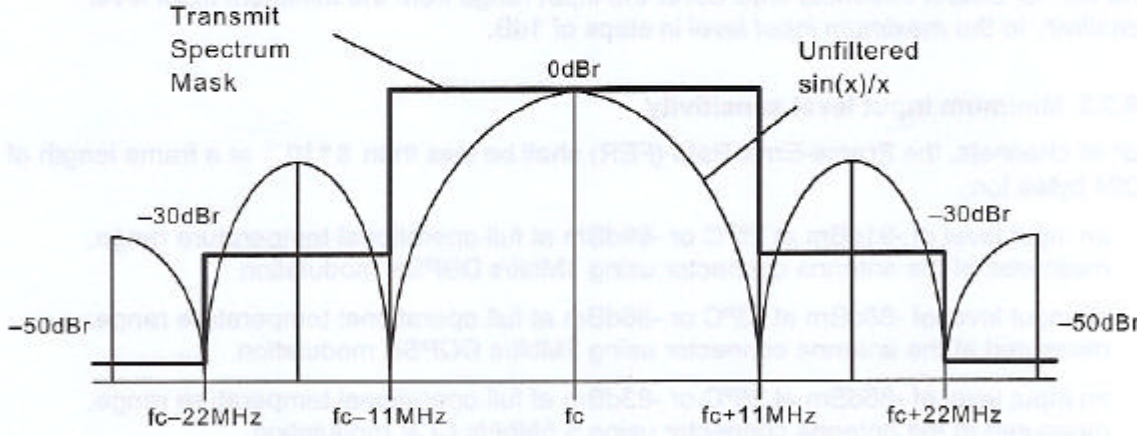

Figure 3. IEEE802.11 transmit spectrum mask.

10.2.4. RF carrier suppression

The RF carrier suppression measured at the channel center frequency shall be at least 15dB below the peak sin(x)/x power spectrum.

10.3. Receiver

10.3.1. Medium busy

The DSP reports to the WMAC the presence of a spread-spectrum signal on the medium b the MBUSY signal.

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MBUSY is set if a spread-spectrum signal is present on the medium with a level above the *defer threshold*. This *defer threshold* shall cover the input range from the *minimum input level sensitivity* to the *maximum input level* in steps of 1dB.

MBUSY is set at the end of an antenna slot according to Figure 4. If the signal is present within 5µs from the start of a slot (15µs before the end) MBUSY must be set at the end of the same slot, else MBUSY may be set at the end of the next slot. The antenna slot time is 20µs.

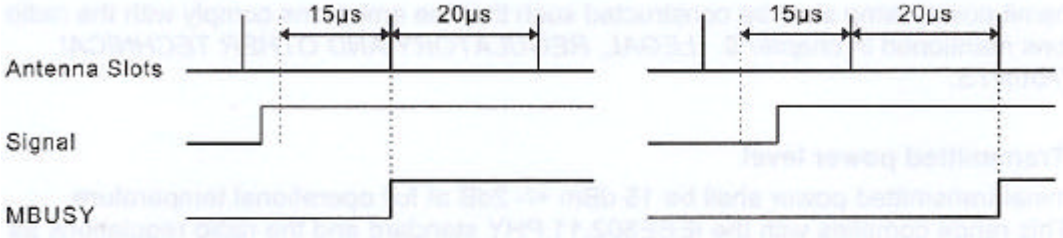

Figure 4. MBUSY active timing.

MBUSY is cleared at the end of a received frame.

10.3.2. Carrier Detect threshold

The receiver is activated if a spread-spectrum signal is present on the medium with a level above the *Carrier Detect threshold*. Incoming signals below that threshold are ignored.

The Carrier Detect threshold shall cover the input range from the *minimum input level sensitivity* to the *maximum input level* in steps of 1dB.

10.3.3. Minimum input level sensitivity

For all channels, the Frame-Error Rate (FER) shall be less than $8*10^{-2}$ at a frame length of 1024 bytes for:

- an input level of -91dBm at 25°C or -89dBm at full operational temperature range, measured at the antenna connector using 1Mbit/s DBPSK modulation
- an input level of -88dBm at 25°C or -86dBm at full operational temperature range, measured at the antenna connector using 2Mbit/s DQPSK modulation
- an input level of -85dBm at 25°C or -83dBm at full operational temperature range, measured at the antenna connector using 5.5Mbit/s CCK modulation.
- an input level of -82dBm at 25°C or -80dBm at full operational temperature range, measured at the antenna connector using 11Mbit/s CCK modulation.

The test for the minimum input level sensitivity shall be conducted with the *Carrier Detect threshold* set less than –95dBm.

10.3.4. Maximum input level

The FER shall be less than $8*10^{-2}$ (1024 byte frames) for a maximum input level of –4Bm measured at the antenna connector. This applies to all modulation types and data rates.

10.3.5. Over-voltage protection

The receiver shall not be damaged by over-driving levels up to +17dBm at the antenna connector. No DC voltage shall be exposed to the antenna connector.

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10.3.6. Adjacent channel rejection

The adjacent channel rejection shall be at least 35dB with a FER of $8*10^{-2}$ (1024 byte frames) using DQPSK and CCK modulation.

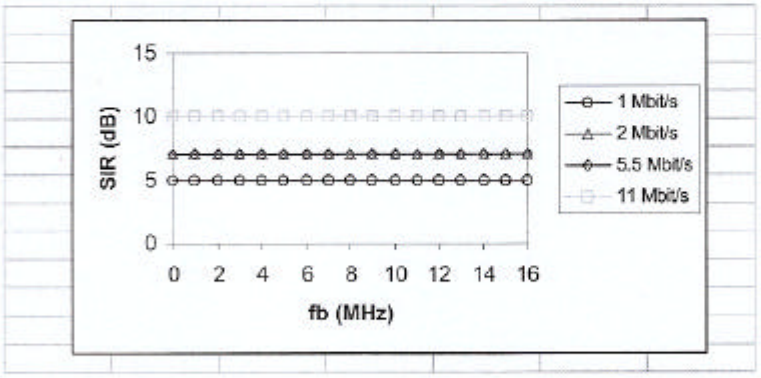
The adjacent channel rejection shall be measured using a WaveLAN input signal at a level of 6dB above the *minimum input level sensitivity* (Ref. 14: *-80dBm for 2Mb/s DQPSK modulation, -76dBm for 11Mb/s CCK modulation)* as desired input signal. The adjacent channel signal being modulated in a similar manner and compliant to the *transmitted spectrum mask*, shall have a level of 41dB above the *minimum input level sensitivity*. The adjacent channel signal must be derived from a separate signal source. The center frequency spacing shall be 25MHz or more. Under these conditions, the FER shall be no worse than $8*10^{-2}$.

10.3.7. FCC spreading gain

The unit shall comply with a minimum processing gain of 10dB, as specified in Ref. 1.
A WaveLAN signal is applied together with a Continuous Wave (CW) interference signal at the receiver input. The level of the WaveLAN signal is –55dBm. The interference signal is stepped in 50kHz increments across the passband of the system. The minimum Signal to Interference Ratio (SIR) needed for a BER better than $1*10^{-8}$ is shown in Figure 5 for each data rate as a function of fb=|fc-fint|, where:

fb is the down converted base-band interference frequency.
fc is the carrier frequency of the WaveLAN signal.
fint is the CW interference frequency.

The SIR is calculated discarding the worst 20% of the SIR data points. Note that total losses in the system should be assumed to be no more than 2dB. (See Ref. 1)



SIR(1Mbps) = 5dB
SIR(2Mbps) = 7dB
SIR(5.5Mbps) = 7dB
SIR(11Mbps) = 10dB

Figure 5. SIR frequency mask.

10.3.8. Out-of-band signal rejection

A WaveLAN signal is applied together with two Continuous Wave (CW) interference signals at the receiver antenna input. The level of the WaveLAN signal is –55dBm. The CW interference signals have equal level and 1.2MHz frequency distance. The maximum level of each of the two interfering CW signals for a FER better than $8*10^{-2}$ (1024 byte frames) is shown in Table 1 as a function of the average frequency of both interfering frequencies.

Average frequency of interferers	max. level of each interferer, 2Mbit/s DQPSK - $T_{AMBIENT}$ = 25°C

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<1.0GHz	-6dBm
1.0-2.0 GHz	-10dBm
2.0-2.35 GHz	-26dBm
2.55-2.9 GHz	-26dBm
>2.9 GHz	-10dBm

Table 1. Out of band maximum interference levels.

10.3.9. Irreducible Frame Error Ratio

The Irreducible FER (1024 byte frames) in an RF-clean environment (anechoic chan nominal temperature between two Network Interfaces one meter apart using 2Mbit/s DQPSK will be better than $1*10^{-8}$.

11. INTERFACES

11.1. Host interface

The Network Interface is connected to the Host through the Mini PCI interface bus, for which the interface lines are defined the "Mini PCI Specification, October 1999" [Ref. 16].

The PCI interface consists of a PCI to PC card controller, which is compliant with the "PCI Local Bus Specification [Ref. 18]".

11.2. Mini PCI Host interface

AD [31:00]	32bit Address and Data bus
C/BE[3:0]#	Bus Command and Byte Enable signals
PAR	Parity is even signal
FRAME#	Cycle Started and duration signal
IRDY#	Initiator Ready signal
TRDY#	Target Ready signal
STOP#	Target Stop Request signal
DEVSEL#	Target Accept Cycle Signal
IDSEL	Initialization Device Select signal (only by configuration)
PERR#	Parity error signal
SERR#	System error signal
REQ#	Request bus from arbiter signal
GNT#	Bus granted by arbiter signal
PME#	Power management event signal
CLKRUN#	Clock running signal
CLK	Bus Clock
INTA#	Interrupt A signal
RST#	Reset signal
MPCIACTV#	MiniPCI function active signal
M66EN	66MHz enable

11.2.1. MiniPCI connector implementation

Name (Mini PCI Pin Number odd)	Name (Mini PCI Pin Number even)
ETD0 (#3) Used by Lucent! (Original (8PMJ-3)	**ETCK (#4) Used by Lucent! (Original (8PMJ-1)**
ETD1 (#5) Used by Lucent! (Original (8PMJ-6)	**ETSYN (#6) Used by Lucent! (Original (8PMJ-2)**
ETD2 (#7) Used by Lucent! (Original (8PMJ-7)	**ENGTEST (#8) Used by Lucent! (Original (8PMJ-4)**
SDA (#9) Used by Lucent! (Original (8PMJ-8)	**SCL (#10) Used by Lucent ! (Original (8PMJ-5)!**
LED1_GRNP (#11) network activity LED	LED2_YELP (#12) Power / network connection LED
LED1_GRNN (#13) Used by Lucent (Radio on/off switch)	INTA_B (#20)
PCLK (#25)	RST_B (#26)
REQ_B] (#29)	GNT_B (#30)
AD31 (#33)	PME_B (#34)
AD29 (#35)	AD30 (#38)
AD27 (#39)	AD28 (#42)
AD25 (#41)	AD26 (#44)
CBE3_B (#45)	AD24 [(#46)
AD23 (#47)	IDSEL (#48)
AD21 (#51)	AD22 (#52)
AD19 (#53)	AD20 (#54)
AD17 (#57)	PAR (#56)
CBE2_B (#59)	AD18 (#58)
IRDY_B (#61)	AD16 (#60)
CLKRUN_B (#65)	FRAME_B (#64)
SERR_B (#67)	TRDY_B (#66)
PERR_B (#71)	STOP_B (#68)
CBE1_B (#73)	DEVSEL_B (#72)
AD14 (#75)	AD15 (#76)
AD12 (#60)	AD13 (#78)
AD10 (#81)	AD11 (#80)
AD8 (#85)	AD9 (#84)
AD7 (#87)	CBE0_B (#86)
AD5 (#91)	AD6 (#90)
AD3 (#95)	AD4 (#92)
AD1 (#99)	AD2 (#94)
(5VB) (#97)	AD0 (#96)
Ground (#101) **Used as open signal**	M66EN (#104)
	MPCIACTV_B (#122)

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11.3. DSP serial test interface

The test interface of the DSP is mapped onto the following Mini PCI bus interface pins:

ETD0	mapped to 8PMJ-3	(pin #3)
ETCK	mapped to 8PMJ-1	(pin #4)
ETD1	mapped to 8PMJ-6	(pin #5)
ETSYN	mapped to 8PMJ-2	(pin #6)
ETD2	mapped to 8PMJ-7	(pin #7)
ENGTEST	mapped to 8PMJ-4	(pin #8)
SDA	mapped to 8PMJ-8	(pin #9)
SCL	mapped to 8PMJ-5	(pin #10)

These signals are board outputs if the ENGTEST signal is driven high. ENGTEST is pulled down with 1k on the board. When ENGTEST is low, the DSP test signals are tri-stated.

The signals SDA and SCL are used to program the I2C serial EEPROM that contains configuration information for the PCI1410.

11.4. LED implementation

LED control signals for power presence and network activity are routed to the reserved pins of the system connector. On-board resistors of 301Ω limit the current consumption. The signals are active high.
The table below shows the LED implementation.

LED signal	Power presence	Network activity
Signal pin	12	11
Signal name	TDO_LED	TDO_LED_R

Table 2. LED signal implementation

11.5. Radio on/off switch implementation

The driver will come with a device on/off switch implementation. However, the hardware has a provision to switch the radio on or off as well. The PCI / MAC / PC-card interfaces are not affected by the state of the switch.
Edge connector pin #13, originally LED1_GRNN signal is used to control the state of the radio. When tied to ground, the radio will be disabled. The impact on the system can be compared to an out-of-range situation, which is different form the switch implementation in the driver.

11.6. External antenna connection

The location of the external antenna connectors is shown in Figure 2.

The MAIN antenna connector is a single coax connector that carries the RF transmit and receive signal as well as the antenna select signal. The antenna select signal is a bias voltage that has 3.3V CMOS levels; high for selecting the transmit/receive antenna and low for selecting the second receive antenna.

The AUX antenna connector, acts as a second receive antenna to provide a single solution Antenna Diversity Unit. Switch electronics for selection between the two antennas for reception of the strongest receive signals is provided onboard.

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