

PRODUCT SPECIFICATION

6223H-SRD

Wi-Fi Single-band 1x1 + Bluetooth 4.2 Combo Module

Version: v1.1



6223H-SRD Module Datasheet

Ordering Information	Part NO.	Description
	FG6223HSRD-00	RTL8723DS,b/g/n,Wi-Fi+BT4.2,1T1R,18X20mm,SDIO+Uart with shielding,PCB V1.0

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL:+86-755-2955-8186

Website:www.fn-link.com

CONTENTS

1. General Description	5
1.1 Introduction	5
1.2 Description	5
2. Features	6
3. Block Diagram	6
4. General Specification	7
4.1 2.4GHz RF Specification	7
4.2 Bluetooth Specification	8
5. ID setting information	8
6. Pin Definition	9
6.1 Pin Outline	9
6.2 Pin Definition details	9
7. Electrical Specifications	11
7.1 Power Supply DC Characteristics	11
7.2 Power Consumption	11
7.3 Interface Circuit time series	11
7.3.1 SDIO interface features	11
7.3.2 SDIO Power-on sequence	12
8. Size reference	14
8.1 Module Picture	14
8.2 Marking Description	15
8.3 Physical Dimensions	15
8.4 Layout Recommendation	16
9. The Key Material List	16
10. Reference Design	17
11. Recommended Reflow Profile	18
12. Package	19
12.1 Reel	19
12.2 Carrier Tape Detail	19
12.3 Packaging Detail	20
13. Moisture sensitivity	21

Revision History

[illegible]

1. General Description

1.1 Introduction

6223H-SRD is a high-performance WiFi & BT dual-mode transparent transmission module based on RTL8723DS-CG scheme. The module WiFi supports IEEE 802.11b/g/n standard, BT part supports br / EDR 4.2 standard and ble4.0. The WiFi part integrates WLAN Mac, 1t1r baseband and WLAN RF, supports 40m bandwidth, and the physical rate can be up to 150Mbps; BT part integrates BT protocol stack, BT baseband and BT RF. The data transmission interface supports sdio 1.1 / 2.0 interface and hs-uart interface. It is suitable for many application scenarios such as smart home, smart building, smart security, smart medicine, industrial Internet of things and so on.

1.2 Description

Model Name	6223H-SRD
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 18 x 20 x 2.5 mm
Wi-Fi Interface	Support SDIO2.0
BT Interface	UART
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 85°C

2. Features

General Features

- Support 20M and 40M bandwidth
- 2.4~2.4835GHz ISM band, supporting IEEE 802.11b/g/n
- 1T1R, Maximum physical rate 150Mbps (40MHz bandwidth)
- support 802.11i (WPA, WPA2), 802.11e QoS Enhancement (WMM)

Host Interface

- WLAN support SDIO Interface

3. Block Diagram



For confidential use only

4. General Specification

4.1 2.4GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz: Ch1 ~ Ch14	
Test Items	Typical Value	EVM
Output Power	802.11b /11Mbps : 17dBm $\pm$ 2 dB	EVM $\leq$ -10dB
	802.11g /54Mbps : 14dBm $\pm$ 2 dB	EVM $\leq$ -25dB
	802.11n /MCS7 : 13dBm $\pm$ 2 dB	EVM $\leq$ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	$\pm$ 20ppm	
Test Items	TYP Test Value	Standard Value
Receive Sensitivity (11b,20MHz) @8% PER	- 11Mbps PER @ -87 dBm	$\leq$ -76
Receive Sensitivity (11g,20MHz) @10% PER	- 54Mbps PER @ -73 dBm	$\leq$ -65
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=7 PER @ -70 dBm	$\leq$ -64
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=7, PER @ -67 dBm	$\leq$ -61

Note:

Ch1 ~ Ch13 for EU&KCC&RCM use only

Ch1 ~ Ch14 for MIC use only

Ch1 ~ Ch11 for FCC use only

Power in dBm units for FCC

4.2 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth 2.1/4.2; v4.2 BR/EDR, v4.0 BLE		
Host Interface	UART		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, $\pi/4$ -DQPSK, 8-DPSK		
RF Specification			
	Min(dBm)	Typical(dBm)	Max(dBm)
Output Power (BR/EDR/BLE)		4.5	8
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-78	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-75	
Sensitivity @PER=30.8% FOR BLE		-95	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

Note:

Power in dBm units for FCC

5. ID setting information

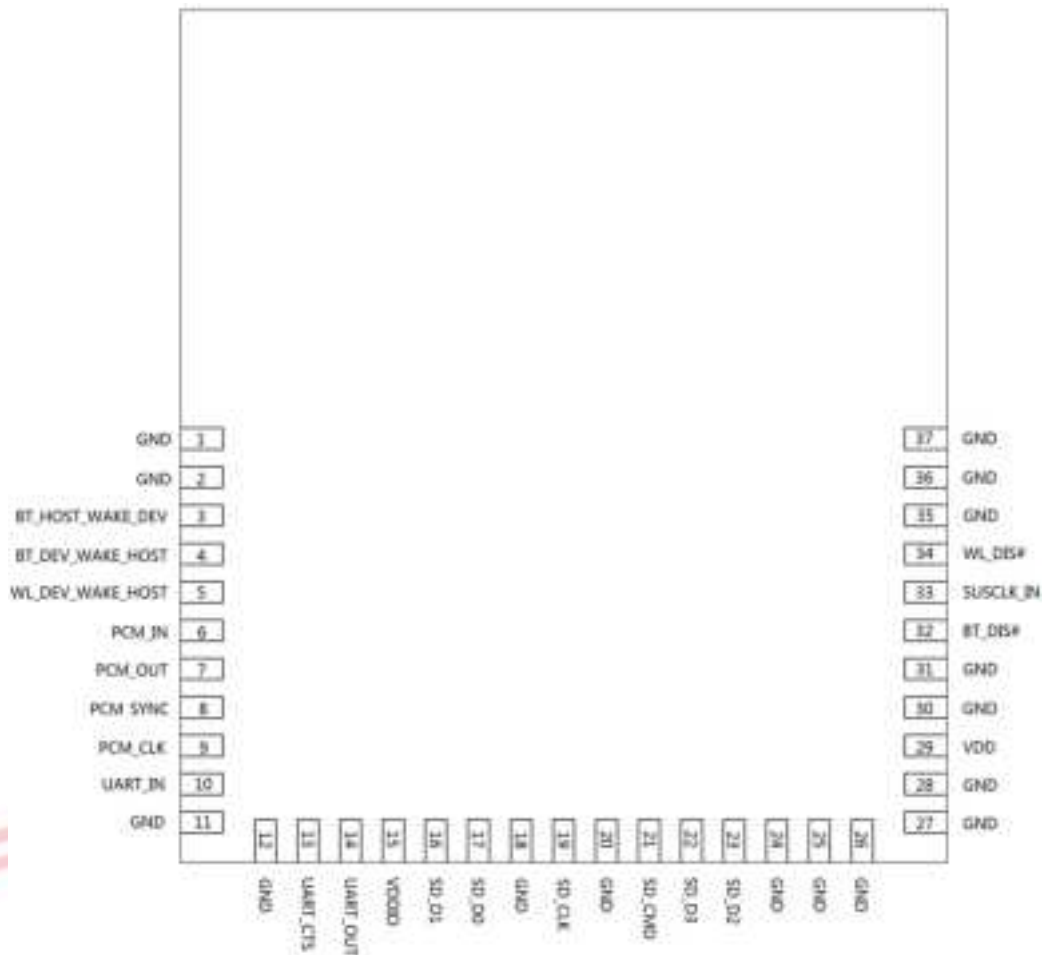
WI-FI

Vendor ID	-
Product ID	-

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND		Ground connections	
2	GND		Ground connections	
3	BT_HOST_WAKE_DEV	I	BT host wake-up device	
4	BT_DEV_WAKE_HOST	O	BT device wake-up host	
5	WL_DEV_WAKE_HOST	I	WiFi device wake-up host	
6	PCM_IN	I	PCM Input	VDDIO
7	PCM_OUT	O	PCM Output	VDDIO
8	PCM_SYNC	O	PCM Sync	VDDIO
9	PCM_CLK	I/O	PCM Clock	VDDIO

10	UART_IN	I	UART Input	VDDIO
11	GND		Ground connections	
12	UART_RTS	O	UART_RTS	
13	UART_CTS	I	UART_CTS	VDDIO
14	UART_OUT	O	UART Output	VDDIO
15	VDDIO		IO 口电源	
16	SD_D1	I/O	SDIO data line 1	
17	SD_D0	I/O	SDIO data line 0	
18	GND		Ground connections	
19	SD_CLK	I	SDIO clock line	
20	GND		Ground connections	
21	SD_CMD	I/O	SDIO command line	
22	SD_D3	I/O	SDIO data line 3	
23	SD_D2	I/O	SDIO data line 2	
24	GND		Ground connections	
25	GND		Ground connections	
26	GND		Ground connections	
27	GND		Ground connections	
28	GND		Ground connections	
29	VDD		Main power source input	3.3V
30	GND		Ground connections	
31	GND		Ground connections	
32	BT_DIS#	I	Pull high: ON , Pull low: OFF External pull low can disable BT	3.3V
33	SUSCLK_IN	I	External Clock input(32.768kHz). Can keep NC.	
34	WL_DIS#	I	Pull high: ON , Pull low: OFF External pull low can disable WL	3.3V
35	GND		Ground connections	
36	GND		Ground connections	
37	GND		Ground connections	

P:POWER I:INPUT O:OUTPUT VDDIO:3.3V

7. Electrical Specifications

7.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	0	25	70	deg.C
VCC33	3.0	3.3	3.6	V

7.2 Power Consumption

Power Consumption	2.4GHz TX	11M	303.46770 mA
		54M	124.17243 mA
		MCS7 HT20	111.39868 mA
		MCS7 HT40	107.41647 mA
	BT TX	DH1	167.63446 mA
		2DH3	165.29668mA
		3DH5	167.12981 mA
		BLE	151.16540mA

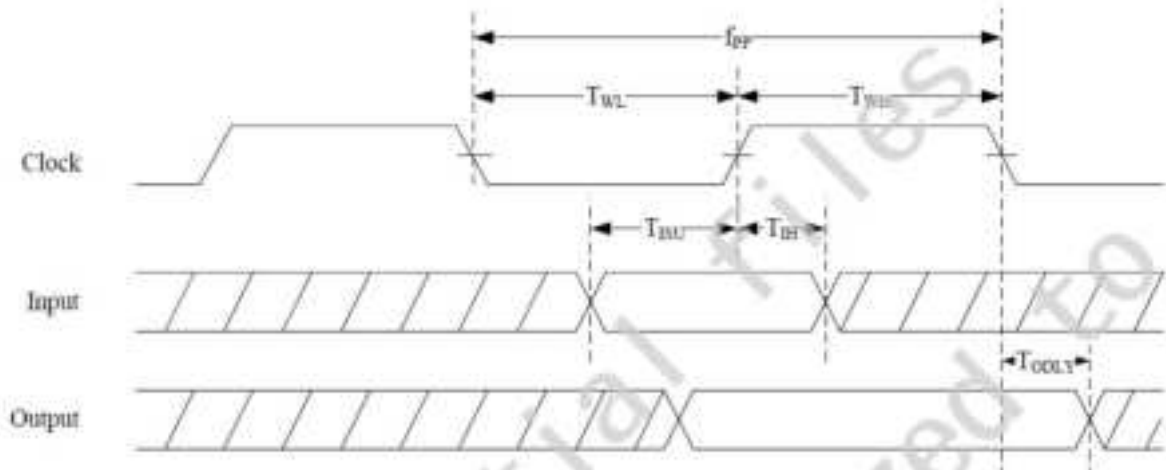
7.3 Interface Circuit time series

7.3.1 SDIO interface features

PIN4 BT_DEV_WAKE_HOSTD suggests to do drop-down processing, When the module is powered on, the low-level holding time shall be $\geq 200\text{ms}$.

SDIO routing requirements: 1. SDIO CLK routing shall surround the ground wire and be far away from CMD and data routing; 2. The number of via of SDIO routing layer shall be less than 4; 3. The length error of each routing line of SDIO shall be less than $\pm 100\text{mil}$, and the total length shall be less than 2.5inches;

SDIO interface characteristic requirements:



NO	Parameter	Mode	MIN	MAX	Unit
fpp	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
TWL	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
TWH	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
TISU	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
TIH	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
TODLY	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

7.3.2 SDIO Power-on sequence

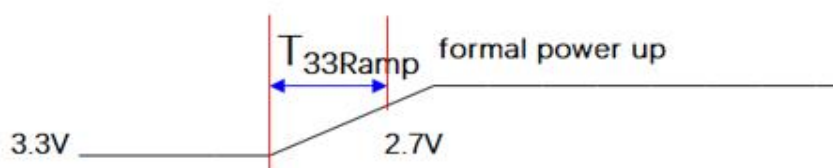


	Min	Typical	Max	Unit
T33ramp	0.2	0.5	2.5	ms
T18ramp	0.2	0.5	2.5	ms
Tnon-rdy	1	2	10	ms

Symbol	Description
T _{33ramp}	The 3.3V main power ramp up duration.
T _{18ramp}	The 1.8V main power ramp up duration.
T _{non_rdy}	SDIO Not Ready Duration. In this state, the RTL8723DS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

7.3.2 module power-on&off time sequence

	Min	Typical	Max	Unit
T33 power on ramp	0.2	0.5	2.5	ms
T33 power off ramp	0.2	5	10	ms



Note:

1. 上下电时序请满足表格要求;

The power up ramp and power down ramp must meet the following table.

2. 上下电过程如有较长时间中间电压停留都会有几率导致 efuse 被窜写;

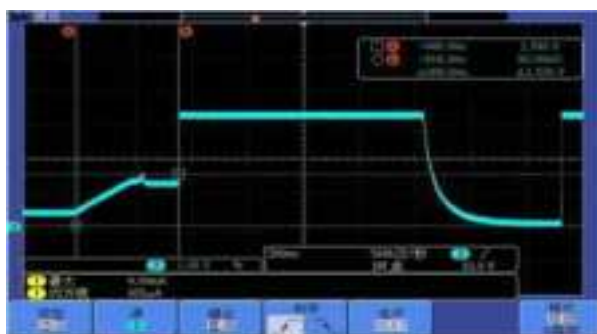
If climbing process for a long time during power-on and power-off, It may cause efuse to be overwritten.

3. 建议主芯片上电完成后, 再给模组上电;

it is recommended to power on the module after platform side.

4. 如有下图所示异常上下电时序, 务必做相应调整符合时序规格;

If your power on/off timing as below shown, must modify to meet the timing specification.



异常上电时序



异常下电时序

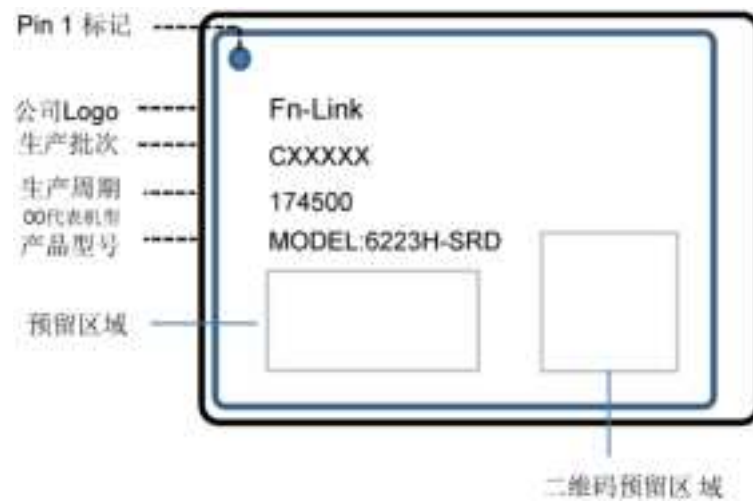
8. Size reference

8.1 Module Picture

L x W : 18 x 20 (+0.3/-0.1) mm For confidential use only	
H: 2.5 (±0.2) mm	
Weight	1.25±0.2g

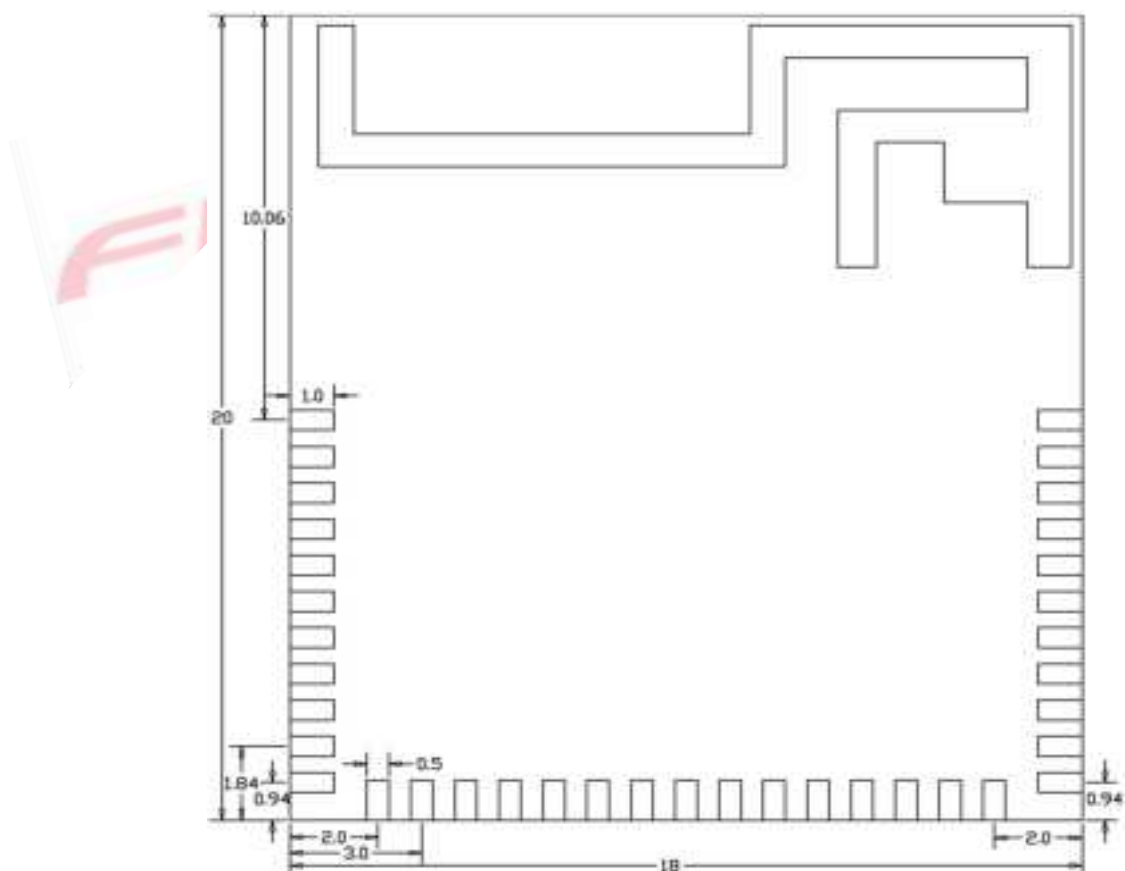
8.2 Marking Description

< TOP VIEW >

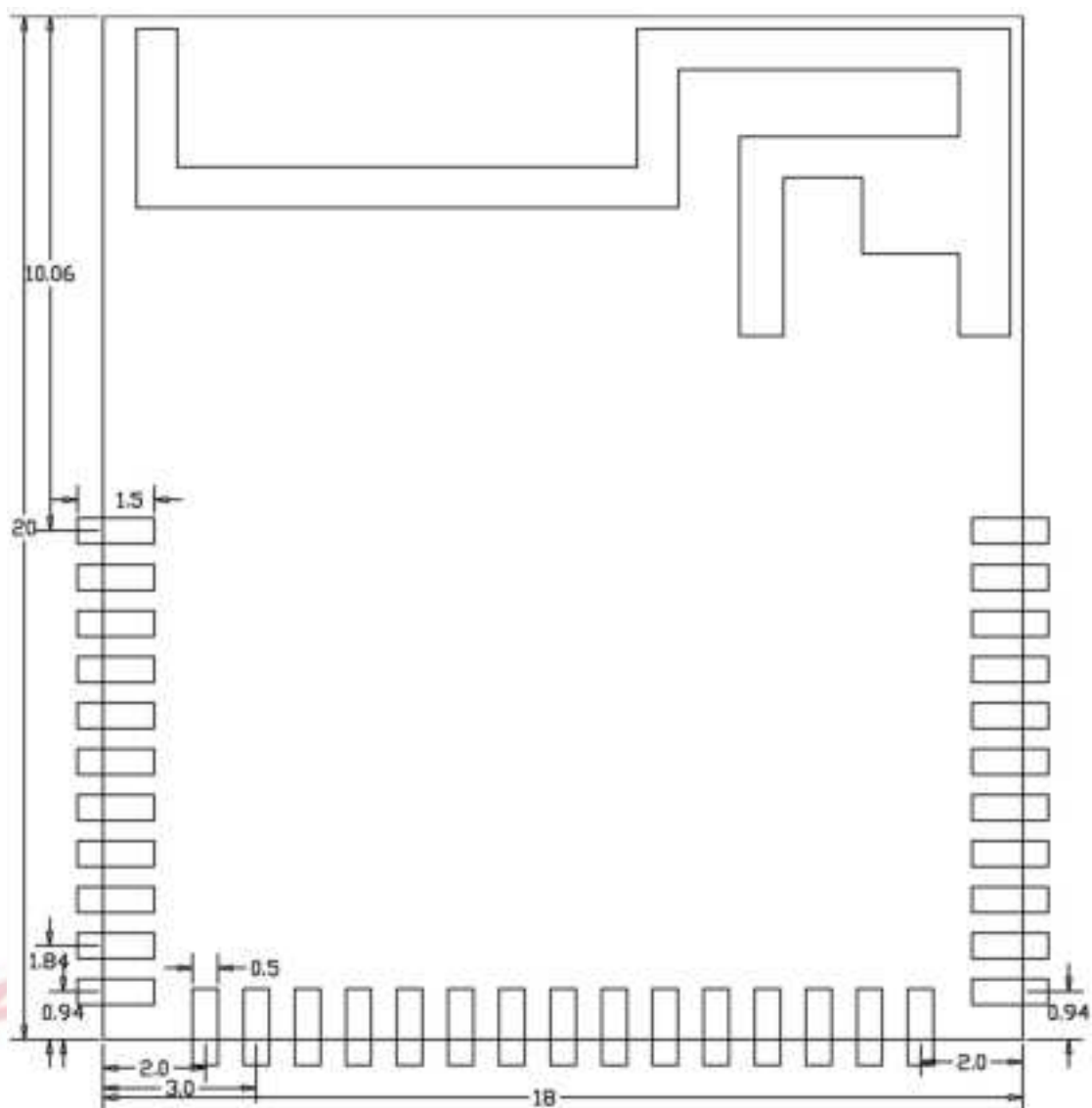


8.3 Physical Dimensions

<TOP View>



8.4 Layout Recommendation



9. The Key Material List

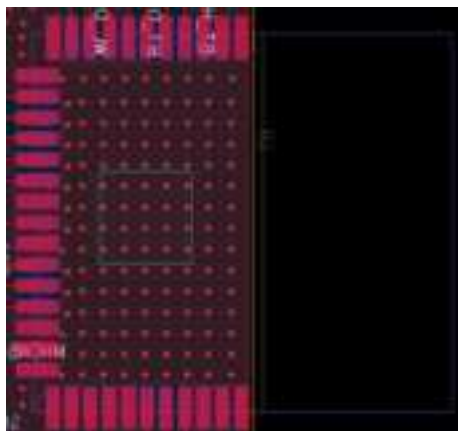
Item	Part Name	Description	Manufacturer
1	PCB	6223H-SRD 4L,FR4,18X20X0.8mm	XY-PCB, GDKX, Sunlord, SLPCB
2	Crystal	2520 24MHz 10pF ± 10 ppm	ECEC, Hosonic, TKD, JWT
3	Chipset	RTL8723DS-CG QFN48	Realtek
4	Shielding	6223H-SRD Shielding	信太, 精力通

10. Reference Design

For confidential use only



Design requirements for the relative position between mhcwbt1p-b onboard antenna and the backplane: the module pin is placed close to the edge of the backplane, as shown in the figure below:



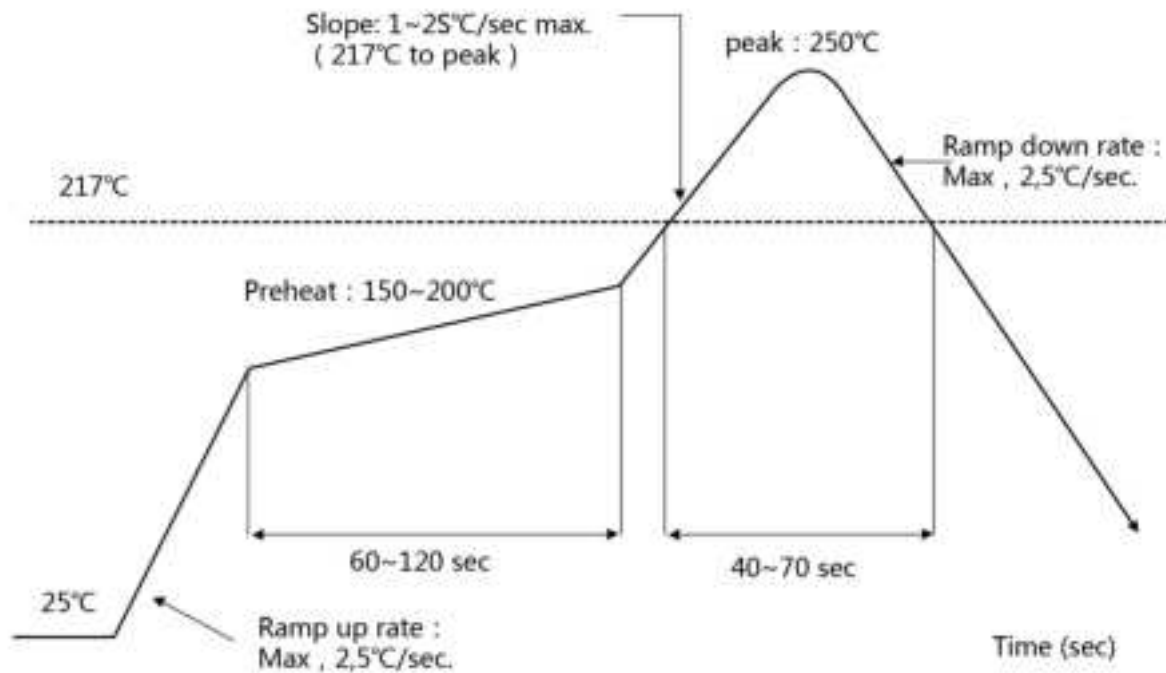
Note: 1. The distance between the module peripheral device pad and the module pad shall be at least greater than 1mm.
2. It is recommended that the module pad be made of stepped steel mesh.

11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : $<250^{\circ}\text{C}$

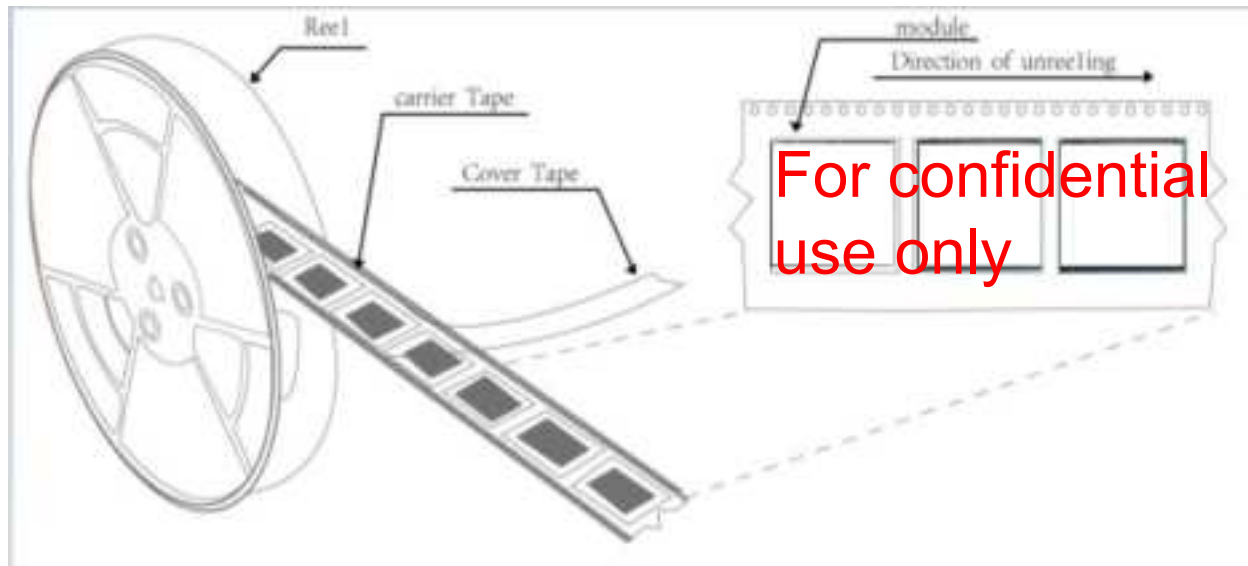
Number of Times : ≤ 2 times



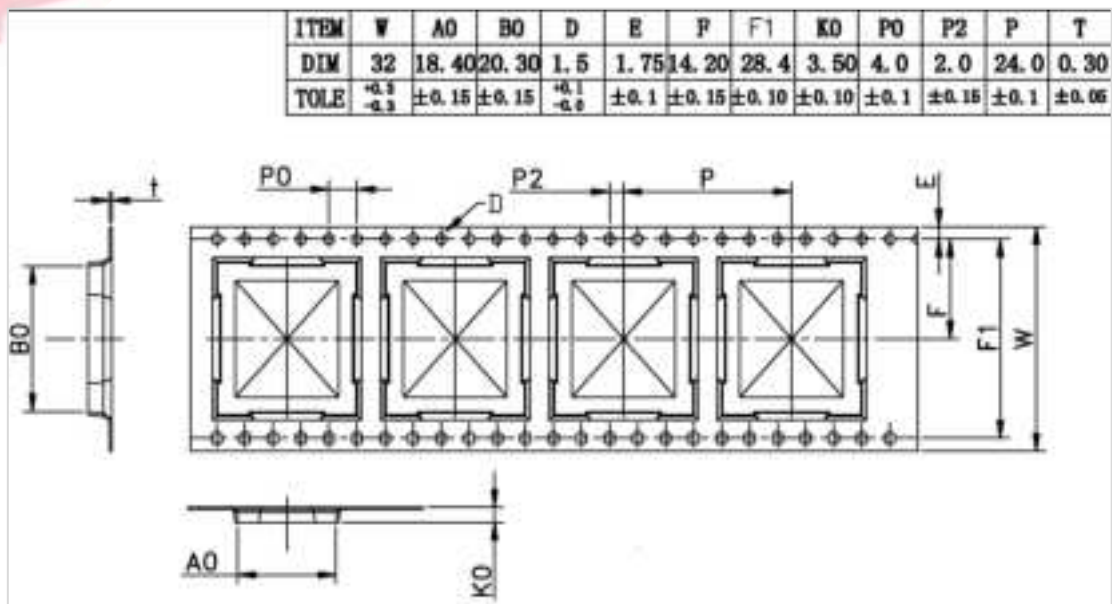
12. Package

12.1 Reel

A roll of 800 pcs



12.2 Carrier Tape Detail



12.3 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape: 32mm*20.2m the cover tape :25.5mm*32.6m

Color of plastic disc: blue



NY bag size:450mm*415mm



size : 350*350*35mm



The packing case size:360*210*370mmg

13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
- b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- d) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
- e) Baking is required if conditions b) or c) are not respected
- f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

