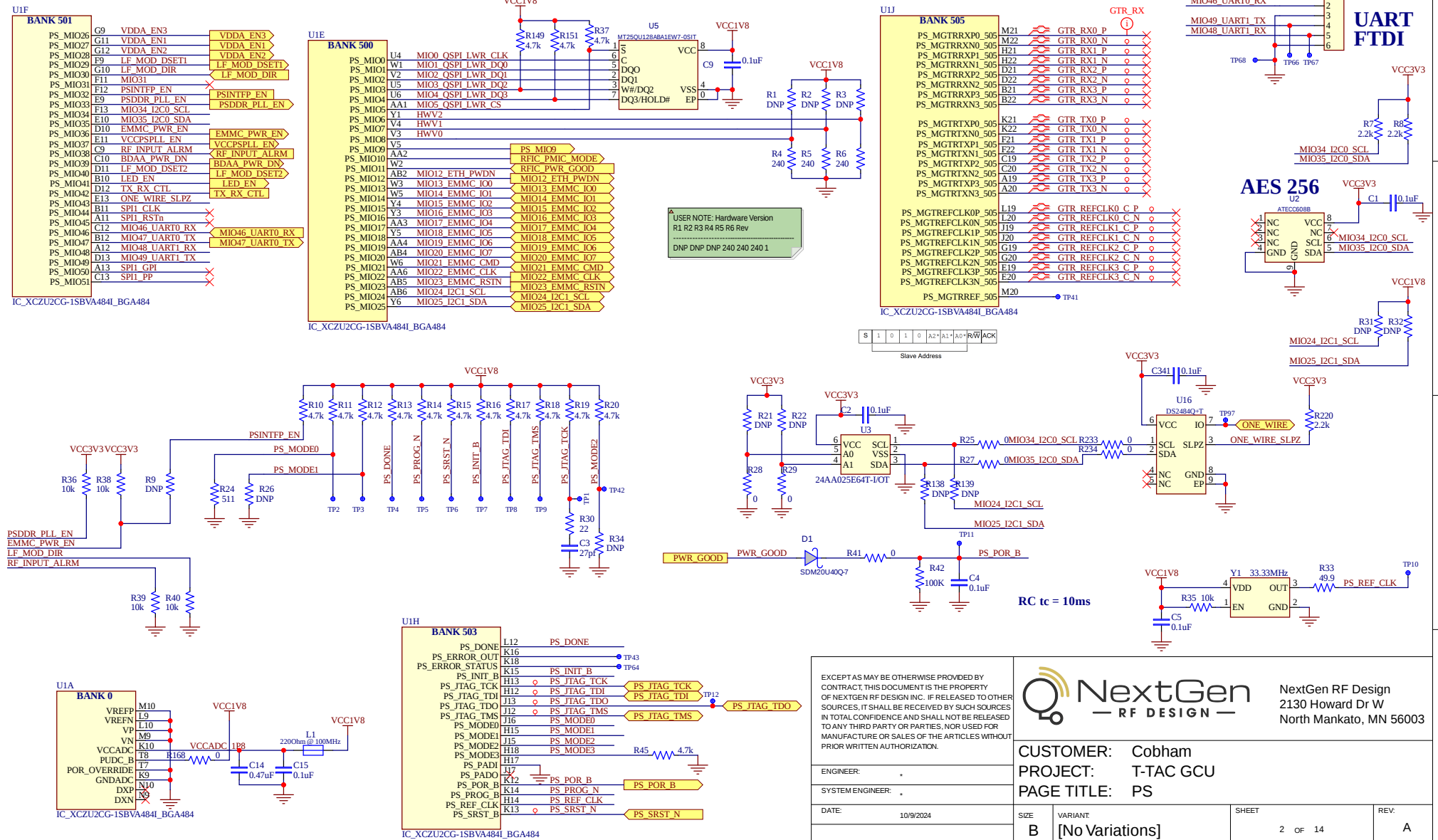


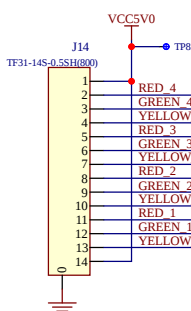
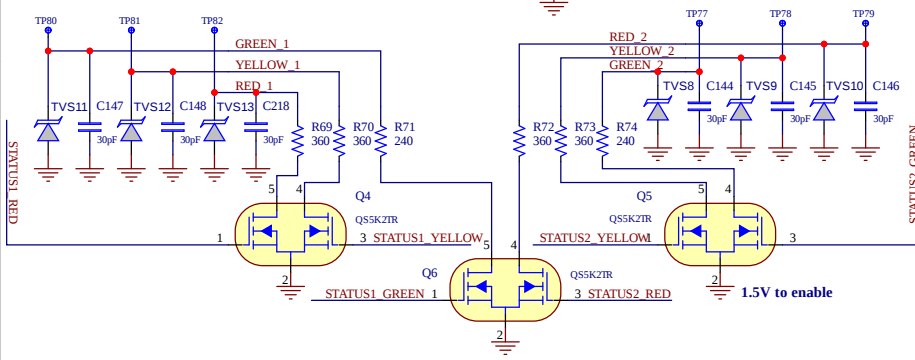
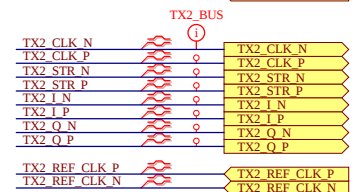
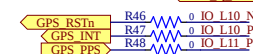
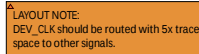
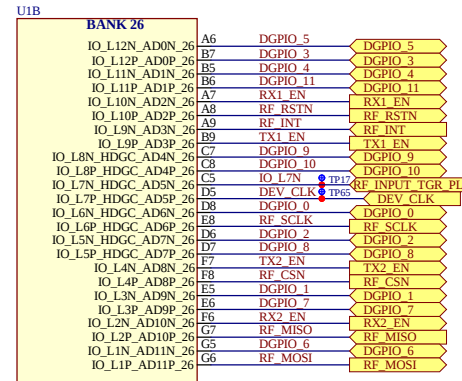
BASEBAND PROCESSING SYSTEM (PS)



Bank 65 and 66 are HP banks supporting <= 1.8V standards with full differential support. Bank 65 supports several MIPI PHY channels when supplied with 1.2V.

Bank 26 is a HD bank supporting <= 3.3V standards. Only differential receive is supported in HD banks. External differential termination is required.

All banks have 4 pair of global clocks.



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NextGen RF Design
2130 Howard Dr W
North Mankato, MN 56003

CUSTOMER:	Cobham
PROJECT:	T-TAC GCU
PAGE TITLE:	PI

SIZE	VARIANT:
B	[No Variations]

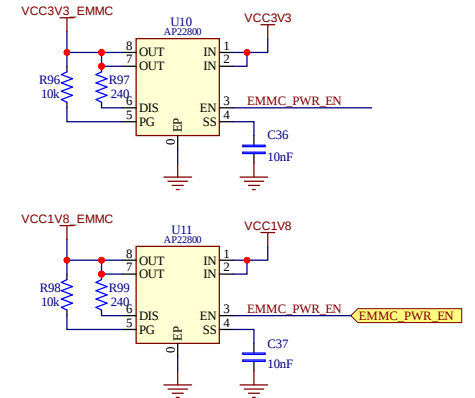
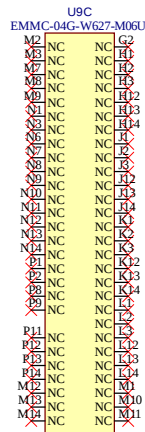
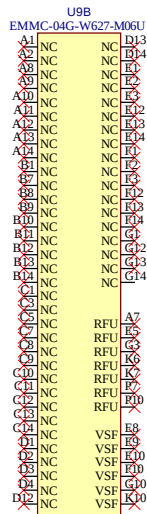
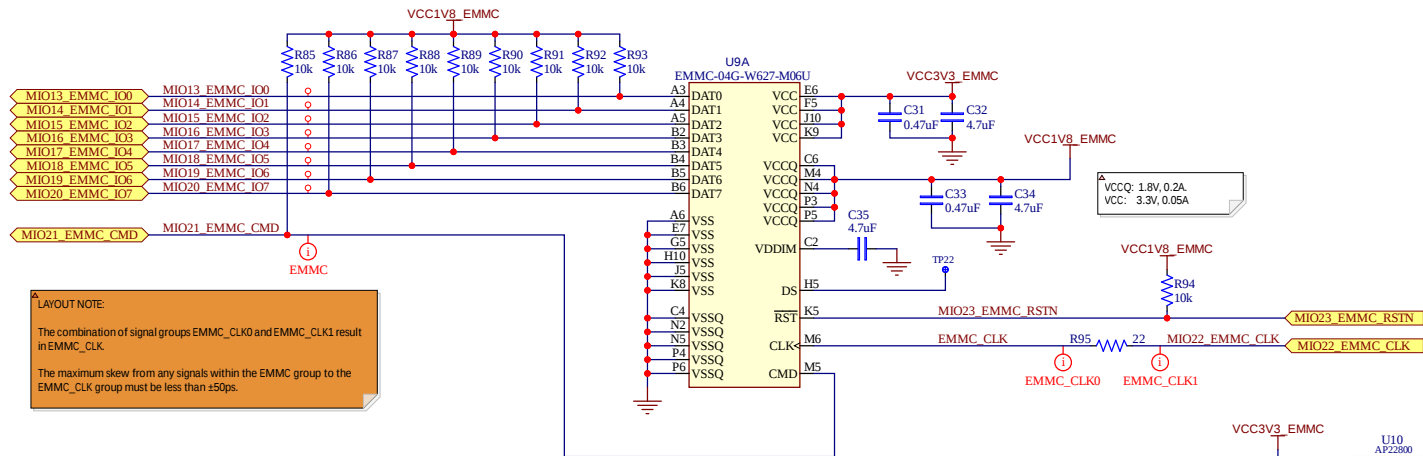
SHEET

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REV: A



4GB eMMC



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CUSTOMER: Cobham
PROJECT: T-TAC GCU
PAGE TITLE: eMMC

SIZE: B
VARIANT: [No Variations]
SHEET: 5 OF 14
REV: A

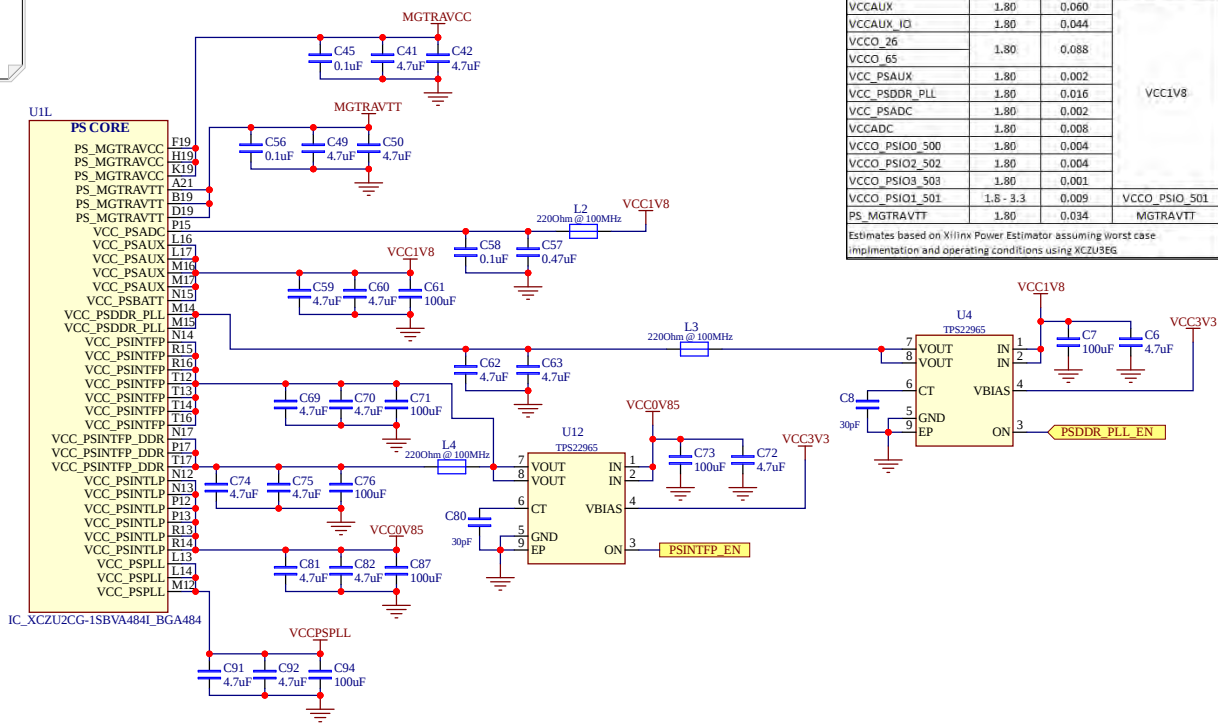
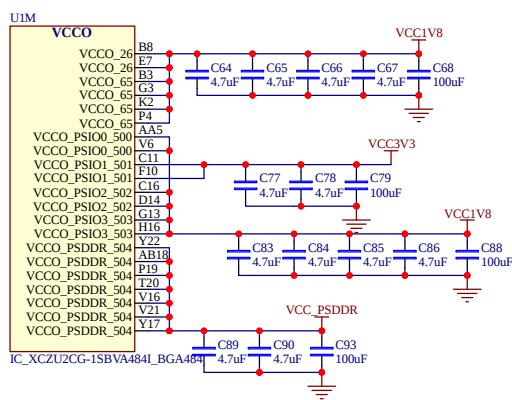
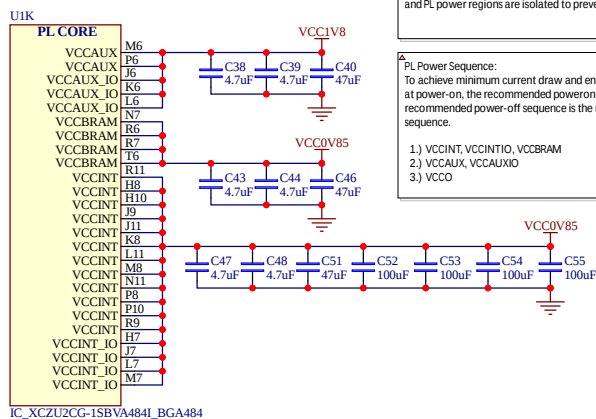
BASEBAND PROCESSOR POWER

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

PL Power Sequence:
To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power on sequence is listed. The recommended power-off sequence is the reverse of the power-on sequence.

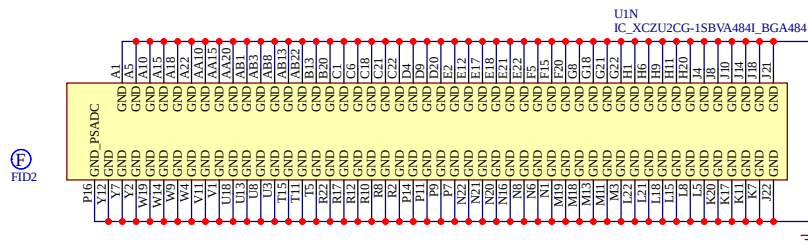
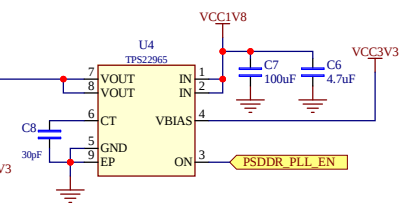
- 1.) VCCINT, VCCINTIO, VCCBRAM
- 2.) VCCAUX, VCCAUXIO
- 3.) VCCO

LAYOUT NOTE:
Larger 100uf capacitors can be placed away from pins.
Smaller 0201 capacitors should be placed next to
corresponding pin. Each capacitor should have its own
ground and power vias.



Power Supply Estimates			Supply
	Voltage	Current (A)	
VCCINT	0.85	4.090	VCC0V85
VCCINT_IQ	0.85	0.105	
VCCBRAM	0.85	0.070	
VCC_PSINTLP	0.85	0.207	
VCC_PSINTFP	0.85	1.148	
VCC_PSINTFP_DDR	0.85	0.399	
PS_MGTTRAVCC	0.85	0.251	MGTTRAVCC
VCC0_PSDDR_504	1.10	0.147	VCC0_PSDDR
VCC_PSPLL	1.20	0.063	VCC_PSPLL
VCCAUX	1.80	0.060	VCC1V8
VCCAUX_IQ	1.80	0.044	
VCC0_26	1.80	0.088	
VCC0_65			
VCC_PSAUX	1.80	0.002	
VCC_PSDDR_PLL	1.80	0.016	
VCC_PSDAC	1.80	0.002	
VCCADC	1.80	0.008	
VCC0_PSI00_500	1.80	0.004	
VCC0_PSI02_502	1.80	0.004	
VCC0_PSI03_503	1.80	0.001	VCC0_PSI0_501
VCC0_PSI01_501	1.8 - 3.3	0.009	
PS_MGTTRAVTT	1.80	0.034	

Estimates based on Xilinx Power Estimator assuming worst case implementation and operating conditions using XCZU3EG



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PROJECT:	T-TAC GCU
PAGE TITLE:	BBP Power

SIZE	VARIANT:
B	[No Variations]

SHEET

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REV:	A
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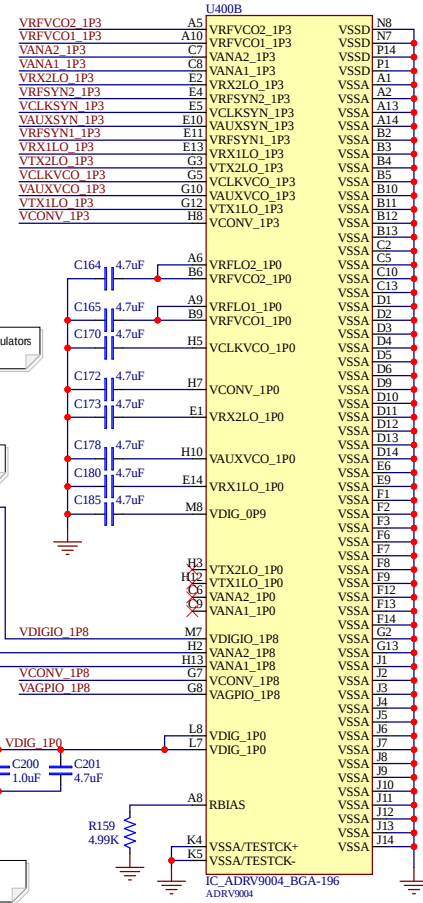
RFIC POWER

VDDA_1P3
1.3V @ 1.3A max

VDDA_1P8
1.8V @ 0.4A max

Internal LDO Regulators

VDDA_1P0
1.0V @ 0.6A max



LAYOUT NOTE:
Ferrite bead and 47uF cap can be placed further from ADRV9002. All 0201 capacitors should be placed close to corresponding ADRV9002 power pin. Bottom side routing between the 0603/47uF capacitor and 0201 capacitor is permitted for short traces. Longer traces should be striplines. Each capacitor should have its own ground via. Each power pin should have its own power via and not be connected to adjacent pins directly.

See UG-1828 for recommended PCB routing of ADRV9002

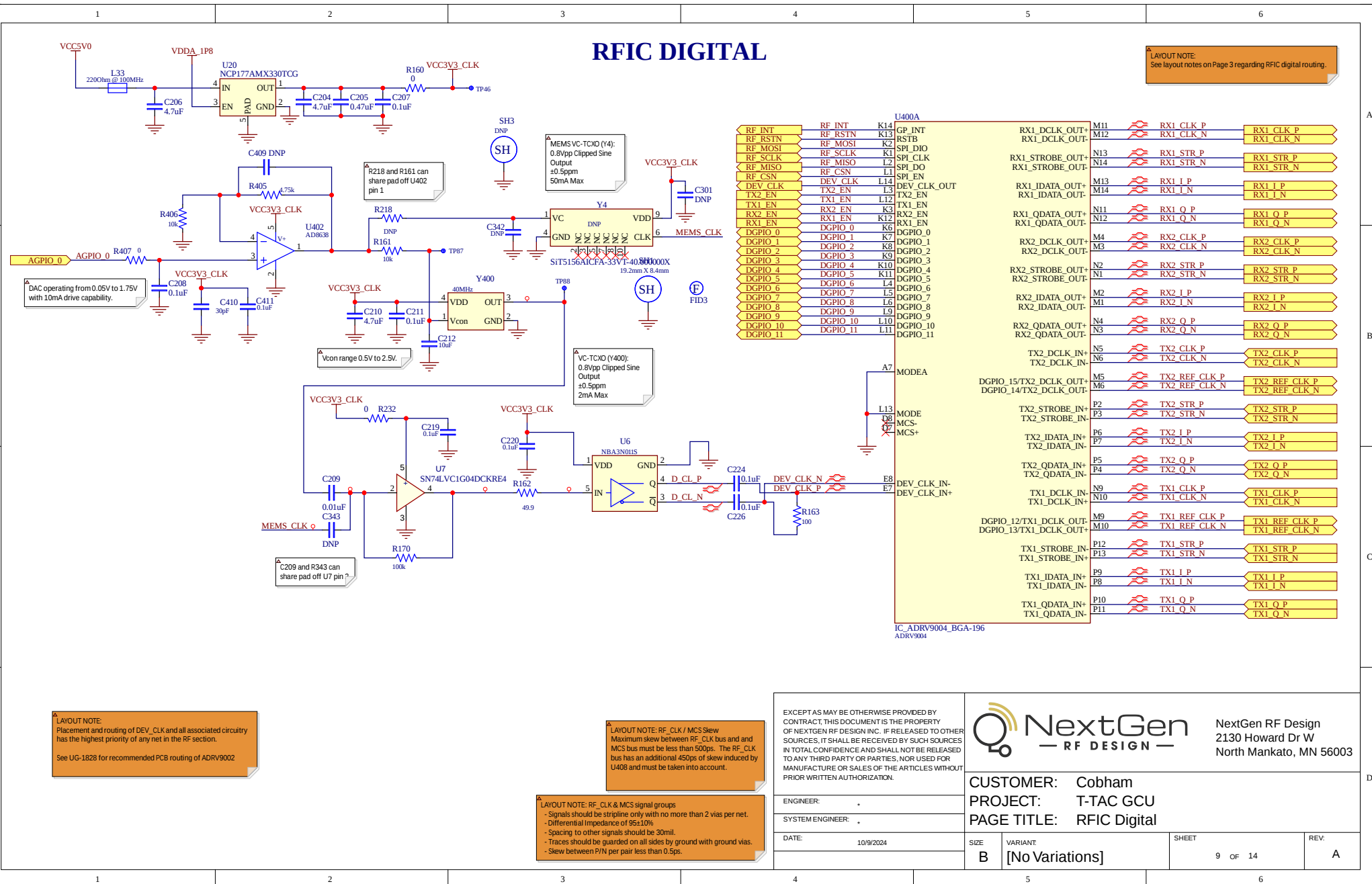
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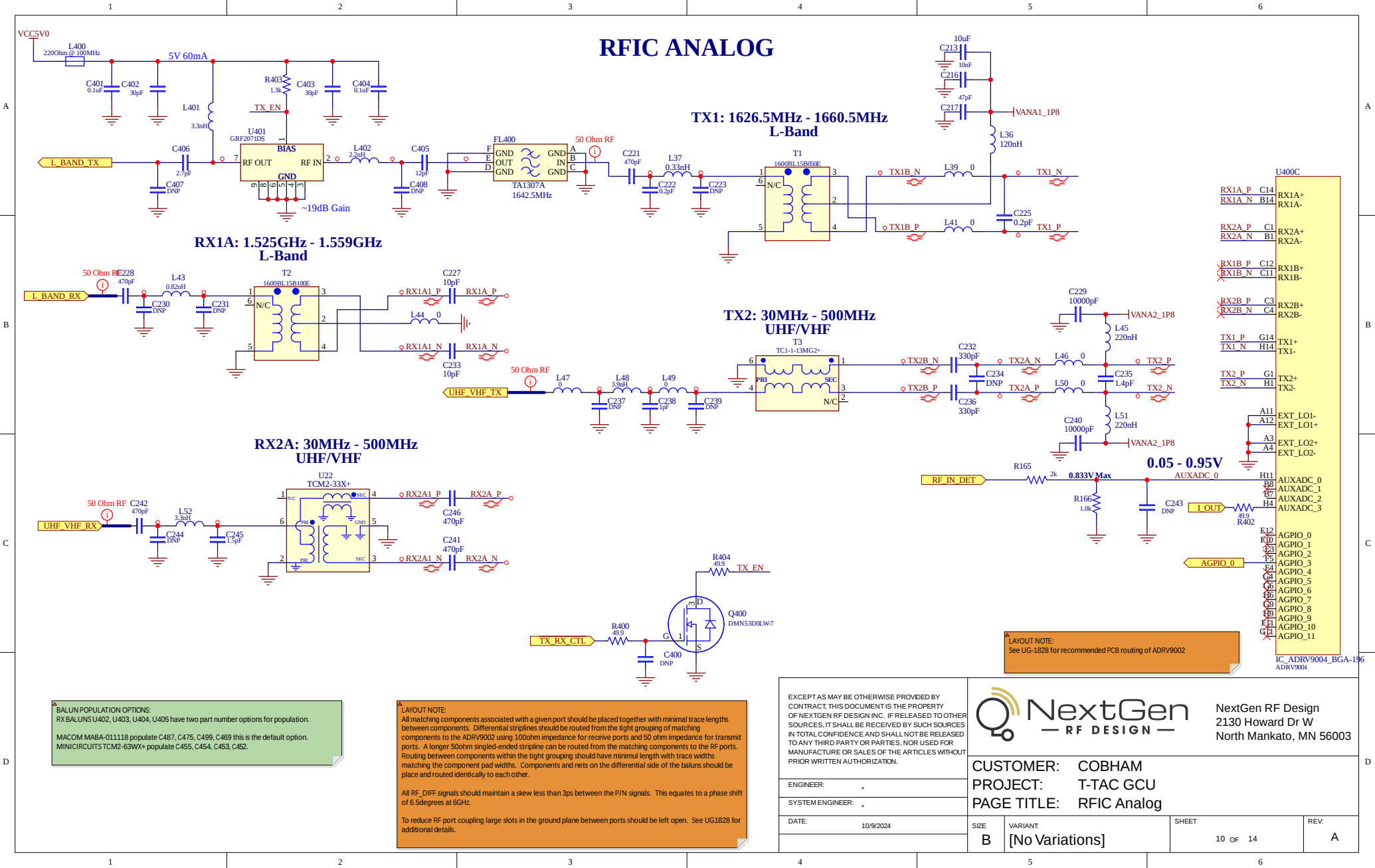
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PROJECT: T-TAC GCU
PAGE TITLE: RFIC Power

SIZE	VARIANT	SHEET	REV.
B	[No Variations]	8 OF 14	A



RFIC ANALOG



BALUN POPULATION OPTIONS:
 RX BALUNS U402, U403, U404, U405 have two part number options for population.
 MACOM MABA-011118 populate C487, C475, C499, C469 this is the default option.
 MINICIRCUITS TCM2-63WX+ populate C455, C454, C453, C452.

LAYOUT NOTE:
 All matching components associated with a given port should be placed together with minimal trace length between components. Differential striplines should be routed from the tight grouping of matching components to the ADRV9002 using 100ohm impedance for receive ports and 50 ohm impedance for transmit ports. A longer 50ohm single-ended stripline can be routed from the matching components to the RF ports. Routing between components within the tight grouping should have minimal length with trace widths matching the component pad widths. Components and nets on the differential side of the baluns should be placed and routed identically to each other.
 All RF DIFF signals should maintain a skew less than 3ps between the P/N signals. This equates to a phase shift of 6.5degrees at 6GHz.
 To reduce RF port coupling large slots in the ground plane between ports should be left open. See UG1828 for additional details.

LAYOUT NOTE:
 See UG-1828 for recommended PCB routing of ADRV9002

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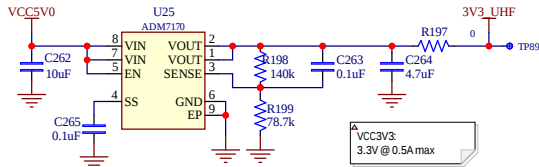
SYSTEM ENGINEER: *

DATE: 10/9/2024

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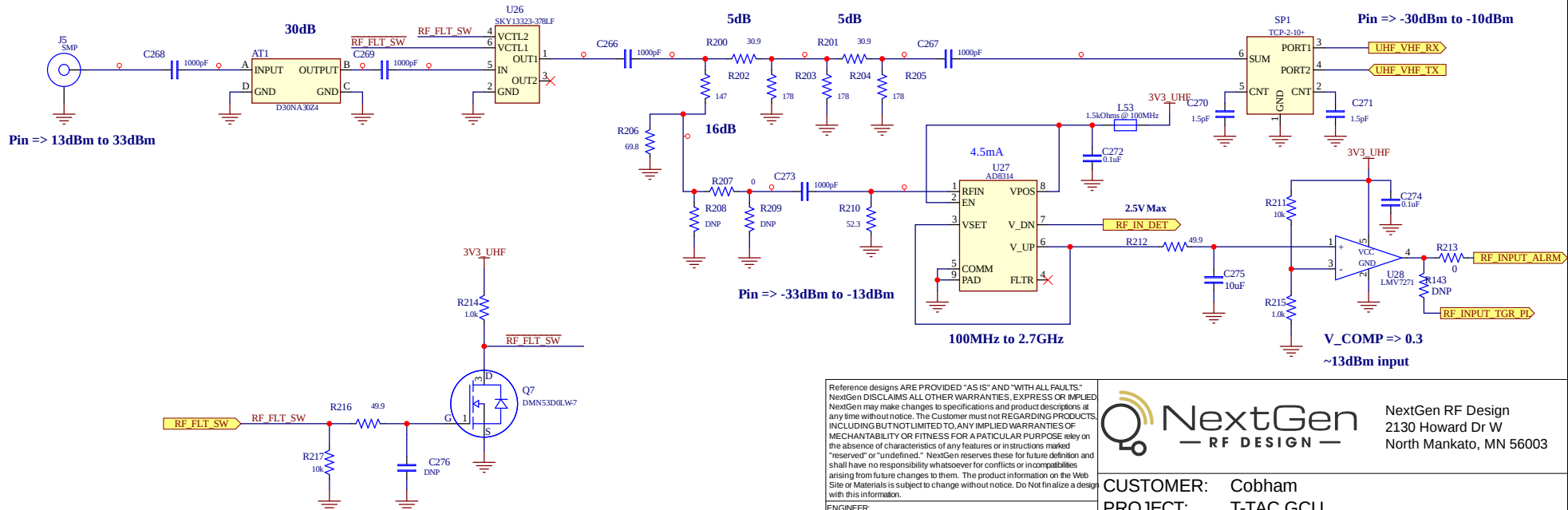
CUSTOMER: COBHAM
PROJECT: T-TAC GCU
PAGE TITLE: RFIC Analog

SIZE	VARIANT	SHEET	REV.
B	[No Variations]	10 OF 14	A



UHF/VHF IO (MCX to BNC)

RX FAULT SWITCH
VCTL1 =>1 ; VCTL2 =>0 ; IN to OUT1 (Default)
VCTL1 =>0 ; VCTL2 =>1 ; IN to OUT2



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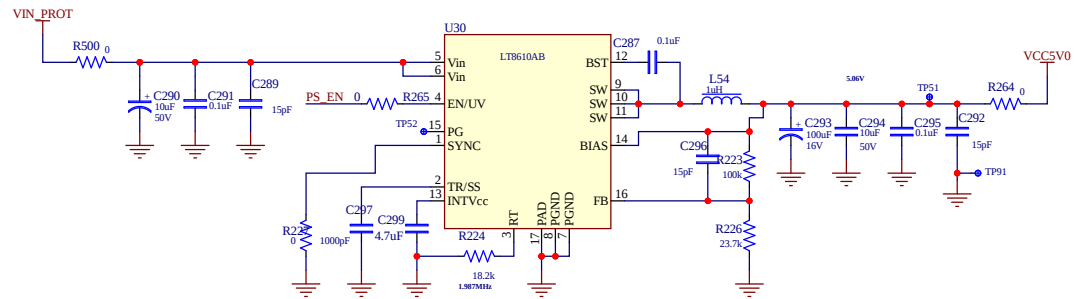
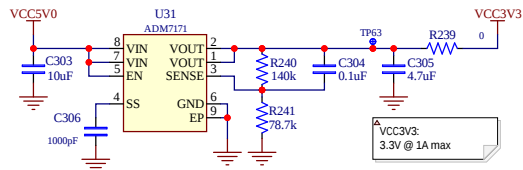
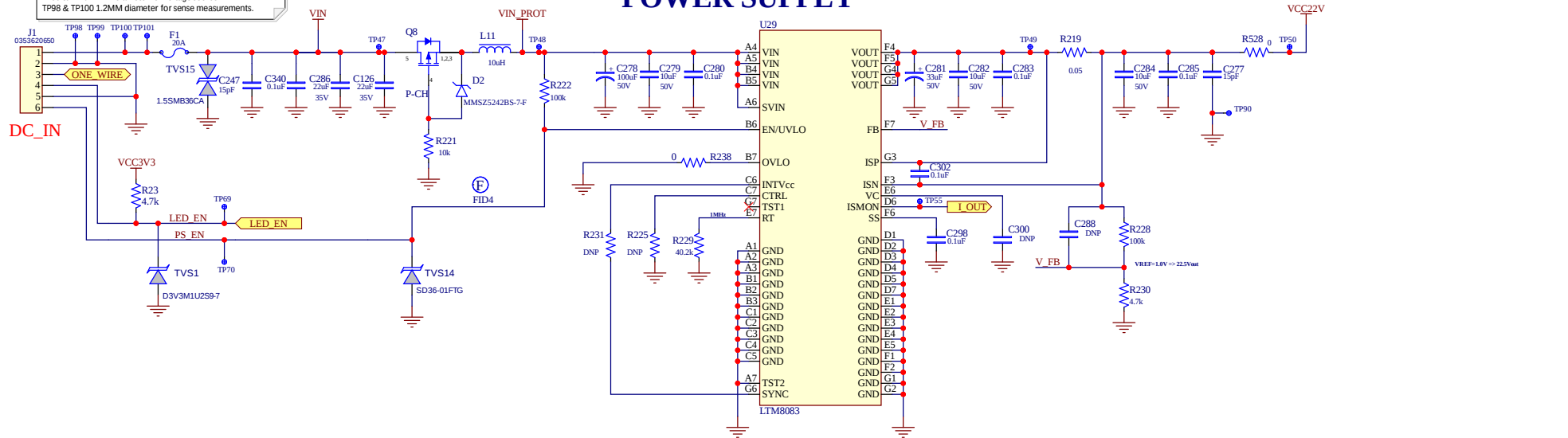
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PROJECT: T-TAC GCU
PAGE TITLE: UHF/VHF

SIZE B	VARIANT [No Variations]	SHEET 12 OF 14	REV. A
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POWER SUPPLY

Test Points:
TP99 & TP101 2MM diameter for voltage source.
TP98 & TP100 1.2MM diameter for sense measurements.



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PAGE TITLE: JTAG & Power

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DATE: 10/9/2024

SIZE: B
VARIANT: [No Variations]
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REV: A

L-Band IO

Verify SMP

Bias-T

VCTL1=>1 : VCTL2=>0 : IN to OUT1 (Default RX)
VCTL1=>0 : VCTL2=>1 : IN to OUT2

3V3_RX
3.3V 15mA

VCC3V3

VCC1V8

15dBm Max

GPS PPS

GPS INT

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

GPS RSTn

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PAGE TITLE: L-Band RF LF Modem

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SIZE: B
VARIANT: [No Variations]
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REV: A