Measurement Result of Processing Gain for GH2405MS DSST Basic Phone

1. Introduction

1.1 Scope

These documents are a telian engineering test report for model GH2405MS basic cordless phone, which contains the results of measurement of the processing gain of Dsst phone.

1.2 Reference documents

This section lists documents that are referenced or are materially relevant to these documents.

Code of federal regulations, Title 47,Chapter1, Part 15 Radio frequency device(FCC)

1.3 Definitions

1	FCC	Federal Communication Commission
2	SNR	Signal to Noise Ratio
3	JSR	Jammer to Signal Ratio
4	CW	Continuous Wave (Jammer)
5	HS	Handset
6	BS	Base station
7	DBPSK	Differential Binary Phase Shift Keying

Table 1: Definitions & Abbreviations

2. An overview of the FCC method for measuring processing gain

Two methods are specified for measuring the processing gain by the FCC in 15.247(e). The first method simply involves calculating the signal to noise ratio (SNR) with the spreading code switched on and the signal to noise ratio (SNR) with the spreading code switched off.

The difference between two methods is called as the processing gain. The SNR is measured at the demodulated output of the receiver. In principle this is an acceptable method to measure the processing gain of any direct sequence spread spectrum communication system , however, it does not take into consideration that the non-spread spectrum portion of the system may operate under the assumption that the signal being transmitted is a spread spectrum signal and when the spreading code is switched off the system may fail to operate at greatly reduced efficiency, in either case the measurement of processing gain will be meaningless.

The second method specified by the FCC to measure processing gain is detailed in 15.247 (e)(1). This involves transmitting a CW jammer in the RF pass-band of the system and measuring the jammer to signal ratio (JSR) required to achieve a certain bit error rate. The choice of the actual value of the bit error rate (BER) is left up to the tester. The jammer is stepped in 50KHz increments across the entire pass-band and in each case the JSR to achieve the desired bit error rate is measured. The JSR is measured at the RF input to the system under test. The lowest 20% of the JSR data are discarded. The processing gain can then be calculated as follows;

$$Gp = (S/N)theory + (J/S)\ measured + Lsystem$$

Where Gp is the processing gain, the SNR is the theoretically predicted for the system under the test to achieve the desired bit error rate, the JSR is the lowest value (in dB) in the remaining data set and Lsys adjusts for non-ideal system losses. Lsys can not be greater than 2dB.

3. Processing gain

The following parameters were used in the test set-up.

1	HS TX Power(dBm)	-3.6	
2	BS LNA Gain(dB)	0	
3	Test system losses (Signal) (dB)	-14.5	-4.0dB(system),-3.0dB(signal combiner) -7.5dB(cable loss)
4	Test system losses (Jammer) (dB)	-5.6	-3.0 dB (signal combiner) -2.6 dB (cable loss)

Table 2: Test set-up parameter

The following measurement results were taken at the base station.
The desired bit error rate was set at e-3

Jammer Freq. (MHz)	BER(BS)	Received jammer Power(dBm)	Received signal Power (dBm)	Jammer/Signal Ratio(dB)
2404.8 MHz	1.14 x e-3	-16.5	-18.6	2.1
2406.8 MHz	9.74 x e-4	-16.0	-18.2	2.2
2408.4 MHz	1.14 x e-3	-17.2	-19.3	2.1
2410.2 MHz	9.6 x e-3	-16.1	-18.6	2.5
2412.0 MHz	9.7 x e-4	-17.4	-19.6	2.2
2413.8 MHz	1.1 x e-3	-16.0	-18.2	2.2
2415.6 MHz	1.2 x e-3	-17.5	-19.6	2.1
2417.4 MHz	1.6 x e-4	-16.0	-18.5	2.5
2419.2 MHz	1.3 x e-3	-17.5	-19.6	2.1
2421.0MHz	9.2 x e-4	-16.9	-19.2	2.3
2422.8 MHz	1.4 x e-3	-16.6	-19.6	3.0
2424.6 MHz	1.1 x e-3	-17.0	-18.1	1.1
2426.4 MHz	1.0 x e-3	-17.5	-18.6	1.1
2428.2 MHz	9.2 x e-4	-17.0	-19.2	2.2
2430.0 MHz	1.1 x e-3	-16.0	-19.2	3.2
2431.8 MHz	1.2 x e-3	-17.4	-19.6	2.2
2433.6 MHz	9.7 x e-4	-16.5	-18.1	1.5
2435.4 MHz	9.1 x e-4	-17.0	-18.5	1.5
2437.2 MHz	1.2 x e-3	-17.2	-19.2	2.0
2430.0 MHz	1.1 x e-3	-17.4	-19.6	2.2
2440.8 MHz	1.2 x e-4	-17.0	-18.1	2.1
2442.6 MHz	1.2 x e-3	-16.0	-19.2	3.2
2444.4 MHz	1.0 x e-3	-16.0	-18.1	2.1
2446.2 MHz	9.2 x e-4	-17.1	-18.1	1.0
2448.0 MHz	1.2 x e-3	-17.0	-19.6	2.6
2449.8 MHz	9.2 x e-4	-17.3	-19.3	2.0
2451.6 MHz	9.1 x e-4	-17.0	-18.4	1.4
2453.4 MHz	1.0 x e-3	-18.0	-19.6	1.6
2455.2 MHz	1.2 x e-3	-17.0	-19.5	2.5
2457.0 MHz	1.0 x e-3	-17.6	-18.6	2.0
2458.8 MHz	1.3 x e-3	-17.0	-19.5	2.5
2460.6 MHz	9.2 x e-4	-17.0	-19.1	2.1
2462.4 MHz	1.4 x e-3	-16.7	-18.6	1.9
2464.2 MHz	1.2 x e-3	-17.0	-19.1	2.1
2466.0 MHz	9.4 x e-4	-16.7	-19.5	2.3
2467.8 MHz	9.2 x e-4	-16.0	-18.6	2.6
2469.6 MHz	9.2 x e-3	-17.3	-19.5	2.2
2471.4 MHz	9.2 x e-4	-17.0	-19.6	2.6
2473.2 MHz	9.2 x e-3	-16.0	-18.1	2.1
2475.0 MHz	9.4 x e-4	-17.0	-19.2	2.2

Table 3: Test results

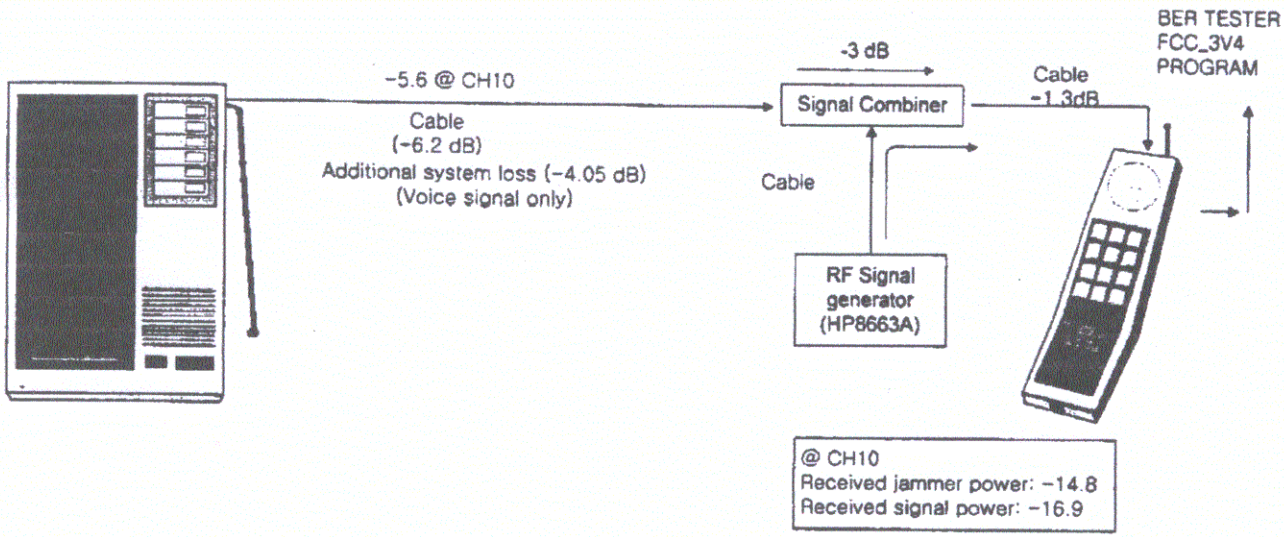

Figure 1: Test set-up

For DBPSK @ e-3 bit error rate the required SNR is 8.0dB. Using the results above and the data in the table below the processing gain is calculated to be 12.0dB.

Required SNR (dB)	8.0
System losses (dB)	2.0
J/S ratio @ 80% point (dB)	2.0
FCC processing gain (dB)	12.0

4. Conclusions

The result measured for processing gain of 12.0 dB is close to the actual processing gain due to a 12 chip spreading code of

$$10 \times \log (12) = 10.8 \text{ dB}$$